EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

THIS IS PRINT SET

	SEQUENCE
BLOCK DIAGRAM	E-BD-MM8-E-1
BLOCK DIAGRAM	E-BD-MM8-EJ-5
4K XY DRIVER	E-CS-G227-Ø-1
STACK BOARD	E-CS-G619-Ø-1
SENSE INHIBIT (4K)	E-CS-G1Ø4-Ø-1
8K XY DRIVER	E-CS-G233-Ø-1
SENSE INHIBIT (8K)	E-CS-G111-Ø-1
8K STACK ASSY	E-CS-H212-Ø-1
MEMORY ASSY (4K)	D-UA-MM8-E-Ø
MEMORY ASSY (PL)	A-PL-MM8-E-Ø
MEMORY (8K)	D-UA-MM8-EJ-Ø
STACK 4K 12 BIT	D-UA-H220-0-0
ACCESSORY LIST	A-AL-MM8-E-3
12 BIT STACK BOARD	D-CS-G646-0-1
ACCEPTANCE PROCEDURE	A-SP-7665139-0-0
ACCEPTANCE PROCEDURE	A-SP-MM8-EJ-1

MFG SET

	SEQUENCE
MANUFACTURING PROC.	A-SP-MM8-E-2
MANUFACTURING PROC.	A-SP-MM8-EJ-2
TEST PROCEDURE	A-SP-MM8-EJ-3
PURCHASE SPEC.	A-PS-3010654-0-0
PURCHASE SPEC.	A-PS-3009834-0-0

MM 8-E J-ONLY

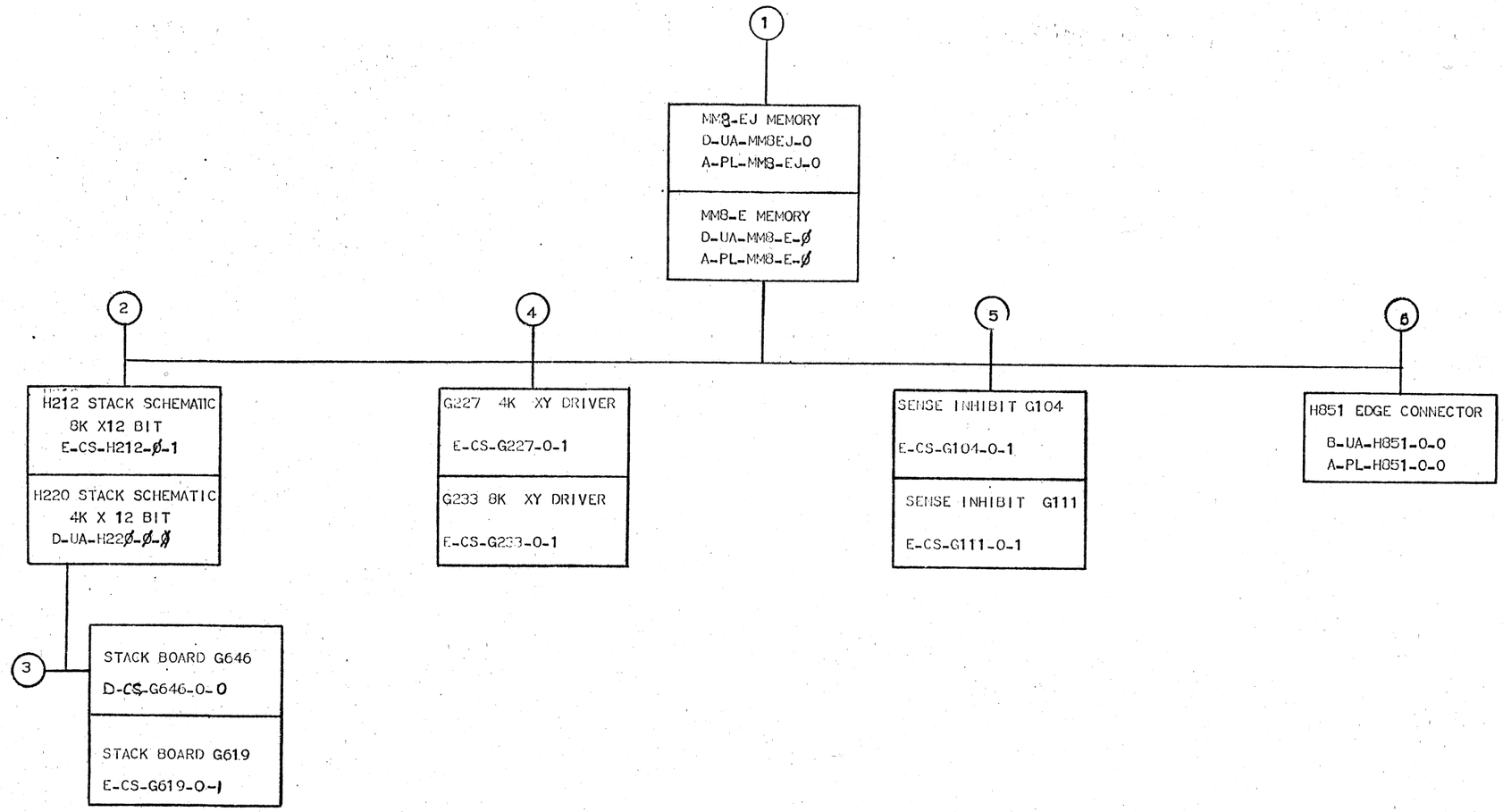
UNIT VARIATIONS

VARIATION	TITLE	MM8-1	MM8-2				
MM8-E	4K 12 BIT MEMORY	X					
MM8-EJ	8K 12 BIT MEMORY		X				

REVISIONS	REV	CHG. NO.	DATE
	A	MM8EJ-1	[illegible]

USED ON OPTION/MODEL		
DRN. F. CARBERRY	DATE 2/17/72	TITLE MEMORY
CHK'D [illegible]	DATE 6-6-72	
PROJ ENG. [illegible]	DATE	
PROD.	DATE	
FIELD SERV.	DATE	
SIZE B	CODE DD	NUMBER MM8-E	REV A
SHEET 1 OF 3	DIST	

DRB 106



TITLE		SIZE	CODE	NUMBER	REV
MEMORY	SHEET 2 OF 3	B	DD	MM8-E	A

ELECTRICAL

CUSTOMER PRINT SET							MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO.
X								1	E-BD-MM8-E-1	#	1	BLOCK DIAGRAM TIMING	
							X		A-SP-MM8-EJ-3	#	-	MM8-EJ TEST PROCEDURE	
	X								E-BD-MM8-ET-5	#	1	BLOCK DIAGRAM TIMING	
	X							2	E-CS-H212-Ø-1	#	2	STACK SCHEMATIC 8K X 12 BIT	
X								3	E-CS-G619-Ø-1	#	2	PLANAR STACK SCHEMATIC	
	X								D-CS-G646-Ø-1	#	1	12 BIT STACK BOARD	
X								4	E-CS-G227-0-1	#	2	4K XY DRIVER BOARD	
	X								E-CS-G233-0-1	#	5	8K XY DRIVER BOARD	
X								5	E-CS-G104-0-1	#	2	SENSE INHIBIT	
	X								E-CS-G111-0-1	#	3	4K OR 8K SENSE INHIBIT BOARD	

MECHANICAL

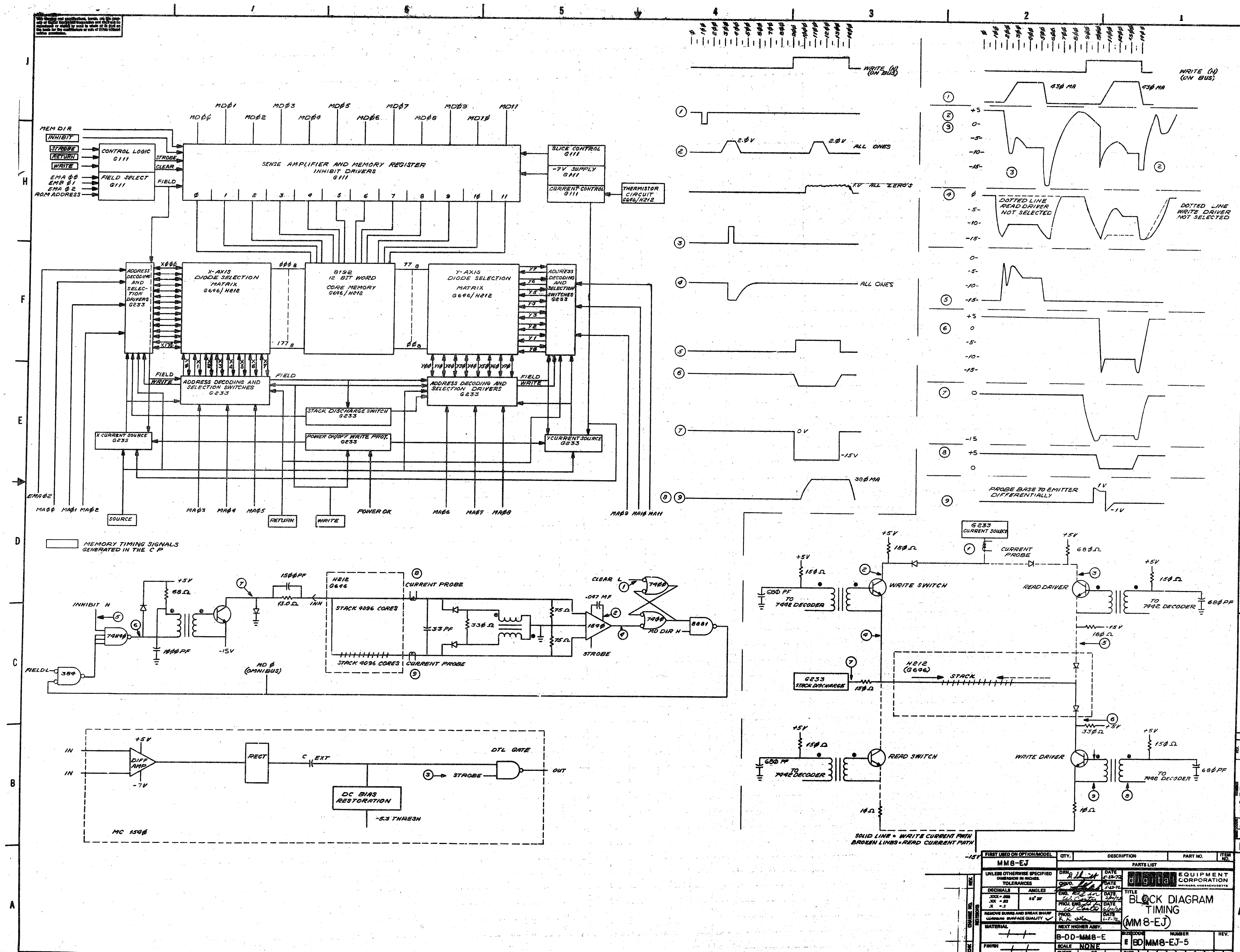
CUSTOMER PRINT SET							MFG SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO.
X								1	D-UA-MM8-E-0		1	4K 12 BIT MEMORY	
X									A-PL-MM8-E-0		1	4K 12 BIT MEMORY (PL)	
	X								D-UA-MM8-EJ-0	A	1	8K 12 BIT MEMORY	
X									A-SP-7665139-0-0		1	ACCEPTANCE PROC	
							X		A-SP-MM8-E-2			MANUFACTURING PROC.	
	X								A-SP-MM8-EJ-1			ACCEPTANCE PROC.	
							X		A-SP-MM8-EJ-2			MANUFACTURING PROC.	
X	X								A-AL-MM8-E-3		1	ACCESSORY SHIPPING LIST	
	X								A-SP-MM8-EJ-4			ENGINEERING SPECIFICATION	
								2	B-DD-H212-0		2	STACK 8K 12 BIT	
X									D-UA-H220-0-0			STACK 4K 12 BIT	
							X	3	A-PS-3010654-0-0			PURCHASE SPEC	
							X		A-PS-3009834			PURCHASE SPEC	
									C-MD-5509025-0-0		1	COVER PLATE	
								6	B-UA-H851-0-0			EDGE CONNECTOR	
									A-PL-H851-0-0			EDGE CONNECTOR PL	
									B-MD-5509071-1-0			RECEP 36 PIN REWORK	
									D-IA-5008903-0-0			ETCH BOARD	

TITLE	SIZE	CODE	NUMBER	REV
MEMORY	B	DD	MM8-E	A

SHEET 3 OF 3

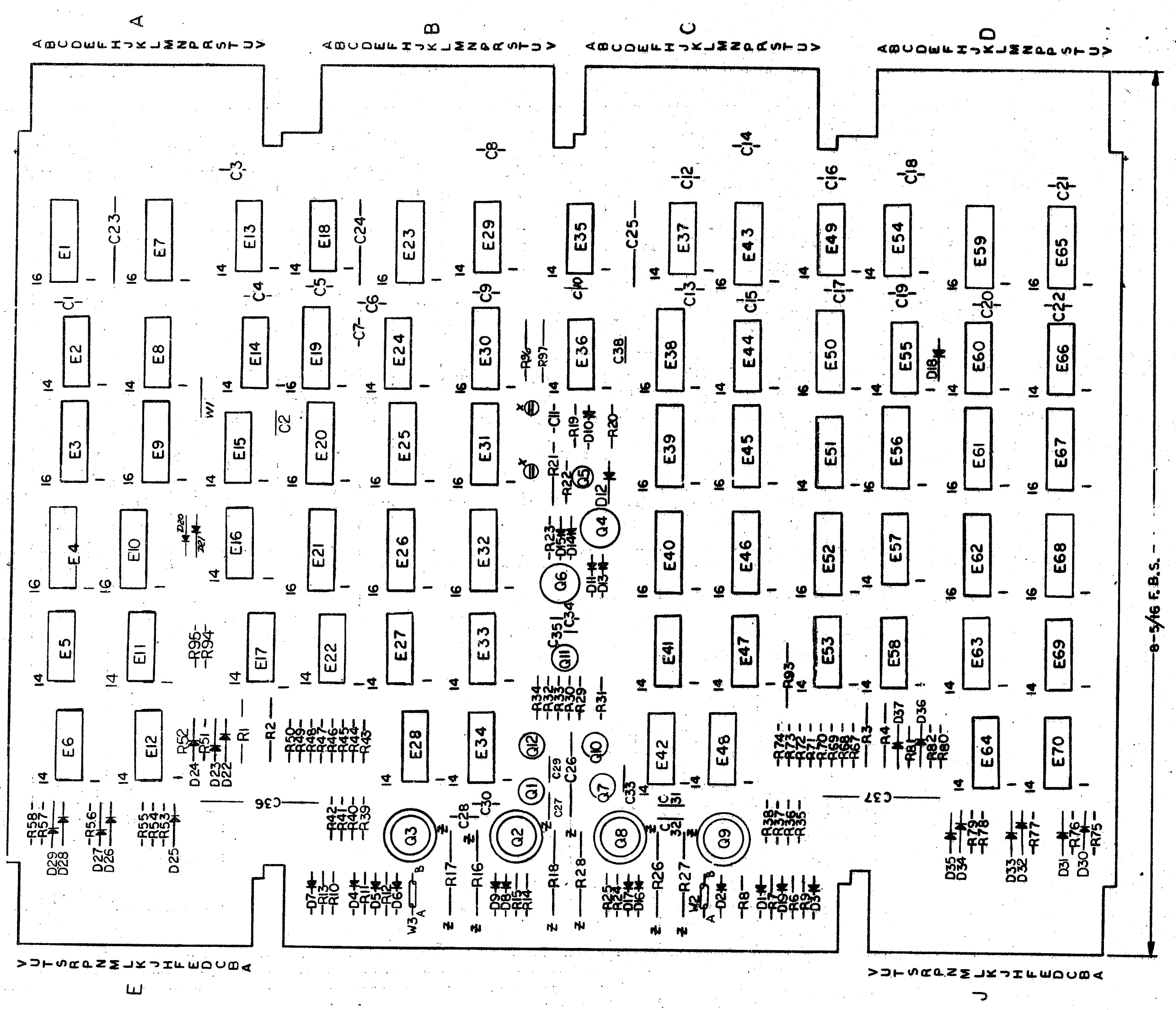
DRB 108

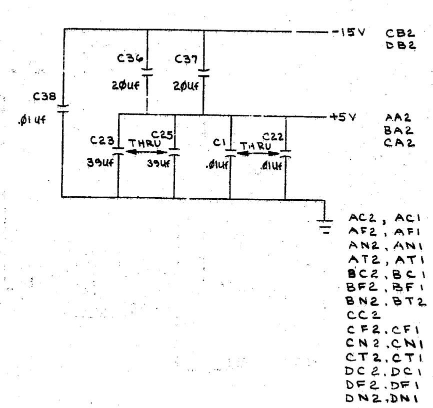
DEC - 16- (325)-1062-2A-R272



SENSE AMPLIFIER AND MEMORY REGISTER INHIBIT DRIVERS G111
CONTROL LOGIC G111
FIELD SELECT G111
MEM DIR
INHIBIT
STROBE
RETURN
WRITE
EMA ØØ
EMA Ø1
EMA Ø2
ROM ADDRESS
SLICE CONTROL G111
-7V SUPPLY G811
CURRENT CONTROL G111
THERMISTOR CIRCUIT G696/H212
X-AXIS DIODE SELECTION MATRIX G696/H212
8192 12 BIT WORD CORE MEMORY G696/H212
Y-AXIS DIODE SELECTION MATRIX G696/H212
ADDRESS DECODING AND SELECTION SWITCHES G233
ADDRESS DECODING AND SELECTION DRIVERS G233
STACK DISCHARGE SWITCH G233
POWER ON/OFF WRITE PROT. G233
X CURRENT SOURCE G233
Y CURRENT SOURCE G233
SOURCE
RETURN
WRITE
POWER OK
MEMORY TIMING SIGNALS GENERATED IN THE C P
WRITE (H) (ON BUS)
ALL ONES
ALL ZEROS
DOTTED LINE READ DRIVER NOT SELECTED
DOTTED LINE WRITE DRIVER NOT SELECTED
PROBE BASE TO EMITTER DIFFERENTIALLY
INHIBIT H
FIELD L
CURRENT PROBE
STACK 4096 CORES
MD Ø (OMNIBUS)
STROBE
MD DIR H
CLEAR L
DIFF AMP
RECT
DC BIAS RESTORATION
-5.3 THRESH
DTL GATE
MC 1540
WRITE SWITCH
READ DRIVER
READ SWITCH
WRITE DRIVER
TO 7442 DECODER
G233 CURRENT SOURCE
G233 STACK DISCHARGE
STACK
SOLID LINE = WRITE CURRENT PATH
BROKEN LINES = READ CURRENT PATH
FIRST USED ON OPTION/MODEL MM8-EJ
UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES TOLERANCES
DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE BLOCK DIAGRAM TIMING (MM8-EJ)
NEXT HIGHER ASSY. B-DD-MM8-E
SCALE NONE
SIZE E CODE BD NUMBER MM8-EJ-5
PARTS LIST

NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS TO BE 150 Ω





PARTS LIST

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	C32	CAP 390 PF 100V 5%	1001631	45
1	C26	CAP .15UF, 35V, 20% S.TANT	1002180	44
1	R95	RES 5.6K, 1/4W, 5%	1301874	43
1	R97	RES 34.8K, 1/8W, 1%	1303156	42
2		SPLIT LUG	9006735	41
A/R	W2, W3	WIRE #24 AWG, PVC INS, STRD, BLK	9107450-00	40
10	E1, E7, E19, E30, E38, E43, E50, E59, E65, E23	IC DEC 7442	19-10046	39
1	E36	IC MC 3001L	19-09514	38
5	E13, E29, E37, E54, E35	IC DEC 74H10	19-09057	37
10	E2, E8, E15, E24, E34, E42, E44, E51, E60, E66	RES 100 ; CAP 1500 Pf	1911200	36
20	E3, E4, E9, E10, E20, E21, E25, E26, E31, E32, E39, E40, E45, E46, E52, E56, E61, E62, E67, E68.	IC TRANSFORMER	16-09996	35
20	E5, E8, E11, E12, E16, E17, E22, E27, E28, E33, E41, E48, E63, E64, E69, E70, E47, E53, E57, E58	IC XSTR DEC 4008 - Y, T, CR X	15-10015	34
4	Q2, Q3, Q8, Q9	XSTR 2N3762	15-09649	33
2	Q1, Q7	XSTR 2N4258	15-05321	32
2	Q11, Q5	XSTR DEC 6534B	15-03409-01	31
1	Q10	XSTR DEC 3009B-S	15-03100	30
3	Q4, Q6, Q12	XSTR DEC 1008-S	15-02155	29
2	R32, R33	RES 4.7K, 1/4W, 5%	13-00447	28
4	R16, R17, R26, R27	RES 16.9 6W 1% BERYLLIUM	13-10032	27
2	R18, R28	RES 750, 1W, 5%	13-02385	26
4	R6, R9, R10, R13	RES 680, 1/4W, 5%	13-01424	25
16	R51 THRU R58, R75 THRU R82	RES 180, 1/4W, 5%	13-01322	24
4	R7, R8, R11, R12	RES 3.9K, 1/4W, 5%	13-00444	23
5	R14, R15, R24, R25, R34	RES 1.5K, 1/4W, 5%	13-00391	22
1	R21	RES 470, 1/2W, 5%	13-00315	21
3	R20, R22, R31	RES 330, 1/4W, 5%	13-00295	20
1	R96	RES 14.7K, 1/8W, 1%	1302941	19
26	R29, R35 THRU R50, R67 THRU R74, R94	RES 150, 1/4W, 5%	13-00250	18
2	R23, R30	RES 100, 1/4W, 5%	13-00229	17
1	R19	RES 68, 1/4W, 5%	13-00219	16
5	R1, R2, R3, R4, R93	RES 5.1 1/2W, 5%	13-11220	15
4		HEAT SINK	12-10001	14
9	D1 THRU D7, D12, D19, D22—D37	DIODE D672	11-05275	13
12	D8 THRU D11, D13 THRU D18, D20, D21	DIODE D664	11-00114	12
1	C28	CAP 680PF, 100V, 5% DM	10-00026	11
3	C27, C34, C31	CAP .047UF, 16V, 15-20%	10-09678	10
2	C36, C37	CAP 20UF, 50V, -10 75%	10-02839	9
25	C1 THRU C22, C30, C35, C38	CAP .01UF, 100V, 20% DISC	10-01610	8
3	C23, C24, C25	CAP 39UF, 10V, 10% STANT	10-00076	7
2	C29, C33	CAP 39PF, 100V, 5% DM	10-00010	6
4	E14, E18, ~~E49~~ E55	IC DEC 6380	19-09971	5
1	5009837	ETCHED CIRCUIT BOARD	5009837	4
REF		MODULE ECO HISTORY	B-MH-G233-0-6	3
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-G233-0-5	2
REF		X-Y COORDINATE HOLE LOCATION	K-CO-G233-0-4	1

IC PIN LOCATIONS

IC	GND	+5V
IC DEC 6380	1	8
IC DEC 7442	8	16

GND AND 5V ARE LOCATED ON PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE

JUMPER LIST

ITEM NO.	AWG	FROM PT	TO PT
40	24	W3-A	W3-B
40	24	W2-A	W2-B

DEC FORM NO. DEC 101

SEMICONDUCTOR CONVERSION CHART

DEC NO.	EIA NO.
D672	IN 3653
D664	IN 3606

REVISIONS

REV	CHANGE NO.	CHK
C	G233-00001/1A	L. LORANGER 5/23/72
D	G233-00002	W. COATES 9/12/72
E	G233-00003	R. REGAN 9-21-72
F	G233-00004	R. REGAN 11-14-72

FIRST USED ON: PDP-8/E

ETCH BOARD REV: E

DRN. J. Carberry DATE 1/26/72
CHK'D. DATE 3-29-72
ENG. W. Coates DATE 3/29/72
PROJ. ENG. W. Coates DATE 3/29/72
PROD. R. K. DATE 3-31-72

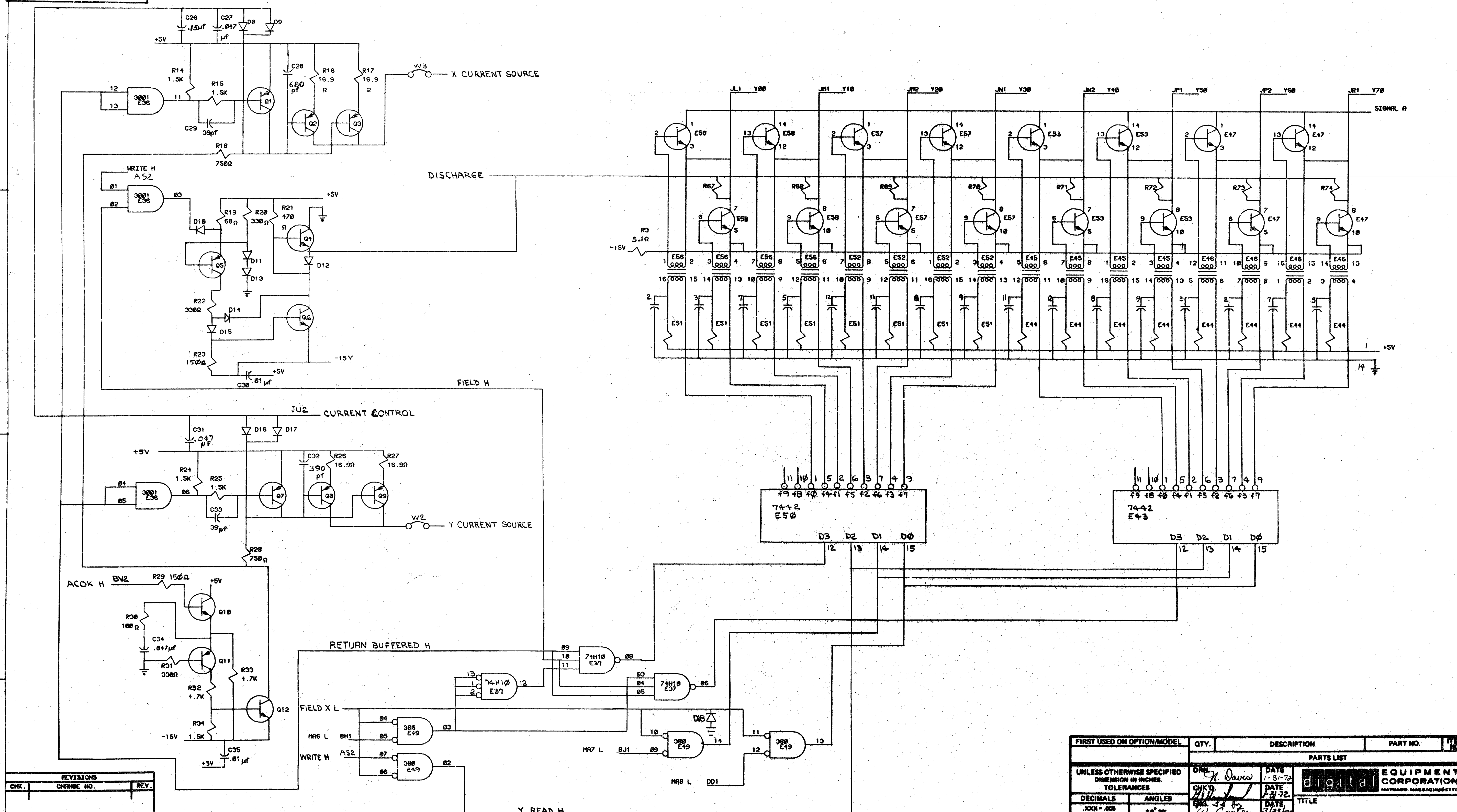
NEXT HIGHER ASSY: B-DD-MM8-EJ-0

digital EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS

TITLE: 8K X-Y

SIZE E | CODE CS | NUMBER G233-0-1 | REV F

SCALE NONE | SHEET 1 OF 5



REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES	
DECIMALS: .XXX = .005, .XX = .02, .X = .1	ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	
MATERIAL	-/-
FINISH	-/-

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

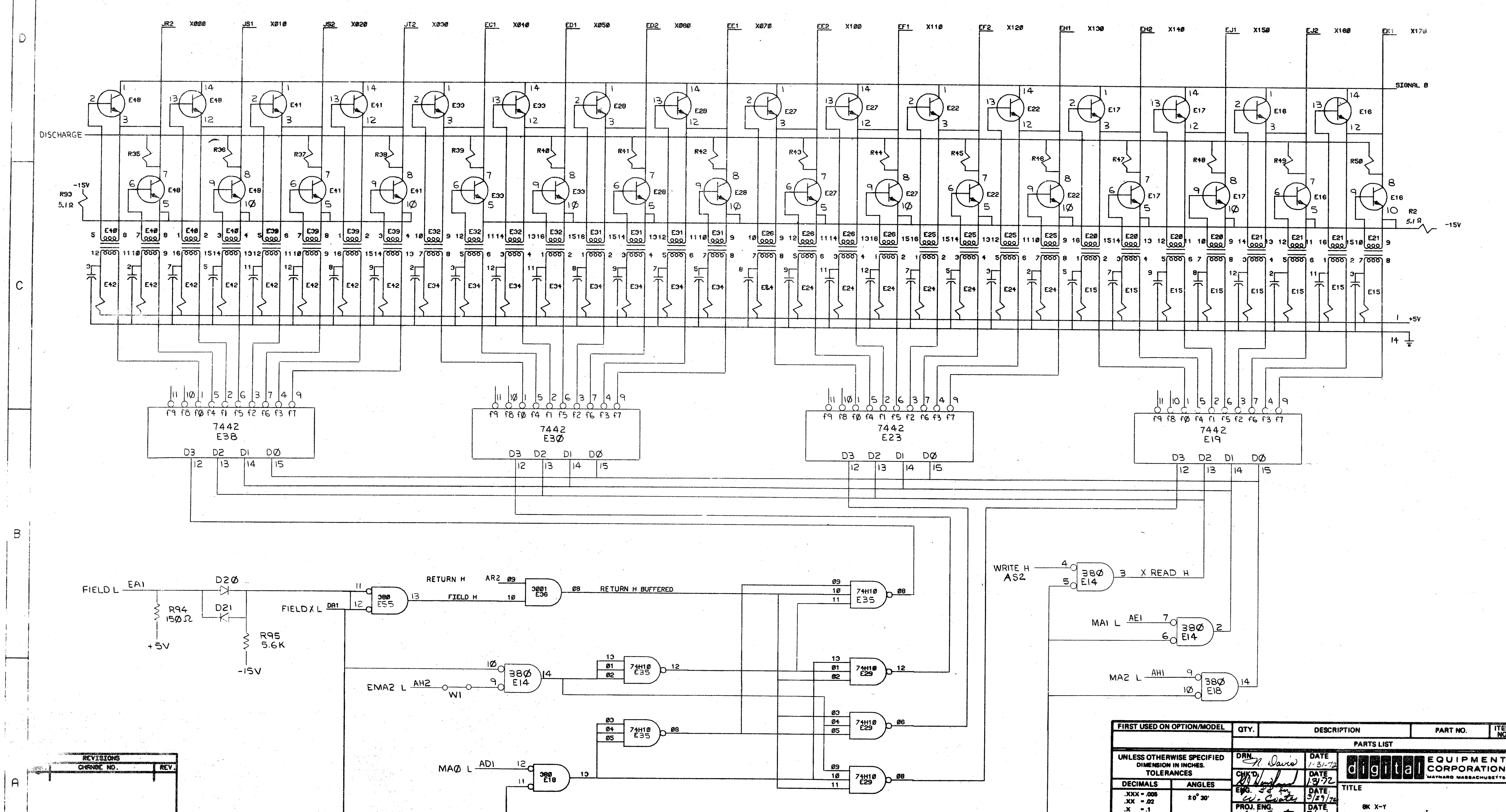
DRN. N. Davis	DATE 1-31-72
CHK'D.	DATE 3/21/72
ENG. W. Coates	DATE 3/29/72
PROJ. ENG. W. Coates	DATE 3/29/72
PROD. R. F.	DATE 3-31-72
NEXT HIGHER ASSY.	
SCALE NONE	
SHEET 2 OF 3	

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: 8K X-Y

SIZE	CODE	NUMBER	REV.
D	CS	8233-0-1	

DIST.



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —//—

FINISH —//—

		DATE
DRN.	N. Davis	1-31-72
CHK'D.	[illegible]	1-31-72
ENG.	[illegible] for W. Coates	3/29/72
PROJ. ENG.	W. Coates	3/29/72
PROD.	R. K. [illegible]	3-31-72

NEXT HIGHER ASSY.

SCALE NONE

SHEET 3 OF 5

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE 8K X-Y

SIZE	CODE	NUMBER	REV.
D	CS	G233-0-1	

DIST.

REVISIONS

CHANGE NO.	REV.

X CURRENT SOURCE

SIGNAL B

D4 D5 D6 D7

R11 3.9K R12 3.5K R13 680Ω R10 680Ω

+5V -15V

R1 5.1A 1/2W

EL1 RX0 EM1 RX1 EN1 RX2 EP1 RX3 ER1 RX4 ES1 RX5 EU2 RX6 EV2 RX7

EK2 WX0 EL2 WX1 EM2 WX2 EN2 WX3 EP2 WX4 ER2 WX5 ES2 WX6 ET2 WX7

R51 180Ω R52 180Ω R53 180Ω R54 180Ω R55 180Ω R56 180Ω R57 180Ω R58 180Ω

D22 D23 D24 D25 D26 D27 D28 D29

E11 E12 E12 E11 E6 E6 E5 E5

E8 E8 E8 E8 E8 E2 E2 E2 E2 E2

+5V

74H10 E13 — SOURCE H — FIELD H — 74H10 E13

74H10 E13 — X READ H

7442 E7 D3 D2 D1 D0

7442 E1 D3 D2 D1 D0

MA3 L — AJ1 — FIELD X L — 38Ø E14

74H10 E13

MA4 L — BD1 — 38Ø E18

MA5 L — BE1 — 38Ø E18

+5 V — R96 14.7K — R97 34.8K — EB1

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL

FINISH

DRN.	DATE	1-31-72
CHK'D.	DATE	1-31-72
ENG.	DATE	3/29/72
PROJ. ENG.	DATE	3/21/72
PROD.	DATE	3-31-72

NEXT HIGHER ASSY.

SCALE NONE

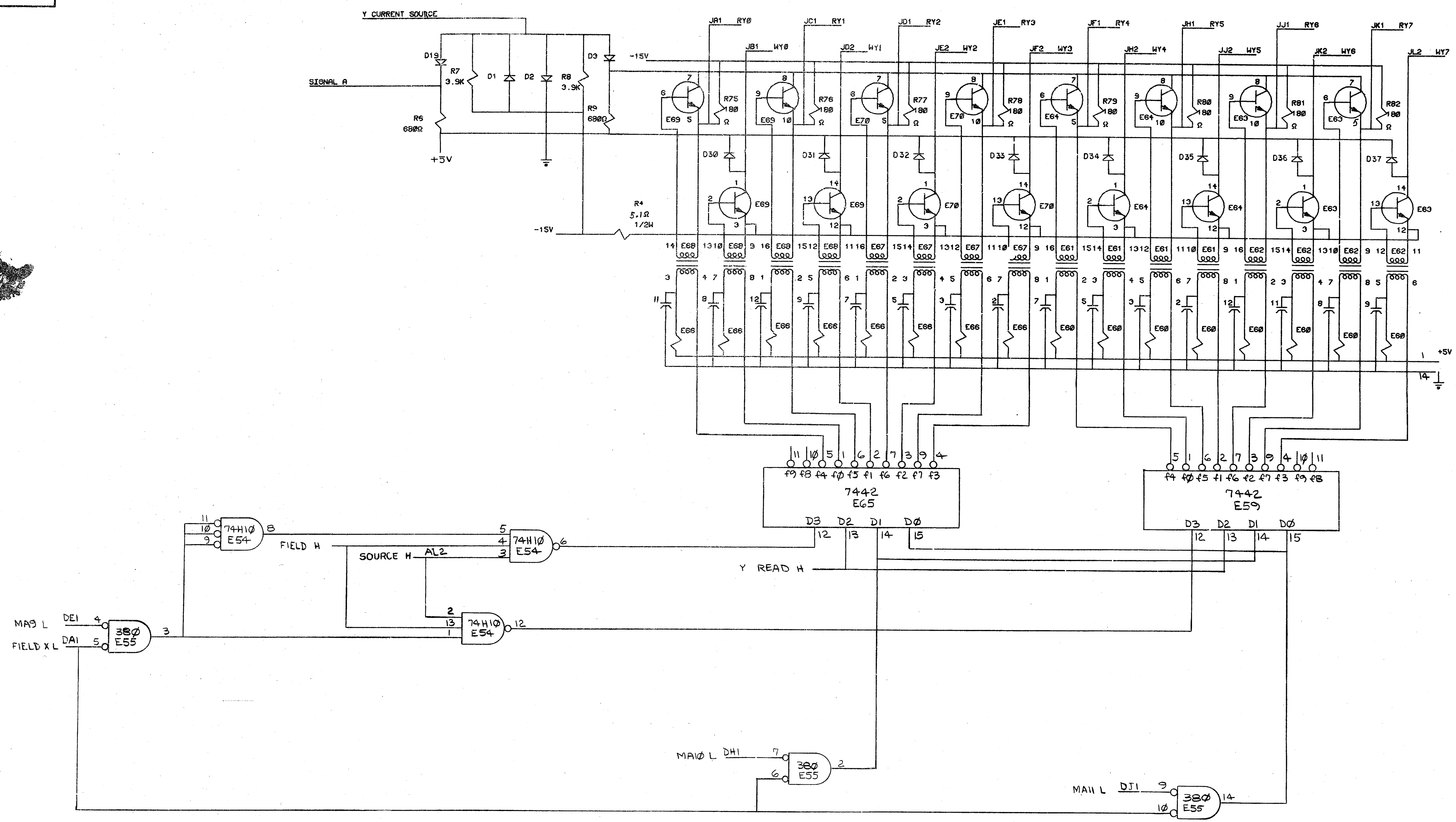
SHEET 4 OF 8

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: 8K X-Y

SIZE	CODE	NUMBER	REV.
D	CS	6233-B-1	

DIST.



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —/—/—

FINISH —/—/—

		DATE
DRN	R. Davis	1-21-72
CHK'D		1-31-72
ENG.	for W. Coates	3/29/72
PROJ. ENG.	W. Coates	3/29/72
PROD.	R. K.	3-31-72

NEXT HIGHER ASSY.

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE 8K X-Y

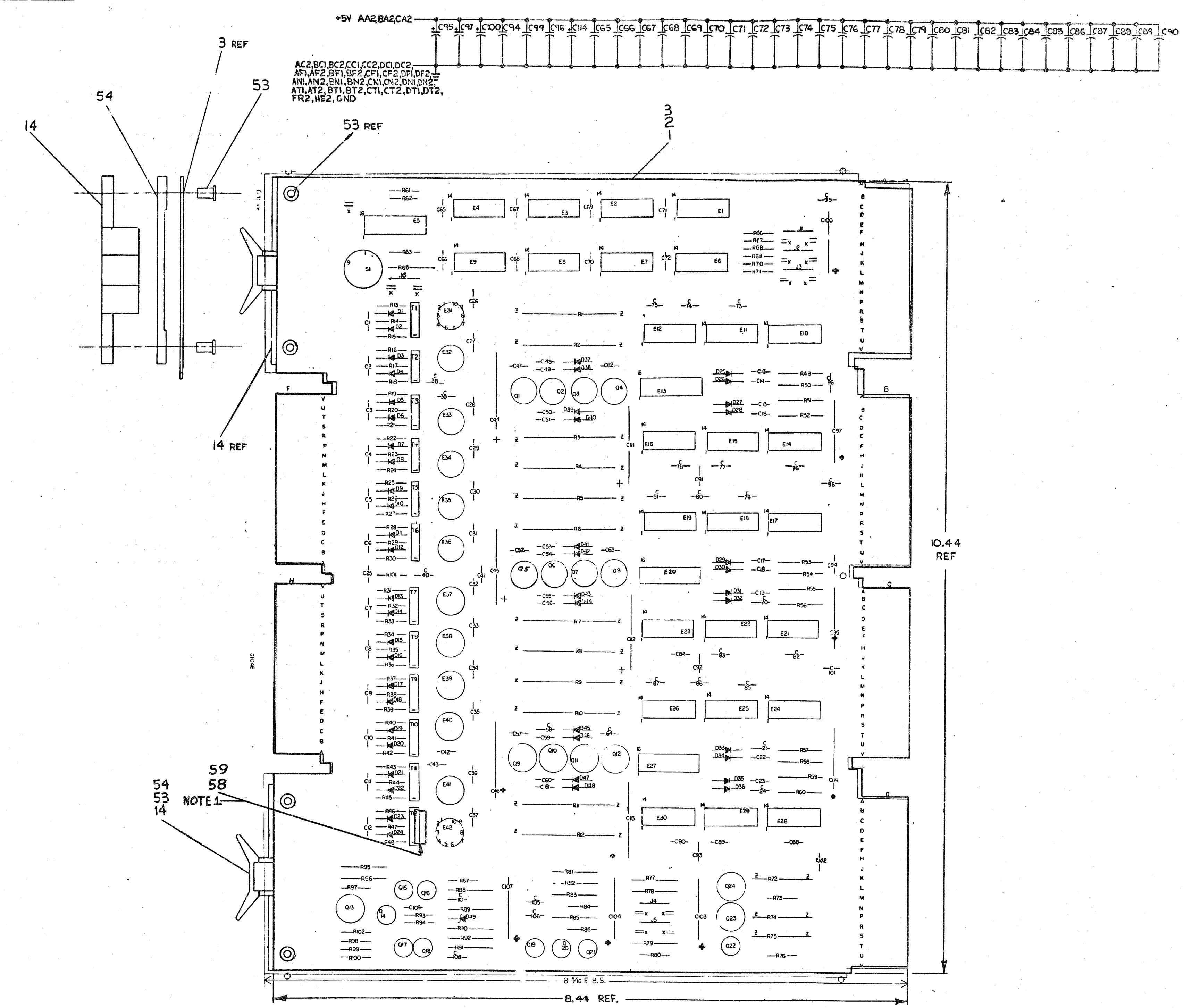
SIZE	CODE	NUMBER	REV.
D	CS	6233-8-1	

SCALE NONE SHEET 5 OF 5

DIST.

NOTES:

1. CUT CATERPILLER GROMMET (DEC 9007622) 7-1/8" LONG. ON ONE SIDE CUT TOOTH OUT 3-5/8" FROM ONE END. ON EACH END SPRAY WITH SCOTCH-GRIP ADHESIVE NO 77 (DEC 9008907) FOLLOW DIRECTIONS FOR NON-PERMANENT BONDS ON BACK OF CAN. PLACE THE GROMMET OVER 17Z5 TRANSFORMERS WITH CUTOUT TOOTH OVER CAPACITOR C40.
2. IN PLACE OF DEC 6380 (ITEM #49), DEC 380 (1909485) MAY BE USED.
3. R65 IS DETERMINED BY THE VOLTAGE AT PIN HA1 WITH RESPECT TO +5V.



QTY.	REF DESIGNATION	DESCRIPTION	PART NO.	
1	R65	SEE NOTE ABOVE		63
1	R102	RES. 10, 1/4W, 10%	1300170	62
13		SPLIT LUGS	9006735	61
1	R81	RES 2.74 1/8W 1% 100 MFP	1304868	60
A/R		SCOTCH GRIP ADHESIVE	9008907	59
A/R		CATERPILLAR GROMMET	9007622	58
REF		ASSY/DRILLING HOLE LAYOUT	E-AH-G111-0-5	57
2	R90, R101	RES. 100, 1/8W, 1% 100 MFP	1302858	56
A/R		WIRE #22 AWG SOLID BUS	9107560-01	55
2		SPACER (CABLE CLAMP)	1202704	54
4		EYELET #GS4-11 E.B. STIMPSON	9006750	53
1	E6	I.C. DEC 7486	1910011	52
3	E10, E17, E24	I.C. DEC 8881	1909705	51
4	E1, E14, E21, E28	I.C. DEC 384	1909486	50
1	E2	I.C. DEC 6380	1909971	49
2	E3, E8	I.C. DEC 74H11	1909267	48
1	E9	I.C. DEC 74H00N	1909056	47
6	E11, E15, E18, E22, E25, E29	I.C. DEC 74H40N	1905586	46
1	E7	I.C. DEC 7440N	1905579	45
6	E12, E16, E19, E23, E26, E30	I.C. DEC 7400N	1905575	44
1	E4	I.C. DEC 7474N	1905547	43
12	E31-E42	I.C. MC 1540G	1905521	42
1	DL1	100NS DELAY LINE	1610033-0	41
3	E13, E20, E27	PULSE TRANSFORMER	1609996	40
12	T1-T12	TRANSFORMER 17Z-5	1609478	39
12	Q1-Q12	TRANSISTOR DEC 3734	1510062	38
2	Q23, Q24	TRANSISTOR DEC 3762	1509649	37
9	Q14-Q22	TRANSISTOR DEC 6534-B	1503409-01	36
1	Q13	TRANSISTOR DEC 2219-S	1501881	35
12	R1-R12	RES. 13.0K 6W, 1%	1310032-01	34
12	R49-R60	RES. 68, 1/2W, 5% CC	1309405	33
1	R89	RES. 68.1K, 1/8W, 1%	1305252	32
1	R88	RES. 5.62K, 1/8W, 1%	1305128	31
1	R91	RES. 348, 1/8W, 1%	1304858	30
2	R79, R95	RES. 4.64K, 1/8W, 1%	1304856	29
1	R77	RES. 9.09K, 1/8W, 1%	1304855	28
2	R92, R85	RES. 1.96K, 1/8W, 1%	1304833	27
3	R82, R83, R96	RES. 1K, 1/8W, 1%	1303114	26
1	R78	RES. 1.21K, 1/8W, 1%	1302871	25
24	R13, R15, R16, R18, R19, R21, R22, R24, R25, R27, R28, R30, R31, R33, R34, R36, R37, R39, R40, R42, R43, R45, R46, R48	RES. 75 1/8W 1%	1303064	24
1	R86	RES. 680, 1/4W, 5% CC	1301424	23
6	R66, R68, R70, R80, R94, R99	RES. 10K, 1/4W, 5% CC	1300479	22
3	R73, R76, R97	RES. 4.7K, 1/4W, 5% CC	1300447	21
2	R61, R87	RES. 1K, 1/4W, 5% CC	1300365	20
19	R14, R17, R20, R23, R26, R29, R32, R35, R38, R41, R44, R47, R62, R67, R69, R71, R84, R93, R98	RES. 330, 1/4W, 5% CC	1300295	19
1	R63	RES. 220, 1/4W, 5% CC	1300271	18
1	R100	RES. 100, 1/4W, 5% CC	1300229	17
3	R72, R74, R75	RES. 68, 1W, 10% CC	1300222	16
1	S1	ROTARY SWITCH	1210043-0	15
2		HANDLE FLIP CHIP - GREEN	9008337-01	14
1	D49	DIODE 1/4M 6.8AZ1	1109991	13
36	D1-D24, D37-D48	DIODE D672	1105275	12
12	D25-D36	DIODE D664	1100114	11
32	C25-C43, C47, C52, C57, C62-C64, C91-C93, C98, C101, C102, C110	CAP. .047 uf 16V 20% DISC	1009678	10
33	C65-C90, C94, C96, C99, C105, C106, C108, C109	CAP. .01 uf 100V 20% DISC	1001610	9
6	C44-C46, C111-C113	CAP. 47 uf 20V 20% S. TANT	1000079	8
7	C95, C97, C100, C103, C104, C107, C114	CAP. 6.8 uf 35V 20% S. TANT	1000067	7
12	C48-C51, C53-C56, C58-C61	CAP. 1500 PF 200V 10% DISC	100005[illegible]	6
12	C13-C24	CAP. 1000PF 100V 5% MICA	1000042	5
12	C1-C12	CAP. 82 PF 100V 5% D. MICA	1000015	4
1		ETCHED CIRCUIT BOARD	5009344	3
REF		MODULE ECO HISTORY	B-MH-G111-0-6	2
REF		X-Y COORDINATE HOLE LOCATION	K-CO-G111-0-4	1

PARTS LIST

REV COLUMN C

PRINTED CIRCUIT BOARD REVISION

DEC NO.	EIA NO.
DEC 3734	SAME
DEC 3762	SAME
DEC 6534-B	MPS6534
DEC 2219-S	2N 2219
1/4 M 6.8AZ	1N4099
D672	1N3653
D664	1N3606

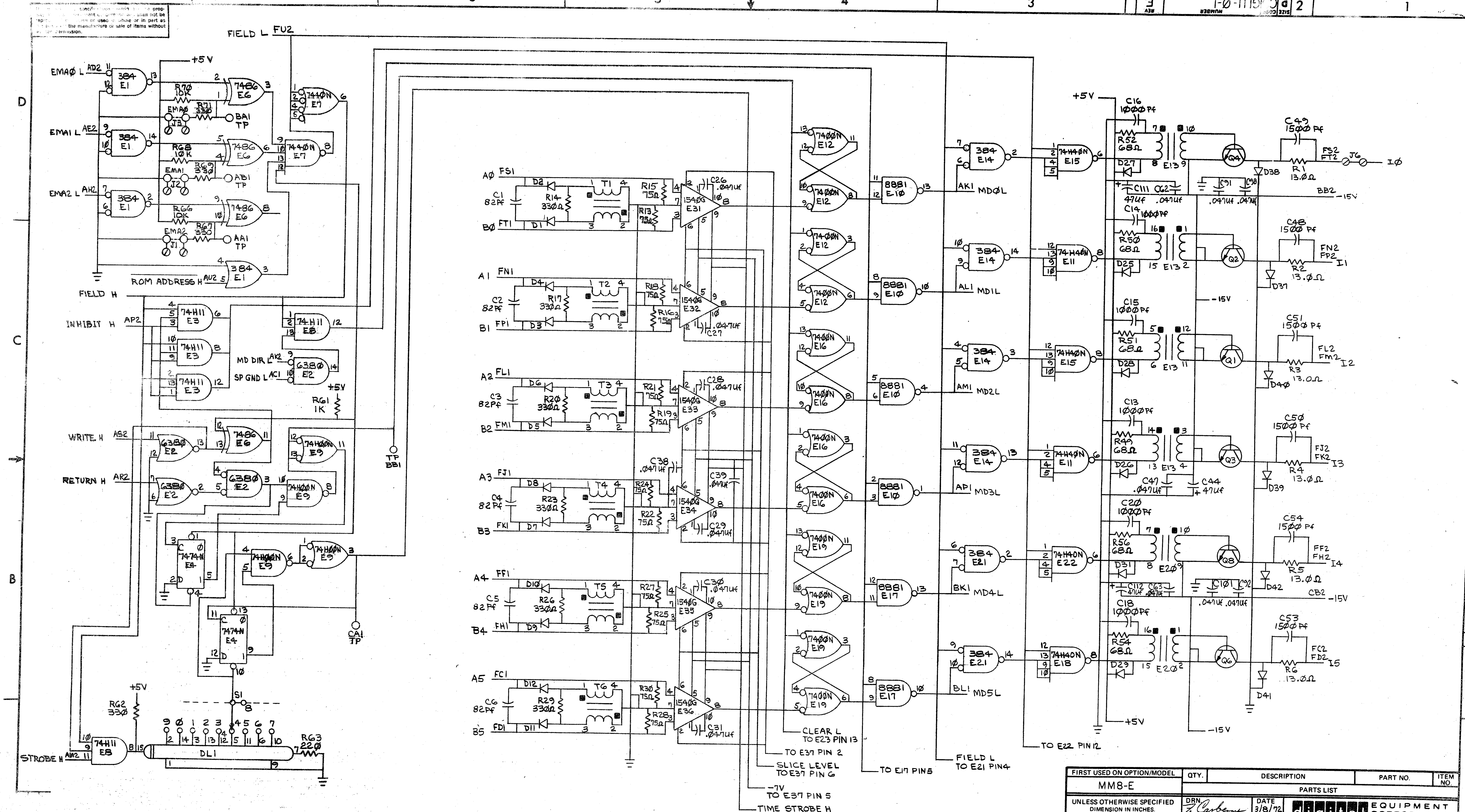
SEMICONDUCTOR CONVERSION CHART

USED ON MM18-EJ

EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: SENSE INHIBIT

E ICS G111-Ø-1 REV. F



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
MM8-E		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —//—

FINISH —//—

DRN. L. Carberry DATE 3/8/72
CHK'D DATE 3-21-72
ENG. W. Coates DATE 3/29/72
PROJ. ENG. W. Coates DATE 3/29/72
PROD. R.K. DATE 3-31-72

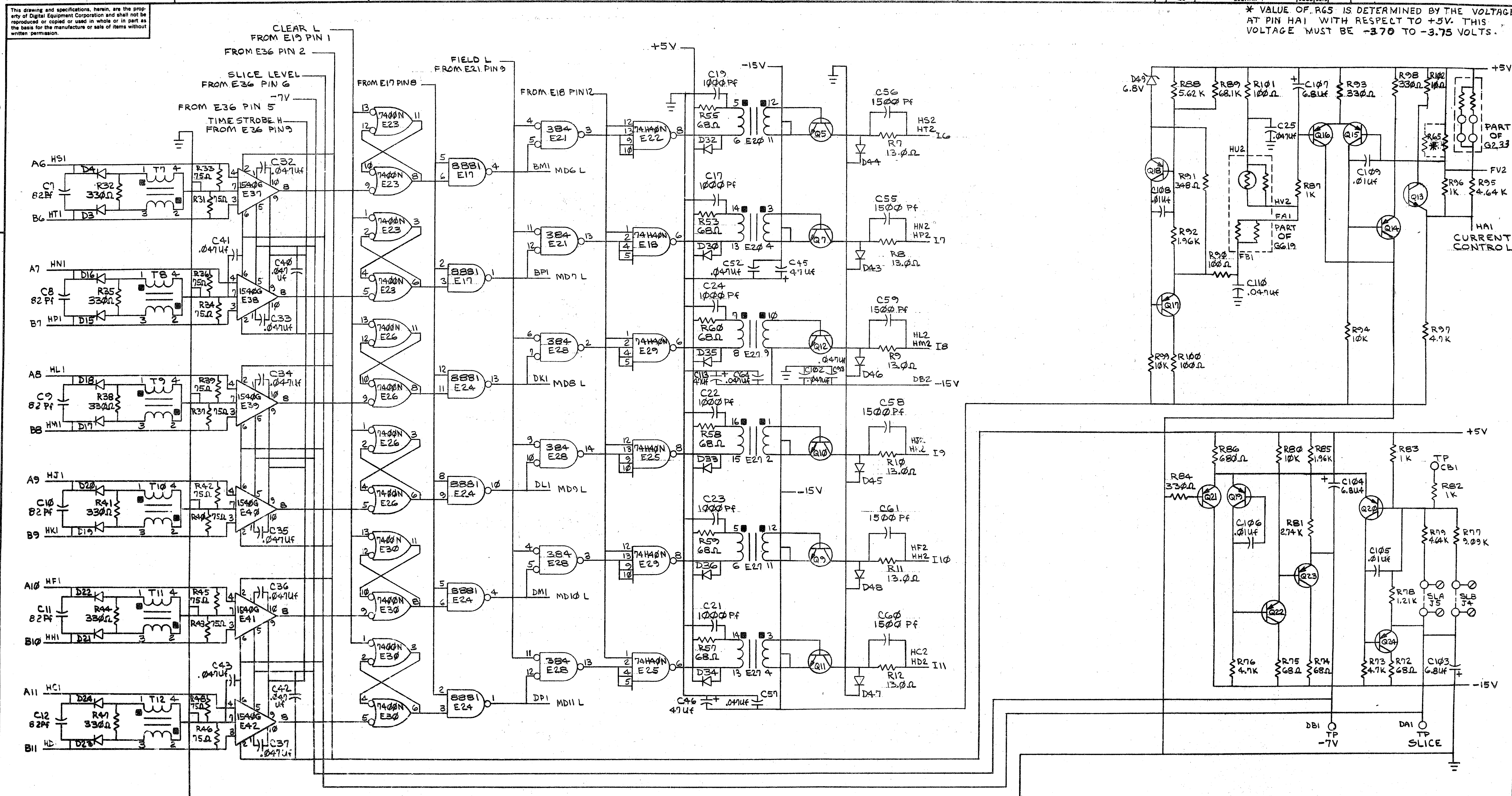
NEXT HIGHER ASSY. A-PL-MM8-E-Ø

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE 4K OR 8K SENSE INHIBIT BOARD

SIZE D CODE CS NUMBER G111-Ø-1 REV. F

SCALE —//— SHEET 2 OF 3 DIST.



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS .XXX = .005 .XX = .02 .X = .1 — ANGLES ±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —

FINISH —

DRN F. Carberry DATE 3/10/72

CHK'D J. Kelegher DATE 3-27-72

ENG. DATE 3/29/72

PROJ. ENG. W. Coates DATE 3/29/72

PROD. R.K. DATE 3-31-72

NEXT HIGHER ASSY.

SCALE — SHEET 3 OF 9

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE 4K OR 8K SENSE INHIBIT BOARD

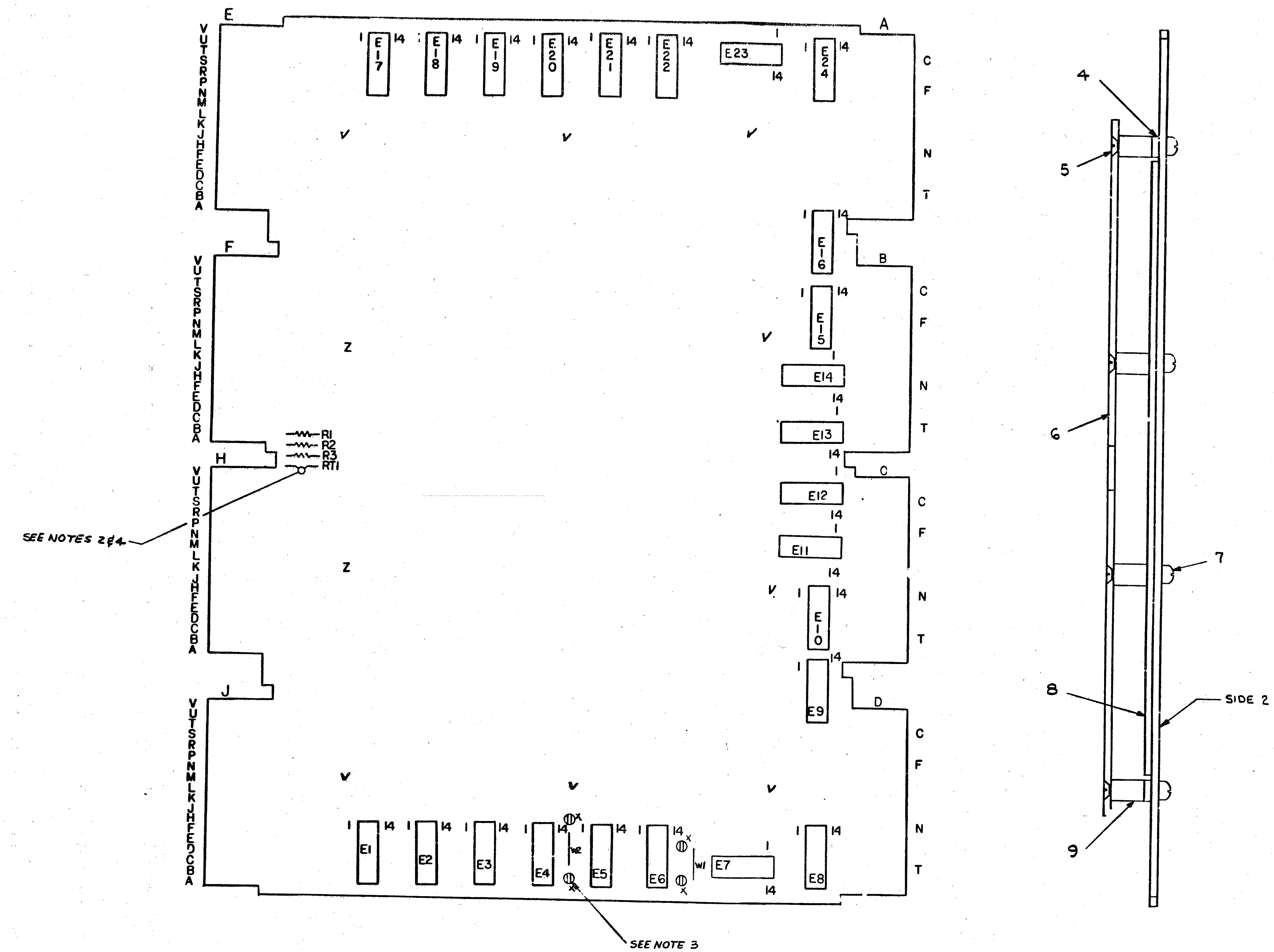
SIZE D CODE CS NUMBER G111-Ø-1 REV. F

DIST.

REVISIONS — REV — CHANGE NO — CHK

DEC FORM NO DRD 102-2

NOTES:
1. ALL COMPONENT LEADS TO BE LESS THAN 1/16 INCH LONG ON SIDE 2 OF MODULE.
2. RT1 TO LAY FLAT AS SHOWN.
3. THE 4 SPLIT LUGS (X) ARE OPTIONAL.
4. VALUES OF R1, R2, R3 AND RT1 ARE SHOWN ON STACK BOARD DWG G646 AND NOTED HERE FOR CONVENIENCE:
   - R1: 562Ω, 1/8W, 1%
   - R2: 9.76KΩ, 1/8W, 1%
   - R3: 147Ω, 1/8W, 1%
   - RT1: 1K THER.
5. 2501-1 (DEC. PT. NO. 1910010-01) MAY BE USED INTERCHANGEABLY WITH ITEM #2



QTY.	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
12		8192-CORE MATS (STRUNG)	VENDOR SUPPLIED	[illegible]
1		STICKER WITH DEC PART & P.O. #	VENDOR SUPPLIED	[illegible]
10		STANDOFF, 4-40 X 1/4 DIA X 1/4 LG.	VENDOR SUPPLIED	[illegible]
1		SUBSTRATE	VENDOR SUPPLIED	[illegible]
10		SCREW, NYLON FILISTER 4-40 X 3/16	VENDOR SUPPLIED	[illegible]
1		COVER PLATE	VENDOR SUPPLIED	[illegible]
10		SCREW, FLAT HEAD NYLON, 4-40 X 3/16	VENDOR SUPPLIED	[illegible]
4		WASHER, NYLON 1/32 X 1/4 O.D. X 1/8 I.D	VENDOR SUPPLIED	4
2		INSULATED JUMPER	VENDOR SUPPLIED	[illegible]
24	E1-E24	IC DEC 2501 (SEE NOTE 5)	19120 C	[illegible]
		STACK BOARD	A-PL-[illegible]	[illegible]

PARTS LIST

FIRST USED ON: MM8-EJ

ETCH BOARD REV: B

REV.	CHANGE NO.		
B	H212-00001	W. COATES 3-6-73	3/6/73
C	H212-00002	W. COATES 5/21/73	R.J. Hale 5/1/73

REVISIONS

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN.	DATE 1/26/71
CHK'D.	DATE 2-24-72
ENG.	DATE 3/29/72
PROJ. ENG.	DATE 3/29/72
	DATE 3-31-72

NEXT HIGHER ASSY: B-DD-MM8-EJ

SCALE 2/1 SHEET 1 OF 2

EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: STACK SCHEMATIC 8K X 12BIT

SIZE: F CODE: CS NUMBER: H212-0-1 REV.: C

DIST.

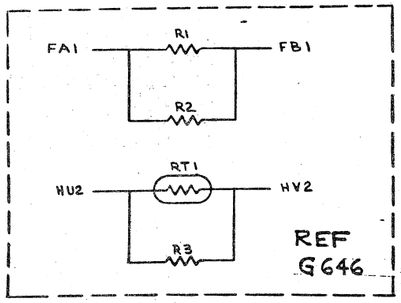
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

ITEM NO	AWG	FROM PT	TO PT

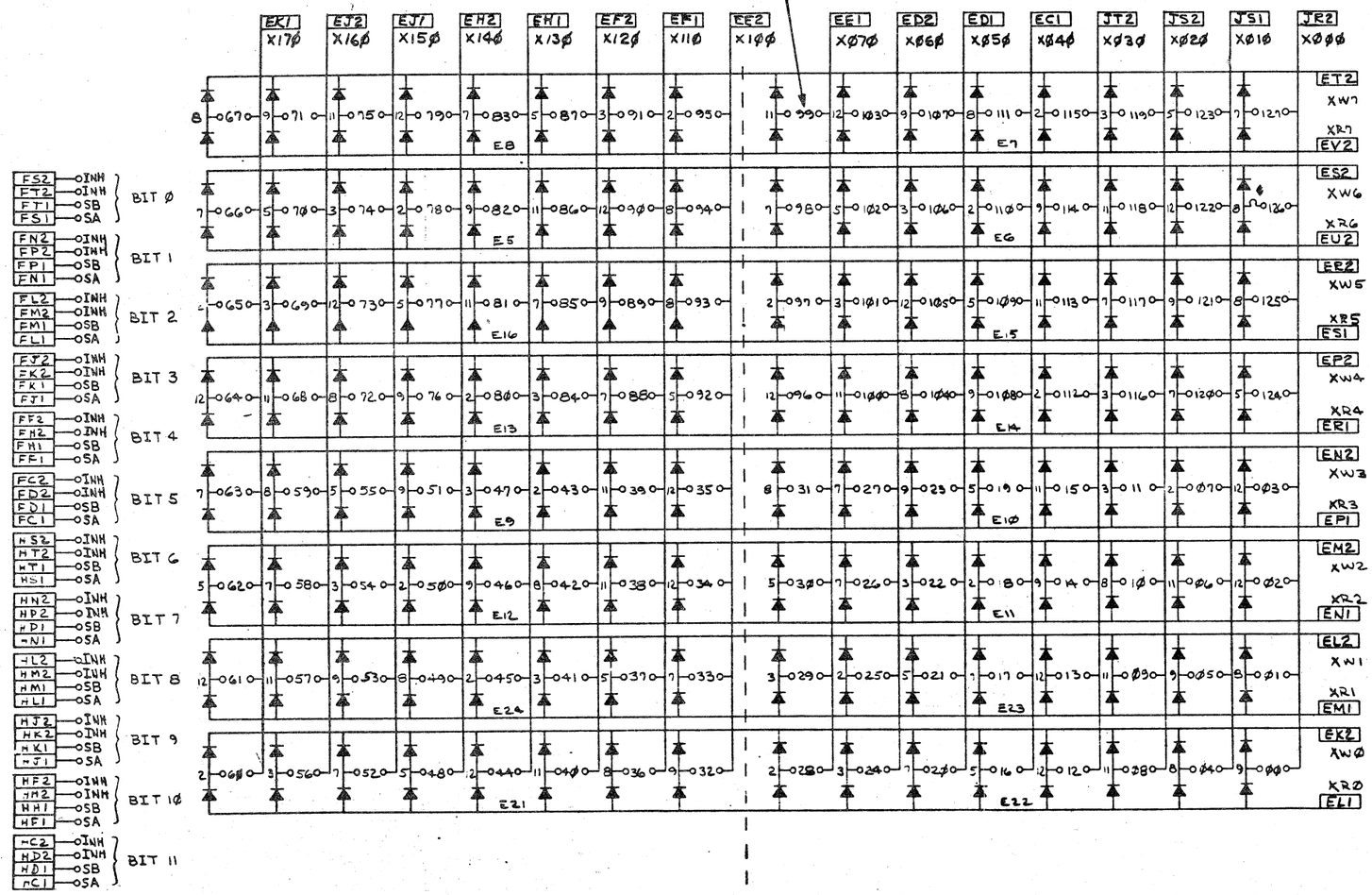
JUMPER LIST

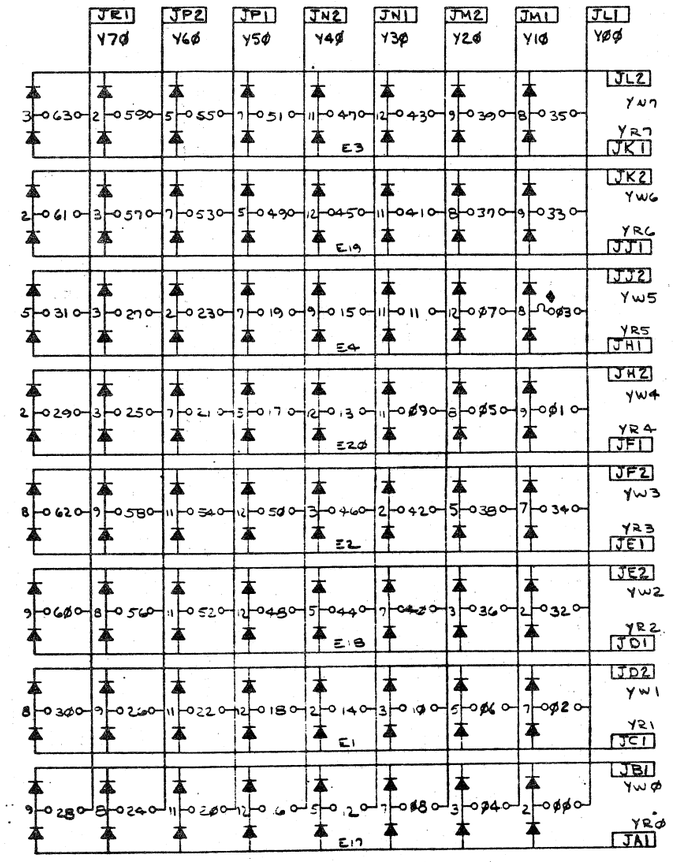


ETCH JUMPERS

JV2	HB1
JU2	HA1
EB1	EV2
EA1	EU2

NOTES:
1. UNLESS OTHERWISE SPECIFIED: IC'S E1-E24 ARE TO BE DEC STOCK# 25Ø1.
2. INDICATES STACK LINE NUMBER. (TYP)
3. INDICATES CURRENT LOOP.
4. INDICATES MAGNET WIRE TERMINATION(SOLDERED TO PC PAD).
5. 25Ø1-1 (DEC.PT. NO. 1912ØØ1Ø-Ø1) MAY BE USED INTERCHANGEABLY WITH ITEM #2





FIRST USED ON OPTION/MODEL: MM8-EJ	QTY.	DESCRIPTION: PARTS LIST	PART NO. / ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES: DECIMALS .XXX ± .005, .XX ± .02, .X ± .1; ANGLES ± 0° 30'	DRN.	DATE	EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
	CHK'D.	DATE	
	ENG.	DATE	TITLE: STACK SCHEMATIC 8K X 12BIT
	PROJ. ENG.	DATE	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	PROD.	DATE	
MATERIAL	NEXT HIGHER ASSY. B-DD-MM8-EJ		SIZE D CODE CS NUMBER H212-Ø-1 REV C
FINISH	SCALE		
	SHEET 2 OF 2		DIST.

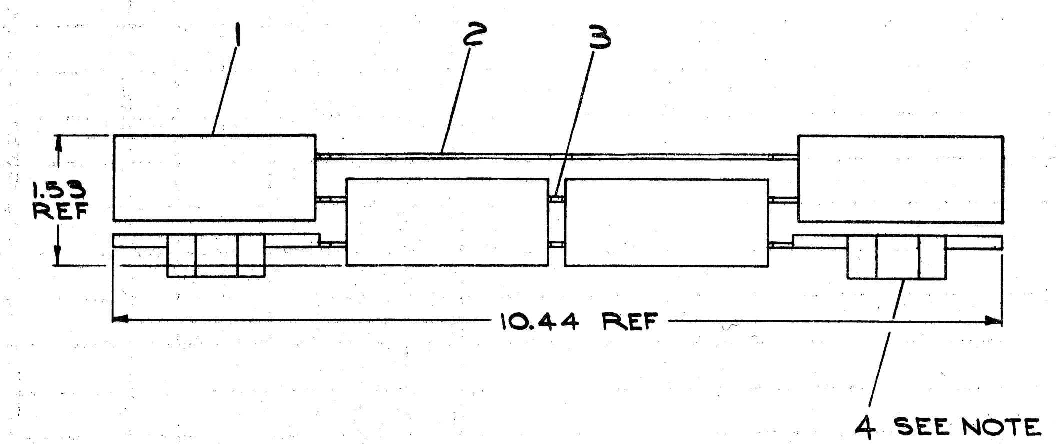
REVISIONS: REV | CHANGE NO. | CHK

BRUNING 40-888 19840

DEC FORM NO DBD 102-B

NOTES:

1. ITEM NO. 4 (SENSE INHIBIT G111 BOARD) MUST ALWAYS BE FACING THE FRONT OF THE MACHINE.



REF	ACCESSORY SHIPPING LIST	A-AL-MM8-EJ-4	5
1	SENSE INHIBIT	E-CS-G111-Ø-1	4
1	STACK ASSY	E-CS-H212-Ø-1	3
1	XY DRIVER	E-CS-G233-Ø-1	2
4	H851 EDGE CONNECTOR	B-UA-H851-Ø-Ø	1
QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION/MODEL: PDP8/E

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL: —

FINISH: —

DRN.	F. Carlsberg	DATE 4/13/72
CHK'D.	J. Toleyko	DATE 4-13-72
ENG.	W. Coates	DATE 5/23/72
PROJ. ENG.	W. Coates	DATE 5/23/72
PROD.	R. K.	DATE 6-7-72

NEXT HIGHER ASSY. B-DD-MM8-EH

SCALE 1/1 SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: 8K 12 BIT MEMORY

SIZE D CODE UA NUMBER MM8-EJ-0 REV A

DIST. G

REVISIONS

CHK	CHANGE NO.	REV
	MM8EJ-00001	A

W. COATES

DEC FORM NO DRD 102A

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ACCESSORY LIST

MADE BY	D. Kaney	CHECKED		SECTION	1
DATE	3/31/72	DATE	6-2-72		
ENG	W. Coates	PROD		ISSUED SECT.	1
DATE	4/4/72	DATE	6-2-72		

LEGEND

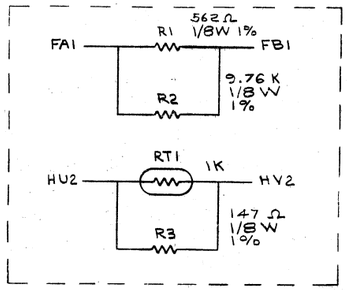
D DOCUMENT
DN DOCUMENT CHANGE NOTICE
PA PAPER TAPE ASCII
PB PAPER TAPE BINARY
PM PAPER TAPE READ-IN-MODE

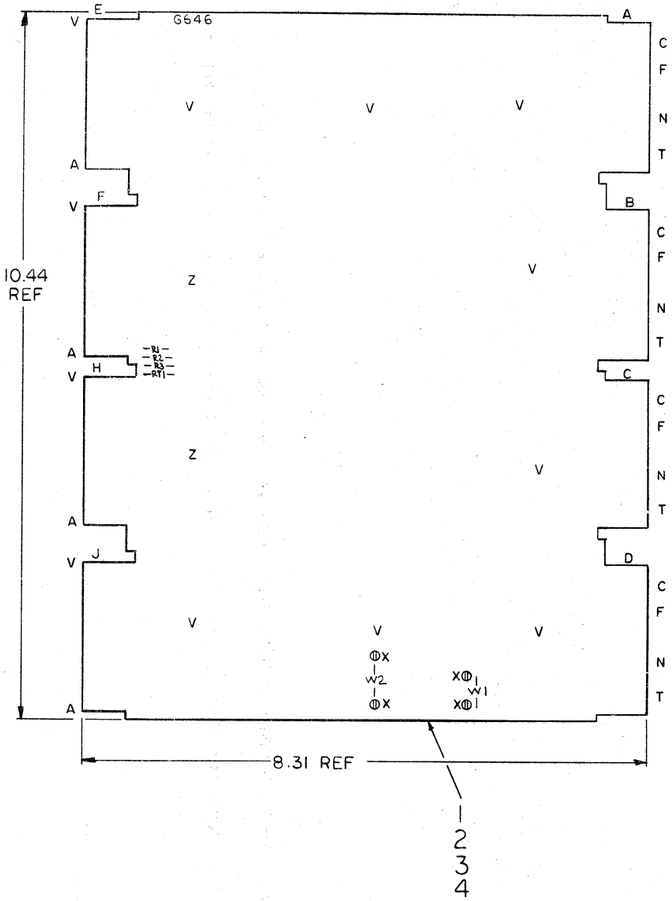
ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION MM8-E	MM8-EJ
1	B-DD-MM8-E	Print Set	1	1
2	DEC-8E-HR1B-D	Maintenance Manual *	1	1
3	Lib Kit- KM8E	Library Kit	1	1
4	H212	8K Stack Board		1
5	G111	8K Sense Inhibit Board		1
6	G233	8K XY Driver Board		1
7	H220	4K Stack Board	1	
8	G104	4K Sense Inhibit Board	1	
9	G227	4K XY Driver Board	1	
10	H851	Edge Connector	4	4
11	A-SP-MM8-EJ-4	Engineering Specification		1

KIT CHECK BY _____ DATE _____

INSTALLATION CHECK BY _____ DATE _____

TITLE	ASSY. NO.	SIZE	CODE	NUMBER	REV.	ECO NO
MM8-E Accessory Shipping List	SHEET 1 OF 1	A	AL	MM8-E-3		
		DIST.				





QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	R3	RES 147Ω 1/8W 1%	1302874	10
1	R1	RES 562Ω 1/8W 1%	1304693	9
1	R2	RES 9.76K 1/8W 1%	1309414	8
1	RT1	THERMISTOR 1K	1310071	7
4		EYELET (M-1033)	9006735	6
A/R	W1, W2	WIRE, 24AWG STRD TPC INS	91-0745-00	5
1		ETCHED CIRCUIT BOARD	5009842	4
REF		MODULE ECO HISTORY	B-MH-G646-0-6	3
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-G646-0-5	2
REF		X-Y COORDINATE HOLE LOC	K-CO-G646-0-4	1

PARTS LIST

ETCH BOARD REV C

REV	REVISIONS	CHANGE NO.	
A	ORIGINATED	G646-00001	R. Regan 3-2-72
B		G646-00002	W. Coates 3-2-72
C		G646-00003	R. Regan 10-17-72

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN. R. Regan DATE 10-17-72
CHK'D F. Raleigh DATE 2-17-72
ENG. W. Coates DATE 2-17-72
PROJ. ENG. W. Coates DATE 2-17-72
PROD. R. Regan DATE 2-17-72

NEXT HIGHER ASSY E-CS-H212-0-1

SCALE 1/1

SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE 12 BIT STACK BD

SIZE D | CODE CS | NUMBER G646-0-1 | REV. C

DIST.

DEC FORM NO DRD-135

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 6/1/72

TITLE MM8-EJ ACCEPTANCE PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	APPD	SIZE	CODE	NUMBER	REV
S.S. for W. Cotay	Richard D. O.	A	SP	MM8-EJ-1	

DEC 16-(392)-1079-N971
DRA 107

1.0 SCOPE

1.1 This procedure defines the minimum performance standards required of a MM8-EJ option which is not accepted as an integral part of a PDP8/E, i.e. add-on options.

2.0 SET UP

2.1 Remove the four (4) edge connectors from the tops of the G111, H212 and G233 (MM8-EJ) modules.

2.2 Inspect the G111, H212 and G233 (MM8-EJ) modules for conformance to "Final Inspection Procedure for Flip-Chip Modules" (A-SP-7665039-0-0) and "Module Rework Standard" (A-SP-7605845-0-0).

2.3 Check the G111 and G233 modules for a legible three character numerical date code.

2.4 Check the G111 and G233 modules to insure the circuit and etch revisions are up to current ECO levels. Make sure all EMA jumpers on the G111 module are installed.

2.5 Inspect the G111 to make sure a center strobe position is stamped on the module.

2.6 Insure that strobe switch is set to center position indicated on the G111.

2.7 Ascertain that the MM8-EJ option has been checked out in heat and vibrated by Production.

2.8 Make sure the power to the PDP8/E is turned OFF.

2.9 Insert the G111, H212 and G233 (MM8-EJ) modules into the omnibus. Be sure you adhere to the "Recommended Omnibus Assignment List" (A-SP-PDP8-E-0-4).

SIZE	CODE	NUMBER	REV
A	SP	MM8-EJ-1	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

2.10 Connect the MM8-EJ modules together using the four (4) edge connectors. The G111 should be in front, the H212 in the middle and the G233 third.

3.0 ELECTRICAL TEST

3.1 Turn on power to the PDP8/E.

3.2 Follow the loading procedure for PDP8/E Extended Memory Data and Checkerboard Test (MAINDEC-Ø8-DHKMA).

3.3 Run the diagnostic following the instructions in the program write-up, this test must run error free for a minimum of 20 minutes.

3.4 At the completion of 3.3 halt the PDP8/E by raising SRØ5 and turn off the power to the PDP8/E.

3.5 Remove the two (2) edge connectors that connect the G111 and H212 together.

3.6 Remove the G111 module from the omnibus.

3.7 Turn strobe switch one position clockwise from the center position that is indicated on the G111 module. Reinsert the G111 module into the omnibus.

3.8 Reconnect the G111 and H212 modules using the two (2) edge connectors.

3.9 Repeat 3.3 through 3.6.

3.10 At the completion of 3.6 turn strobe switch one position counter-clockwise from the center position that is indicated on the G111 module. Reinsert the G111 module into the omnibus.

3.11 Repeat 3.8.

3.12 Repeat 3.3 through 3.6.

3.13 At the completion of 3.6 return strobe switch to the center position indicated on the G111 module.

3.14 Reinsert the G111 module into the omnibus.

3.15 Repeat 3.8.

3.16 Follow the loading procedure for PDP8/E Extended Memory Address Test (MAINDEC-8E-D1FB).

3.17 Run the diagnostic following the instructions in the program write-up. This test must run error free for a minimum of 20 minutes.

3.18 If the construction requisition specifically states a particular memory field is desired, have production cut the appropriate EMA jumper or jumpers.

4.0 FAILURE CLASSIFICATION

4.1 Mechanical Failure:

4.1.1 Any G111, H212 or G233 (MM8-EJ) module that does not meet the criterion outlined in 2.1, 2.2, 2.3, 2.4 and 2.5 will be classified as a failure.

4.1.2 The acceptance supervisor has the option of either waivering the failure (using DEC form 12-1026) or returning the defective module or modules to production for repair.

4.2 Electrical Failure:

4.2.1 Any MM8-EJ (G111, H212 and G233 module) which while performing 3.3, 3.17 halts, generates error printouts, garble or runs other than continuous and as specified in the diagnostic write-up will be classified defective and returned to production for repair.

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

1.0 MEMORY SYSTEM - GENERAL DESCRIPTION

The 8K PDP8/E core memory (designated MM8/EJ) is a random access, coincident-current, magnetic READ/WRITE core memory with cycle times of 1.2 μs and 1.4 μs. The memory comprises ferrite cores wired in a 3-D, 3-wire, planar configuration. The unit can store up to 8192 (8K) 12-bit words. The memory can be expanded to 32K words.

2.0 MEMORY SYSTEM - FUNCTIONAL DESCRIPTION

The memory system performs three basic functions for the PDP8/E processor:

a) It decodes and selects the desired core location in which a 12-bit word is stored or will be stored,

b) It reads a 12-bit word from the selected location, and

c) It writes a 12-bit word into the same selected location.

These functions are illustrated in Figures 1 and 2, for which one memory cycle is represented. The processor must first supply the address (refer to Chapter 4 of the Small Computer Handbook) before a read or write operation can be considered. The CPMA Register is loaded at time TP4, and the contents of the CPMA

are placed on the Memory Address (MA) lines. Memory address decoders receive the MA bits and turn on the corresponding Read current switch when control signals RETURN, SOURCE, and WRITE (Not) are present. The Memory Register is cleared early in the READ portion of the memory cycle.

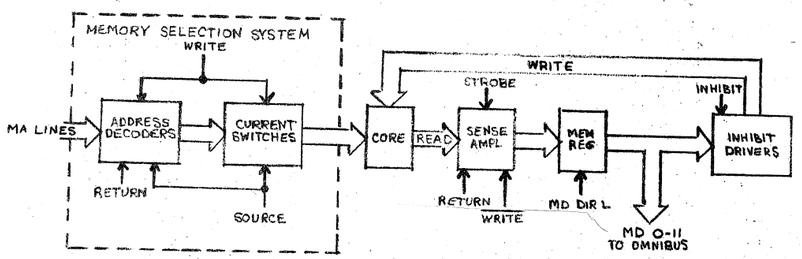


Figure 1 Memory System Functional Flow Diagram

The outputs from the 12 selected cores are fed to their respective sense amplifiers. A strobe signal is used to gate the Sense Amplifier into the local Memory Register. If MD DIR is low (as it always is during the READ portion of the memory cycle), the output of the Memory Register is placed onto the Memory Data (MD) lines. During the WRITE portion of the memory cycle, the memory selection system uses the same address inputs and control signals; however, control signal WRITE will change states, causing the write current switches to be activated. To write the content of the Memory

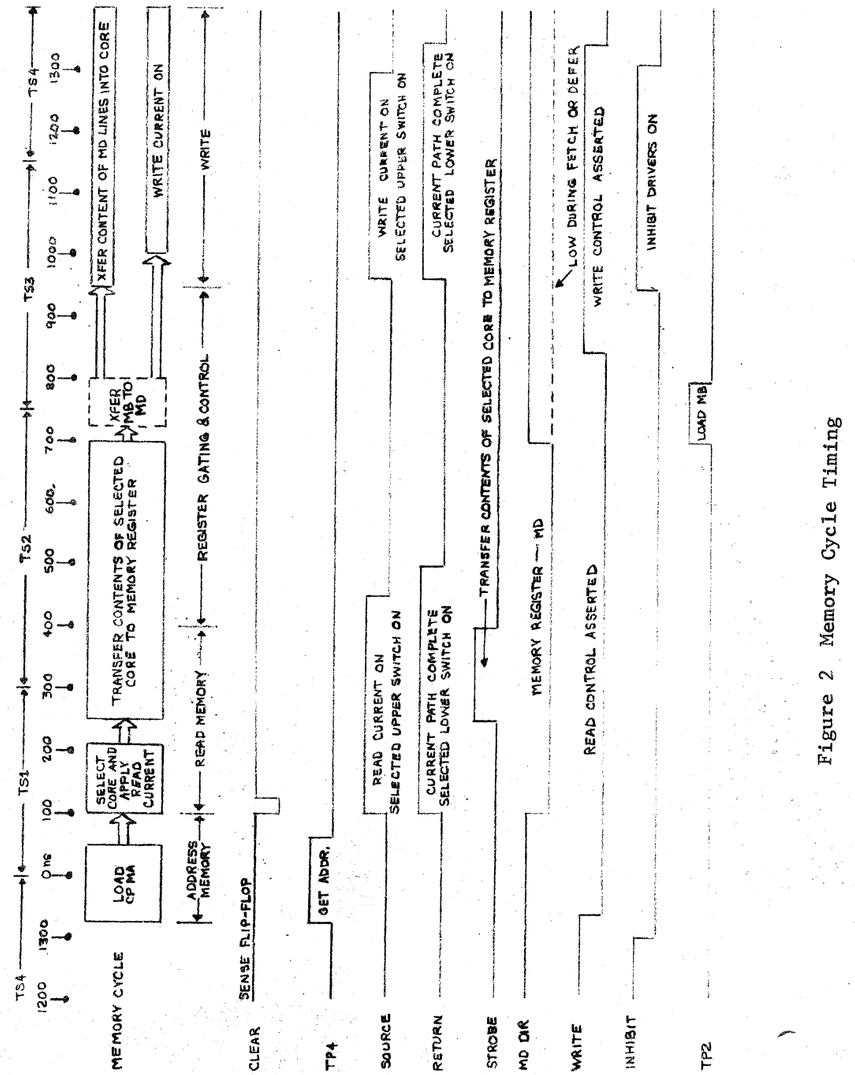


Figure 2 Memory Cycle Timing

Register back into core, MD DIR will be low (active). Otherwise, the contents of the MB Register (within the CP or an active break device) will be placed on the MD lines, and the word in the MB Register will be written into core. The INHIBIT signal controls the gating circuits, and only when INHIBIT is active will the Inhibit Drivers be activated. A Ø received from the MD lines and INHIBIT will cause the corresponding Inhibit Driver to produce inhibit current.

3.0 MEMORY SYSTEM - DETAILED THEORY

The organization of the memory system is illustrated in Figure 3. Three QUAD-size boards are used to contain the memory system as follows:

a) Sense/Inhibit G111 contains 12 Sense Amplifiers, Memory Registers, and Inhibit Drivers with the corresponding control logic, slice control, -7V supply for the Sense Amplifiers, and current control;

b) Memory Stack G646 contains 12 mats of 8192 cores per mat, and X/Y diode selection matrix;

c) X/Y Driver and Current Source contains address decoding and selection switches, X-current source, Y-current source, and stack discharge switch-power ON/OFF protection circuit.

The detailed theory of core memory, memory selection system, and the memory sense/inhibit function are described in the following paragraphs.

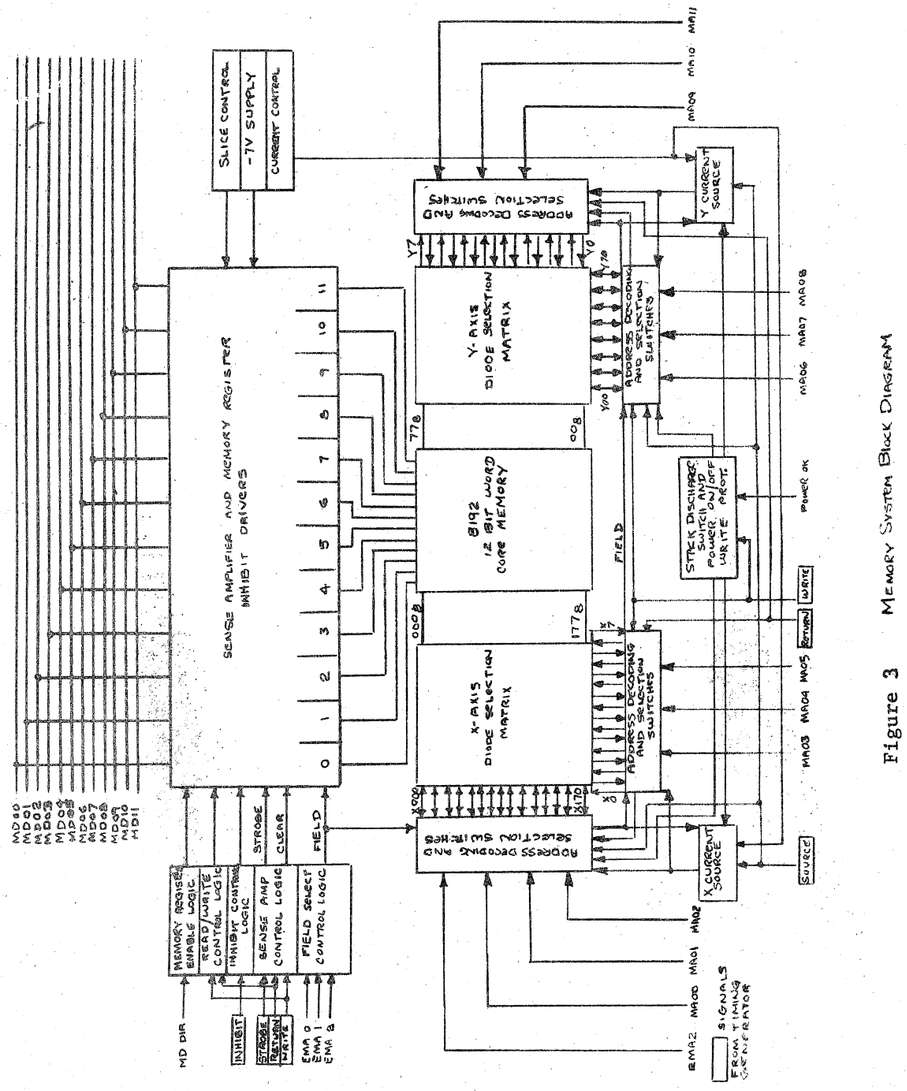


Figure 3 Memory System Block Diagram

4.0 CORE MEMORY

The basic storage element in the MM8/EJ Memory System is a small toroidal (ring-shaped) piece of magnetic material, called a magnetic core. A single core, mounted on a ground plane, is illustrated in Figure 4. Three wires pass through each core to accomodate the X- and Y-selection, and the sense/inhibit function. A primary difference between the PDP8/E and its predecessors is the combination of the SENSE line with the INHIBIT line to form a three-wire system instead of a four-wire system.

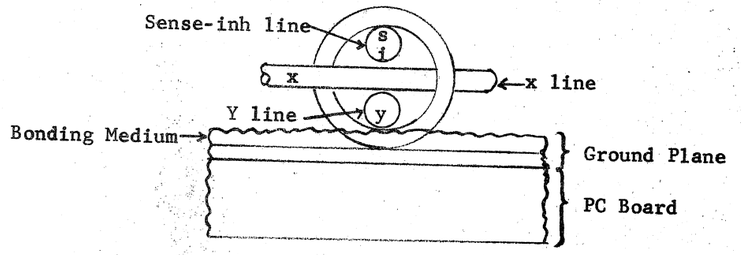


Figure 4 Magnetic Core

4.1 Hysteresis Loop

The characteristics of the magnetic core can be shown by a graph, plotting the current (the magnetizing force) versus flux-density (the resulting magnetism) hysteresis loop as illustrated in Figure 5. This hysteresis loop illustrates the magnetizing current I, produced by the current contained

in the three wires plotted along the horizontal axis, and the resulting flux density B through the core along the vertical axis. Two directions of current are shown. READ current, with respect to the graph, is directed from right to left. If a logic 1 is stored in the core, B will move from the remanent point ($+B_r$) down to saturation at $-B_m$ when the READ current is turned on. When the magnetizing current is removed, the flux density settles down to the remanent point at $-B_r$. WRITE current is directed from left to right with respect to the graph. If a 1 is to be written into core, the flux density will move from $-B_r$ to point $+B_m$ on the graph and then settle down to $+B_r$ when the magnetizing current is removed. Thus, points $-B_m$ and $+B_m$ are the extreme points of saturation, and points $-B_r$ and $+B_r$ are the extreme points in the normal logic states.

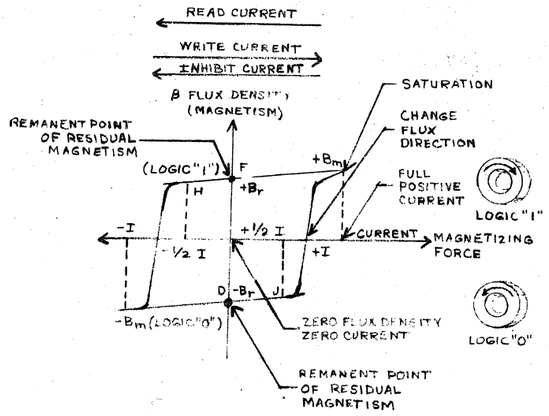


Figure 5 Magnetic Core Hysteresis Loop

4.2 X/Y Select Lines

Saturation of a core occurs only when both the X- and Y-select lines each contain half the amount of current required to reach saturation. This is called the coincident current technique and results in a fully-selected core. If either the X- or Y-line contains no current, there is no significant change in the flux density. For example, for a READ, if the core is in logic 1 state, the flux change is from point $+B_r$ to H on the graph and then reverts back to point $+B_r$. For a WRITE, the flux change is from point $-B_r$ to point J and then reverts back to $-B_r$.

4.3 READ Operation

READ occurs during the first half of the memory cycle. Its function is to sample either a logic 1 or logic Ø in a fully-selected core. Thus, both the X- and Y-Read half-select currents must be applied for the sense/inhibit line to receive a pulse resulting from a change in flux density if the core is in the logic 1 state. If the core is in the logic Ø state, no change in flux density occurs and, therefore, no pulse appears on the sense/inhibit line.

4.4 WRITE Operation

WRITE occurs during the second half of the memory cycle. Because WRITE follows READ, the cores at the selected address have been cleared to a logic Ø state. If the fully-selected

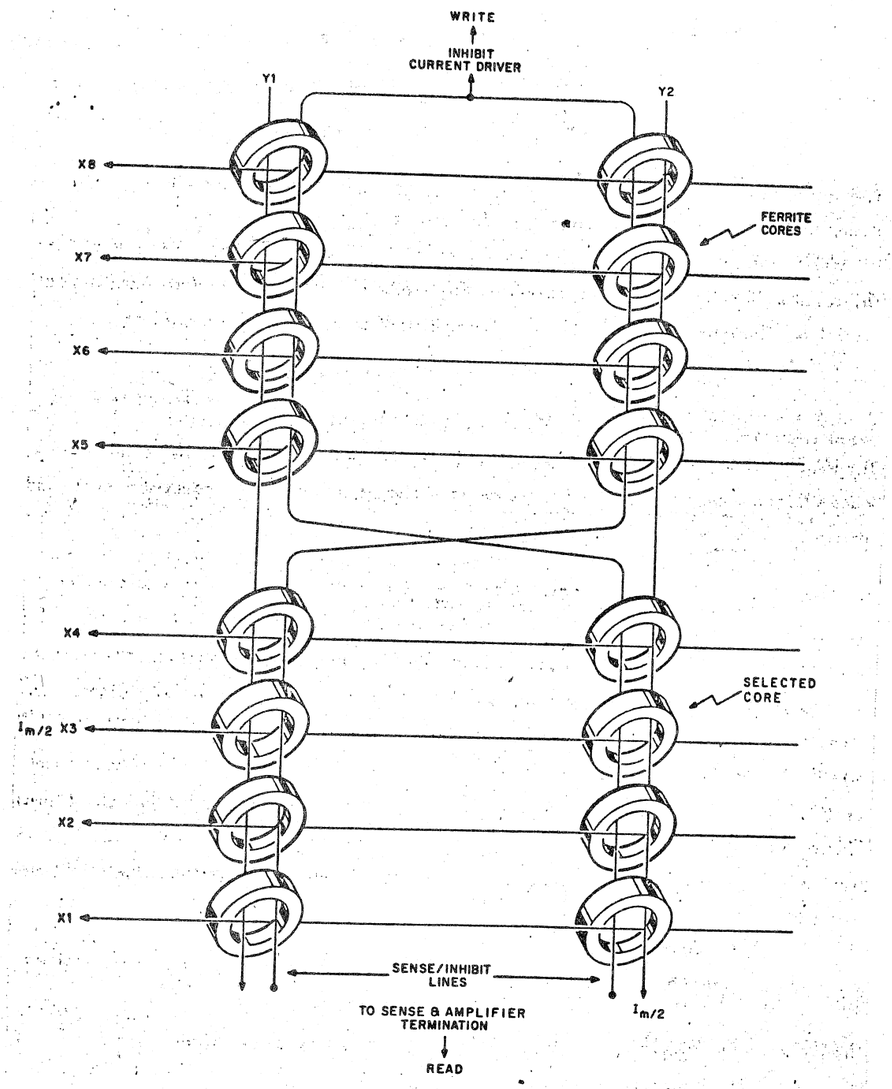


Figure 6: Three-Wire Memory Configuration

core is not inhibited, the magnetic flux moves from point $-B_r$ to $+B_r$ on the graph, and a 1 is stored in core. However, to store a Ø into core, it is necessary to cause a less than fully-selected condition. This is achieved by generating an inhibit current and applying this current to the sense/inhibit line. This inhibit current is in the opposite direction to the Y-WRITE current. The net result of the change in flux will be from point $-B_r$ to point J on the graph. When all currents are removed, the flux density reverts back to $-B_r$ on the graph.

4.5 Magnetic Core in Two-Dimensional Array

A partial three-wire memory configuration is illustrated in Figure 6. Half-select currents are produced for one X-line and one Y-line. If, for example, the core at X3, Y2 is selected, the corresponding wires going through each row would contain half-select current. For the X3 row, X3, Y1 core would contain only half-select current, and X3, Y2 core would contain full-select current. All other cores in row Y2 would contain half-select current. The sense/inhibit line terminates at the Sense Amplifier and the Inhibit Driver in the manner shown in Figure 6.

Current direction is from the top of the illustration down to the Sense Amplifier. For WRITE, the current direction is from the bottom of the illustration to the top to the Inhibit Current Driver. This direction opposes the current in the Y-selection line and, therefore, causes a half-select condition. This half-select procedure is only required where a Ø is to be written into core.

4.6 Assembly of 12-Stacked Core Mats

The MM8/EJ memory is a 128 x 64 configuration (128 X-Rows and 64 Y-Rows). This configuration provides 8192 cores per mat, for which one core may be selected during any one memory cycle and, therefore, one bit of information per mat.

The MM8/EJ is a 12-bit word memory system; thus, 12 mats are used. Each mat stores one unique bit of information, which is deposited and sensed by one unique line called the sense/inhibit line. Thus, 12 sense/inhibit lines are used to deposit and sense 12 unique bits of information. The arrangement of the selection lines are quite different. All 12 mats contain 128 X-lines and 64 Y-lines. The threading of each of the X- and Y-lines continues from one mat to the next through all 12 mats. For example, row X31 of mat Ø is common to row X31 of mat 1, which is common to all subsequent mats at row X31. The common factor to each mat is the selection line that is threaded through 12 times (64 or 128 cores or (768 or 1536 cores). The

intersection of X31 and X29, therefore, occurs 12 times in the 12 mats. Because each mat contains a unique sense/inhibit line, 12 unique bits of information can be stored and sensed to form a 12-bit word.

4.7 Physical Orientation of Core Memory

The layout of memory stack is illustrated in Figure 7. Figure 8 illustrates the X- and Y-windings within the memory stacks.

5.0 CORE SELECTION SYSTEM

Core selection is accomplished by enabling the desired X-line and the desired Y-line and allowing current to pass through the selected lines. To accomplish the selection of the X- and Y-lines, a decoding network that receives the memory address bits and decodes for line selection is required. An X- and Y-current source is also required so that each line has a half-selected current.

A selection system functional block diagram illustrating the parts of the memory system involved in core selection is given in Figure 9. The primary components involved are:

a) the memory address decoder, which receives memory address bits and control signals to select (enable) the corresponding switch and driver,

b) a current source to provide the necessary select current,

c) a driver and switch to apply current to the selected row and forward-bias the selection diode,

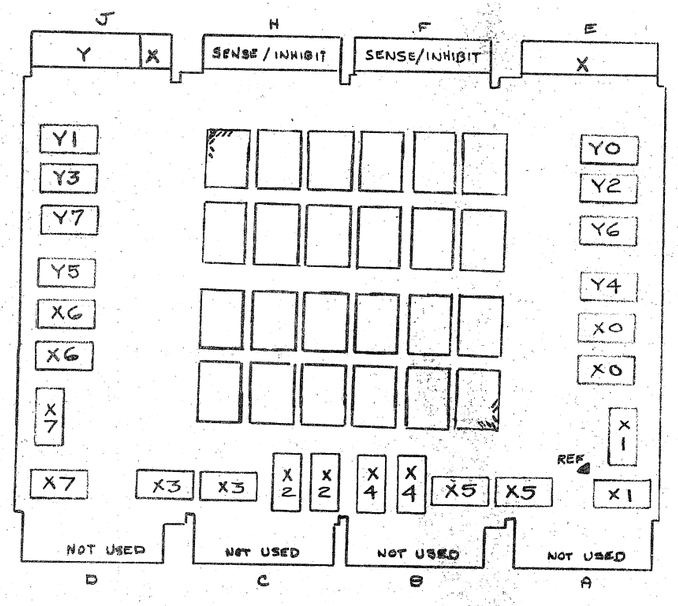


Figure 7 Memory Stack Layout (Core Orientation)

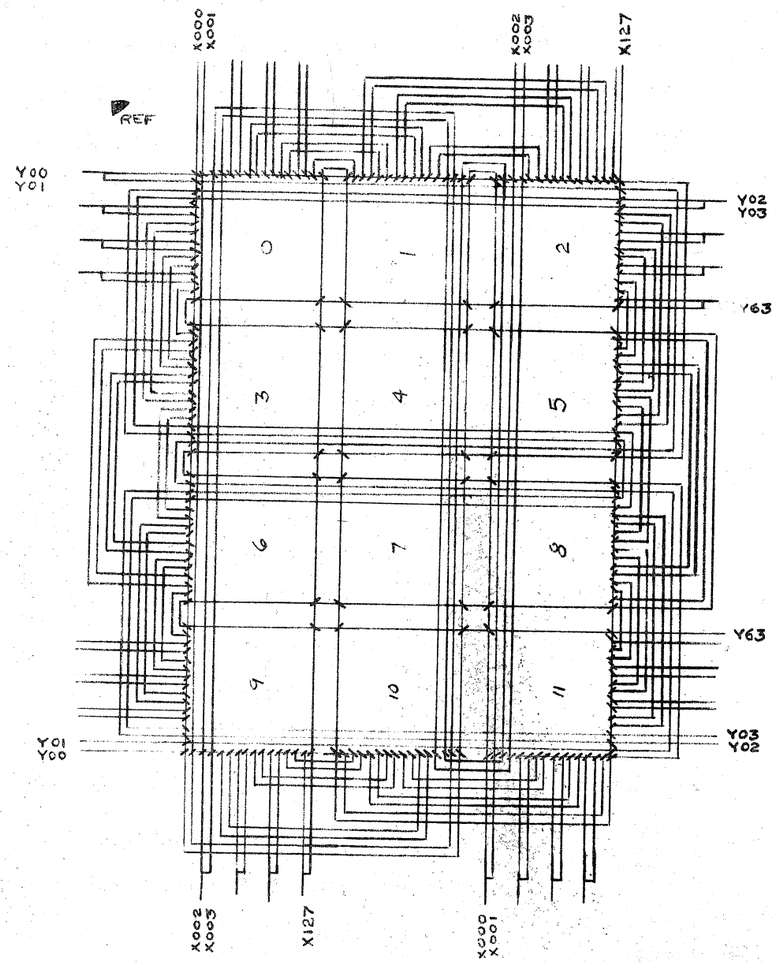


Figure 8 Memory Stack X, Y Windings

d) one read or write diode, which becomes forward-biased by the driver and switch while all other diodes are back-biased, and

e) one selected row containing 768 cores (or 1536 cores if a Y-line).

The driver and switch shown in Figure 9 are one of 24 drivers and one of 24 switches. A WRITE operation for row X13 is illustrated to show the current path.

Both the READ and WRITE current paths are illustrated in Figure 10. Although not all of the circuitry is shown, the current path relationship between a READ and WRITE operation (Figure 10) illustrates how the direction of current for WRITE is opposite to the direction for READ. The illustration also shows how the unselected components are interconnected but passive.

NOTE: Electron Current flow is presented in this manual. The reader should consider current originating at a more negative voltage level and taking the path to a more positive voltage level. A forward-biased diode results when the current takes the direction opposite to the diode arrow.

5.1 Organization of X/Y Drivers and Current Source

Figure 11 illustrates the organization of the X/Y drivers and current source, and the primary signals required to make line selection and current switching possible. Ten decoders are used to select one of 128 X-lines and one of 64 Y-lines as determined by the content of MA bits Ø through 11 and EMA 2.

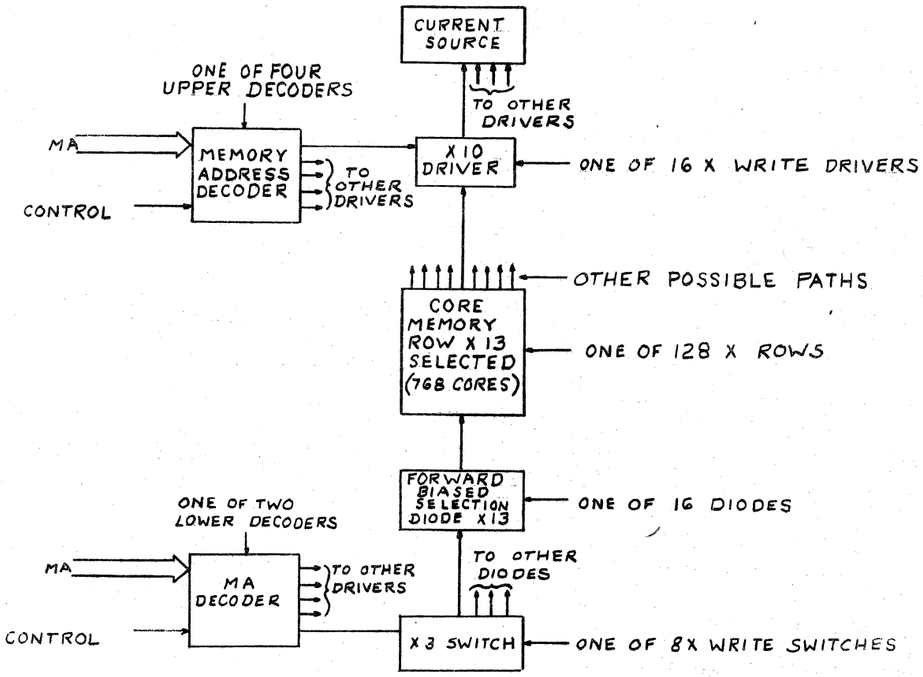
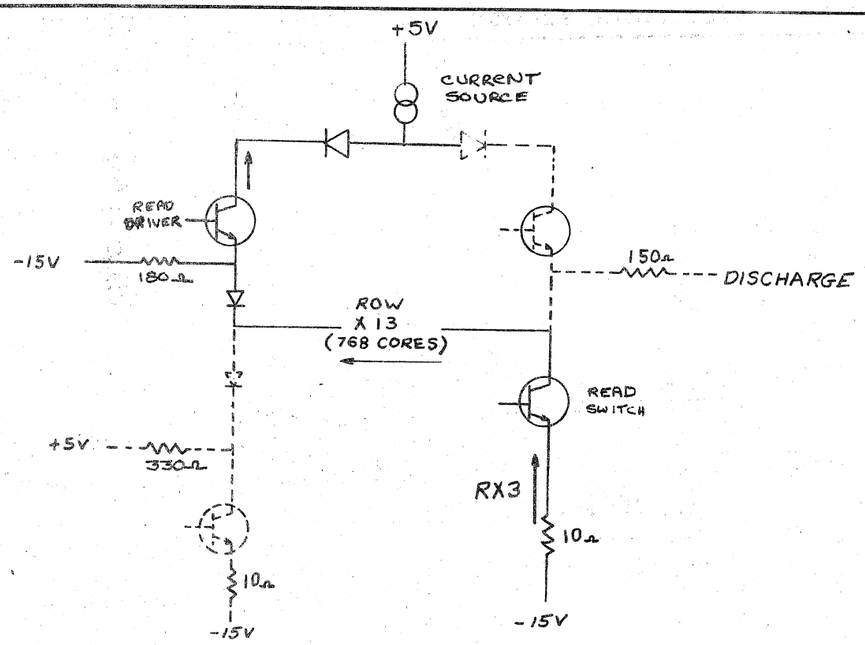
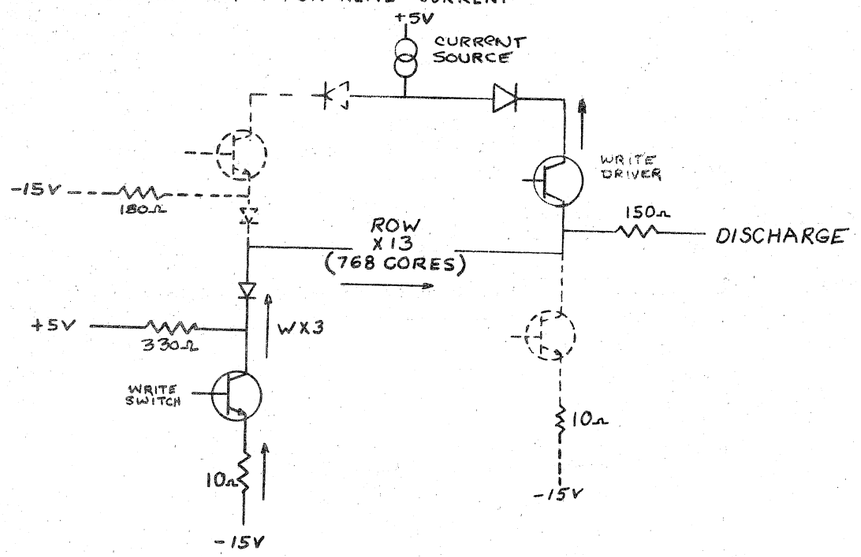


Figure 9 Selection System Functional Block Diagram for Write Current of X Rows



(a) CURRENT PATH FOR READ CURRENT



(b) CURRENT PATH FOR WRITE CURRENT

FIGURE 10 READ/WRITE CURRENT PATHS

X-current and Y-current, provided by the X- and Y-current source are applied to the drivers. The READ signal is applied to both the decoder control gates and the Bias Driver. When a READ operation is to be performed, the selected READ switches and drivers are enabled and the READ/WRITE current switch changes its output signal from ground to -15V. The negated READ signal acts to enable the WRITE function in a similar manner.

5.2 X- and Y-Current Sources

The X- and Y-current sources supply constant current to the READ and WRITE drivers (Figures 12 and 13). The X- and Y-current sources receive bias voltage from the current control circuit located on the sense/inhibit board and are turned on when both FIELD and SOURCE are active. They have a slow turn-on rate and a fast turn-off characteristic due to the capacitor in the circuitry. A fast turn-off is achieved by the interaction between the capacitor and two transistors. When SOURCE is negated, one of the transistors is turned on, causing the capacitor to discharge, which causes the output transistor to be biased off. The slow turn-on time reduces the coupling effects within the core stack. Furthermore, the slow turn-on time also means that the READ current is completely controlled by the current source. Because the current source is controlled, the position of the sense output voltage relative to the drive currents is constant.

5.3 Bias Driver

The Bias Driver (Figure 14) switches the bias voltage from ground for a READ operation to -15V for a WRITE operation. When control signals READ (H) and X FIELD are both active, level shifting circuits along with an output transistor switch the output to ground. When READ (H) is not asserted, the output switches to -15V. The Bias Driver provides the reverse bias condition on the nonselected diodes in the memory stack. Reverse biasing the diodes reduces the capacitance and, therefore, reduces the "sneak currents" that might be on the line. See Paragraph 5.7 for the organization of the planar stack diode matrix.

5.4 Power Fail Circuitry

The power fail circuitry (Figure 15) responds to the POWER OK signal from the power supply. Its primary function is to ensure that selected memory locations are not changed due to a power failure. The power supply senses a voltage change when the dc voltage drops and grounds the POWER OK (H) line when the voltage is too low. This shuts off the timing chain but ensures that the memory cycle is completed. In the memory power fail circuitry, power fail circuitry turns off the X- and Y-current source after a sufficient delay to complete the WRITE operation. When the machine is turned on initially and the POWER OK (H) signal is asserted, the current source is immediately activated.

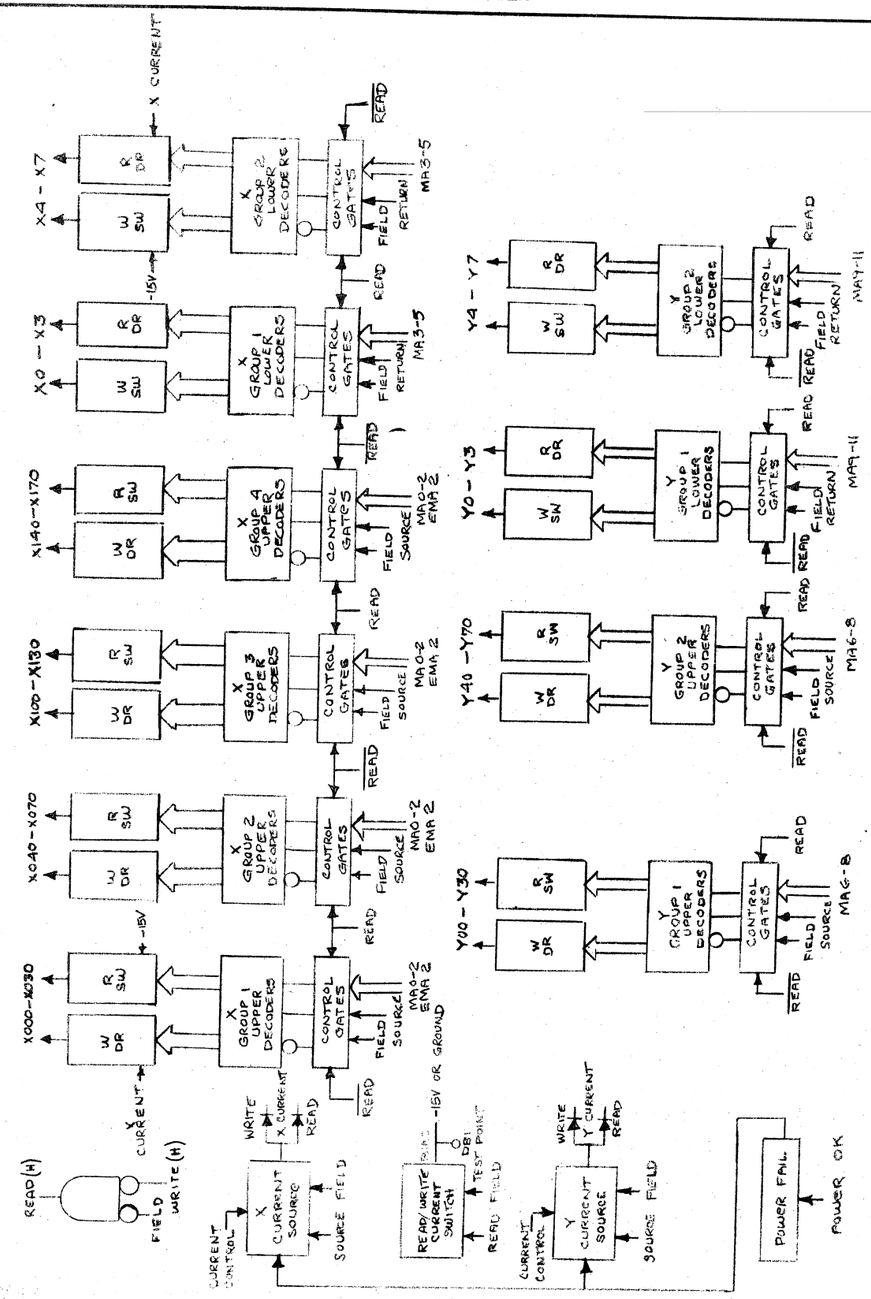
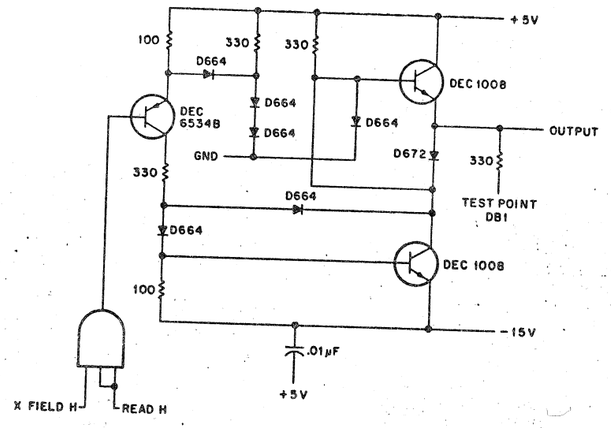
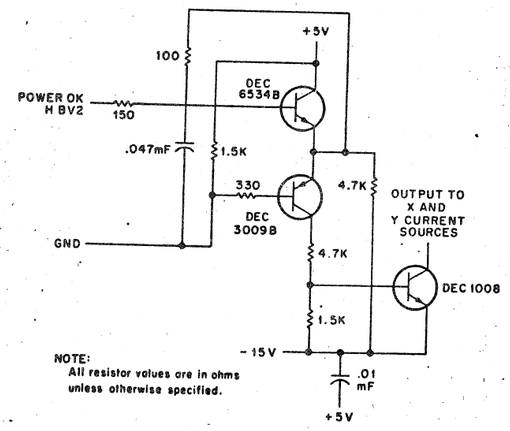


Figure 11 XY Drivers and Current Source (Block Diagram Representation of G233 Circuit Schematic)



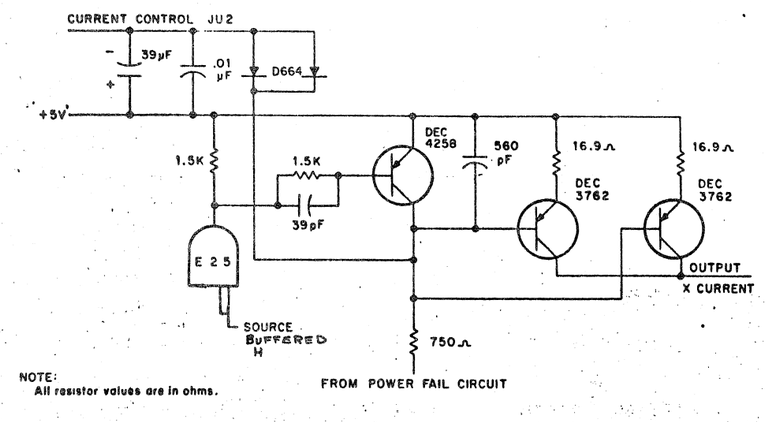
NOTE:
All resistor values are ohms.

Figure 14: Bias Driver



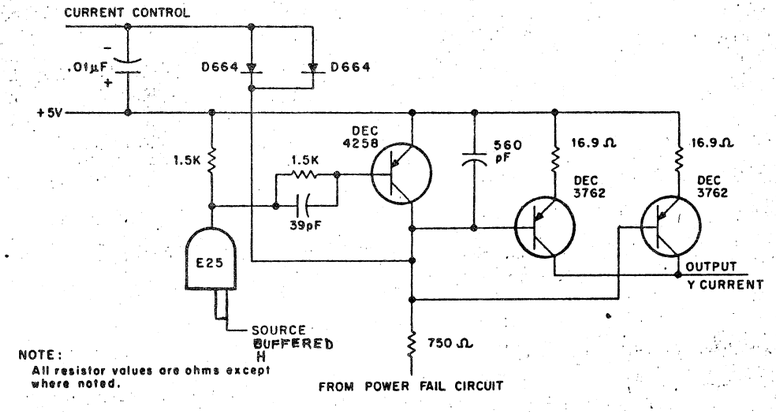
NOTE:
All resistor values are in ohms unless otherwise specified.

Figure 15: Power Fail Circuit



NOTE:
All resistor values are in ohms.

Figure 12: X-Current Source



NOTE:
All resistor values are ohms except where noted.

Figure 13: Y-Current Source

Thus, the memory power fail circuit has a characteristic of a fast-on and slow-off switch.

5.5 Core Selection Decoders

Ten decoders (IC7442) (Figure 11) are used to decode the memory address bits Ø through 11 and EMA 2 from the Memory Address Register. These bits are combined with READ, FIELD, SOURCE, and RETURN signals to enable the appropriate switch and driver. Signal READ is generated when WRITE is not asserted, or negated READ results when WRITE is active. The WRITE signal is developed in the Timing Generator during the last half of the memory cycle. SOURCE is necessary to turn on the selected driver or switches corresponding to the upper X- and Y-select lines, and RETURN is necessary to turn on the selected drivers or switches corresponding to the lower X- and Y-select lines. Both RETURN and SOURCE are developed in the Timing Generator. RETURN remains on for 50 ns longer than SOURCE so that the lines completely discharge. FIELD is developed in the Sense Inhibit board by decoding the two most significant extended memory address lines (EMA Ø and 1).

5.6 Address Decoding Scheme

The block diagram in Figure 11 illustrates the method through which the MA bits are decoded; the results enable either a WRITE driver or READ switch and the corresponding driver or switch counterpart required to complete the current path. The

decoder is arranged as follows: the upper select line decoders are on the left-side and the lower select line decoders are on the right-side of the illustration. The upper X-select line decoders decode bits EMA 2, while the lower X-select line decoders decode bits MA 3-5. The upper Y-select line decoders decode bits MA 6-8, while the lower Y-select line decoders decode bits MA 9-11. There are a total of sixteen upper X-select lines, eight upper Y-select lines, eight lower X-select lines, eight lower Y-select lines. The decoder outputs are applied to the selected switches. The outputs of the selected switches connect to the X-selection diodes (refer to Paragraph 5.7) which, in turn, is connected to a line that is threaded through 768 memory cores. The arrangement of the illustration (Figure 11) is such that each component corresponds to the approximate location on the engineering drawing schematic (G233). This arrangement allows a quick reference to the circuits of interest. The decoding scheme of the memory address bits is illustrated in Figure 16. The illustration shows the five parts of the memory address. Table I lists the necessary input control signals, the content of the memory address, the input pins, the output pins, and the selected X- or Y-line. With this information, the user can easily trace through all of the components on any signal/current path to find the selected components.

TABLE I
Core Selection Decoding Scheme
Upper X and Y Decoders

Y	X	7442 Input Pins: MA6 MA7 MA8	Group 1: D3 D2 D1 DØ	Group 2: D3 D2 D1 DØ	Group 3: D3 D2 D1 DØ	Group 4: D3 D2 D1 DØ	Selected Line: X	Selected Line: Y
		EMA2 MA0 MA1 MA2	MA3 MA4 MA5					
		H H H H	L * L L				000	00
		H H H L	L * L H				010	10
		H H L H	L * H L				020	20
		H H L L	L * H H				030	30
		H L H H		L * L L			040	40
		H L H L		L * L H			050	50
		H L L H		L * H L			060	60
		H L L L		L * H H			070	70
		L H H H			L * L L		100	
		L H H L			L * L H		110	
		L H L H			L * H L		120	
		L H L L			L * H H		130	
		L L H H				L * L L	140	
		L L H L				L * L H	150	
		L L L H				L * H L	160	
		L L L L				L * H H	170	

L=Gate Enable
H=Gate Disable
* L=WRITE, H=READ

TABLE I (Cont'd)
Core Selection Decoding Scheme
Lower X and Y Decoders

Y	X	7442 Input Pins: MA 9 MA10 MA11	Group 1: D3 D2 D1 DØ	Group 2: D3 D2 D1 DØ	Selected Line: X	Selected Line: Y
		MA3 MA4 MA5				
		H H H	L * L L		0	0
		H H L	L * L H		1	1
		H L H	L * H L		2	2
		H L L	L * H H		3	3
		L H H		L * L L	4	4
		L H L		L * L H	5	5
		L L H		L * H L	6	6
		L L L		L * H H	7	7

L=Gate Enable
H=Gate Disable
* L=WRITE, H=READ

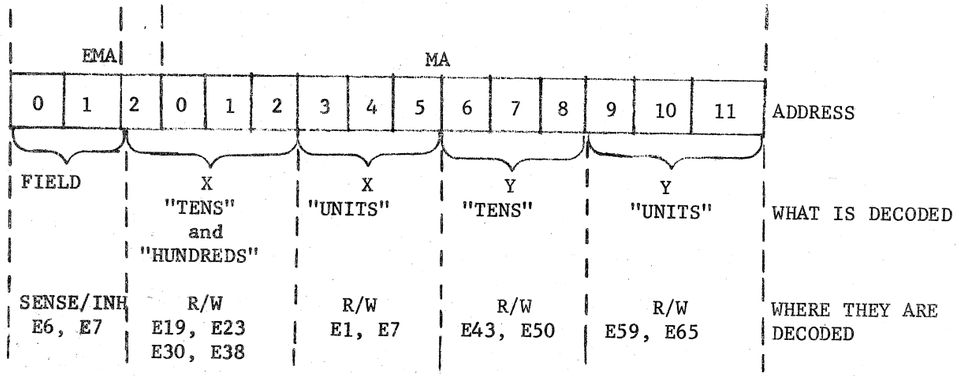


Figure 16 Decoding Relationships

5.7 Operation of Diodes

Each of the X- and Y-select lines are connected to a corresponding string of diodes (see Figure 17). Selection is such that any one of the upper select lines will pass current in a path determined by whether the operation is a READ or WRITE. In the illustration given in Figure 17, for the X-selection, the example illustrates line X_{12} being selected. The current passes through 768 cores and back through one of the diodes. The path the current takes from this point is determined by the diode that is forward-biased. The forward-biasing of a diode is accomplished by the operation of a switch and driver. If the operation is WRITE, WX2 is forward-biased, and the current takes the path from WX2 to X10. If the operation is READ, RX2

is forward-biased, and the current takes the path from RX10 to RX2.

NOTE: The READ and WRITE currents are opposite in direction through the core. This is accomplished by signal READ, which controls the Bias Driver circuit.

In both cases, the selection diodes are instrumental in determining the current path. All diodes except the selected diode are reverse-biased.

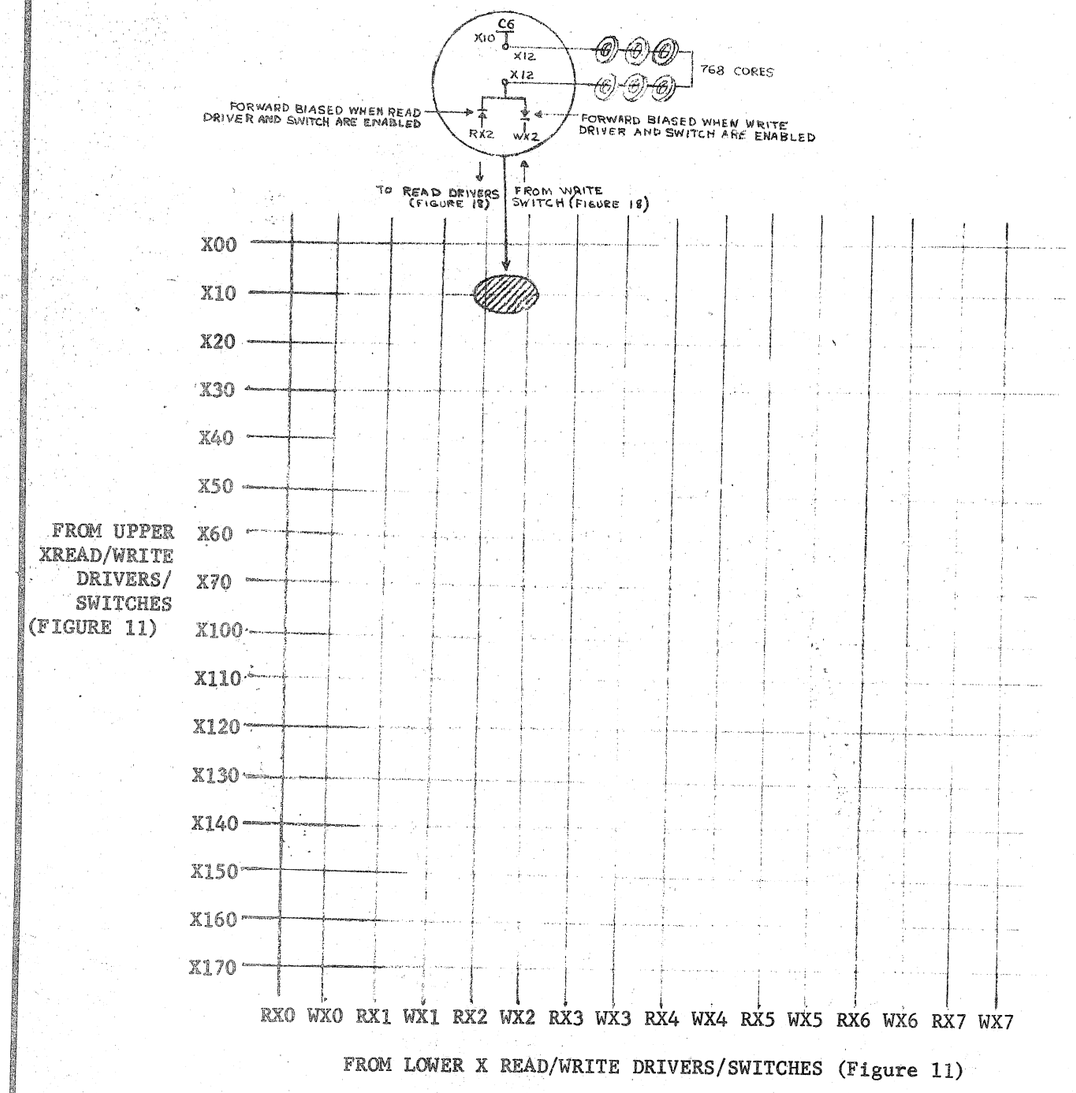


Figure 17 Organization of Planar Stack Diode Matrix for X Select Lines

5.8 Operation of Selection Switches

Figure 18 illustrates the switching operation of the currents through X12 select line. On the upper side, a pair of transistors are used to either drive or switch current, depending on whether the operation is READ or WRITE. A complementary pair of transistors on the lower side are used to either drive or switch the current. Between the upper and lower side is a line that is threaded through 768 cores. The READ operation begins with the decoders. When an X-line such as X12 is to be selected, the READ driver and READ switch must first be turned on. To turn on the READ driver and READ switch, the base of each transistor must be positive with respect to the emitter. This occurs only when the output of the decoder is low (active). Otherwise, a +5V is applied to the emitter-side of the transformer as illustrated by S = open.

When the READ driver is off, the +5V causes the READ diode at the current source to be reverse-biased. As soon as the READ driver is turned on, the READ diode immediately becomes forward-biased. A second requirement to pass READ current through core is to forward-bias the READ diode in the diode matrix. Current then passes through the READ switch, through the READ diode, through the READ driver, through the current source READ diode, into the current source.

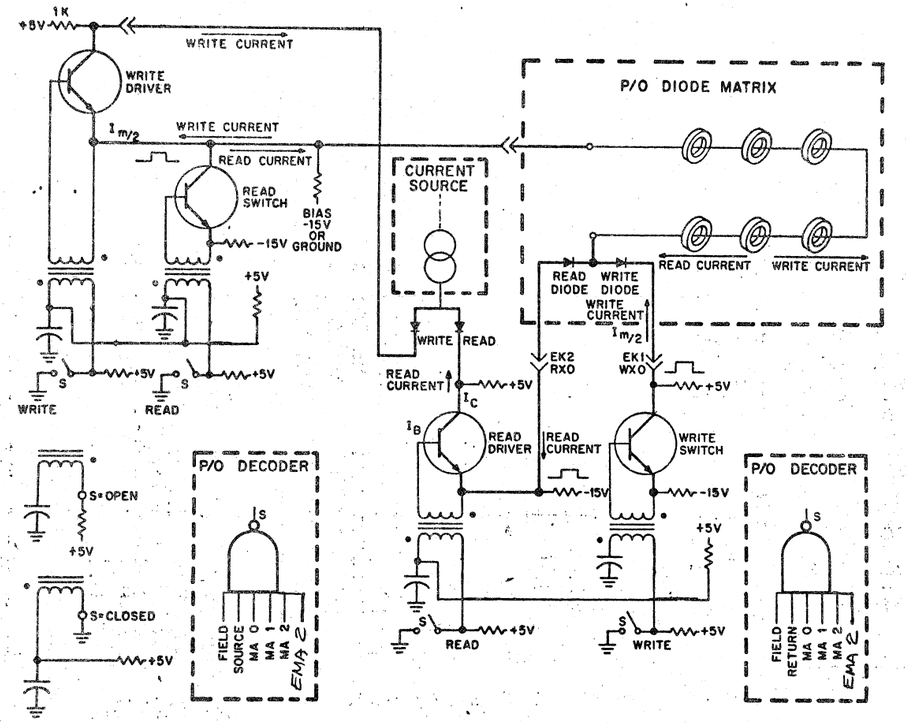


Figure 18 Operation of Selection Switches

The WRITE operation is similar to the READ and begins with the decoder. To select line X12, the decoder causes the WRITE switch transformer to reverse polarity, which then turns on the WRITE switch When the WRITE driver is turned on, a complete path is made for current to go through the WRITE switch, WRITE diode, 768 cores, WRITE driver, WRITE current source diode, to the current source.

5.9 Operation of the Core Selection System

The cores that contain a selected X-line and a selected Y-line define the location for which a 1 or a Ø will be either written in or read out. Figure 19 illustrates a small portion of memory and the corresponding selection devices. Using Figure 19, the selection of any given core can be traced from the Memory Address Register, through the decoders and switches, to the selected core.

6.0 SENSE/INHIBIT FUNCTION

The previous paragraphs have described the memory core, the selection of memory core, and the selection of memory core in terms of the READ/WRITE operation. However, to perform a READ or a WRITE operation, sense amplifiers are necessary to sense the state of the selected cores, and Inhibit Drivers are necessary to write Øs into core. Control logic and data registers are also required to control the data flow to and from memory. These necessary circuits are illustrated in a simplified diagram (see Figure 20). The circuitry corresponding to the READ operation is shown on the lower portion of the illustration, and the circuitry corresponding to the WRITE operation is illustrated in the upper portion of the illustration.

6.1 Sense/Inhibit Line

The line that is used to sense during READ is used to transmit current when a Ø is to be written during the WRITE portion of

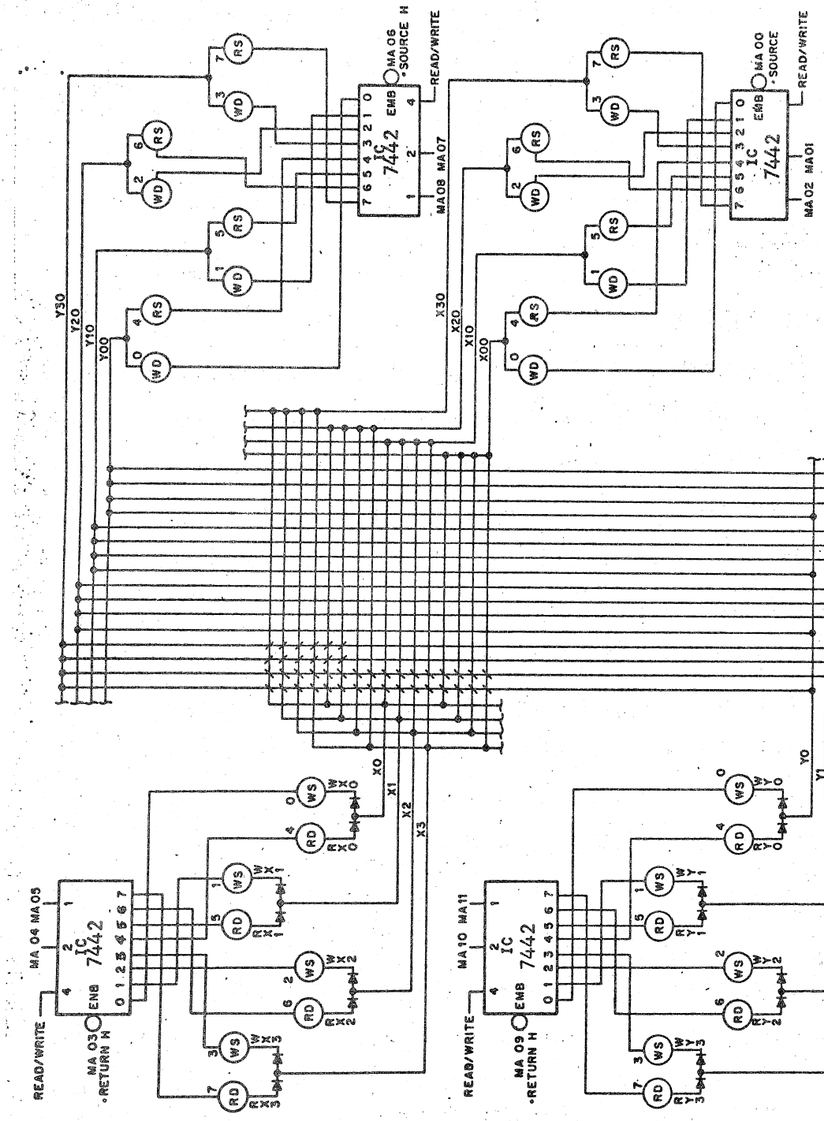


Figure 19 Operation of X/Y Selection Switches

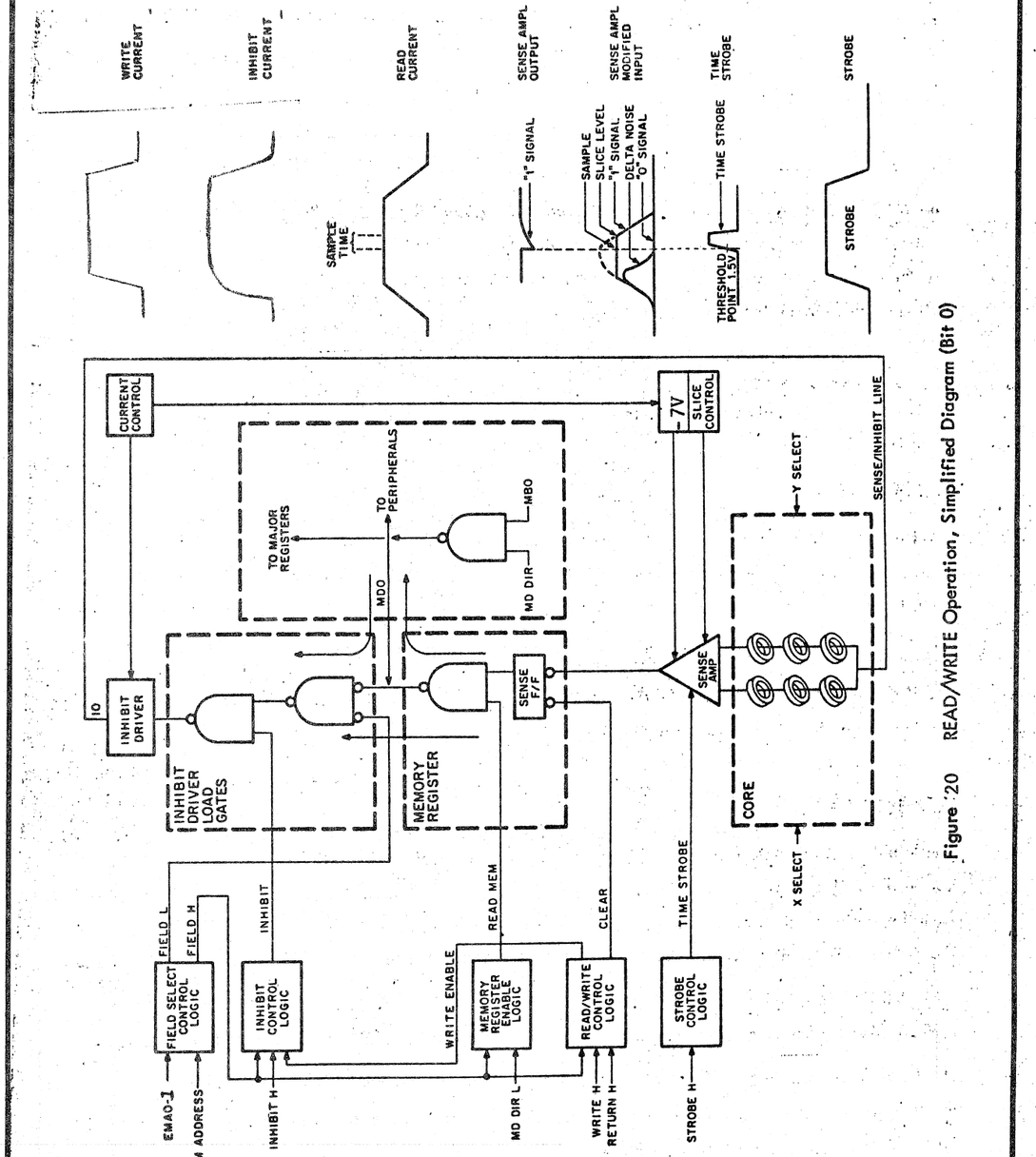


Figure 20 READ/WRITE Operation, Simplified Diagram (Bit 0)

the memory cycle. The sense/inhibit passes through 8192 cores of a corresponding mat. Both ends of this line are terminated at the input to the Sense Amplifier, and a terminal connection is made so that the Inhibit Driver output joins this same line.

6.2 READ Operation

The READ operation involves the Sense Amplifier, the Memory Register, and the necessary control logic in conjunction with the selection system. During the READ portion of the memory cycle, the selected core develops a signal on the sense/inhibit line if a 1 was previously stored in core. The Sense flip-flops are cleared and TIME STROBE gates either 1 or a Ø out of the Sense Amplifiers and applies a corresponding pulse (if it is a 1) to the Memory Register. When a 1 is sensed, the Sense Amplifier applies a negative-going pulse to the Sense flip-flop. The Memory Register output gate receives the Sense flip-flop signal and gates the 1 or Ø out to the MD line. Note that the Memory Register outputs are gated onto the MD lines only when MD DIR is low; consequently the only requirement to write the contents of the Memory Register back into memory is to keep MD DIR low during the WRITE portion of the memory cycle. The output of the Memory Register can, therefore, be applied to the inhibit circuits for a rewrite; or because the data is first applied to the MD BUS, the output of the Memory Register can be loaded into one of the major registers or a peripheral.

When the Memory Register applies data to the MD lines the data can be loaded into any one of the Major Registers, as well as applied to the Inhibit Drivers for redeposit into core. Conversely, the data contained in the Memory Buffer (MB) register can be applied to the MD lines and applied to the Inhibit Drivers.

6.3 WRITE Operation

The WRITE operation involves the Inhibit Drivers, load gates, the Memory Register, and the necessary control logic in conjunction with the selection system. The Inhibit Driver load gates receive 1's and Ø's via the MD lines from either the MB Register in the processor or from the Memory Register. Control gating signals for the Inhibit Driver load gates are:

a) FIELD (L), Which indicate that field Ø or 1 has been selected, and

b) INHIBIT (H) from the Timing Generator. Inhibit current is generated by the Inhibit Drivers only when a Ø is to be written into core.

6.4 Field Select Control Logic

The field select control logic (Figure 21) determines if the basic memory has been selected. When field Ø or 1 is selected, the logic develops a signal, called FIELD, for gating other control logic and the Inhibit Driver load gates. The logic receives extended address memory bits EMA Ø through EMA 2.

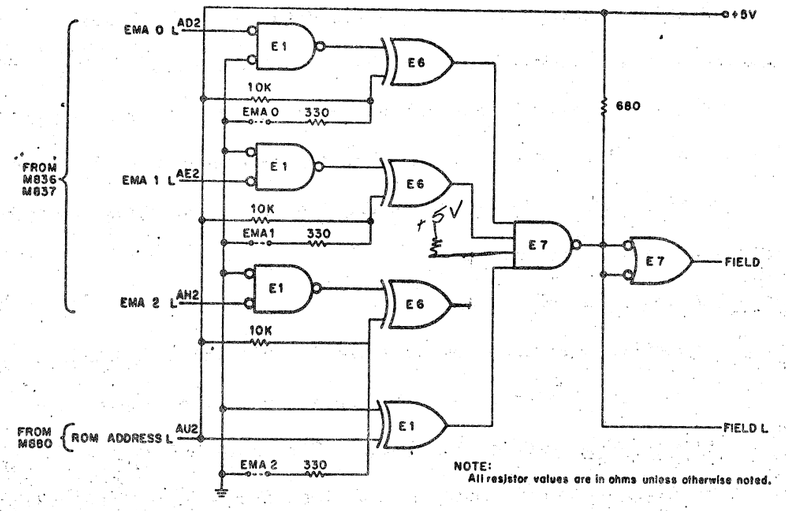


Figure 21 Field Select Control Logic

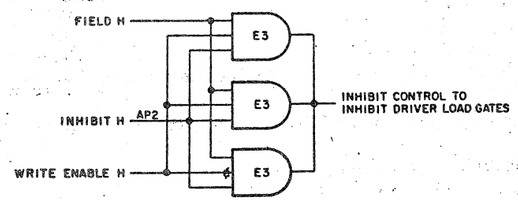


Figure 22 Inhibit Control Logic

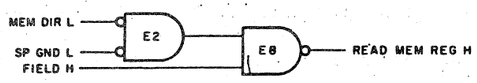


Figure 23 Memory Register Enable Logic

A comparison circuit compares the bits on the EMA lines with the EMA jumpers. If the two are equal and if the ROM address is high, the field is selected. Bank Ø or 1 is always selected with all jumpers in. The Exclusive OR gate provides a high output only when one input is high.

6.5 Inhibit Control Logic

The Inhibit Control logic (Figure 22) provides a gating control signal to the Inhibit Driver load gates during the WRITE portion of the memory cycle. The logic receives INHIBIT H from timing, RETURN H from the Timing Generator, FIELD H from the Field Select Control logic, and WRITE ENABLE from the READ/WRITE control logic.

6.6 Memory Register Enable Logic

The Memory Register Enable logic (Figure 23) functions when the contents of the Memory Register are to be gated onto the Inhibit Drivers and MD lines. When MD DIR is low, the output of the control logic (READ H) gates the contents of the Sense flip-flops to the MD BUS.

6.7 READ/WRITE Control Logic

The READ/WRITE Control logic (Figure 24) clears all Sense flip-flops and enables the Inhibit Control logic.

The CLEAR signal becomes active only when WRITE H is not active and RETURN H is asserted. This begins at the start of the READ portion of the memory cycle and continues for a period of approximately 50ns. The CLEAR signal becomes inactive when the flip-flop (E4) becomes reset by the CLEAR signal input.

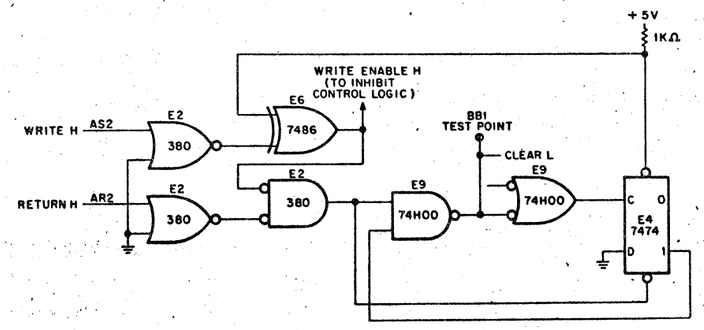


Figure 24 READ/WRITE Control Logic

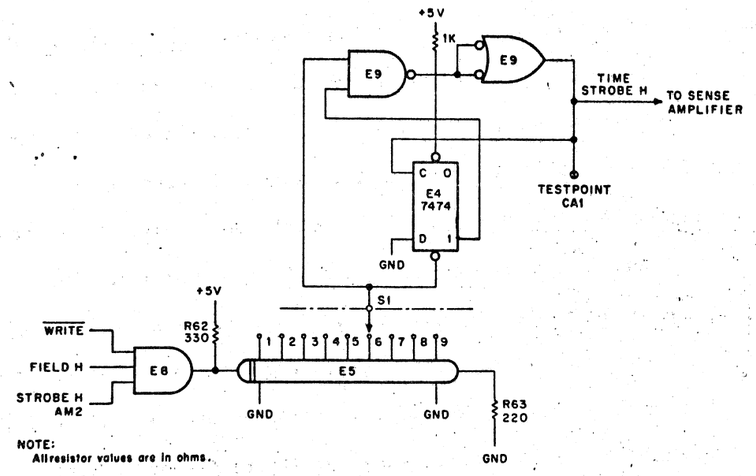


Figure 25 Strobe Control Circuit

6.8 Strobe Control Logic

The strobe control logic (Figure 25) is used to control the sample time of the Sense Amplifiers during the READ portion of the memory cycle. TIME STROBE occurs when WRITE is not asserted, FIELD has been selected, and the STROBE timing signal from the Timing Generator has been received. STROBE is gated in and passed through an adjustable time-delay circuit. The flip-flop (7474) senses the rise and fall times of the strobe pulse and enables the output gate. The signal can be observed at test point CA1 (using a module extender). TIME STROBE width is dependent on the delay of the 7474 and both E9's.

6.9 Sense Amplifiers

Twelve Sense Amplifiers (Figure 26) are required to sense signals on the twelve sense lines. If the selected core in a given mat contains a 1, a pulse is received on the sense/inhibit winding. This pulse is amplified by the Sense Amplifier and then used to set a 1 into the Memory Register. If the selected core contains a Ø, the signal received by the Sense Amplifier is small, and no pulse appears at the output of the Sense Amplifier; the Memory Register remains in the Ø state. The Sense Amplifier is "strobed" with a narrow pulse to ensure that the contents of the sense lines are sampled at the proper time. This timing is necessary because the cores in the Ø state produce a small signal when "sensed" and because many of the cores in each mat receive half-selected pulses.

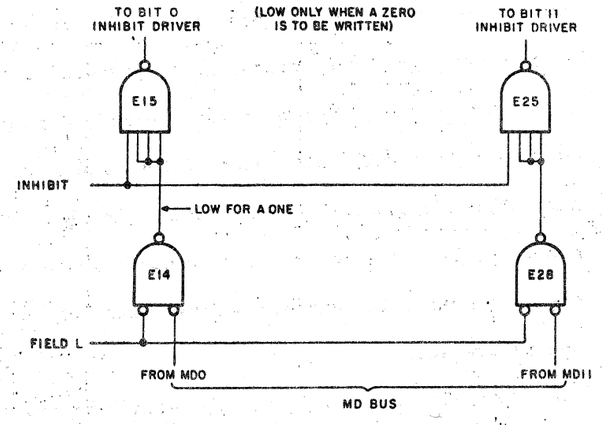


Figure 28 Inhibit Driver Load Gates

FETCH or DEFER state is being processed, MD DIR is made low and the memory cycle is a fast cycle (1.2μs). This allows the contents of the Sense flip-flops to be gated out to the Inhibit Driver Load Gates during WRITE and, subsequently, applied to the Inhibit Drivers. Whenever data is to be written into memory from the MB Register, memory cycle timing is 1.4μs, and MD DIR is high during the WRITE portion of the memory cycle. The Sense flip-flops are then made inactive, and the Inhibit Driver input gates look at only the MB Register. If data break is used, data is immediately transferred from a peripheral to the MB Register and gated into memory during the current memory cycle. During most

other types of transfer operations, data must be transferred from the AC Register to the MB Register and applied to the Inhibit Driver input gates.

6.12 Inhibit Drivers

Inhibit Drivers (Figure 29) apply inhibit current to the selected core whenever a Ø is to be written. Each of the 12 drivers receives either a positive level (for a 1) or a ground input (for a Ø) at the 1:1 input transformer. During a Ø output of any Inhibit Driver Load Gate, the transistor-base side of the transformer secondary is positive with respect to the emitter side. This turns on, the transistor allowing inhibit current to conduct and be applied to the selected core. Because the inhibit current direction is opposite to the write select current, a half-select condition results, and the core remains in the Ø state. During a 1 output of any one Inhibit Driver input gate, the transistor-emitter at the same potential as the base and the transistor does not conduct. The full select current is then applied to the corresponding core, which results in a 1 state. The Inhibit Driver acts as a relay driver/solenoid driver. There is an inductor, a resistor, and a switch. The resistor determines the current, and the inductor is a magnetic device. When the transistor is turned on, the Inhibit line contains current defined by the emitter and the resistor. When the switch turns off, the resulting energy stored in the magnetic device creates a backswing that can damage the transistor circuit. The diode-

to-ground at the collector output is used to protect the transistor from this unwanted backswing condition.

6.13 Current Control Circuit

The current Control circuit (Figure 30) controls the current level in the X- and Y-select lines. The control circuit operates on a +5V and -15V supply. The output to the X- and Y-current sources (Figure 12 and Figure 13) is a voltage-regulated supply that varies with the temperature changes. The temperature sensing is accomplished by the thermistor, located on the memory stack board. The two jumpers are factory installed to control the preset X- and Y-current reference point.

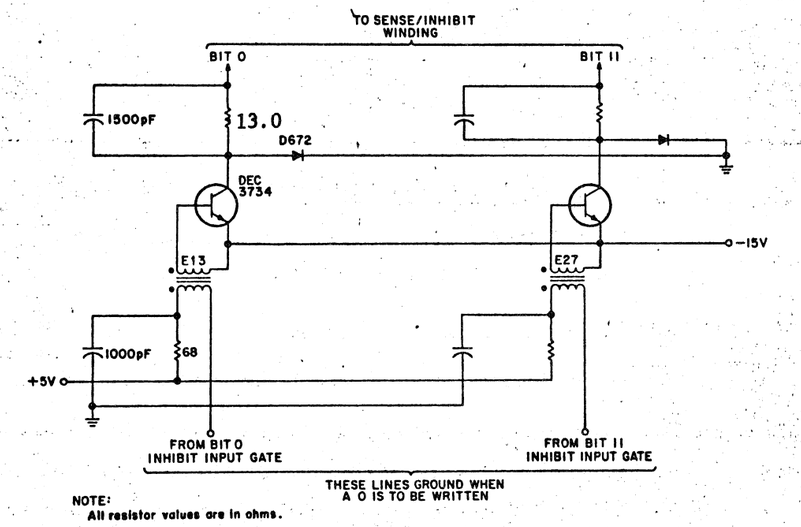


Figure 29 Inhibit Drivers

6.14 -7V supply and Slice Control Circuits

The -7V Supply and Slice Control circuits, shown in Figure 31, provide a voltage slice level to the Sense Amplifier (Figure 26) and a regulated -5Vdc output to the Sense Amplifier. The slice level is controlled by jumpers SLA and SLB, which are factory installed.

7.0 MEMORY TRANSFER CONTROL LOGIC

Memory transfer control is accomplished by signal MD DIR. When MD DIR is low, the content of the Memory Register, containing information from the READ operation, is gated out to the MD BUS. When MD DIR is high, the content of the MB Register is gated out to the MD BUS for

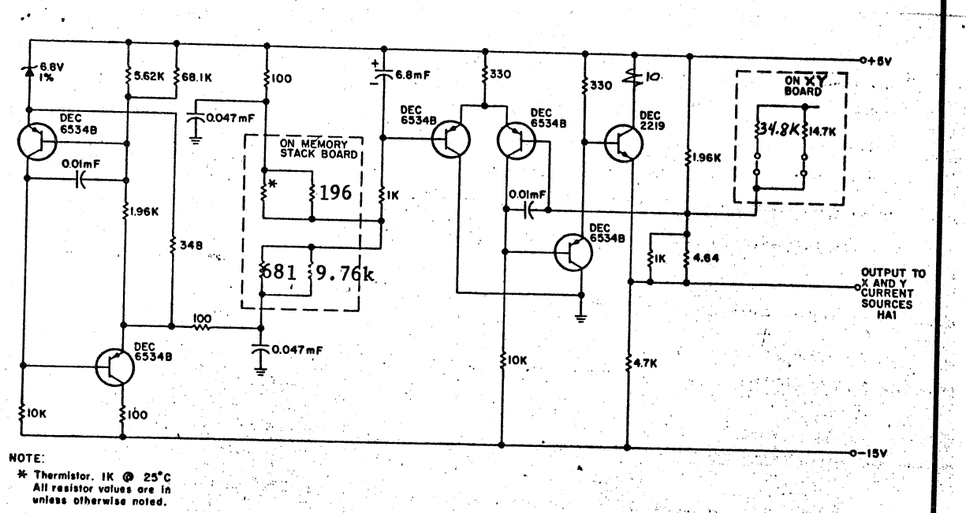


Figure 30 Current Control

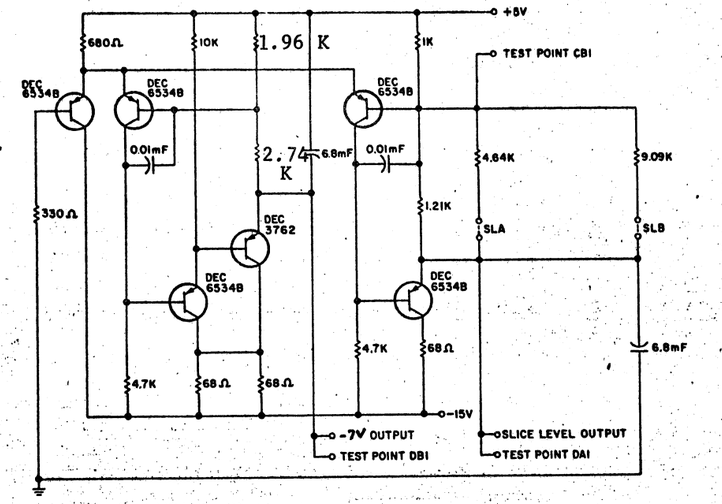
deposit into memory during the WRITE operation. When the processor directs memory to write back into memory the word retrieved during READ, (manipulating signal MD DIR) MD DIR remains low during the WRITE operation. The contents of the Memory Register are on the MD BUS; consequently, the same word is written back into memory. This procedure always applies during FETCH and DEFER (NON-AUTO INDEX).

7.1 Transfer Control During FETCH, DEFER, or EXECUTE States

The memory transfer control logic for FETCH, DEFER, or EXECUTE states is illustrated in Figure 32. A CLEAR signal is generated by timing 100ns after the start of TS1. This resets E19, which causes MD DIR L. The flip-flop remains unchanged until TP2 is received as a clock input. If the major state is FETCH, a low will be clocked into the data input of the flip-flop, and E19 remains unchanged until TP2 of the next cycle. If the major state is DEFER (NON-AUTO INDEX), a low will be clocked into the data input of the flip-flop, and E19 remains unchanged. Thus, in both cases, the data from the Memory Register is re-deposited in memory.

If the major state is DEFER and AUTO INDEX (MA0-7 equals Ø and MA8 equals 1), a high is clocked into the flip-flop, and E19 is set. A low into E27 causes MD DIR H, and memory receives the data from the MB Register.

If the major state is EXECUTE, a high is clocked into the data input of the flip-flop, and E19 is set; this condition, as in the previous case, causes MD DIR H.



NOTE:
Resistor values are in ohms unless otherwise noted.

Figure 31 Supply and Slice Control Circuits

7.2 DMA State - Manual Operation Transfer Control

MD DIR H is asserted at TP2 unless pulled low by the Memory Transfer Control logic in the Programmer's Console (refer to Figure 33).

Because FETCH or DEFER is not asserted, due to the DMA state, the Memory Transfer Control logic in the Timing Generator remains high, because no reset pulse is generated by timing. Either the LOAD ADDR or EXAM key, when depressed, will generate MD DIR (L), which places the contents of the Memory Register onto the MD BUS.

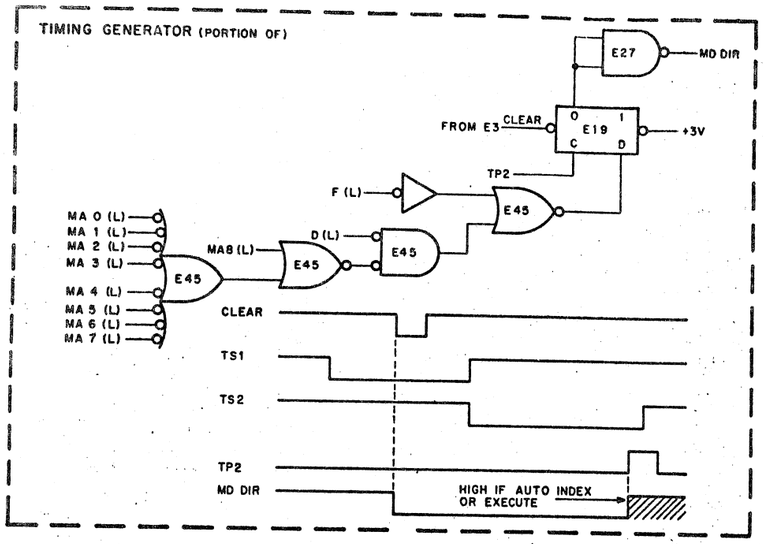


Figure 32 Memory Transfer Control Logic
(FETCH, DEFER or EXECUTE)

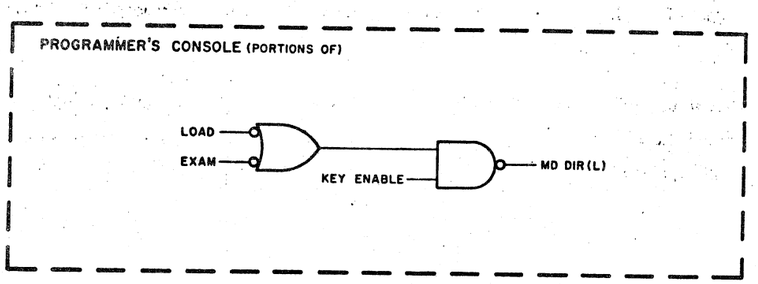


Figure 33 Memory Transfer Control Logic - DMA State
(MANUAL OPERATION)

7.3 DMA State-Data Break Operation

Each data break device contains Memory Transfer Control logic.

MD DIR will always be low except when:

a) Incrementing the word count (three-cycle data break device)

b) Incrementing the current address (three-cycle data break device)

c) Data is transferred from the device to memory, or memory is incremented.