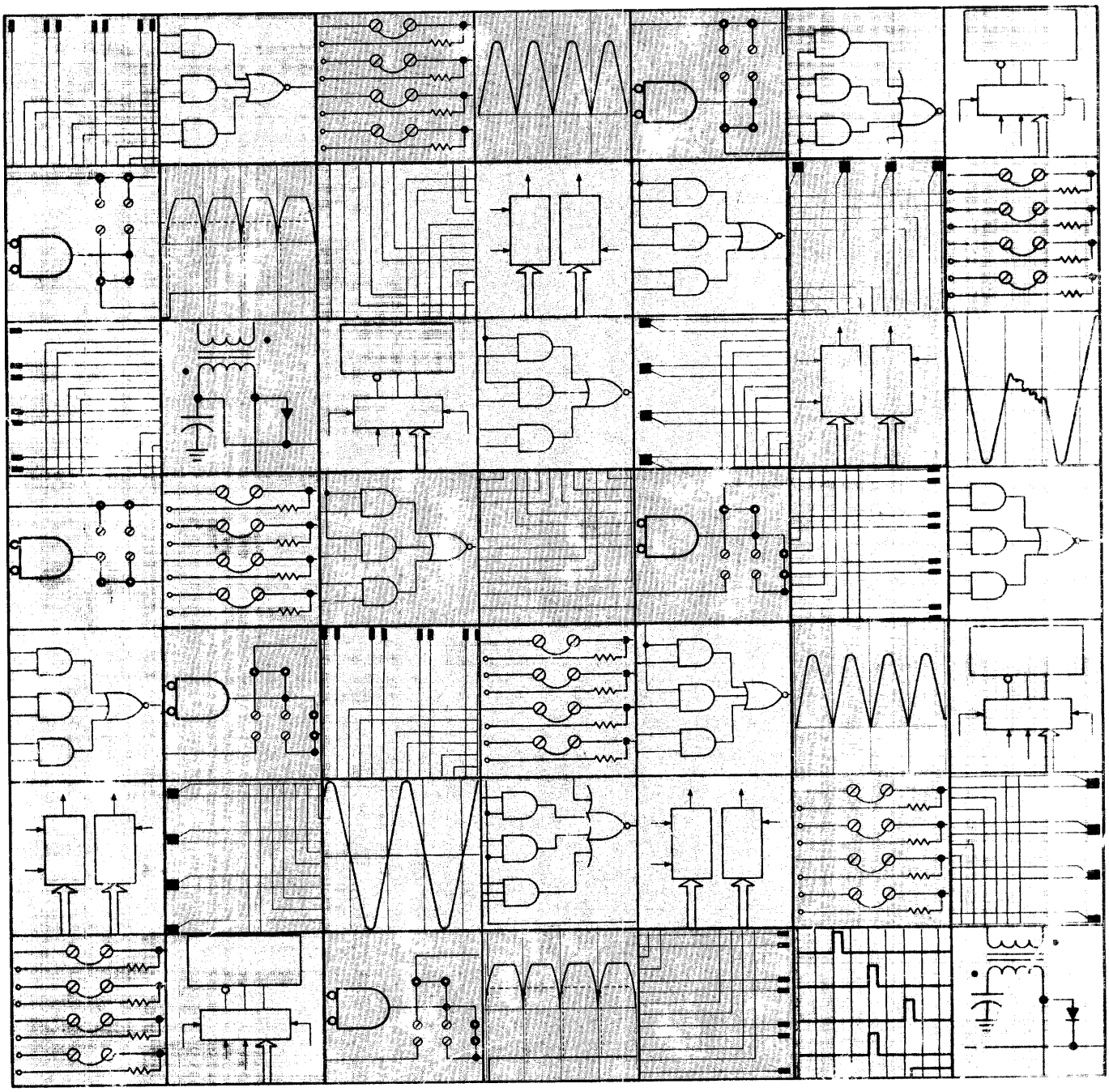
pdp8/e

pdp8/f & pdp8/m

processor maintenance manual volume 1



digital

pdp8/e, pdp8/f & pdp8/m

MAINTENANCE MANUAL
VOLUME 1

For additional copies order No. DEC-8E-HR1C-D from Direct Mail, Digital Equipment Corporation, Maynard, Massachusetts 01754 Price: $25.00

digital equipment corporation · maynard. massachusetts

1st Edition, April 1971
2nd Printing, March 1972
3rd Printing, August 1972
4th Printing, October 1972
2nd Edition, December 1972
6th Printing, February 1973

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CHAPTER 1
INTRODUCTION AND DESCRIPTION

1.1 PURPOSE OF MANUAL

This manual describes the PDP-8/E, PDP-8/F, and PDP-8/M Computer Systems manufactured by Digital Equipment Corporation, Maynard, Massachusetts. Each system consists of a basic computer, internal options, and external options. The three basic computers are quite similar in performance, operating procedures, and physical contents. The noticeable differences between the PDP-8/E and the PDP-8/F are physical size and front panel appearance: the depth of the PDP-8/E is almost twice that of the PDP-8/F, a fact that has significance when options are added to the basic computer; in addition to a slight difference in the silk-screening of the two front panels, the PDP-8/F indicating devices (light-emitting diodes) give off a red glow in contrast to the orange glow of the PDP-8/E indicator bulbs. Differences that are not noticeable are the type of power supply (the PDP-8/F power supply is less expensive) and the logic used on each KC8 Programmer's Console (the PDP-8/F logic is simpler); these differences are detailed in later chapters. These slight differences mean that the PDP-8/F is a less expensive basic computer than the PDP-8/E, even though it provides almost as much expansion capacity as the PDP-8/E. The PDP-8/M is an Original Equipment Manufacturer (OEM) version of the PDP-8/F that provides the OEM with a low-cost 12-bit computer giving performance identical to that of the PDP-8/F.

Because system dissimilarities are minor, it is possible to provide a description that, in most instances, applies equally to each. Thus, the maintenance manual refers to the PDP-8/E only, except where differences exist and must be pointed out. This manual consists of three volumes, each containing installation procedures, detailed logic theory, and maintenance instructions:

a. Volume 1 deals with the basic computer; viz., memory, central processor, timing, I/O control (for the companion Teletype®), front panel controls, and power supply.

b. Volume 2 deals with internal bus options; they are self-contained devices that, when added to the basic computer, function with no external connections (two of these options, the positive I/O bus interface and the data break interface, defy this definition for reasons that will be given later).

c. Volume 3 deals with external bus options; they are options that consist of a peripheral and a control that is added to the basic computer and is connected by external cabling to the peripheral.

Maintenance procedures for the PDP-8/E system are provided in Chapter 4 of this manual. These procedures have been developed from the careful analysis and long experience of DEC's Field Service staff. They will be extremely helpful in maintaining the PDP-8/E in good operating condition. Maintenance personnel must be familiar with the detailed logic theory and operating procedures for the PDP-8/E.

® Teletype is a registered trademark of Teletype Corporation.

NOTE

Chapter 2 of the PDP-8/E & PDP-8/M Small Computer Handbook describes the PDP-8/E front panel controls and indicators; the Teletype controls, indicators, and keyboard; manual operation of the PDP-8/E controls; preliminary program-loading procedures; and initiation of automatic system operation.

Companion documents include:

a. *Introduction to Programming,* DEC 1972

b. *Programming Languages,* DEC 1970

c. PDP-8/E Engineering Drawings

d. PDP-8/F Engineering Drawings

e. PDP-8/M Engineering Drawings

f. *PDP-8/E & PDP-8/M Small Computer Handbook,* 1972.

1.2 DESCRIPTION

The PDP-8/E performs arithmetic calculations, controls machine operations, makes on-line measurements of both analog and digital information, and stores large quantities of data for future use and/or modification.

The machine design enables the user to purchase the basic PDP-8/E computer and add options as his requirements increase. The internal bus options logic and the peripheral controls logic is mounted on printed circuit boards called "quad" modules. These quad modules plug into slots in a two-way bus, called OMNIBUS, that is mounted on the computer chassis (see Chapter 9 of the *PDP-8/E & PDP-8/M Small Computer Handbook* for a description and photographs of the OMNIBUS and representative quad modules). One OMNIBUS contains 20 slots that are, for the most part, non-dedicated (see Table 2-3 for the recommended arrangement of quad modules on the OMNIBUS). Ten slots are needed for the basic computer; thus, 10 are available for expansion. An OMNIBUS expander enables the user to increase the number of slots by 20 (PDP-8/E only).

Further expansion of the PSP-8/E only, by a total of 40 slots, can be accomplished by connecting an expander box containing an OMNIBUS and an OMNIBUS expander to the basic computer. The PDP-8/F and PDP-8/M basic computer can be expanded by a total of 40 slots when an expander box containing the OMNIBUS and an OMNIBUS expander are connected to the basic chassis.

The PDP-8/E is currently available in table-top and rack-mountable versions (Figures 1-1 and 1-2, respectively). The PDP-8/F and the PDP-8/M are available in rack-mountable versions (Figures 1-3 and 1-4, respectively). Note that the PDP-8/E and the PDP-8/F are equipped with the KC8 Programmer's Console (KC8-EA and KC8-FL, respectively), while the PDP-8/M is equipped with the KC8-M Operator's Panel. Various front panel options are available for each basic computer; the user should consult the *PDP-8/E & PDP-8/M Small Computer Handbook* for complete information on all options.

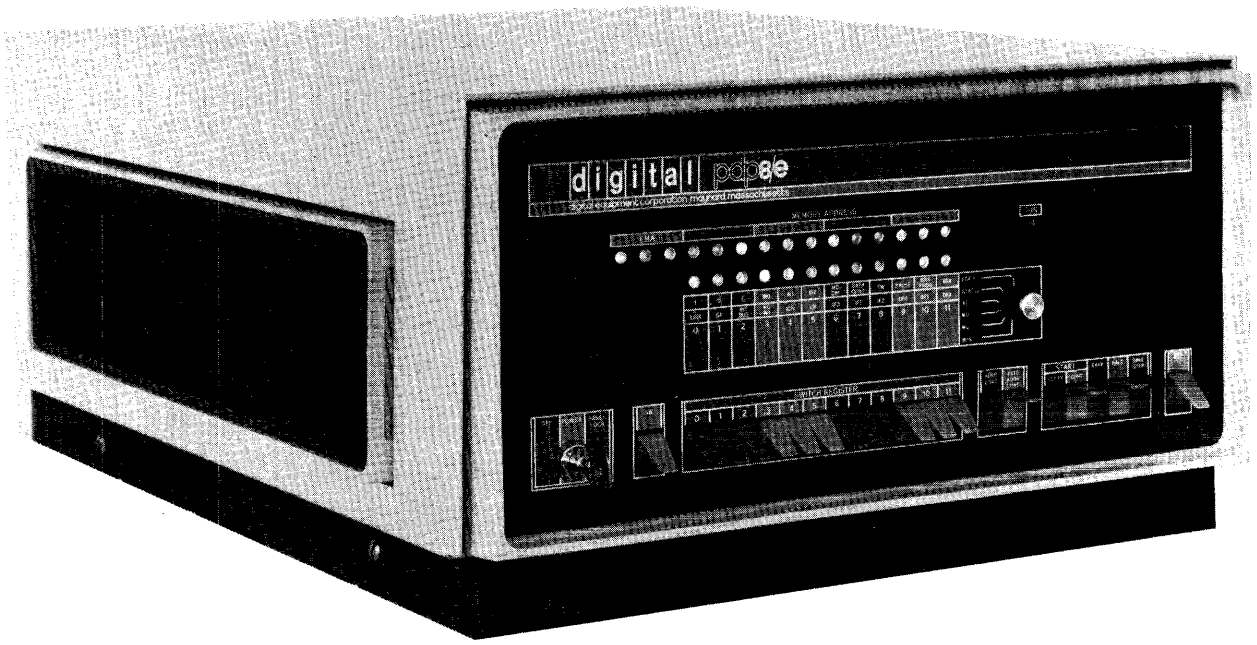


Figure 1-1 PDP-8/E Processor, Table-Top Model

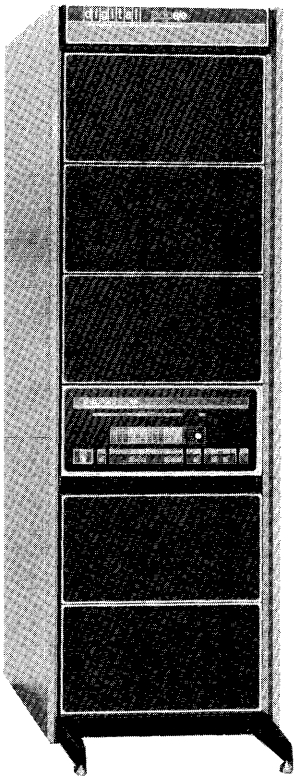


Figure 1-2 PDP-8/E Processor, Rack-Mounted Model

Figure 1-3 PDP-8/F Computer

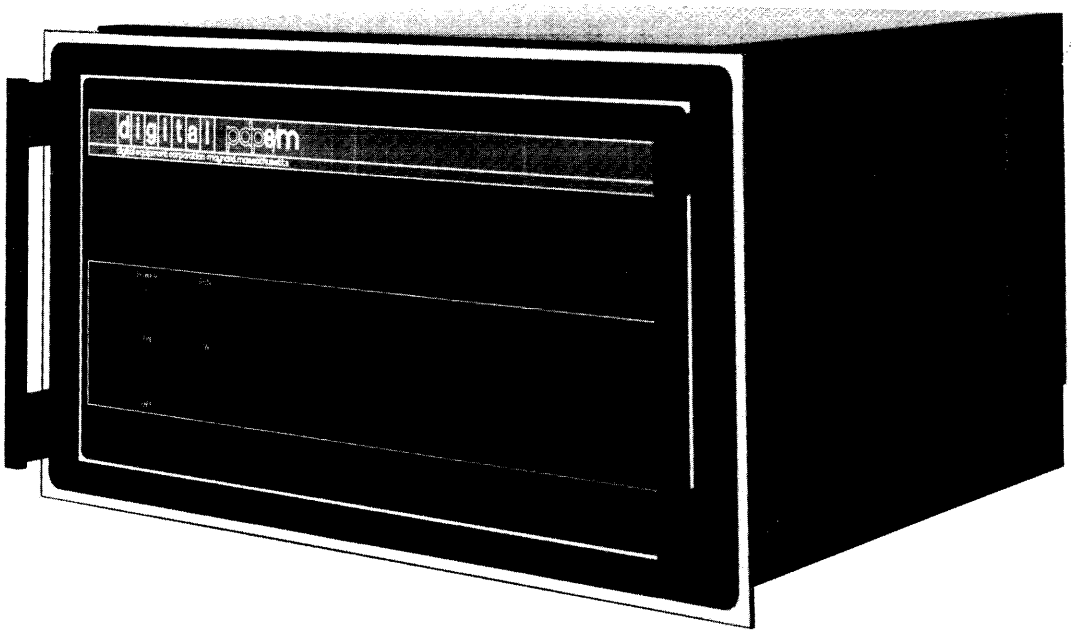


Figure 1-4 PDP-8/M Computer

The computer can be operated manually from the front panel (programmer's console) or automatically from program tapes that are either punched or entered via the companion Teletype reader/punch. More efficient methods of entering programs are available with magnetic tape system options, such as DECtape systems. Mass storage can be achieved by using magnetic tape or disk systems. Data can be displayed, via the 33 ASR Teleprinter, or by employing one of DEC's display system or line printer options.

1.2.1 Functional Description

The PDP-8/E basic computer uses 10 quad modules that connect to the OMNIBUS as illustrated in Figure 1-5 (also shown is the positive I/O bus interface, the data break interface, the power supply, and a block labeled "options" that represents connected internal and external options). Memory comprises three modules: Sense/Inhibit, X/Y Driver and Current Source, and Stack. The Central Processor Unit (CPU) comprises two modules: Major Register Control and Major Registers. The Timing Generator, bus loads, Teletype control, RFI shield, and the Programmer's Console each use one module. Power supply connections to the OMNIBUS are made through standard tabs located on the back of the OMNIBUS.

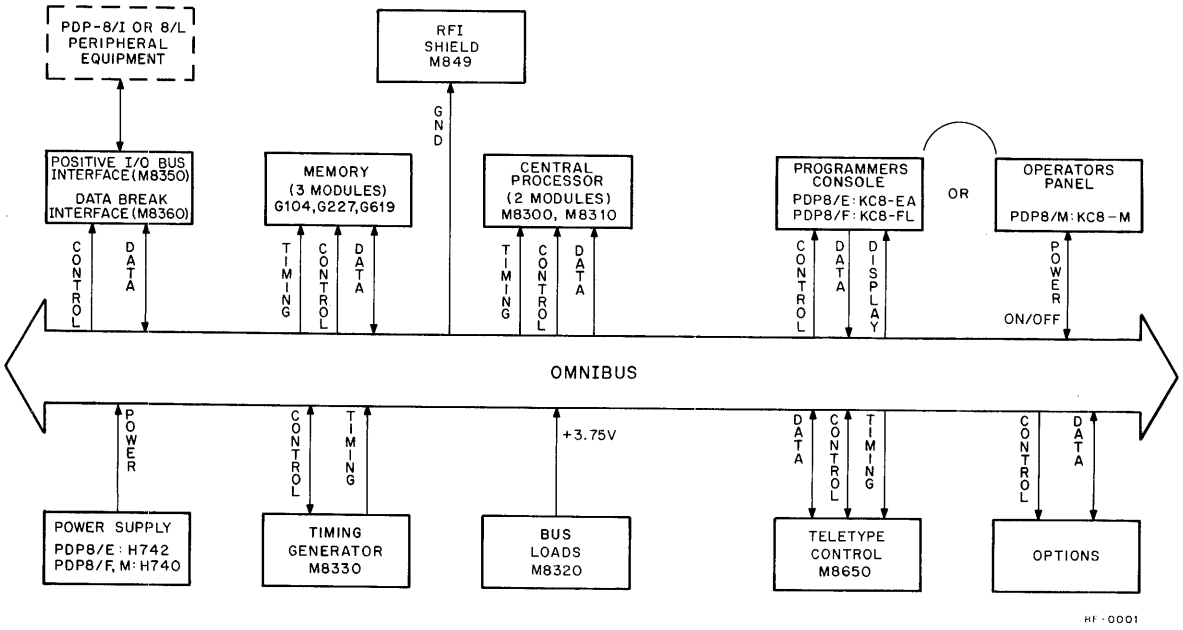


Figure 1-5 Basic Computer, Functional Block Diagram

System expansion can be accomplished in two ways: options can be added directly to the OMNIBUS, as already described; or, if the user has PDP-8/I or PDP-8/L compatible peripherals, the M8350 and M8360 interfaces will enable connection to the PDP-8/E OMNIBUS. The OMNIBUS is the signal path between options. Bus loads keep each signal line at a +3.75V level until a signal is asserted that causes the line on the OMNIBUS to go to ground. This permits maximum interplay between signal generators and data generating circuits. Three types of signals are used on the OMNIBUS, viz., control, timing, and data.

1.2.2 Physical Description

The PDP-8/E table-top model is 10½ inches high, 19 inches wide, 24 inches deep, and weighs 100 pounds. The rack-mountable model is 10½ inches high, 19 inches wide, 23¼ inches deep, and weighs 90 pounds. Both the PDP-8/F and the PDP-8/M are 10½ inches high, 19 inches wide, 13 inches deep (14½ inches deep with chassis slides), and weigh 35 pounds.

The machine construction minimizes the wiring (most signals are applied via the OMNIBUS). An internal view of the PDP-8/E is shown in Figure 1-6. The OMNIBUS, into which all modules are inserted, is secured to the bottom of the main frame next to the power supply. A cutaway on the side of the power supply provides an area in which all interface cabling can be run and secured.

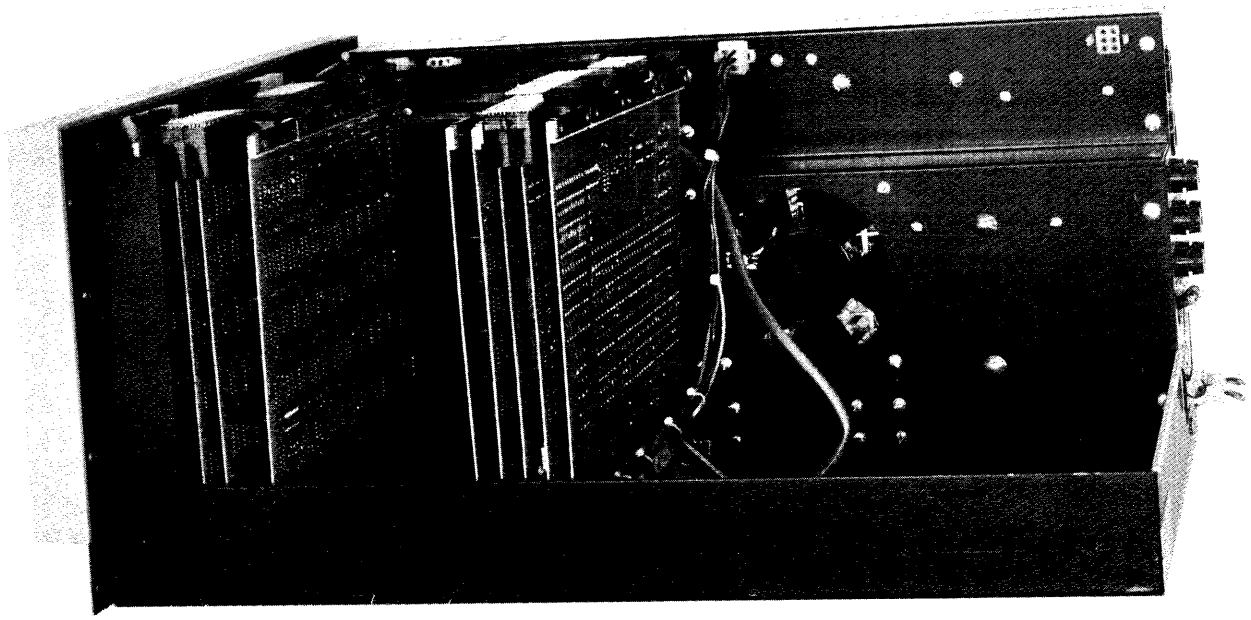


Figure 1-6 PDP-8/E Processor Without Cover

The PDP-8/E table-top model includes a super cover that completely encloses the top, rear, and sides of the main frame. A top cover is provided for the rack-mountable model (PDP-8/F and PDP-8/M, also). No air conditioning is required for the basic computers; fans located in the power supply provide adequate cooling.

1.3 TECHNICAL CHARACTERISTICS

The technical characteristics of the PDP-8/E processor are summarized in Table 1-1.

Table 1-1
PDP-8/E Technical Characteristics Summary

Characteristics	PDP-8/E Specifications
Speed	Two memory cycle speeds are provided: a. Fast cycle accomplishes a FETCH, internal IOT instruction, or DEFER (non-autoindex) in 1.2 μs. b. Slow cycle accomplishes (after FETCH) an instruction execution or DEFER (autoindex) in 1.4 μs.
Instruction Execution Time (MRI only)	The instruction execution time, beginning with FETCH and ending with the instruction completely executed, requires one fast and one slow memory cycle or 2.6 μs.
Word Length	12 bits.
Addressing Capability	Direct memory addressing is controlled on the front panel or through the Data Break System. Programmed addressing is accomplished as a function of software. 400_8 memory locations can be directly addressed (except when on page 0) by the program during any one memory cycle, and 7400_8 locations indirectly addressed.
Instruction Set	Eight basic instructions constitute the instruction set. AND 0000 Logical AND TAD 1000 2's complement add ISZ 2000 Increment and skip if zero DCA 3000 Deposit and clear AC JMS 4000 Jump to subroutine JMP 5000 Jump to another memory location IOT 6000 In/Out transfer OPR 7000 Operate
I/O Capability	Three types of I/O transfers are provided: a. Programmed I/O data transfer b. Programmed interrupt I/O data transfers c. Data break I/O data transfers
Memory Capacity	4096 12-bit word memory locations (up to 32K optional).
Power Input (processor)	95-130 Vac, 47-63 Hz, approx. 6A, single phase or 185-250 Vac, 47-63 Hz, approx. 3A, single phase 450W power dissipation.

Table 1-1 (Cont)
PDP-8/E Technical Characteristics Summary

Characteristics	PDP-8/E Specifications
Power Input (Teletype)	115 ±10% Vac, 60 Hz ±0.45 Hz, or 230 ±10% Vac, 50 Hz ±0.50 Hz, 2A line current drain 150W power dissipation.
Environmental	The PDP-8/E is designed to operate from +0° to 55°C and with a relative humidity of from 10 to 95% (without condensation).
Cable Requirements	The PDP-8/E I/O cable is a combination shield and ribbon or coaxial cable. The maximum length of the data break I/O bus cable is 30 ft using a coaxial or 25 ft using ribbon cable. Maximum length of the programmed I/O bus is 50 ft using coaxial or 45 ft using ribbon cable.

CHAPTER 2
INSTALLATION

This chapter contains supplementary information and procedures for installing the PDP-8/E Computer System. Basic installation and planning information, such as space requirements, environmental requirements, installation requirements, and system configuration data, is provided in Chapter 11 of the *PDP-8/E & PDP-8/M Small Computer Handbook*. Installation functions and responsibilities are summarized in Table 2-1.

Table 2-1
Summary of Installation Functions

Responsibility	Function
User	Identify space and power required for system configuration.
User/DEC Representative	Survey proposed site.
User/Optionally DEC Representative	Prepare site in accordance with environmental space and power requirements.
User/DEC Representative	Unpack equipment and check inventory checklist.
DEC Representative	Install equipment.
User/DEC Representative	Run customer acceptance test.
User	Enter results of acceptance test in log book.

2.1 SITE CONSIDERATIONS

Adequate site planning and preparation can simplify the installation process and result in an efficient, more reliable PDP-8/E system installation. DEC Sales Engineers or Field Service Engineers are available for counseling and consultation with user personnel regarding the installation.

Site planning should include a list of the actual components to be used in the installation; this list should also include such items as: storage cabinets, Teletype supplies, work tables, etc.

Primary planning considerations are:

a. the availability and locations of adequate power

b. protection against direct heat sources

c. electrical noise radiation

d. shock

e. the existence of fire protection devices.

If existing environmental conditions dictate, air conditioning and/or dehumidifying equipment (though not required for the PDP-8/E) can become part of the site planning program.

2.1.1 Power Source

The power source should be free of conductive interference. To ensure interference-free power input, DEC offers a line filter option. In addition, all computer system supplies should be connected to the same power source to avoid loading and source differentials that may affect computer operation.

2.1.2 I/O Cabling Requirements

The cabling for table-top and rack-mounted computers differs slightly. For rack-mounted equipment, cables can be routed into the cabinet through a panel located at the bottom of the cabinet. Subflooring is not necessary because casters elevate the cabinet high enough to provide sufficient cable clearance. For table-top models, cables are routed from the lower rear side and then through the adjustable strain relief of the processor (Figure 2-1). The cabling should be located where it cannot be damaged. This is especially important if the processor and peripherals are not in close proximity.

2.1.3 Fire and Safety Precautions

The PDP-8/E power supply contains a thermal cut-out switch, circuit breaker, and six fuses for protection against overheating and overloading. Both the cabinet and the power receptacle must be adequately grounded to ensure safe operation. A water pipe or steel beam provides an adequate ground. Refer to Chapter 11 of the *PDP-8/E & PDP-8/M Small Computer Handbook* for grounding and power installation procedures.

WARNING
The frame of the computer must be grounded to protect personnel from dangerous electrical shock.

Grounding is achieved automatically if a table-top computer with a 3-wire plug is used. However, a voltage reading from frame to ground should be performed initially.

Electrical fires, although extremely unlikely, should always be extinguished by a Class 3 (CO_2) fire extinguisher.

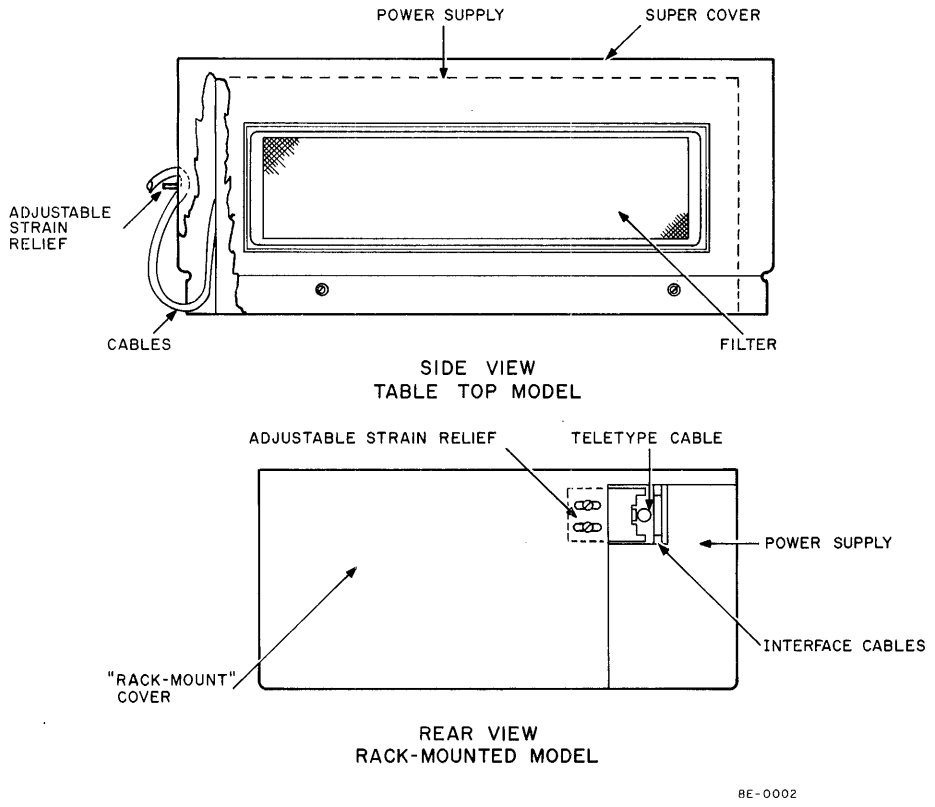


Figure 2-1 Rack-Mounted and Table-Top Models

2.2 INSTALLATION

The PDP-8/E, PDP-8/F, and PDP-8/M Computers are shipped in secure, individual containers. Both the PDP-8/E and the PDP-8/F can also be shipped mounted in DEC cabinets; if this is the case, a fork-lift truck is necessary to move the pallet-mounted containers. To unpack and install the computer or cabinet only small hand tools — pliers, screwdrivers, etc. — and a volt-ohmmeter to check installation potentials are needed.

2.2.1 Unpacking

NOTE

Do not attempt to unpack or install the system until the DEC Sales Office has been notified and a Field Service representative is present. His presence is required to validate the warranty.

2.2.1.1 Individual Containers — If the computer is packaged in its own container, follow the steps listed below. Be sure to keep all packing material — cartons, spacers, pads, polyethylene bags, etc. — for reshipment, if such a step is contemplated.

1 Open the outer carton and remove the inner carton.

2 Open the inner carton.

3 If the computer is a PDP-8/E, remove the switch protector and carefully slide the computer, in its polyethylene bag, out of the carton.

If the computer is a PDP-8/F or PDP-8/M, lift off the side spacer; remove the filter, cables, software, etc., from the rear of the computer; push the computer against the rear of the box so that the switch protector can be removed; lift the computer, in its polyethylene bag, out of the carton.

4 Remove the polyethylene bag; untape the power cord from the rear of the computer.

5 If the computer is a PDP-8/E table-top model, attach the air filters to the sides of the super cover (the filters are shipped in a separate carton together with cables, software, manuals, etc.).

If the computer is a PDP-8/F or PDP-8/M, attach the air filter to the side of the computer; attach the chassis tracks with the hardware provided (the chassis tracks and hardware are shipped in a separate carton).

6 Check that all equipment specified on the accessory list has been received.

2.2.1.2 Cabinet-Mounted Containers – If the computer is mounted in a cabinet, follow the steps listed below.

1 Remove the outer shipping container.

NOTE

The container can be either heavy corrugated cardboard or plywood. Remove all metal straps first, and then remove any fasteners and cleats securing the container to the skid. If applicable, remove the wood framing and supports from around the cabinet.

2 After removing the outer container, if applicable, remove the cardboard container.

3 Remove the polyethylene cover from the cabinet.

4 Remove the tape or plastic shipping pins from the cabinet rear door.

5 Unbolt the cabinet from the shipping skid. The bolts are located on the lower supporting side rails and can be reached by opening the access door.

6 Raise the leveling feet above the level of the casters.

7 Use wooden blocks and planks to form a ramp from the skid to the floor and carefully roll the cabinet onto the floor.

8 Roll the cabinet to the prepared site.

2.2.2 Inspection

After unpacking, inspect and inventory the equipment.

1 Inspect the external surfaces of the chassis for surface, bezel, switch and light damage, etc.

2 Inspect the inside of the cabinet for console and processor damage, loose or broken modules, fan damage, loose nuts, bolts, screws, etc.

3 Inventory all hardware against the key sheet.

4 Inventory all software program tapes against the software checklist.

5 Inventory all prints against the drawing directory.

2.2.3 ac Power Check

Check the site power wiring as outlined below.

WARNING

After the power plug has been inserted in the ac outlet, do not touch the computer or cabinet until it has been determined that the installation is properly grounded.

1 Turn the power switch off.

2 Make sure that all ac power is received from the same source.

3 Insert the power plug into the ac outlet.

4 Use the volt-ohmmeter to ensure that there is no ac voltage from frame-to-ground.

5 Remove the power plug from the ac outlet.

6 Turn the power switch and circuit breaker on.

7 Repeat Steps 3 and 4.

8 Turn the power switch off.

2.2.4 Module Check

Check module jumpers according to Table 2-2; check module locations with the recommended order given in Table 2-3.

NOTE

The recommended order of modules on the OMNIBUS will result in best-case timing and permit widest margins.

Table 2-2
Jumpers

Module	Location	Inserted	Omitted
M8330	Center	Slow Cycle Only	Fast Cycle/Slow Cycle
M8650	Upper Right	1) 37 ASR 2) 33 & 35 ASR	33 & 35 ASR 37 ASR
G104	Lower Right	EMA 0 = "0" EMA 1 = "0" EMA 2 = "0"	EMA 0 = "1" EMA 1 = "1" EMA 2 = "1"
		These are used to select which field this memory will be. (All inserted = Field "0")	
G104	Middle Left	Slice voltage. Factory selected **only.**	
G227	Upper Middle	Current control. Factory selected **only.**	

Table 2-3
Recommended Module Installation Order

Module Designation	Description
KC8-EA KC8-FL KC8-ML	Programmer's Console
M8330	Timing Generator (always after Programmer's Console)
M8340	EAE
M8341	EAE
M8310	C P Major Register Control
M8300	C P Major Registers
M837	Extended Memory & Time Share Control
.	.
.	.
.	.
.	Other Non-Memory Options
.	.
.	.
.	.
M8350	Positive I/O Bus Interface
M849	RFI Shield
G104	Memory Sense/Inhibit (0)
H220	Memory Stack (0)

Table 2-3 (Cont)
Recommended Module Installation Order

Module Designation	Description
G227	Memory X/Y Drivers (0)
.	.
.	.
.	.
G104	Memory Sense/Inhibit (n)
H220	Memory Stack (n)
G227	Memory X/Y Drivers (n)
.	.
.	.
.	.
.	Other Memories
.	.
.	.
.	.
G105	Memory Sense/Inhibit (Parity)
H220	Memory Stack (Parity)
G227	Memory X/Y Drivers (Parity)
M8320	Bus Loads (always in last slot)

2.2.5 Initial Operating Check

Turn on the power switch and check the operation of the front panel switches and indicators. Use the following simple program to check the operation of the basic computer.

a. Load Address 0000
b. Deposit 7001
c. Deposit 2101
d. Deposit 5001
e. Deposit 5000
f. Load Address 0000
g. Rotary Switch to AC position
h. Clear and Cont
i. Observe AC Register incrementing

2.2.6 Teletype Unpacking, Assembly, and Initial Check

1 Open the Teletype carton and remove the packing material. Remove the back cover from the stand. Remove and unwrap the copyholder, chad box, and power pack. Remove the stand from the shipping carton. Remove the Teletype console from the carton, holding it by the wooden pallet attached to the bottom. Snap the power pack in place at the top of the rear side of the Teletype stand. Remove the Teletype console from the pallet, and mount it on the stand. Remove reader, punch, and printer shipping restraints. Connect the Teletype console to the power pack (a 6-lead cable attached at the console is connected to the power pack by means of a white plastic Molex 1375 Female Connector that mates with a male output plug on the power pack). Pass the 3-wire power cable, and the 7-conductor signal cable (which is terminated by a Mate-N-Lok connector) through the opening at the lower left-hand corner of the Teletype stand; then replace the back cover of the stand using the two mounting screws.

2 Turn computer power off.

3 Connect Mate-N-Lok (with 2 ft cable on the M8650) to ensure that the Mate-N-Lok remains inside the cover.

4 Connect the 3-prong male connector of the Teletype power cable to the same ac power source as the computer.

5 Turn the POWER switch on.

6 Install a roll of printer paper into the Teletype keyboard/printer, and install a tape in the punch as described in the Teletype technical manual.

7 Set the LINE/OFF/LOCAL switch to LOCAL.

8 Verify off-line Teletype operation in accordance with the procedures in Chapter 2 of the *PDP-8/E & PDP-8/M Small Computer Handbook.*

9 Verify on-line Teletype punch and reader operation by performing the following test. Load address 0000 and deposit this routine in sequence:

Location	Contents
0000	6032
0001	6031
0002	5001
0003	6036
0004	6046
0005	6041
0006	5005
0007	5001

10 Load address 0000 and press START. Type any character on the keyboard and observe a corresponding echo return on the printer.**11/16,**

2.3 ACCEPTANCE TEST

Perform the acceptance tests referenced in Table 2-4. If abnormal indications are encountered, terminate testing and refer to Chapter 4 for maintenance. Refer to Chapter 2 of the *PDP-8/E & PDP-8/M Small Computer Handbook* for loading the diagnostic programs. The procedure is the same as the example provided in Figure 2-9 of the handbook.

Equipment required: Computer (with 4K of R/W memory), MAINDEC, Programmer's Console, Teletype (33 or 35 ASR modified for operation with computer).

NOTE

If Programmer's Console and Teletype, as described, are not part of the system being installed, they must be made available in good working order by the customer.

Table 2-4
Acceptance Tests

Program Name	MAINDEC No.	SA/SR Setting	Execute Time	Ind.	Accept. Time
Inst. Test I & II	8E-D0AA	200/7777	2 sec	Bell	3 min.
Inst. Test II	8E-D0BA	200/0000	2 sec	Bell	3 min
Adder Test	8E-D0CA	200/0000	35 min	1 SIMAD 2 SIMROT 3 FCT 4 RANDOM	35 min
Basic JMP JMS Test	8E-D0IA	200/0000	10 sec	Bell	3 min
Random TAD Test	8E-D0EA	200/0000	5 sec	T	3 min
Random AND Test	8E-D0DA	200/0000	2 sec	A	3 min
Random ISZ Test	8E-D0FA	200/0000	8 sec	FA	3 min
Random DCA Test	8E-D0GA	200/0000	5 sec	Bell	3 min
Random JMP Test	8E-D0HA	200/0000	8 sec	HA	3 min
Random JMP-JMS Test	8E-D0JA	200/0000	11 sec	JA	3 min
Memory Address Test	8E-DLEA	200/0000	50 sec	EA	5 min
Checkerboard Test	8E-DLAA	200/0000	5 min	5	15 min
Teletype Control Test	8E-D2AA	200/0000			40 min
Mem. ON/OFF Test	8E-DLGA	200/0000			

NOTE When ordering from Program Library:

PB for Binary Tape e.g., after MAINDEC-D0AA-PB
D for Document MAINDEC-D0AA-D

CHAPTER 3
PRINCIPLES OF OPERATION

3.1 INTRODUCTION

This chapter presents three levels of PDP-8/E System operation. First, a simplified block diagram presenting the primary parts of the processor is discussed. Second, a flow chart relating the processor instructions to time states is presented and discussed with appropriate references to the corresponding third-level discussion. The third-level discussion presents the logic theory and is divided into functional groups of logic. A reference to the modules is provided so that continuity between the principles of operation and the engineering drawings exists throughout the discussion.

NOTE

The component designations are for reference only and do not necessarily correspond to those designations on engineering drawings.

Chapter 3 is divided into eight functional sections:

Section 1 — System Introduction

Section 2 — System Flow Diagrams

Section 3 — Timing Generator

Section 4 — Memory System

Section 5 — Central Processor

Section 6 — I/O Transfer Logic

Section 7 — Teletype Control

Section 8 — Power Supply

This format is provided to aid the user in understanding the principles of operation and to distinguish the individual parts of the basic PDP-8/E processor.

3.2 PDP-8/E BASIC SYSTEM

The PDP-8/E processor contains eight functional areas and can accommodate as many as 60 options. A simplified block diagram, Figure 3-1, relates the OMNIBUS to the major signals and the eight functional areas. Each of the functional areas is contained on a single quad-size module with the exception of the MM8-E (three modules are provided).

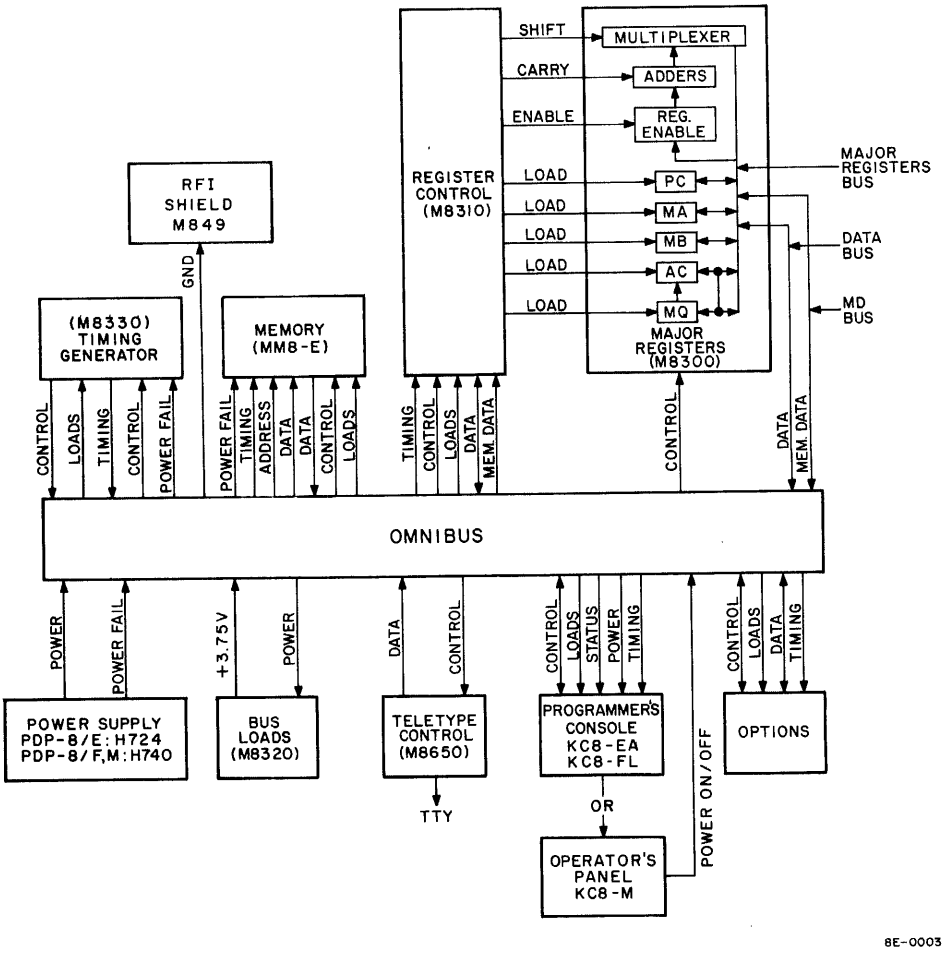


Figure 3-1 PDP-8/E Simplified Block Diagram

3.2.1 OMNIBUS

The OMNIBUS provides a two-way path between the corresponding connector pins of the modules that plug into it. To accommodate 96 signal lines plus ground and power at the module connectors, 144 pins are provided. In general, each signal line is kept at a +3.75 Vdc level and pulled to ground when the signal is asserted. However, exceptions occur, with respect to power levels and some timing and control signals. Bus loads provide this capability by applying +3.75 Vdc to the bus lines via load resistors. When a signal line is asserted, the output driver of that signal pulls the line to ground, the corresponding input circuits (on the same module or a different

module) are activated due to the low signal. This technique facilitates the interaction between modules and makes it possible to connect many modules to the same bus. Some signals do not use the OMNIBUS. The connection of the M8310 Register Control module and the M8300 Major Registers module is partially accomplished using an H851 Edge Connector for all of the control signals. Data is exchanged through the OMNIBUS.

3.2.2 Timing Generator (M8330)

The timing generator provides four time states (TS1 through TS4), four time pulses (TP1 through TP4) and memory timing signals. One memory cycle is accomplished between TS1 and TS4. A choice of two memory cycles is provided: a slow (1.4 μs) and a fast (1.2 μs) cycle. Control inputs are provided by the register control module and the power supply.

3.2.3 Memory (MM8-E)

Three memory modules are provided: the G619 Memory Stack, the G227 X/Y Driver and Current Source, and the G104 Sense/Inhibit.

The memory stack contains 12 core mats, each consisting of 4096 cores and selection diodes to provide a 12 bit-per-word, 4096 word storage capability.

The X/Y driver and current source module contains the selection switches, drivers, and current source required to fully select any one of the 4096 memory locations.

The sense/inhibit module is used to sense (read) any one of the 4096 memory locations and to write into any memory location.

3.2.4 Register Control (M8310)

The register control has many functional logic circuits that generate the major states of the processor, determine the instruction to be performed, and control the operation of the major registers (M8300). The register control receives a word from memory, decodes the word, and determines the operation to be performed. Functional logic is provided to gate bits into the major register adder circuit, shift right, or shift left. The M8310 develops register transfer signals and register load signals. The timing generator determines when these signals are generated.

3.2.5 Major Registers (M8300)

The major registers module provides the Program Counter (PC) Register, the Central Processor Memory Address (CPMA) Register, the Memory Buffer (MB) Register, the Accumulator (AC) Register, and the Multiply-Quotient (MQ) Register. Transfer of information in the AC to the MQ is accomplished directly through enabling logic. Transfer of all other registers is accomplished through the register enable logic, through the adders, and through the output multiplexers, where the information is placed onto the MAJOR REGISTERS BUS. Information can be brought into the MAJOR REGISTERS BUS from the DATA BUS and the MD BUS or transferred out to the same lines. Transfer of MB data to the MD lines is accomplished by MD DIR (H).

3.2.6 Power Supply (H724)

The power supply receives an input of 95 to 130 Vac, 47 to 63 Hz and provides 28 Vac, +8 Vdc, +5 Vdc, -15 Vdc, and +15 Vdc to the PDP-8/E System. The power system is interlocked with the front panel key switch. Power fail and overload detection are provided to ensure the protection of system components and system performance.

3.2.7 Bus Loads (M8320)

The bus loads receive +5 Vdc and +15 Vdc inputs from the power supply and provide a +3.75 Vdc output to the signal lines on the OMNIBUS.

3.2.8 Teletype Control (M8650)

The Teletype control module contains a receive register and transmit register, decoders, and interprets two flags. It performs the conversion of parallel computer words to serial Teletype words, assembles serial Teletype characters into data words for the computer and commands from the computer.

3.2.9 Programmer's Console (KC8-EA)

The programmer's console is a plug-in module, containing logic, lamps, and switches. The face panel, which contains openings for the switch levers and a silk-screened switch/indicator identification, is mounted in front of the programmer's console module. The panel OFF/POWER/PANEL LOCK switch is controlled by a key. The programmer's console enables the operator to deposit a 12-bit word into memory, read any memory location, observe the content of important registers, read the instruction currently being processed, and observe every primary activity the processor is currently performing.

3.2.10 RFI Shield (M849)

The RFI shield module ensures no interference of memory circuits with nonmemory options (those options not synchronized with memory).

3.2.11 Options

More than 60 options are available to the PDP-8/E user. The one option described in this volume is the Teletype control option. All other internal bus options are described in Volume 2. External bus options are described in Volume 3.

3.2.12 Signal Finder

The basic PDP-8/E signals and their descriptions are given in Table 3-1. If the reader desires to study the detailed logic as he is progressing through the flow diagrams, a corresponding paragraph reference to the detailed logic is provided. Refer to Appendix B for source-destination module designations.

Table 3-1
Signal Finder

Signal Name	Logic Reference	Signal Description
DATA T DATA F	3.35.3	Data Control GATE ENABLING signals – DATA BUS TO ADDERS: DATA T, DATA F COMPLEMENT OF DATA BUS TO ADDERS: DATA T, DATA F ZERO TO ADDERS: DATA T, DATA F*
AC → BUS L	3.35.2	Enables the Data Line MUX to allow the contents of the AC to be applied to the DATA BUS.
MQ → BUS L	3.35.2	Enables the Data Line MUX to allow the contents of the MQ to be applied to the DATA BUS.
SHL + LD ENA L AC → MQ ENA L	3.40	Enable signals applied to the MQ MUX to output either the MQ (one place to the left) or the contents of the AC. **SHL + LD ENA L** / **AC → MQ ENA L** / **Output** L / L / MQ (left) L / H / MQ (left) H / L / AC H / H / 0
F SET L D SET L E SET L	3.34.1	Indicates the next major state. For example, F SET L means that the next major state is FETCH.
F L, D L, E L	3.34.1	Indicates the current major state.
DMA	3.8	Direct Memory Access State – asserted when MS, IR DISABLE is grounded.
INT IN PROG	3.42.1	Interrupt in Progress – this signal acknowledges an interrupt request and forces a JMS to the IR and EXECUTE to the Major State Register.
INT REQUEST L	3.42.1	Interrupt Request – when asserted (low) means that a device has set a flag and is requesting an Interrupt.
USER MODE	3.42.1	Used with the time-sharing option to prevent programmed halt, I/O PAUSE, OSR, or LAS.

*This condition cannot exist during OPERATE and TS3.

Table 3-1 (Cont)
Signal Finder

Signal Name	Logic Reference	Signal Description
INT BUS L	3.33.1.2 3.33.2.2	When the programmer's console STATUS switch is in STATUS, an INT REQUEST occurs, and the INT BUS indicator is illuminated.
LOAD, AC MQ MB CPMA PC	3.37	When data is to be placed into one of the Major Registers, the corresponding load signal is developed.
INT STROBE	3.41	Interrupt Strobe – Developed by BUS STROBE and NOT LAST XFER or TP3 to set the INTERRUPT SYNC flip-flop. Used by the interrupt and break systems.
I/O PAUSE L	3.41.2	Signifies that an IOT is being processed. It is used by the peripheral control modules to gate device selectors and to gate data onto the DATA BUS. This signal is used to initiate OUTPUT transfers; in the central processor, it is used to control IOT decoding.
BUS STROBE L	3.41.2	BUS STROBE L is used for IOT instructions to load data into the AC or PC and, with NOT LAST XFER L, generates INTERRUPT STROBE.
INTERNAL I/O L	3.41.4	Used to inhibit the generation of IOPS by the positive I/O bus interface.
C0 L, C1 L, C2 L	3.41.1	Controls the type of I/O data transfer between a device and the processor.
MS, IR DISABLE L	3.34	Major State, Instruction Register Disable – Used during Direct Memory Access to disable FETCH, DEFER, or EXECUTE major state and instruction register.
KEY CONT L	3.33.1.1	Key Control – A control signal developed in the front panel logic.
STOP L	3.16	Stop resets the RUN flip-flop and causes timing to halt at TS1.
CONT	3.33.1.1	Continue – A front panel key to force the processor into automatic timing.
ADDR LOAD L	3.33.1.1	Address Load – A front panel key used to manually load an address into the CPMA.

Table 3-1 (Cont)
Signal Finder

Signal Name	Logic Reference	Signal Description
EXTD ADDR L	3.33.1.1	Extended Address Load – A front panel key used to manually load the address of extended memory.
DATA 0–11 L		The DATA BUS containing 12 bits of information.
FIELD	3.27.4	Corresponds to extended memory up to 32K as follows: BASIC MEMORY: FIELD 0 EXTENDED MEMORY: FIELD 1 – FIELD 7
NOT LAST XFER L	3.41.2	Used primarily with the device on the positive I/O bus, requiring more than 1.2 μs to perform an IOT.
BRK DATA CONT L	3.8.2 and 3.33.1.1	Used to gate the contents of the MD BUS through the Register Input Multiplexer.
EN0 EN1 EN2	3.35.1	Register Input Multiplexer enabling signals to allow the contents of the Major Registers to be placed into the ADDERS.
OVERFLOW L	3.39	Overflow – Occurs when carry-out is asserted from adder state 0 at TP2.
CAR OUT L	3.39	Carry Out – Asserted when 7777_8 is incremented by 1 in the adder.
CAR IN L	3.36.1	Carry In – Developed to add a 1 to a register.
SKIP L	3.38	The output of the SKIP flip-flop is applied to carry-in logic. SKIP is set during a variety of conditions such as OVERFLOW during an ISZ instruction and programmed microinstructions (GROUP 2).
SHIFT– LEFT L RIGHT L TWICE L NO SHIFT L	3.36.2	Shift Signals that cause the adder output multiplexer to shift left, or right, or twice left or twice right, or byte swap.
PAGE Z L	3.36.2	Asserted when Page Zero is to be addressed. PAGE Z is applied to the adder output multiplexer to apply zeros to CPMA0-4.

Table 3-1 (Cont)
Signal Finder

Signal Name	Logic Reference	Signal Description
MD DIR L	3.28	Memory Data Direction – Used to control memory data during the read and write operation. MD DIR L: Places the contents of the MEM REG on the MD BUS. MD DIR: Places the contents of the MB Register on the MD BUS.
DEP	3.33.1.1	Deposit – A front panel key used to manually load information into memory.

3.3 DATA PATHS

Because the OMNIBUS concept is different from other PDP-8 family processors, the reader should understand the relationship of the data paths to the OMNIBUS.

The OMNIBUS should be considered a bus containing several buses. A bus is defined as a group of 12 signal lines, carrying information. With this definition, the PDP-8/E contains the MEMORY DATA (MD) BUS, the DATA BUS, the MEMORY ADDRESS (MA) BUS, and the MAJOR REGISTER BUS. All buses (except MAJOR REGISTER BUS) are on the OMNIBUS. The OMNIBUS also contains the transfer control signals for I/O operations.

Data paths are illustrated in Figure 3-2. Although the illustration does not show all of the signals on the OMNIBUS, it is obvious from the data paths that signal origins and destinations appear in many places. Using the MD BUS as an example, memory data is provided by the Memory Register, the MB Register, and memory options. The MA BUS receives the memory address from the CPMA Register and from some options that generate the 12 address bits. The MA BUS applies these 12 bits to the XY selection decoder of the memory. The DATA BUS is used to receive Switch Register data, provide status to the Programmer's Console, carry information to and from a peripheral or internal option, and provide a path for data to the MAJOR REGISTERS BUS.

The MAJOR REGISTERS BUS completes a return path to each of the major registers. The CPU controls inputs to the major registers, and the enabling logic causes operations such as swapping, shifting, ANDing, ORing, and loading to manipulate data and select one of the registers to place the results. If the results are to be stored in memory, for example, the MB Register is loaded and gated onto the MD BUS by MD DIR L. This same information is carried to the inhibit drivers and stored in the selected memory location. If an option such as the EAE that is plugged into the OMNIBUS wanted the results of the data manipulation, the data path is from the MAJOR REGISTERS BUS to the DATA BUS. This condition is caused by loading either the MQ or the AC with the data and enabling the transfer of the data onto the DATA BUS. To place the data contained in some memory location onto the DATA BUS, the memory location must first be selected. The content of the memory location must be sensed and applied to the Memory Register. Signal MD DIR L gates the Memory Register out to the MD BUS. From the MD BUS the data is applied to the Register Multiplexer and to the MAJOR REGISTERS BUS via the adder and output multiplexer. Signal AC → BUS L places the data onto the DATA BUS.

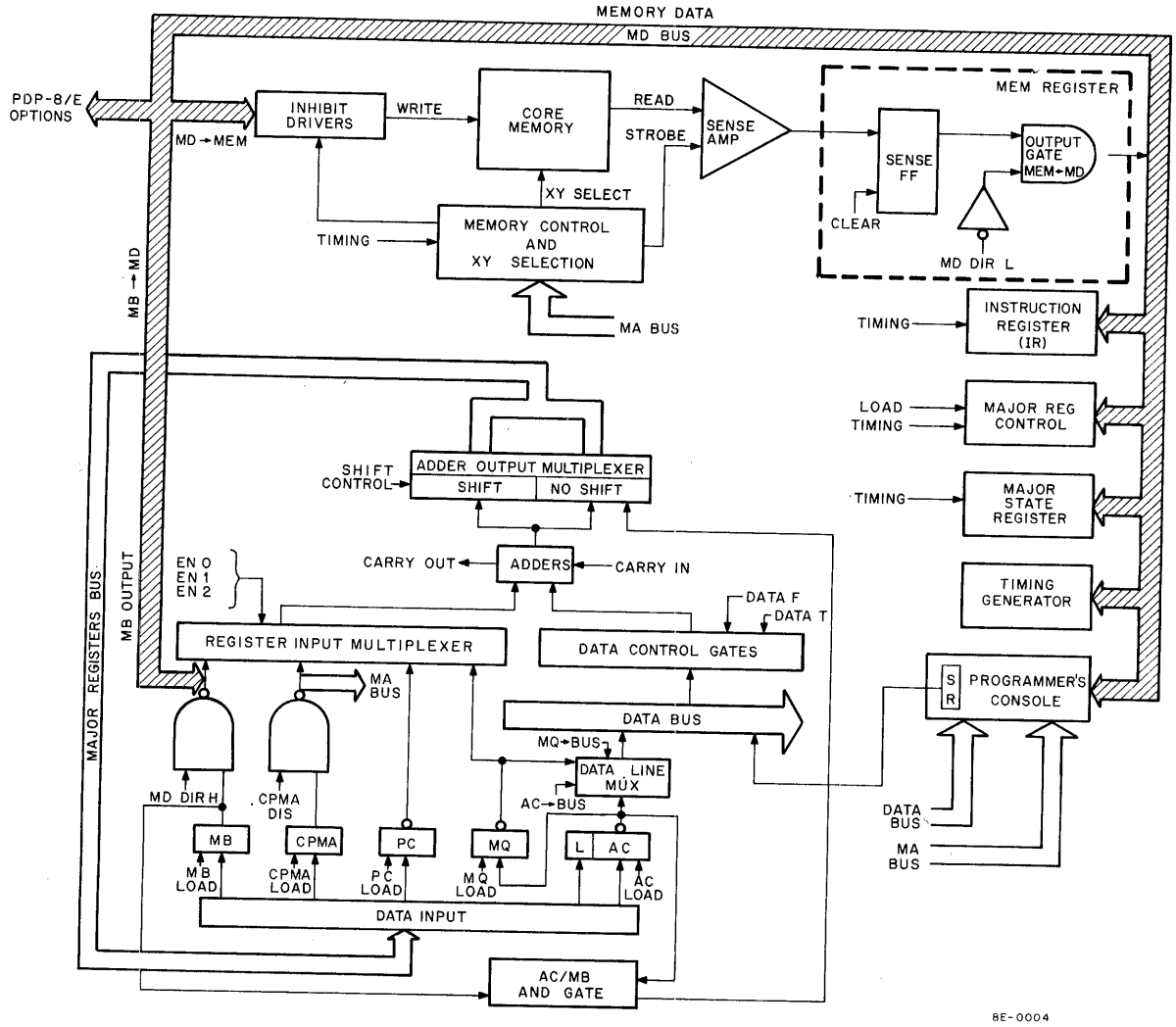


Figure 3-2 Basic Data Paths

3.3.1 Basic Transfer Control Signals

Table 3-2 traces the data paths (Figure 3-2) from the major registers through to the MAJOR REGISTERS BUS and returns to a selected register. Each control signal is referenced to the detailed logic description; thus, the reader can see how the control signal is developed.

Table 3-2
Basic Transfer Control Signals

From	To	Basic Control Signal	Logic Reference
SWITCH Register	DATA BUS	DEPOSIT	3.33.1.1
SWITCH Register	DATA BUS	LOAD ADDRESS	3.33.1.1
AC Register	DATA BUS	AC → BUS	3.35.2
MQ Register	DATA BUS	MQ → BUS	3.35.2
AC Register	MQ REG	AC → MQ ENA LOAD MQ	3.40
DATA BUS	ADDERS	DATA T DATA F	3.35.3
Complement of DATA BUS	ADDERS	DATA T DATA F	3.35.3
MQ Register	ADDERS	EN0 EN1 EN2	3.35.1
PC Register	ADDERS	EN0 EN1 EN2	3.35.1
CPMA Register	ADDERS	EN0 EN1 EN2 CPMA DIS L	3.35.1 asserted low by options
CPMA Register	MA BUS	CPMA DIS L	
MB Register	MD BUS	MD DIR L	3.28
MD BUS	ADDERS	EN0 EN1 EN2	3.35.1
MAJ REG BUS	MB REG	MB LOAD L	3.37.1

Table 3-2 (Cont)
Basic Transfer Control Signals

From	To	Basic Control Signal	Logic Reference
MAJ REG BUS	CPMA REG	CPMA LOAD L	3.37.4
MAJ REG BUS	PC REG	PC LOAD L	3.37.3
MQ MUX	MQ REG	MQ LOAD L	3.40
MAJ REG BUS	AC REG	AC LOAD L	3.37.2
CPMA	CPMA + 1	CARRY IN L	3.36.1
PC	PC + 1	CARRY IN L	3.36.1
MEM REG	MD BUS	MD DIR L	3.28

FROM	TO	Logic Reference
ADDERS	MAJOR REGISTERS BUS	3.36.2

Type of Operation	Shift Control Signals				
	PAGE Z L	RIGHT L	LEFT L	TWICE L	
ZEROs TO MA 0–4 (PAGE ZERO)	H	L	L	L	
AND MB WITH (MB•AC)	L	L	L	H	
SHIFT OUTPUT OF ADDERS RIGHT ONCE	L	L	H	H	
SHIFT OUTPUT OF ADDERS LEFT ONCE	L	H	L	H	
SHIFT OUTPUT OF ADDERS RIGHT TWICE	L	L	H	L	
SHIFT OUTPUT OF ADDERS LEFT TWICE	L	H	L	L	
BYTE SWAP (SWAP first six bits with last six bits)	L	H	H	L	
NO SHIFT	L	H	H	H	

3.4 PROCESSOR BASIC TIMING

Four time states, TS1 through TS4, are provided by the timing generator to divide the processor cycle into four parts (Figure 3-3). The major states control the flow of events during the execution of programmed instructions.

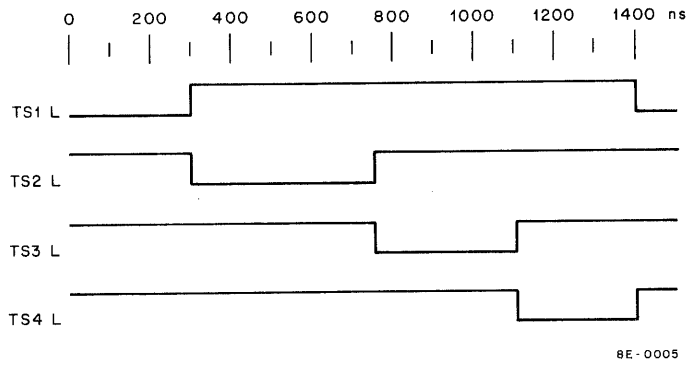


Figure 3-3 Processor Timing States (Slow Cycle)

SECTION 2 – SYSTEM FLOW DIAGRAMS

3.5 PROCESSOR MAJOR STATES FLOW

The PDP-8/e provides four major states:

a. FETCH, to obtain the Memory Reference Instruction and Nonmemory Reference Instructions from memory, and perform Nonmemory Reference Instructions

b. DEFER, for indirect addressing or autoindexing

c. EXECUTE, for performing the Memory Reference Instruction

d. Direct Memory Access (DMA), for manual operation or data break.

The basic major state flow diagram is illustrated in Figure 3-4. This diagram also indicates the order in which the major states are implemented. For any type of processor instruction, the processor must bring the contents of some memory location to the MD BUS. The Instruction Register (IR) decodes the first three bits (0–2). With FETCH major state asserted and the instruction decoded, the Central Processor (CPU) follows a series of steps; these steps are controlled by timing and the logic of the CPU.

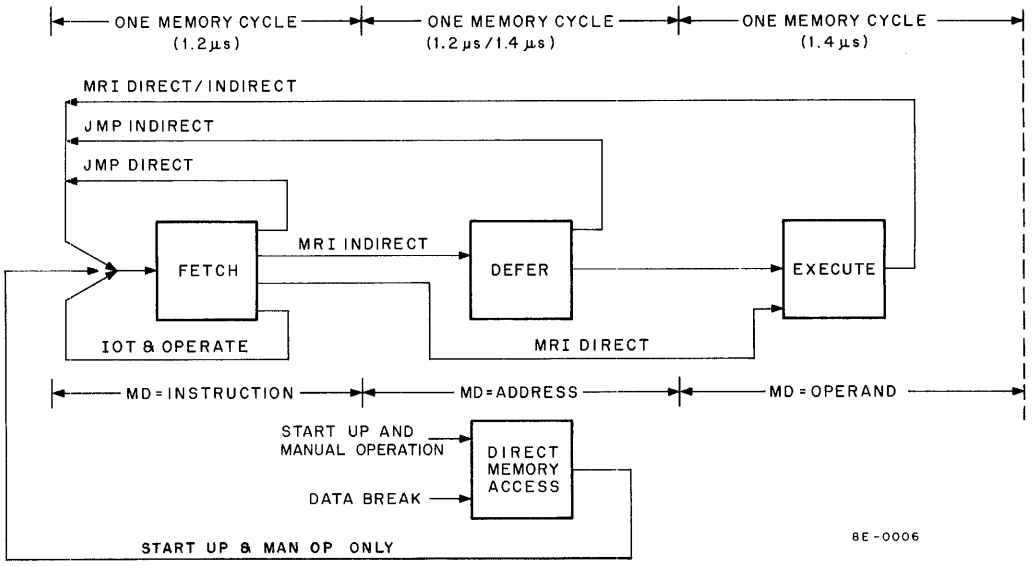


Figure 3-4 PDP-8/E Major State Flow Diagram

The FETCH major state is required for all instructions. For Memory Reference Instructions (MRI), the CPU enters the EXECUTE state via DEFER (for an indirect address) or the EXECUTE state (for a direct address). IOT and OPERATE instructions are completed in one memory cycle during FETCH. However, an MRI can take either 2 or 3 cycles (depending on a direct or indirect address). Most instructions, therefore, take 2.6 μs or 3.8 μs, depending on the addressing.

In Figure 3-4, during the FETCH cycle, the content of the MD BUS is the instruction and an address; during the DEFER cycle, the content of the MD BUS is an address; during the EXECUTE state, the MD BUS contains the operand (that data contained in the addressed location on which the instruction will manipulate or modify). The DEFER cycle is 1.2 μs for an indirect address and 1.4 μs for an autoindex.

A fourth major state is Direct Memory Access (DMA). During the DMA state, manual functions can be accomplished or the data break system can operate. Both the manual and data break operations require access to a memory location with little help from the CPU control.

3.6 START-UP FLOW DIAGRAM

The following information describes the events of the Start-Up flow diagram illustrated in Figure 3-5. A flow reference keys the flow diagram with the corresponding explanation.

Flow Reference	Explanation
(1)	TURN KEY TO POWER – The POWER position of the OFF-POWER-PANEL LOCK switch generates the INITIALIZE signal in the timing generator. INITIALIZE is used to clear the AC Register, the Link, the Skip circuit, flags, etc. Operation of the CLEAR key also generates INITIALIZE.
(2)	LOAD ADDRESS – The operator sets the switch register to the desired address and depresses the ADDR LOAD key. At the same time the address is loaded, signals MS IR DISABLE L and F SET L are asserted; consequently, the next cycle major state is FETCH. If restart is desired, the state of the AC Register, Link circuit, Skip circuit, and flags should be cleared immediately after the address is loaded. CLEAR develops signal INITIALIZE, as previously described.
(3)	EXAMINE OR DEPOSIT – To examine the contents of the addressed memory location or deposit a word into memory, branching into the Dep/Exam Flow (Paragraph 3.8.2) is required. When the operator has finished, the Start-Up flow is resumed.
(4)	DEPRESS CONT KEY – The assertion of the CONT (continue) key asserts MEM START (Paragraph 3.33.1.1) which, in turn, asserts signal RUN (Paragraph 3.16). Because RUN is necessary to start timing, the timing chain begins at the next clock pulse and continues as long as RUN is asserted.
(5)	FETCH CYCLE – The FETCH cycle is automatically entered if D SET L or E SET L of the Major State Register has not been asserted. Refer to Paragraph 3.9 for the FETCH state discussion.

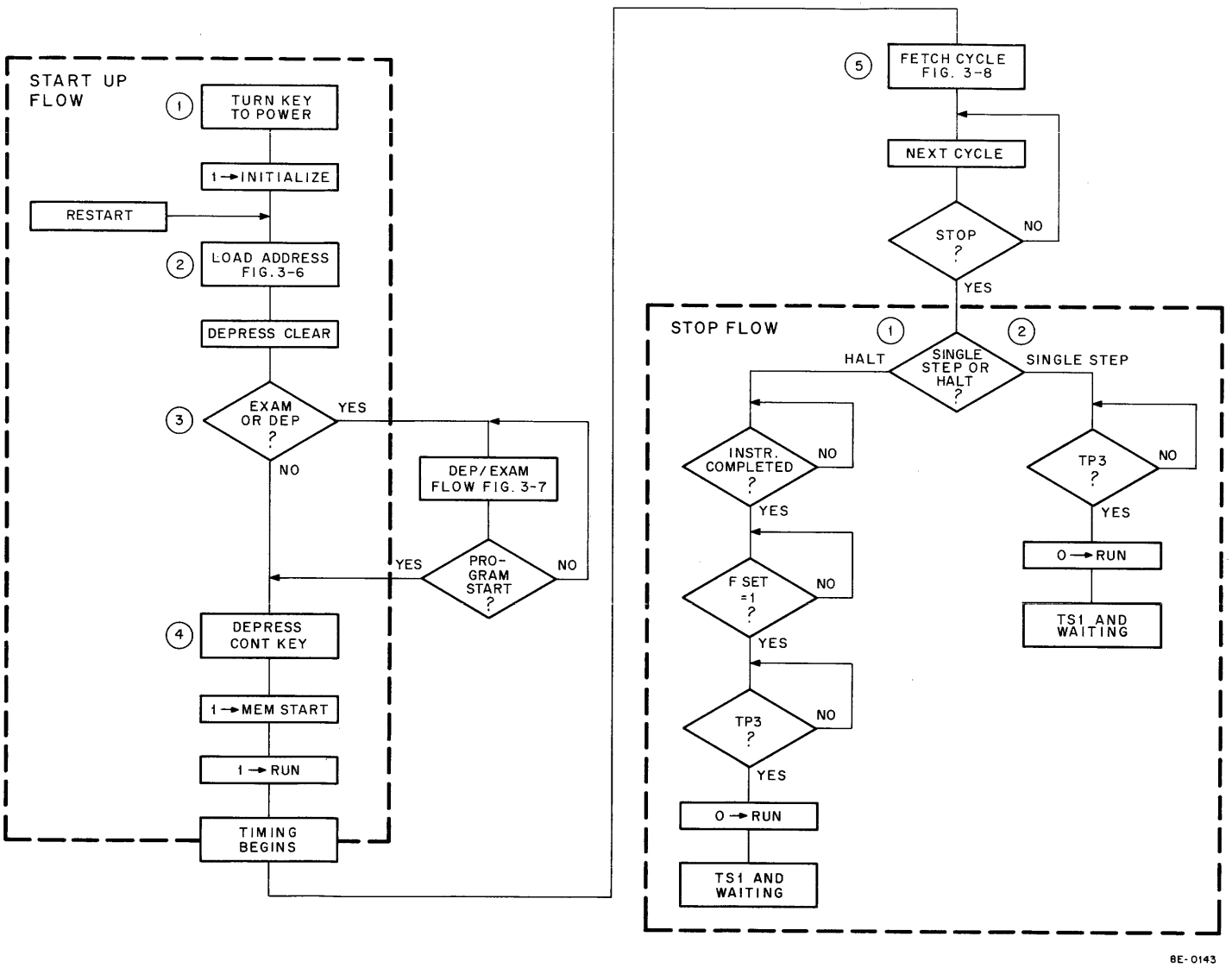


Figure 3-5 Start-Up/Stop Flow Diagram

3.7 STOP FLOW DIAGRAM

The Stop flow diagram is presented in Figure 3-5. The two methods of manually stopping the processor are indicated as either halt or single step.

Flow Reference	Explanation
(1)	HALT – There are two methods of generating a HALT command: (a) program the HALT instruction (Paragraph 3.9.2), or (b) depress the HALT key as shown in Figure 3-5. The HALT command allows the processor to complete the current instruction; this could take up to three processor cycles (FETCH, DEFER, EXECUTE), depending on the type of instruction being processed when the HALT command is received. At TP3 when F SET L is asserted, signal RUN is made inactive (Paragraph 3.16). Thus, the timing chain is interrupted, and the processor is halted in TS1.
(2)	SINGLE STEP – When the SING STEP key is depressed, the processor halts at the end of the current cycle. Because it does not wait until F SET L is asserted, the processor does not necessarily finish the current instruction. (This is the only difference between halt and single step.)

3.8 DIRECT MEMORY ACCESS (DMA) STATE FLOW DIAGRAMS

The Direct Memory Access (DMA) state allows accessing of memory when the Major State Register and Instruction Register of the CPU are disabled. Two types of DMA are available with the PDP-8/E System: (a) the basic type is the use of the Programmer's Console to either deposit into memory or retrieve from memory a 12-bit word, and (b) the second type is called data break and is used with mass storage equipments. A simplified flow diagram representing both types is provided in Figure 3-4. Refer to the *PDP-8/E & PDP-8/M Small Computer Handbook,* Chapter 6, and Volume 3 of this manual for a discussion of data break.

3.8.1 Load Address Flow Diagram

The Programmer's Console is used for manual addressing of memory. Using 12 switches, the operator can load the CPMA Register with a desired address whenever the ADDR LOAD key is depressed. In a similar manner, the Extended Address is loaded. A flow diagram representing the basic functions is presented in Figure 3-6.

Flow Reference	Explanation
(1)	LOAD ADDRESS – A 12-bit address is first set into the switch register, and the ADDR LOAD key is depressed. The following events occur: a. The contents of the Switch Register are transferred onto the DATA BUS. b. The outputs of the Major State (MS) Register and Instruction Register (IR) are disabled; F SET L is asserted. c. The register input multiplexer is disabled. d. The data control gate is enabled. e. Signal CPMA LOAD is asserted, loading CPMA, and setting the FETCH flip-flop in the MS Register.

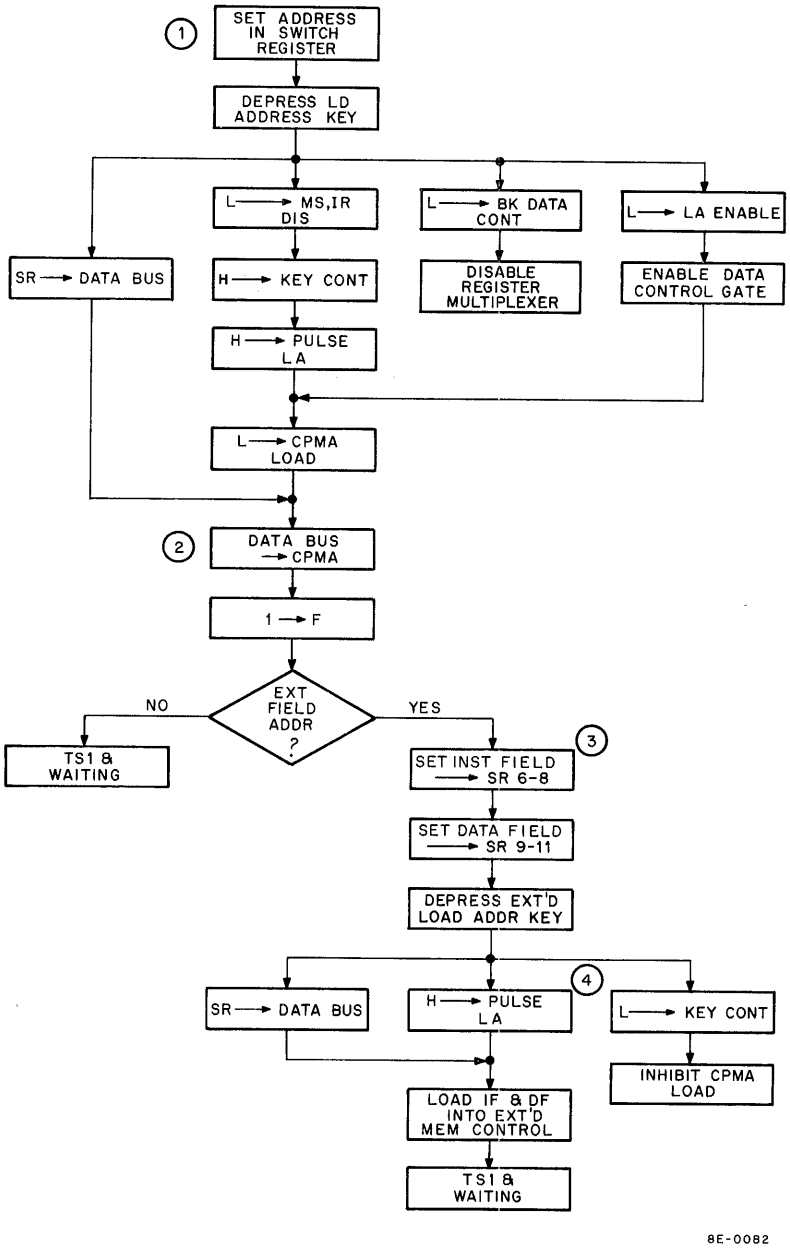


Figure 3-6 Manual ADDR LOAD/EXTD LOAD

Flow Reference	Explanation
(2)	DATA BUS → CPMA – The contents of the DATA BUS (Figure 3-2) follow the path through the data control gate into the adder, through the no shift portion of the output multiplexer, and onto the MAJOR REGISTERS BUS. Signal CPMA LOAD L then gates the contents of the MAJOR REGISTERS BUS into the CPMA Register. FETCH L is developed by CPMA LOAD L (Paragraph 3.34.1). Thus, the processor will be in the FETCH state during the next processor cycle unless direct memory access is again required. However, because the timing chain was never activated during LOAD ADDRESS events, the processor time state will be in TS1 and waiting.
(3)	If extended address is required, the following events must occur: a. Load the Instruction Field into Switch Register (SR) bits 6 through 8. b. Load Data Field into SR bits 9 through 11. c. Depress EXTD ADDR LOAD key.
(4)	The contents of the SR are then transferred to the DATA BUS and applied to the extended memory control module. All circuits within the major registers are inhibited.

3.8.2 Deposit/Examine Flow Diagram

The similarities and differences in the Deposit and Examine events are illustrated in Figure 3-7. For Examine (shown on the left of the figure), it is necessary to read the addressed memory location; for Deposit (shown on the right of the figure), it is necessary to write into the addressed memory location; common events are shown in the center of the figure.

Flow Reference	Explanation
(1)	EXAMINE – Depressing the EXAM key asserts both BRK DATA CONT L and MD DIR L. These signals are necessary to read from memory and also allow the contents of the MD BUS to be applied to the MB Register.
(1)	DEPOSIT – The data word must first be manually selected on the SR. The DEP key is then lifted and the contents of the SR are then applied to the DATA BUS (Figure 3-2).

3.8.2.1 Examine or Deposit Common Events – Depressing either the EXAM or DEP key causes the following events to occur:

Flow Reference	Explanation
(2)	The major states and Instruction Registers are disabled (Paragraph 3.33.1.1).
(3)	Signal RUN L is asserted by MEM START L (Paragraph 3.16) and timing begins.
(4)	Signal STOP is asserted by KEY CONT L. At TP3 time, STOP is used to 0 the RUN flip-flop.

Flow Reference	Explanation
(5)	The contents of the CPMA Register are gated through the Register Input Multiplexer (Figure 3-2) and placed onto the adder circuits. A CAR IN signal is developed (Paragraph 3.36.1), adding 1 to the sum of the adder inputs. The result is then loaded into the PC Register to provide "MA + 1 to the PC".
(6)	MEM TO MD – The READ operation (Paragraph 3.27.2) begins during TS1 and continues into a portion of TS2. This places the contents of the addressed memory location onto the MD BUS (Figure 3-2). Thus, the contents of memory are now ready to be gated onto the MAJOR REGISTERS BUS during TS2.
(7)	EXAMINE – The contents of the MD BUS (12 bits) are gated through the Register Input Multiplexer during TS2 (Paragraph 3.35.1) and placed onto the MAJOR REGISTERS BUS (Figure 3-2). The 12-bit word is now ready to be loaded into the MB Register at TP2. BRK DATA CONT L is pulled low to ENABLE DATA PLUS MD to the MB. The data lines, in this case, are 0s (high).
(8)	DEPOSIT – The contents of the DATA BUS are gated through the Data Control Gate and applied to the MAJOR REGISTERS BUS (Figure 3-2). The 12-bit word is now ready to be loaded into the MB Register.
(8)	MB load occurs at TP2 (Paragraph 3.37.1). At this time, the contents of the MAJOR REGISTERS BUS are loaded into the MB Register.
(9)	With the READ operation completed, it is necessary to write the same information back into memory or deposit new information. However, the contents of the MB Register must first be transferred to the MD BUS. This occurs when MD DIR L is negated (Figure 3-2).
(10)	A 0 is placed in the RUN flip-flop (Paragraph 3.33.1.1) when TP3 and STOP are both asserted. This prevents the processor from starting a new cycle until some action is taken by the operator.
(11)	The WRITE operation automatically starts during TS3 and continues into TS4. At this time, the contents of the MD BUS are written into the addressed memory location.
(12)	For the preparation of the next processor cycle, the next sequential address is automatically placed in the CPMA Register. Because the Program Counter (PC) contains the next address, the contents of the PC are loaded into the CPMA at TP4. If the operator desires to go into programmed operation, the CONT key must be depressed. Because the next active state will be either DMA or FETCH, depressing the EXAM key or raising the DEP key inhibits the Major State Register and allows one more DMA cycle. Otherwise, depressing the CONT key (Figure 3-6) causes a FETCH cycle.
(13)	During TS1 and when RUN = 0, the processor timing stops and waits for the next command from the operator. The contents of the MD BUS can be observed at this time. Also note that the CPMA shows the address for the next cycle and not the address from which the data was examined.

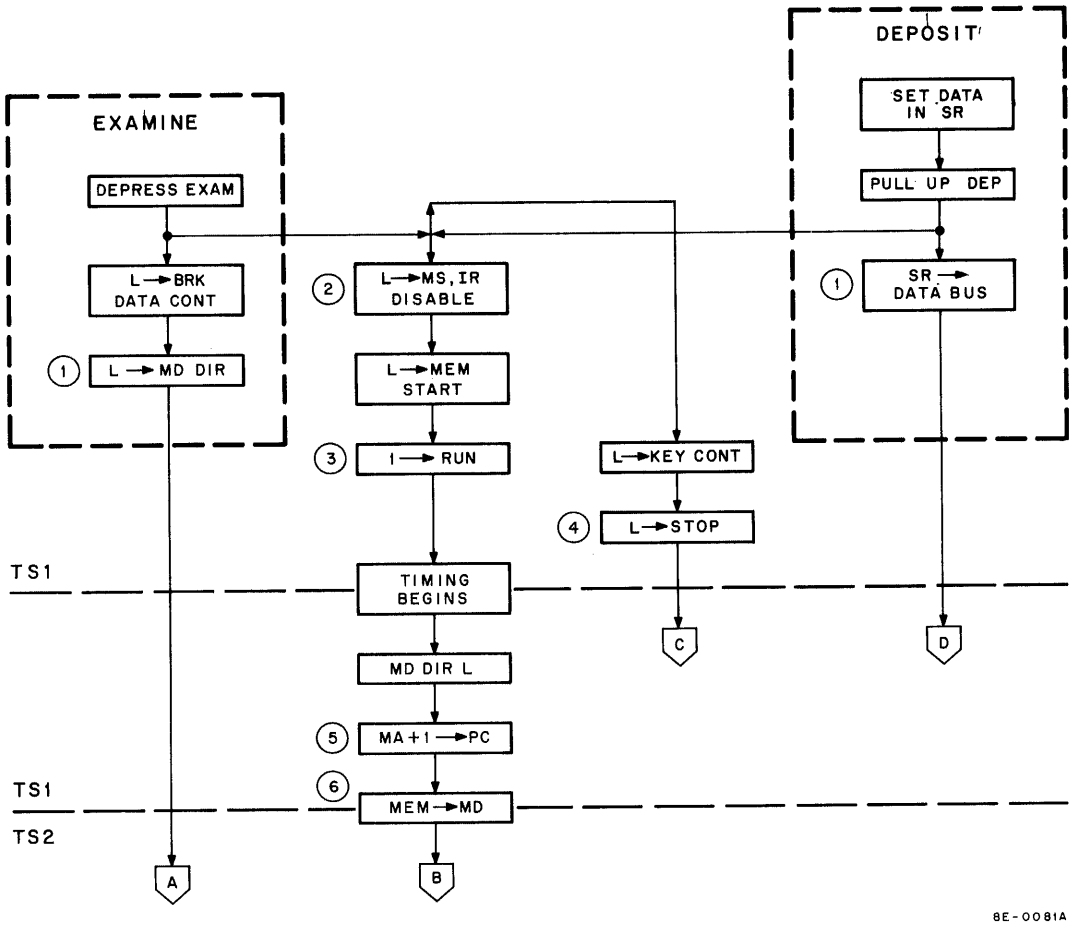


Figure 3-7 Deposit/Examine Flow Diagram (Sheet 1 of 2)

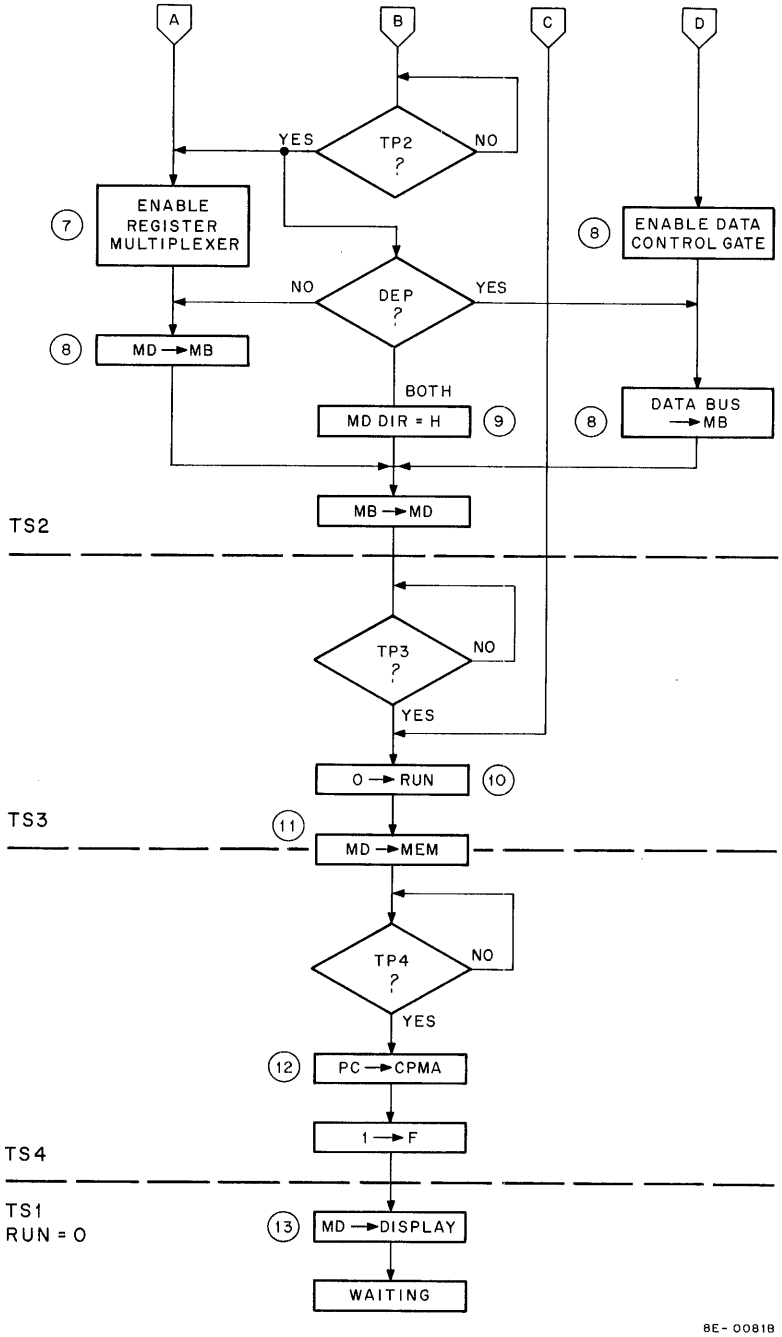


Figure 3-7 Deposit/Examine Flow Diagram (Sheet 2 of 2)

3.9 FETCH STATE INSTRUCTION FLOW DIAGRAM

The logic and instruction flow of events during FETCH is illustrated in Figure 3-8. Because of the complexity of the flow diagrams, the discussion is further divided into subflows as illustrated.

3.9.1 Common Events During FETCH (refer to Figure 3-2 for data paths)

Time State	Common Event
TS1	Update the PC Register, read the addressed memory location, and display the content of Major Registers.
TS2	Read the addressed memory location, transfer the content to the MD BUS, and decode the instruction.
TS3	Perform an augmented instruction (IOT or OPERATE), and begin writing the content of the MD BUS back into the addressed memory location or carry the Memory Reference Instruction to either the DEFER or EXECUTE state. Load the AC Register.
TS4	Update or modify the CPMA and complete the write operation. Enable the next processor major state (FETCH, DEFER, or EXECUTE).

Flow Reference	Explanation
(1)	CLEAR SKIP LOGIC – The SKIP flip-flop (Paragraph 3.38) is cleared during TS1.
(2)	INCREMENT PC – The Carry In logic (Paragraph 3.36.1) is asserted and applied to the adder circuit (bit 11). MA is then brought to the adder circuits and the results placed in the PC.
(3)	TRANSFER AC → PERIPHERAL – The content of the AC is placed on the DATA BUS to be used as determined by the user.
(4)	The content of the Memory Register is gated onto the MD BUS when MD DIR is low.
(5)	During FETCH, the first three bits of MD are decoded by the Instruction Register (Paragraph 3.34.2) to determine the type of instruction to be performed.
(6)	When MD bits 0–2 contain 1s, a 7 is decoded, indicating that an operate instruction is to be performed.
(6)	Three groups of operate instructions are available. The group selected depends on the state of MD3 and MD11. Refer to the following paragraphs for the flow diagrams: Group 1 Paragraph 3.9.2 Group 2 Paragraph 3.9.3 Group 3 Paragraph 3.9.4

Flow Reference	Explanation
(7)	Update CPMA – Before the CPMA can be updated, the interrupt system must be considered. If the INT IN PROG signal is asserted, a JMS is forced into the IR, the major state becomes EXECUTE, and 0s are placed into the CPMA. If the INT IN PROG signal is not asserted, the SKIP L signal is tested next. SKIP L may have been asserted as the result of one of the operate instructions or one of the IOT instructions during TS3. When SKIP L is asserted, a CAR IN L signal is generated which places a 1 in adder stage 11. The Register Input Multiplexer is enabled to allow the content of the PC Register (Figure 3-2) to be applied to the adders. The result is then transferred through the Adder Output Multiplexer to the MAJOR REGISTERS BUS and loaded into the CPMA at TP4. Without SKIP L, only the content of the PC will be loaded into the CPMA. The next major state will be FETCH if an IOT, OPERATE, or direct JUMP is performed. Signal F SET L enables the FETCH state.
(8)	IOT INSTRUCTIONS – When bits MD0 and 1 contain 1s and bit 2 is a 0, a 6 is decoded indicating that an IOT instruction is to be performed. Two types of programmed IOTs are available in the PDP-8/E System. Refer to the following paragraphs for the flow diagrams; I/O Transfers (IOTs) Paragraph 3.9.5 Programmed Interrupt System Paragraph 3.9.6
(9)	JUMP Instruction – When the decoded instruction is 5_8, the PC is modified during TS3. If MD3 L = 0, the new PC is transferred to the CPMA, and the next cycle is FETCH. If MD3 L = 1, the CPMA is modified in the same manner as the PC, and the next cycle is DEFER. Refer to Paragraph 3.9.7 for the flow diagram and an explanation of the JUMP instruction.
(10)	When instructions AND, TAD, ISZ, DCA, and JMS are decoded during FETCH, the processor examines the page bit (MD4 L) and the direct/indirect address bit (MD3 L) to determine if the next address is on Page 0 or the current page, and if the next address contains an address or data. The result is the entrance into the DEFER state or the EXECUTE state. No other operation is performed with these instructions during FETCH.
(11)	Modify CPMA – The page bit is first examined to determine if the next address is on the current page (MD4 L = 1) or Page 0 (MD4 L = 0). When MD4 L = 0, signal PAGE Z is asserted. This places 0s onto the first five stages of the Adder Output Multiplexer. The last seven bits of the MD BUS are applied directly to the Adder Output Multiplexer. All 12 bits are applied to the MAJOR REGISTERS BUS and loaded into the CPMA at TP4. If PAGE Z L is not asserted, MA0 L – MA4 L are applied to the output of the Adder Output Multiplexer. Bit 3 is then examined; if bit 3 = 1, signal D SET L is asserted and the next cycle is DEFER. Otherwise, E SET L is asserted, and the processor obtains data rather than a new address. **NOTE** **Refer to Jump Instruction (Paragraph 3.9.7) and the memory addressing discussion in Chapter 4 of the PDP-8/E & PDP-8/M Small Computer Handbook.**

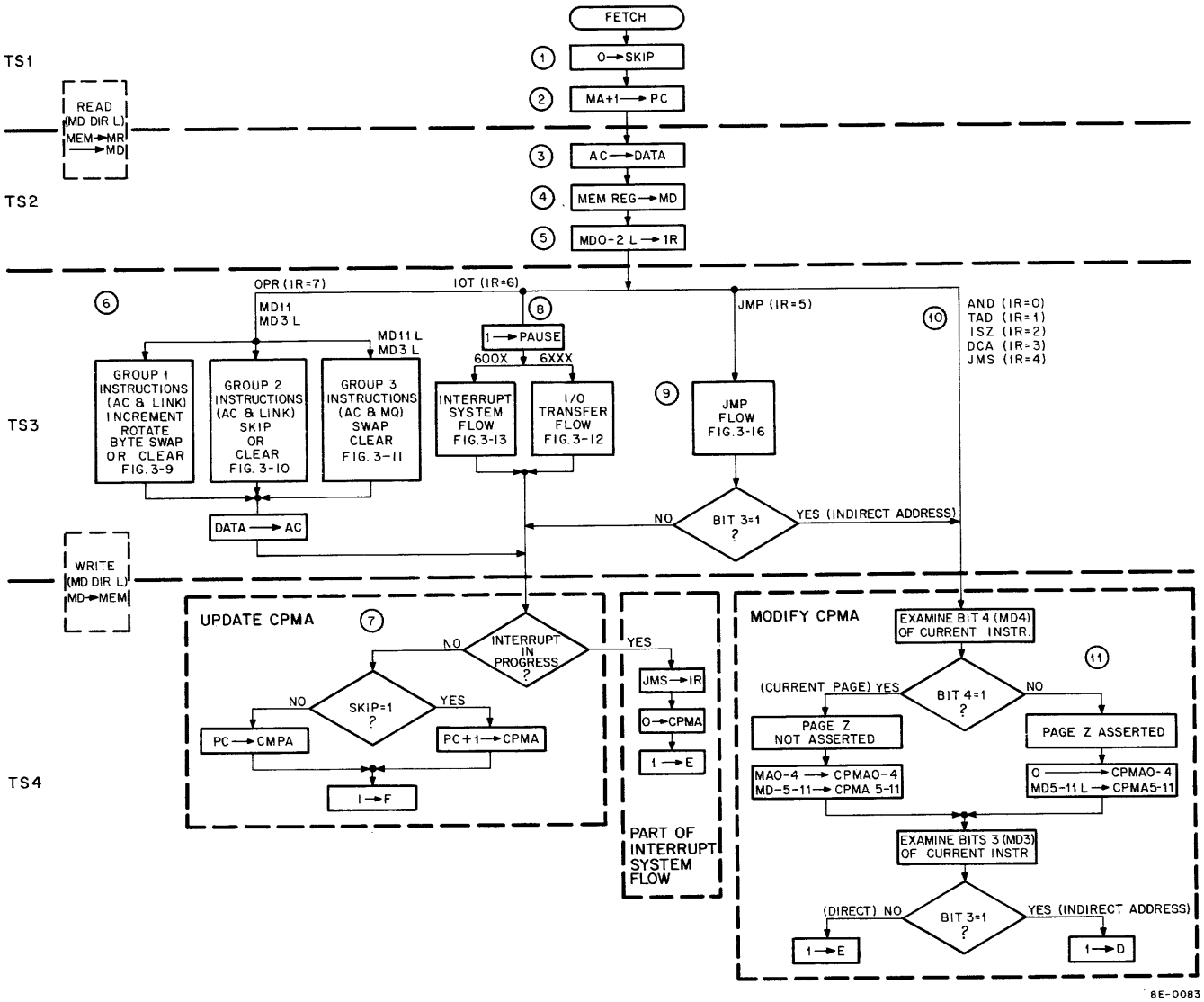


Figure 3-8 FETCH State Flow Diagram

3.9.2 Group 1 Operate Microinstructions Flow Diagram

Group 1 operate microinstructions are established when IR = 7 and when MD3 L = 0 is decoded. Eleven basic instructions are illustrated in Figure 3-9.

3.9.2.1 Data Paths – The data path for all Group 1 instructions is illustrated in Figure 3-2. The common gating and control signals are listed below:

Data Path	Control Signal		Source
AC to DATA BUS (exception is 7200)	AC → BUS L		Paragraph 3.35.3
DATA BUS to adders	True:	DATA T DATA F	Paragraph 3.35.3
	Complement:	DATA T DATA F	DATA T
Adder Output Multiplexer to MAJOR REGISTERS BUS	PAGE Z always L RIGHT L LEFT L TWICE L or none of these		Paragraph 3.36.2
LINK-ADDER-OUTPUT MUX to LINK	LINK data and clock		Paragraph 3.39
MAJOR REGISTERS BUS to AC Register	AC LOAD L		Paragraph 3.37.2

3.9.2.2 Basic Instructions

7000 – NOP -- The NOP instruction allows the processor to cycle through one memory cycle with no important operation being implemented during TS3. Note that an AC-to-AC and LINK-to-LINK transfer is accomplished.

7001 – Increment AC – The content of the AC Register is applied to the DATA BUS when AC → BUS L is asserted. DATA F is high and DATA T L is low to allow the content of the bus to be applied to the adders. MD11 L forces a 1 into the adders from the carry in logic. The 1 is applied to bit 11 of the adders; the result is applied to the data input of the AC Register. AC and LINK are loaded during TP3.

7002 – BYTE SWAP – The first six bits of the AC Register are swapped with the last six bits. The content of the AC Register is placed on the DATA BUS and then applied to the adders by DATA T L and DATA F. AC → DATA BUS is enabled by MD4 L and MD7 L = 0. Signal TWICE L is asserted when MD10 L = 1 and will cause a parallel shift right six positions when MD8 L and MD9 L = 0. AC and LINK are loaded during TP3. However, LINK is unchanged.

7004 – Rotate Once Left – The contents of the AC are placed on the DATA BUS by signal AC → BUS L. DATA F and DATA T L apply the DATA BUS to the adders. MD9 L enables the shift left logic, and the asserted signal (LEFT) is applied to the Adder Output Multiplexer. AC and LINK are loaded during TP3.

7006 – Rotate Twice Left – The content of the AC is placed on the DATA BUS. DATA F and DATA T L apply the DATA BUS to the adders. MD9 L asserts the shift left logic signal and MD10 L asserts the TWICE signal; this moves the outputs of the adders two places to the left. The outputs at the output multiplexers are then loaded into the AC Registers and LINK at TP3.

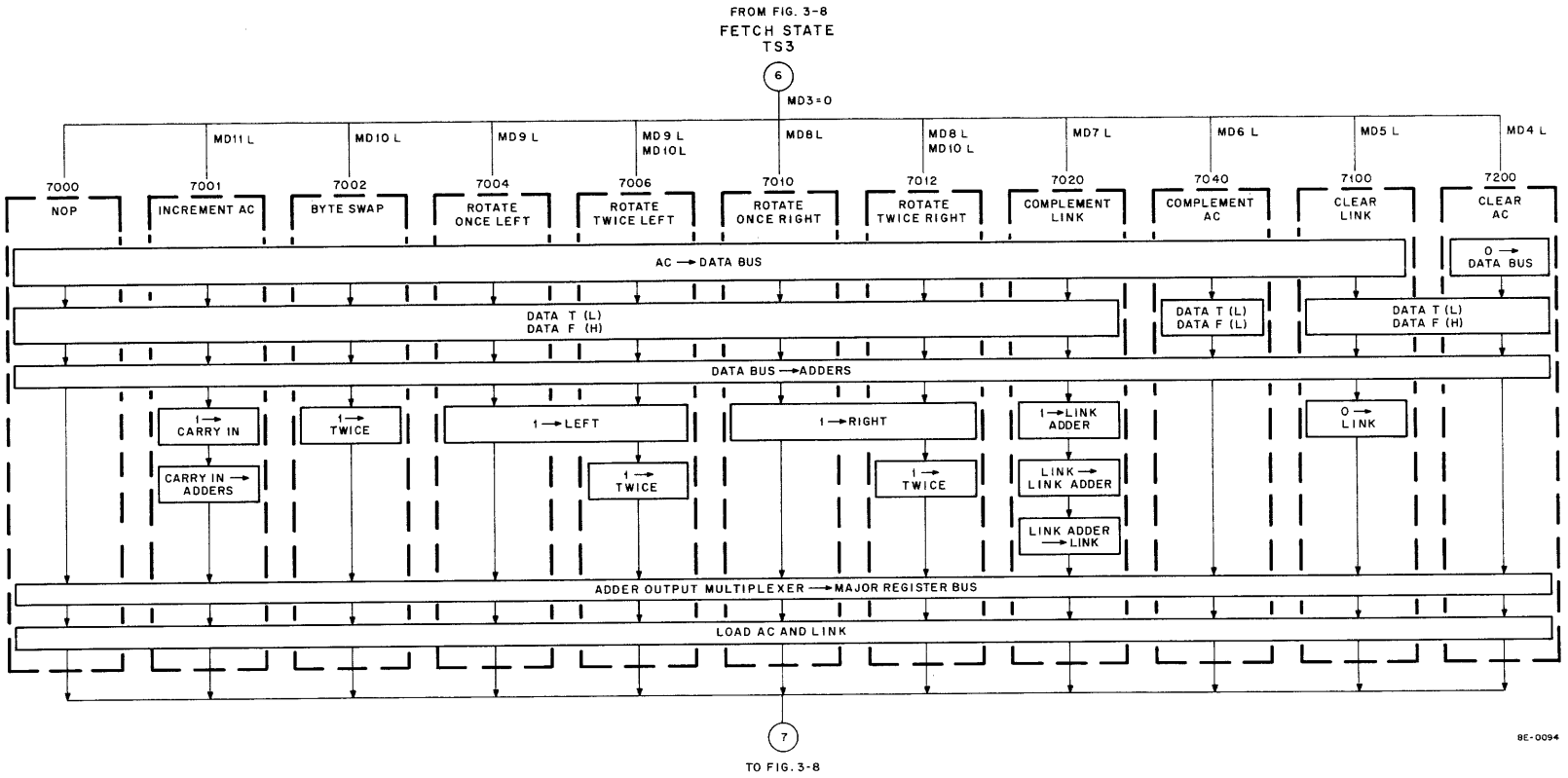


Figure 3-9 GROUP 1 Operate Microinstructions (1 Cycle)

7010 – Rotate Once Right – The content of the AC is placed on the DATA BUS. DATA F and DATA T L apply the DATA BUS to the adders. MD8 L develops signal RIGHT L of the shift right logic. Signal RIGHT L is applied to the output multiplexer circuit, which shifts the contents of the output multiplexers one place to the right. The outputs are then loaded into the AC Registers and LINK at TP3.

7012 – Rotate Twice Right – The content of the AC is placed on the DATA BUS. DATA F and DATA T L apply the DATA BUS to the adders. MD8 L develops signal RIGHT L and MD10 L develops TWICE L. When these two signals are applied to the Adder Output Multiplexer, the contents of the adders are shifted two places to the right. The result is loaded into the AC and LINK at TP3.

7020 – Complement LINK – MD7 L forces a 1 into the LINK circuit. The result will force a 1 to a 0 or a 0 to a 1.

7040 – Complement AC Register – The signal AC → DATA BUS L is first generated; DATA T L and DATA F are asserted so that if 1 is on the DATA BUS, a 0 is placed into the adder or if a 0 is on the DATA BUS, a 1 is placed into the adder. The AC Register is loaded at TP3.

7100 – Clear LINK – A 0 is forced into the LINK circuit when MD5 L = 1, during OPR 1.

7200 – Clear AC – DATA T L is low, DATA F is high. MD4 L disqualifies AC → BUS Logic. This causes 0s to be gated onto the DATA BUS. The contents of the DATA BUS are gated through the Data Control gate and applied to the adders and loaded into the AC Register at TP3 time.

3.9.2.3 Combining Group 1 Microinstructions – Because each instruction takes one memory cycle, it may be desirable to combine many of the instructions so that two instructions can be implemented in one memory cycle. For example, instruction 7001 can be combined with instruction 7040 to give 7041. This combines flow 7001 with flow 7040. The resulting instruction will now complement and increment the AC Register. If a 1 is to be placed into the LINK, instructions 7100 and 7020 can be combined to give 7120. The combined instruction list for commonly used Group 1 operate instructions is as follows:

7041	CIA	Complement and increment AC
7120	STL	Set LINK to a logical 1
7204	GLK	Get LINK and place content into AC bit 11
7300	CLA CLL	Clear AC and LINK
7240	CLA CMA	Set AC = - 1
7201	CLA IAC	Set AC = 1
7110	CLL RAR	Shift positive 1 right
7104	CLL RAL	Shift positive 1 left
7106	CLL RTL	Clear LINK, rotate 2 left
7112	CLL RTR	Clear LINK, rotate 2 right

3.9.3 Group 2 Operate Microinstructions Flow Diagram

Group 2 operate microinstructions are established when MD3 L (1) and MD11 (L) 0 are decoded. Ten basic instructions are provided in Group 2 (Figure 3-10).

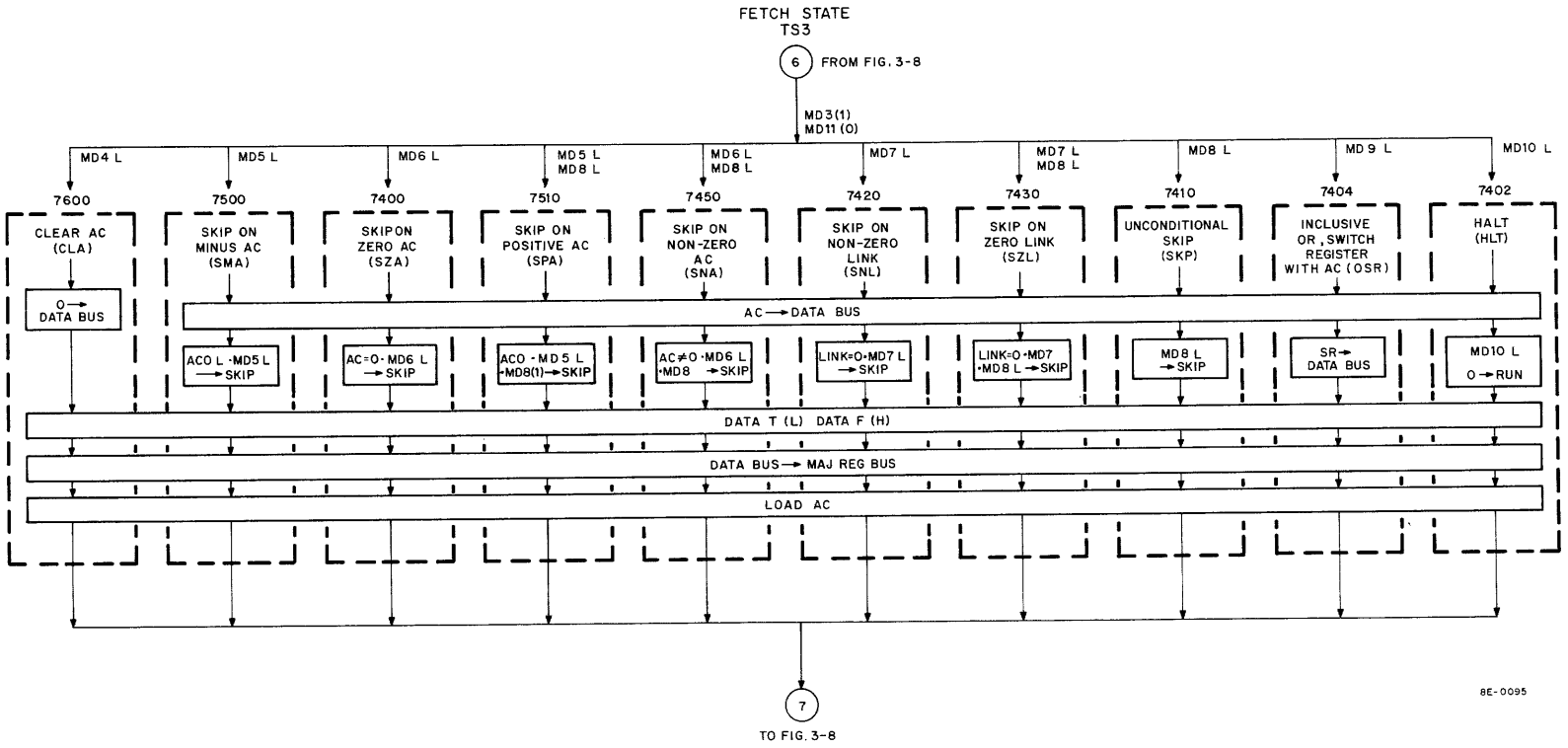


Figure 3-10 GROUP 2 Operate Microinstructions (1 Cycle)

3.9.3.1 Data Path – The data path for all Group 2 instructions is illustrated in Figure 3-2. The common gating and control signals are listed below:

Data Path	Control Signal	Source
AC to DATA BUS (the exception is 7600)	AC → BUS L	Paragraph 3.35.2
DATA BUS to Adders	DATA T DATA F	Paragraph 3.35.3
Adders to Adder Output Multiplexer	None	
Adder Output Multiplexer to MAJOR REGISTERS BUS	None	
MAJOR REGISTERS BUS to AC Register	AC LOAD L	Paragraph 3.37.2

3.9.3.2 Basic Group 2 Instructions

7600 – Clear AC (CLA) – Signal AC → BUS L is not asserted causing a 0 to be gated into the adder circuits. At TP3 time, 0s are loaded into the AC.

7500 – Skip on Minus AC (SMA) – The skip logic tests AC0 for a 1 when MD5 L = 1, indicating that the AC contains a negative 2's complement number. A 1 is then placed in the SKIP flip-flop. During TS4, the content of the PC is incremented by 1 so that the next sequential instruction is skipped.

7440 – Skip on Zero AC (SZA) – The skip logic tests the accumulator for all 0s when MD6 L is asserted with MD8 L (0). If AC = 0, the SKIP flip-flop is set.

7510 – Skip on Positive AC (SPA) – The skip logic tests AC0 for a 0 when MD5 L (1) and MD8 L (1) are asserted. If AC0 = 0, the SKIP flip-flop is set.

7450 – Skip on Non-Zero AC (SNA) – The skip logic tests the contents of the AC Register for all 0s. If one or more AC bits equal 0, a Skip signal is developed when MD6 L and MD8 L are asserted.

7420 – Skip on Non-Zero LINK (SNL) – The skip logic tests the LINK for 1. If LINK = 1, MD7 L = 1, and MD8 L = 0, the SKIP flip-flop will be set.

7430 – Skip on Zero LINK (SZL) – The skip logic tests the link for a 0. When LINK = 0, MD7 L = 1 and MD8 L = 1, the SKIP flip-flop is set.

7410 – Unconditional Skip (SKP) – When MD5 L – MD7 L = 0 and MD8 L = 1, the skip logic sets the SKIP flip-flop.

7404 – Inclusive OR – Switch Register with AC – (OSR) – The contents of the AC Register are transferred to the DATA BUS with signal AC →BUS L asserted. The content of the Switch Register is gated to the DATA BUS when MD9 L = 1 during a Group 2 operate instruction. Signals DATA F and DATA T L gate the ORed content of the DATA BUS through the adders and Output Multiplexers to the input of the AC Register. The AC is loaded during TP3 time. The Link circuit is not affected.

7402 – HALT (HLT) – MD10 L is used to generate a signal (STOP L) that clears the RUN flip-flop, located on the timing generator module. At the next TS1, the processor stops.

3.9.3.3 Combining Group 2 Microinstructions – Combinations of the 10 instructions are listed below:

7604	LAS	Clear AC, and load AC with Switch Register
7640	SZA CLA	Skip if AC = 0, then clear AC
7460	SZA SNL	Skip if AC = 0, or LINK is 1, or both
7650	SNA CLA	Skip if AC $\neq$ 0, then clear AC
7700	SMA CLA	Skip if AC is $<$ 0, then clear AC
7540	SMA SZA	Skip if AC $\leq$ 0
7520	SMA SNL	Skip if AC $<$ 0 or LINK = 1, or both
7530	SPA SZL	Skip if AC $\geq$ 0, and if LINK is 0
7550	SPA SNA	Skip if AC $>$ 0
7710	SPA CLA	Skip if AC $\geq$ 0, then clear AC
7470	SNA SZL	Skip if AC $\neq$ 0, and LINK = 0

NOTE

If Skip instructions are combined and MD8 L = 1, the Skip occurs only if all conditions are simultaneously met. (SPA, SNA, SZL are ANDed.)

If Skip instructions are combined and MD8 L = 0, the Skip occurs if any condition is met. (SMA, SZA, SNL are ORed.)

3.9.4 Group 3 Operate Microinstructions

Group 3 operate microinstructions are established when MD3 L (1) and MD11 L (1) are decoded. Eight Group 3 operate microinstructions are illustrated in Figure 3-11. Six instructions involve operations between the AC and MQ Registers.

3.9.4.1 Data Paths – The data path for all Group 3 operate instructions is illustrated in Figure 3-2. The common gating and control signals are listed below:

Data Path	Control Signal	Source
MQ to DATA BUS	MQ → BUS L	Paragraph 3.35.2
AC to DATA BUS	AC → BUS L	Paragraph 3.35.2
AC to MQ	AC → MQ EN L MQ LOAD L	Paragraph 3.40
DATA BUS to Adders	DATA T L DATA F	Paragraph 3.35.3
Adder Output Multiplexer to MAJOR REGISTERS BUS	None	
MAJOR REGISTERS BUS to AC Register	AC LOAD L	Paragraph 3.37.2
MQ MUX to MQ Register	MQ LOAD L	Paragraph 3.40

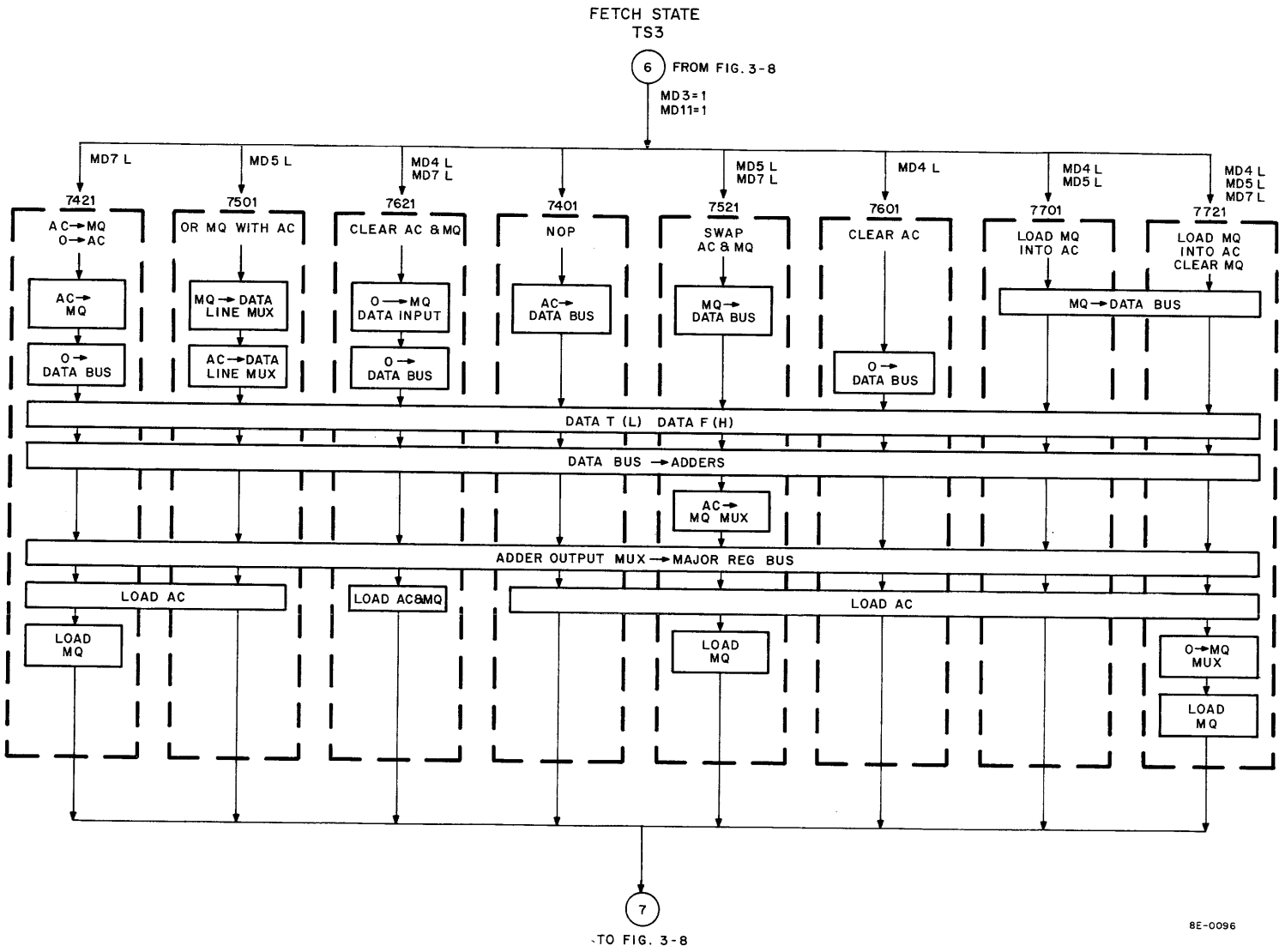


Figure 3-11 Group 3 Operate Microinstructions (1 Cycle)

3.9.4.2 Basic Group 3 Instructions

7421 – Load MQ from AC and Clear AC Register – The content of the AC Register is gated to the data inputs of the MQ Register by the MQ MUX. MQ is loaded by TP3, MD3 L – MD7 L, and MD11 L to clear the AC Register. AC → BUS L is not asserted; this places 0s on the DATA BUS. The 0s follow the data path through the Data Control Gate, through the adders, and are loaded into the AC Register at TP3.

7501 – OR MQ with AC – The contents of the MQ and AC Registers are transferred to the MAJOR REGISTERS BUS during TS3. ORing is accomplished in the Data Line MUX on a bit-by-bit basis. The result is applied to the adder and subsequently applied to the data input of the AC Register. At TP3, the AC Register is loaded.

7621 – Clear AC and MQ – Signal AC → BUS L is not asserted so that only 0s are applied to the adder circuits. AC → MQ EN L is high (MD4 L = 1), disabling the MQ MUX and, thus, placing 0s at the input to the MQ. The AC and MQ are both loaded at TP3.

7401 – NOP – No instructions are executed during NOP. The AC Register is loaded at TP3. The AC is on the DATA BUS and DATA T L is grounded.

7521 – SWAP AC and MQ – The outputs of the AC and MQ Registers take separate paths to accomplish a swap. The MQ Register output is allowed to go through the adders as a result of the MQ → BUS L control signal. The output of the AC Register is applied to the MQ MUX and gated into the MQ Register at TP3. The AC Register is also loaded at TP3.

7601 – Clear AC Register – Signal AC → BUS L is not asserted. Thus, 0s are passed through the adders and applied to the data inputs of the AC Register. At TP3 time, the AC Register is loaded.

7701 – Load MQ Register into AC Register – The contents of the MQ Register are brought into the Data Bus MUX and gated onto the Data Control Gate by MQ → BUS L enabling signal. Data enabling signals DATA T L and DATA F gate the data out to the adders and to the MAJOR REGISTERS DATA BUS. This places the data at the data input of the AC Registers. During TP3, the data is loaded into the AC Register.

7721 – Load MQ into AC and Clear MQ – The contents of the MQ Register are gated through the Data LINE MUX (Paragraph 3.34) to the Data Bus by signal MQ → BUS L. DATA T and DATA F, gate the contents to the adders and, hence, to the data input of the AC Registers. AC → MQ EN L is high, placing 0s at the input to the MQ Registers. The AC and MQ are loaded at TP3.

3.9.5 I/O Transfer Flow Diagram

The I/O transfer flow diagram is presented in Figure 3-12. There are seven sets of conditions to cause I/O transfers and six types of data transfers:

a. Data may be received from a device, ORed with the AC, and the result placed into the AC.
b. Data may be received from a device to be added to contents of the PC.
c. Data may be received from a device to replace the contents of the PC.
d. Data may be sent to a device, and the AC Register cleared.
e. Data may be received from a device and loaded into the AC.
f. Data may be sent to a device.

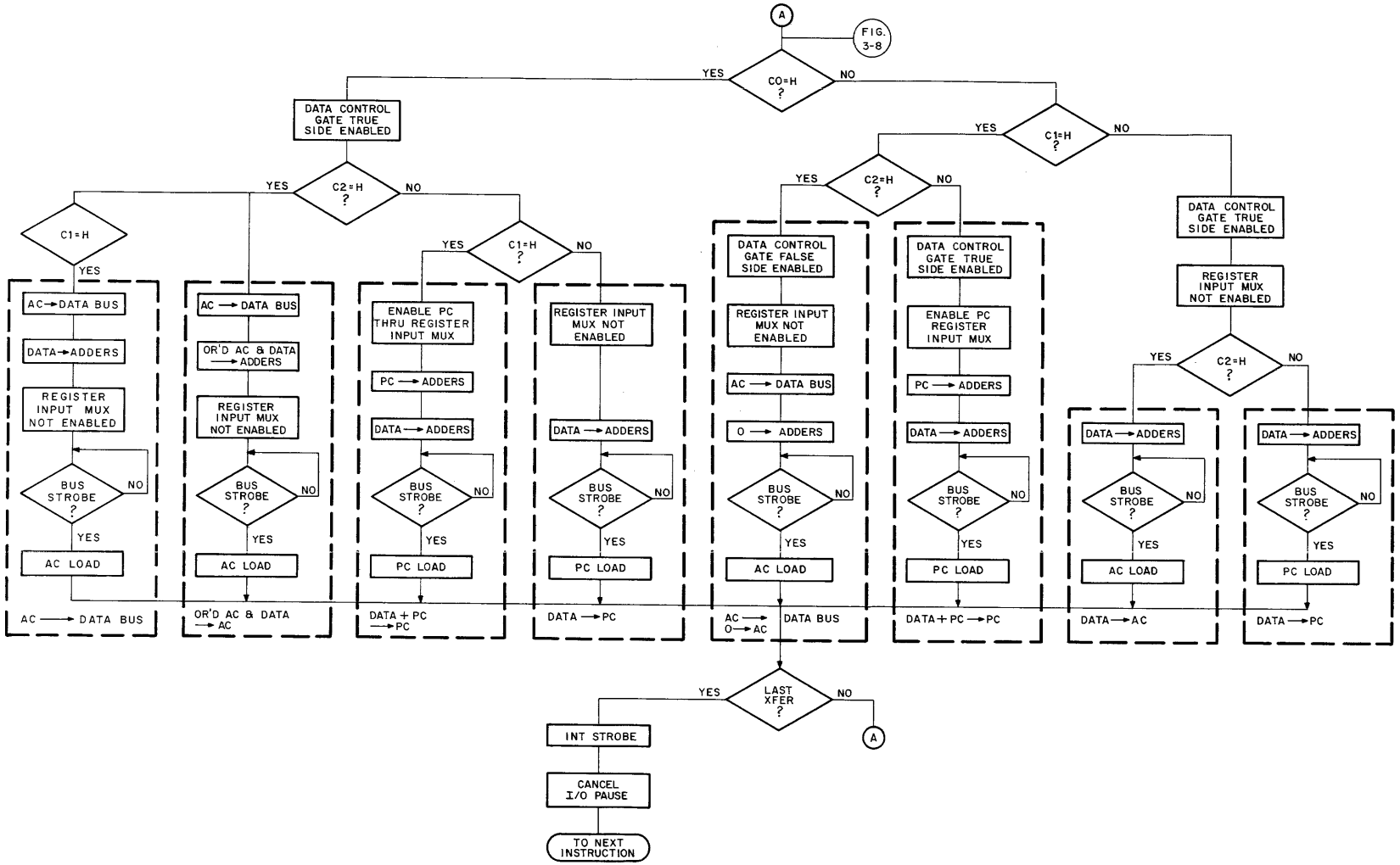


Figure 3-12 I/O Transfer Flow Diagram

The primary control signals for I/O transfer, C0 L, C1 L, C2 L, are generated by the device control logic. These signals are used to indirectly control the Register Input Multiplexer and the data control gate (Figure 3-2) through development of enabling signals EN0 L, EN1 L, EN2 L, for the Input Multiplexer and DATA T L/DATA F signals for the data control gate.

Any device control logic that is connected to the positive I/O bus interface module or requires longer than 1.2 μs provides an additional control signal called NOT LAST TRANSFER L. When this signal is asserted, the timing of the processor stops during TS3 and does not start again until the NOT LAST TRANSFER L signal is no longer asserted and BUS STROBE L is generated. At this time, INT STROBE is asserted, and I/O PAUSE L is negated. If the I/O is high-speed and internal (not involving the positive I/O bus interface), both I/O PAUSE L and INTERNAL I/O L are negated.

3.9.6 Programmed Interrupt System Flow Diagrams

The programmed interrupt system flow diagram is illustrated in Figure 3-13. The basic interrupt system includes:

a. If interrupted, complete instruction and JMS to location 0.

b. Store return address and turn off interrupt.

The interrupt service program handles the determining of the interrupting device, clearing of the flag causing the interrupt, and restoring of the processor to its original condition.

The flow diagram (Figure 3-13) assumes that the interrupt system was turned on during the restoration housekeeping routine.

Flow Reference	Explanation
(1)	CHECK INTERRUPT REQUEST LINE – During the next processor cycle, after the interrupt system was turned on (with instruction ION), the INT DELAY flip-flop is set at TP1 (Paragraph 3.42). This is a necessary condition to set the INT SYNC flip-flop. Because any instruction begins during FETCH and may take several cycles before completion, the last instruction cycle asserts F SET L. At this time, the Interrupt Request line may be tested. If there is no Interrupt Request, the processor returns to the beginning of the FETCH state for the next instruction. Otherwise, it will begin servicing the interrupt.
(2)	With the Interrupt Request line asserted, and the INT DELAY flip-flop set, the INT SYNC flip-flop is set. This asserts the INT IN PROG line which, in turn, forces a JMS into the IR and asserts F E SET. Thus, on the next processor cycle, the EXECUTE major state will be active to store the return address. Because the Register Input Multiplexer (Figure 3-2) is not enabled to allow the PC to transfer to the CPMA during TS4, 0 will be loaded into the CPMA at TP4.
(3)	TURN OFF INTERRUPT SYSTEM – During the EXECUTE major state, the Interrupt System is turned off by clearing the interrupt enable (INT EN) flip-flop, which clears the INT DELAY and INT SYNC flip-flops, negating INT IN PROG.

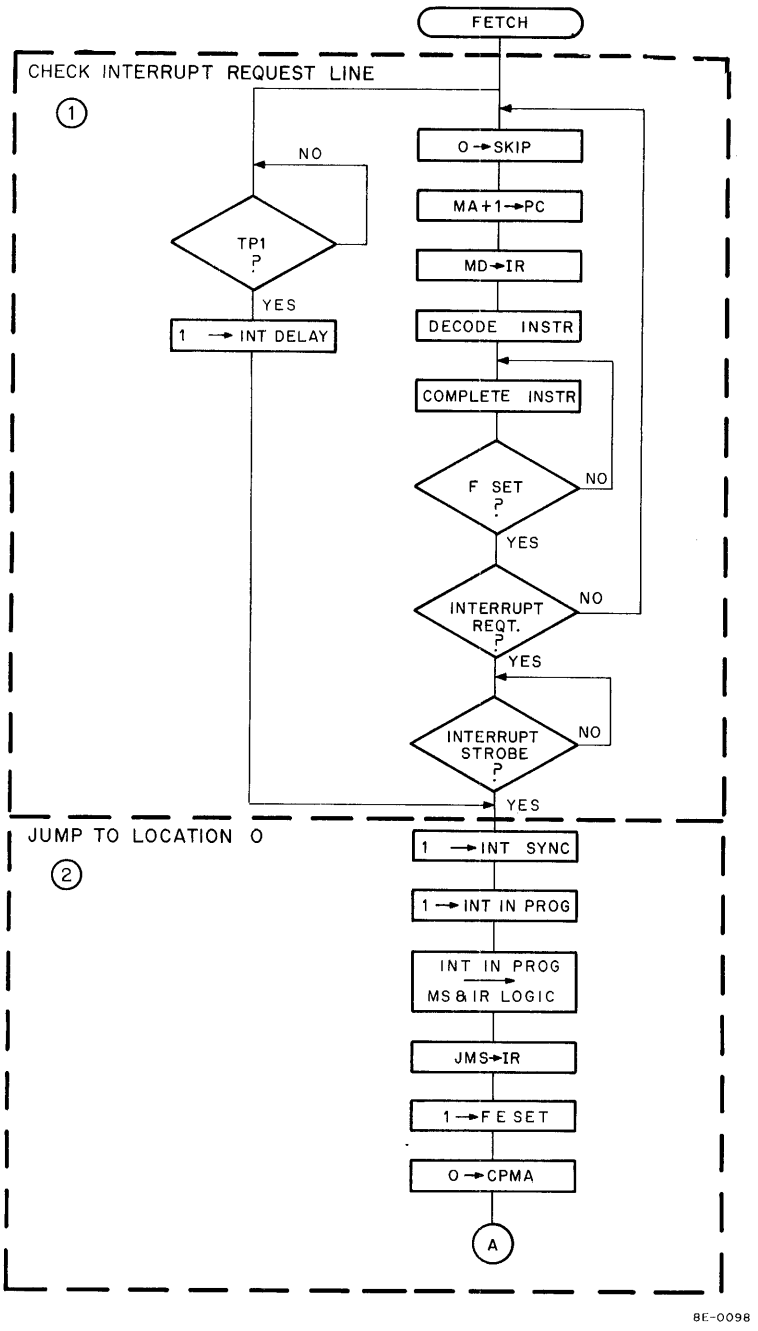


Figure 3-13 Programmed Interrupt System Flow Diagram (Sheet 1 of 2)

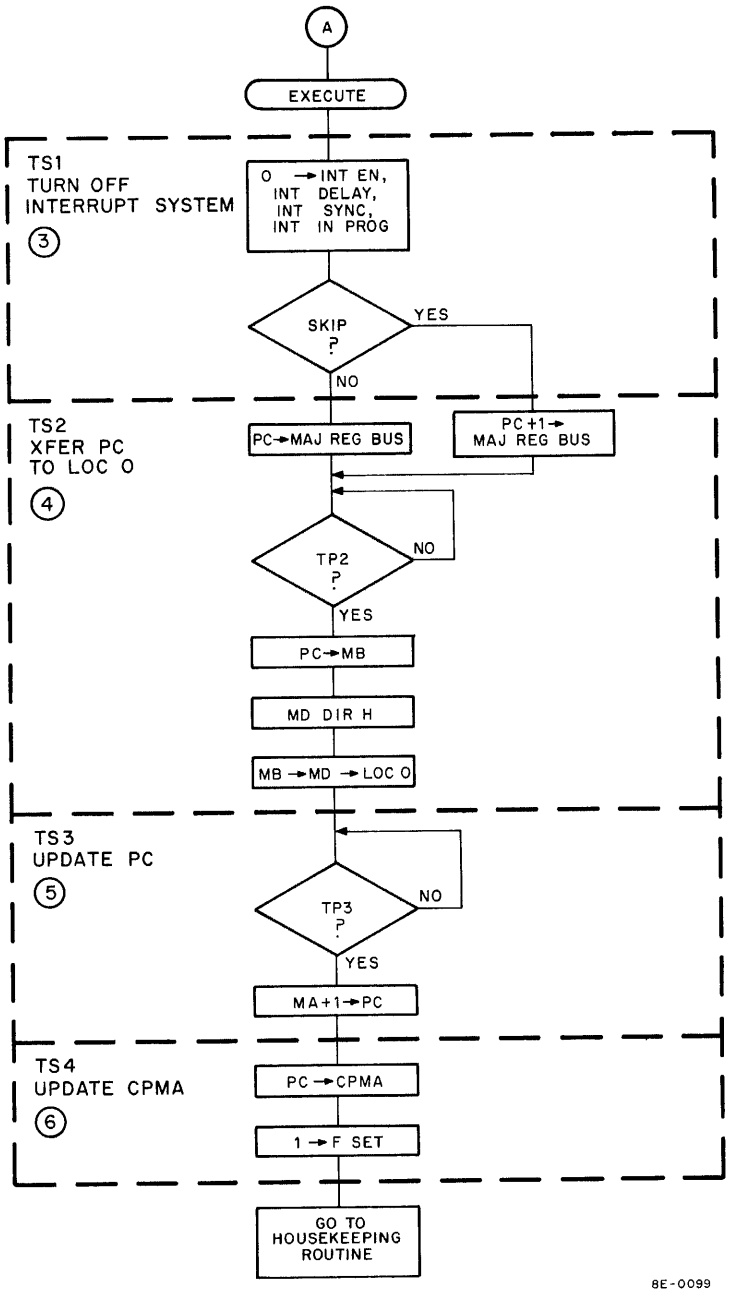


Figure 3-13 Programmed Interrupt System Flow Diagram (Sheet 2 of 2)

Flow Reference	Explanation
(4)	TRANSFER PC TO LOCATION 0 – The contents of the PC are transferred to location 0 during TS2. The Register Input Multiplexer is enabled to allow the contents of the PC to be applied to the MAJOR REGISTERS BUS (Figure 3-2). If the SKIP flip-flop is set, CAR IN is also asserted. At TP2, the content of the MAJOR REGISTERS BUS is loaded into the MB Register. Because MD DIR L is negated (H) at TP2, the content of the MB is immediately applied to the MD BUS, gated into the inhibit drivers, and routed to the addressed memory location (location 0).
(5)	UPDATE PC – During TS3, the content of the CPMA is gated through the Register Input Multiplexer and applied to the adders (Figure 3-2). A CAR IN L signal is developed that places a 1 on adder stage 11. The result is applied to the MAJOR REGISTERS BUS and loaded into the PC at TP3.
(6)	UPDATE CPMA – During TS4, the Register Input Multiplexer is enabled to allow the content of the PC to be applied to the MAJOR REGISTERS BUS and loaded into the CPMA at TP4. Because INT IN PROG is not active, F SET L will be asserted and the next processor cycle will be FETCH. In the event that any important data is in the AC and LINK, a housekeeping routine to store this data must be enacted.

3.9.6.1 Check Interrupt Request Line (SRQ) Instruction Flow Diagram – Refer to Figure 3-14 for the following discussion:

Flow Reference	Explanation
(1)	During TS1, the SKIP flip-flop is cleared. The content of the CPMA Register is gated through the Register Input Multiplexer (Figure 3-2) and placed on the adders. A 1 is developed by the Carry In logic and placed on the adder stage 11. The MA + 1 result is then loaded into the PC Register at TP1. The flow diagram assumes that the current addressed memory location contains instruction (6003) SRQ. READ memory begins during the latter portion of TS1.
(2)	During the second half of TS1 and the first half of TS2, the READ operation is active, and the content of the addressed memory location is read into the memory register (Figure 3-2). Because MD DIR L was asserted during TS1, the content of the memory register will be gated out to the MD BUS and ready for decoding. The Instruction Register looks at the first three bits (0–2) and decodes the IOT. I/O PAUSE L is generated earlier. I/O PAUSE L allows the IOT Decoder to decode the last three bits, providing the middle six bits are 0s. Because the last three bits contain 3_8 (for an SRQ instruction), the Interrupt Request line is now ready to be tested during TS3.
(3)	If an Interrupt Request has been made, signal SKIP L is asserted.
(4)	When SKIP L is asserted, CAR IN L is developed, and a 1 is placed on adder stage 11. The Register Input Multiplexer (Figure 3-2) is enabled so that the content of the PC is placed on the adders. The content of the PC + 1 is applied to the MAJOR REGISTERS BUS and loaded into the CPMA during TS4. If SKIP L was not asserted, only the PC is loaded into the CPMA, and the processor goes on to the next sequential instruction. Otherwise, a Flag Check subroutine is next performed.

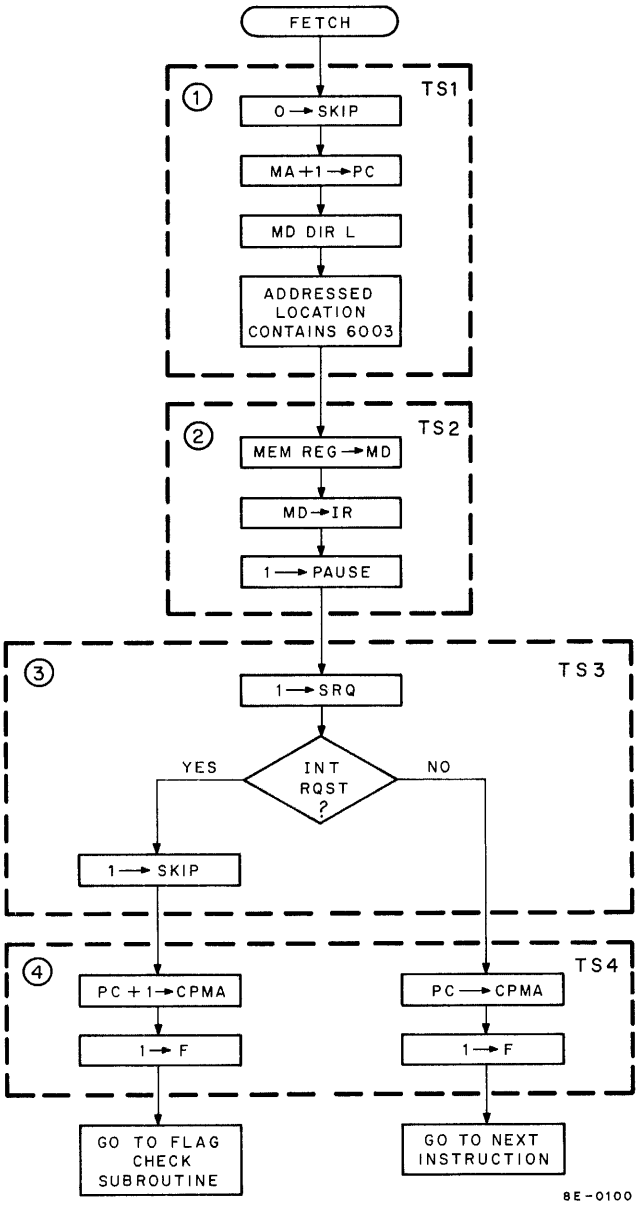


Figure 3-14 Check Interrupt Request Line Instruction Flow Diagram

3.9.6.2 Turn On Interrupt (ION) System – The Interrupt System is turned on during the restoration housekeeping routine (Figure 3-13). Refer to Figure 3-15 for the following discussion:

Flow Reference	Explanation
(1)	The SKIP flip-flop is cleared during TS1, and a 1 is added to the content of the CPMA and loaded into the PC.
(2)	With MD DIR L, the content of the addressed memory location is placed on the MD BUS during the READ operation. The instruction is applied to both the Instruction Register and the IOT Decoder.
(3)	The resulting ION instruction sets the INT EN flip-flop at TP3.
(4)	At TS4, the CPMA Register is updated and F SET L is enabled.

NOTE

During the cycle following TP1, INT DELAY is set; this ensures that the processor cannot honor an interrupt until the end of the next instruction.

3.9.7 JUMP Instruction

The JUMP instruction first modifies the PC and then modifies the CPMA so that both contain the new address at the start of the next instruction. A test is also made to determine if the instruction is direct addressed (the next processor cycle is FETCH), or if the instruction is indirectly addressed (the next processor cycle is DEFER). If the instruction is direct addressed, the content of the addressed memory location will be an instruction. If the address is indirect, the content of the addressed memory location will contain the address of the next instruction.

The JUMP instruction flow diagram is illustrated in Figure 3-16. This flow diagram is a subflow of Figure 3-8 and contains only the TS3 portion of the JUMP instruction.

If MD4 L = 1, PAGE Z L is not asserted (indicating that the new address will be on the current page). The first five CPMA output lines are routed through the Adder Output Multiplexer to the MAJOR REGISTERS BUS. Thus, the first five MA bits are gated through to the MAJOR REGISTERS BUS.

If MD4 L = 0, PAGE Z L is asserted; the first five MA bits are negated and cause 0s to be placed on the MAJOR REGISTERS BUS.

Because MD5 L – MD11 L output lines are routed directly to the Adder Output Multiplexer, these seven bits are applied to the MAJOR REGISTERS BUS. The content of the MAJOR REGISTERS BUS is then loaded into the PC at TP3, and a test for direct or indirect addressing is next accomplished. (Note that if JMP is indirect, the PC is loaded twice, once during FETCH, and the second time during DEFER. The first address is ignored.) The modification of the CPMA is accomplished in a similar manner (Figure 3-8).

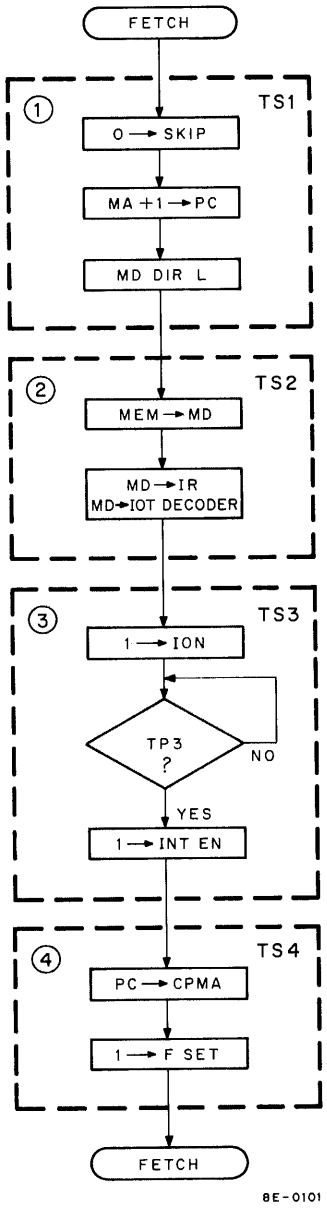


Figure 3-15 Turn On Interrupt (ION) System Flow Diagram

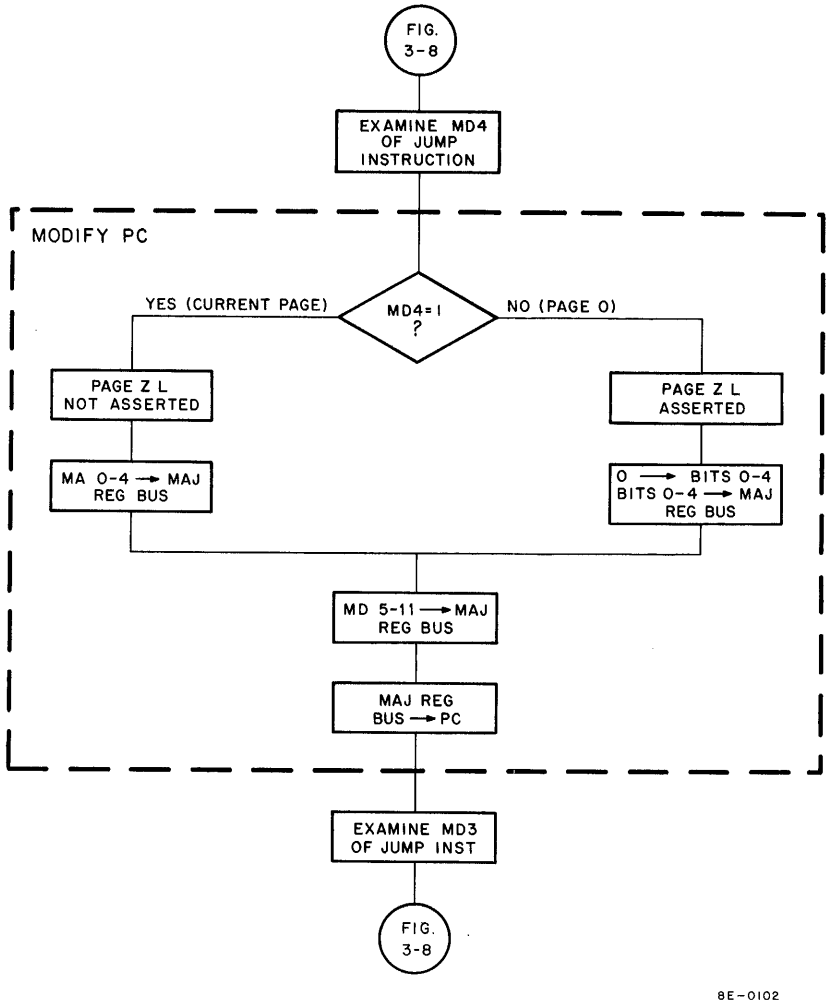


Figure 3-16 Direct JUMP Instruction Flow Diagram

3.10 DEFER STATE INSTRUCTION FLOW DIAGRAM

The DEFER state instruction flow diagram is illustrated in Figure 3-17. DEFER performs two types of functions. During any one processor cycle, DEFER provides an indirect address to the location containing the operand; if the addressed location is between 10_8 and 17_8, it provides the autoindex operation.

Flow Reference	Explanation
(1)	The DEFER state is always entered from the FETCH state, on indirect addressing. During the last half of TS1 and the first half of TS2, the content of the addressed memory location is read from memory and placed in the Memory Register (Figure 3-2). Because MD DIR L is asserted at this time, the content of the Memory Register is gated out to the MD BUS.
(2)	The content of the MD BUS is gated through the Register Input Multiplexer to the adders (Figure 3-2) using Register Input Enable Logic. At the same time, the Carry In logic places a 1 in the adders. The result is then placed on the MAJOR REGISTERS BUS and, at TP2, is loaded into the MB Register.

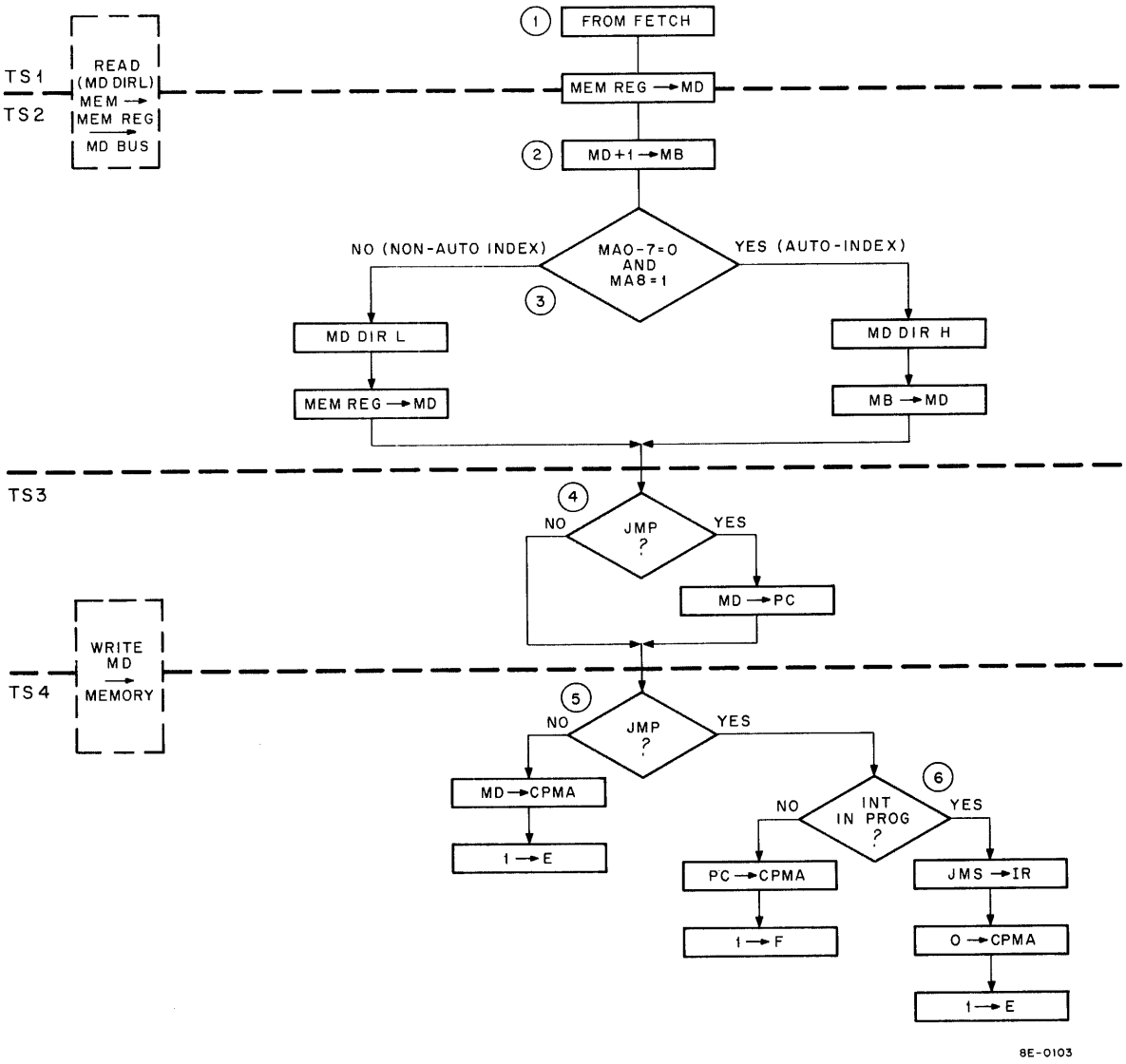


Figure 3-17 DEFER State Instruction Flow Diagram

Flow Reference	Explanation
(3)	The autoindex operation is determined by examining the content of the first nine Memory Address bits. If bits 0–7 contain 0s and bit 8 contains a 1, MD DIR L is allowed to go high and the content of the MB Register (which contains MD + 1) is gated onto the MD BUS. Otherwise, MD DIR L remains low and the content of the Memory Register is gated onto the MD BUS.
(4)	If the JMP instruction is in the IR, the content of the MD is gated through the Register Input Multiplexer, through the adders, onto the MAJOR REGISTERS BUS, and loaded into the PC at TP3. Remember the MD BUS carries either the previous memory contents (if the instruction is not autoindexed), or the incremented memory contents (if the instruction is autoindexed). If JUMP is not in the IR, then no action is taken during TS3, and JUMP is tested again in TS4.
(5)	If the JMP instruction is in the IR, the processor goes on to test the INT IN PROG line. Otherwise, the content of the MD BUS is again gated through the Register Input Multiplexer, through the adders, and onto the MAJOR REGISTERS BUS. At TP4, the CPMA is loaded containing the new address of the operand. The combination of DEFER and JMP does not necessarily cause the next processor state to be EXECUTE.
(6)	If the IR contains JMP, the INT IN PROG line is tested. If no interrupt has occurred, the content of the PC is gated through the Register Input Multiplexer, through the adders to the MAJOR REGISTERS BUS. At TP4, the CPMA is loaded. Because the current major state is DEFER and the instruction is JMP, the next major state must be FETCH. If there is an INT IN PROG, a JMS is forced into the Instruction Register, all 0s are forced into the CPMA, and the next major state is EXECUTE.

3.11 EXECUTE STATE INSTRUCTION FLOW DIAGRAM

The EXECUTE state instruction flow diagram is shown in Figure 3-18. EXECUTE can be entered from FETCH, DEFER, or EXECUTE. During the second half of TS1 and the first half of TS2, the READ operation is performed. MD DIR L is also asserted to allow the content of the addressed memory location to be gated out to the MD BUS (Figure 3-2).

Flow Reference	Explanation
(1)	The operation of the AND and TAD instructions is the same during TS2. The MD gate of the Register Input Multiplexer is enabled and the content of the MD BUS is placed on the MAJOR REGISTERS BUS. At TP2, MB LOAD L is developed and loads the content of the MAJOR REGISTERS BUS into the MB Register. Also at TP2, MD DIR L is allowed to go high and the content of the MB is automatically placed on the MD BUS. Although this operation does not change any register or bus during an AND or TAD instruction, it is automatic for both instructions during the EXECUTE state.

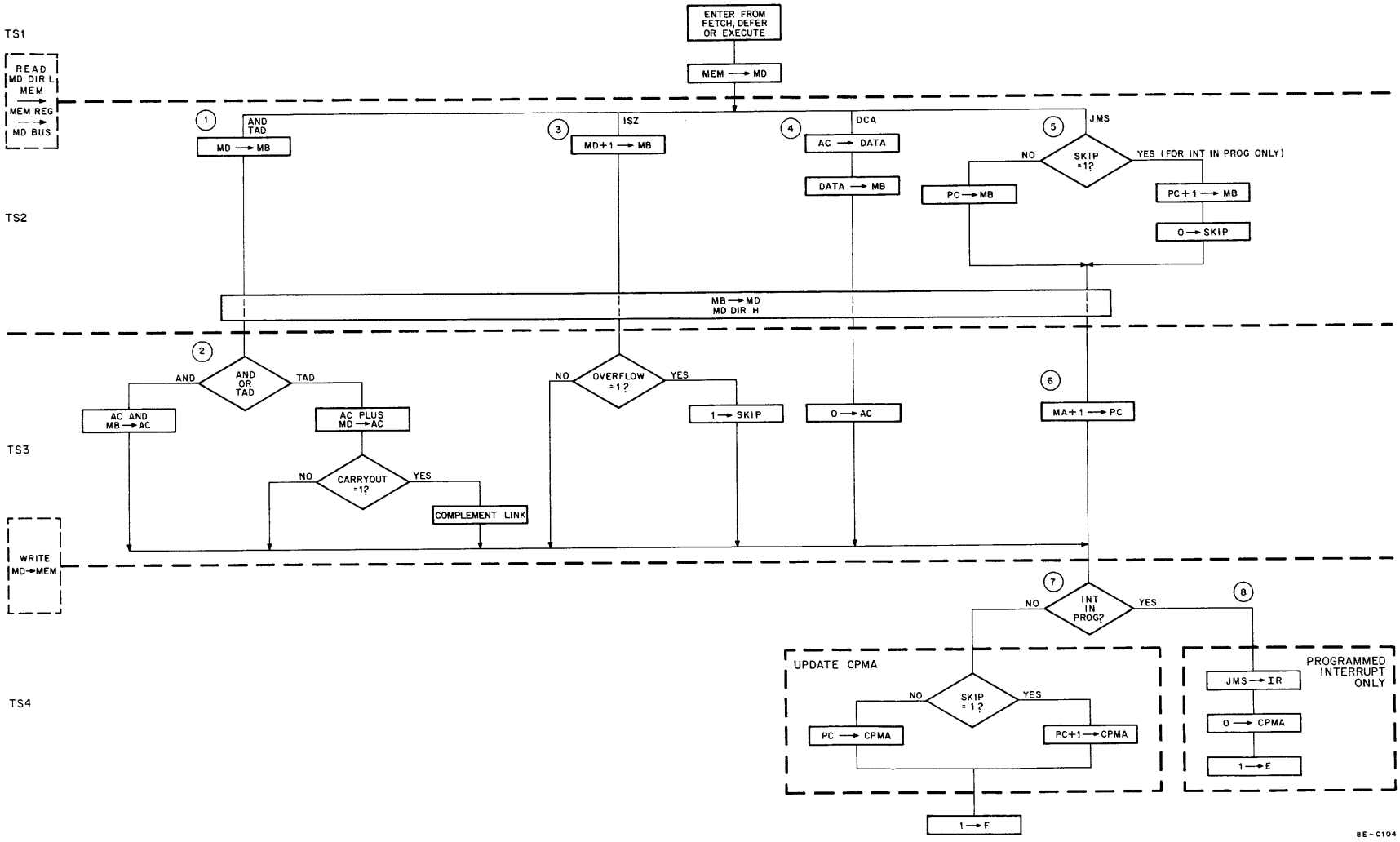


Figure 3-18 EXECUTE State Instruction Flow Diagram

Flow Reference	Explanation
(2)	If the instruction is AND, the AC/MB AND gate (Figure 3-2) receives the content of the AC and the MB. A logical AND function will be performed for each of the 12 bits; there is no carry from one stage to the next. The ANDed result is then applied to the Adder Output Multiplexer and placed on the MAJOR REGISTERS BUS. At TP3, the content of the MAJOR REGISTERS BUS is loaded into the AC. For a TAD instruction, the process differs. The Register Input Multiplexer is enabled to allow the content of the MD BUS to be applied to the adders. To bring the AC to the adders, enabling signal AC → BUS L is first developed. This places the content of the AC on the DATA BUS. To apply the content of the DATA BUS to the other side of the adders, the Data Control Gate (DATA T L) is enabled. The resulting addition is then applied to the MAJOR REGISTERS BUS and loaded into the AC at TP3. If CAR OUT L equals a 1, the result is applied to the Link Adder circuit, and the LINK is complemented.
(3)	If ISZ is in the Instruction Register, CAR IN L is asserted, which places a 1 in the adders at TS2. At the same time, the Register Input Multiplexer is enabled to allow the contents of the MD BUS to be placed onto the adders. If the OVERFLOW flip-flop is not set at TP2, no operation is performed during TS3. If the OVERFLOW flip-flop is set to 1, a 1 is developed on the SKIP line. (See Flow Reference (7) for CPMA Update.)
(4)	If instruction DCA is in the Instruction Register, signal AC → BUS L is developed, and the content of the AC Register is applied to the DATA BUS (Figure 3-2). The Data Control Gate is enabled next; thus, the content of the DATA BUS can be applied to the MAJOR REGISTERS BUS. At TP2, the content of the MAJOR REGISTERS BUS is then loaded into the MB Register and because MD DIR L goes high at TP2, the content of the MB Register is gated onto the MD BUS. To clear the AC, signal AC → BUS L is not asserted, and DATA T L is high. With DATA T L high, 0s are applied to the MAJOR REGISTERS BUS and loaded into the AC Register at TP3. The contents of the MD BUS are then applied to the inhibit drivers for the WRITE operation. WRITE begins during the second half of TS3 and continues through the first half of TS4.
(5)	If a JMS instruction is in the Instruction Register, the Register Input Multiplexer is enabled to allow the content to the PC to be applied through the adders to the MAJOR REGISTERS BUS and loaded into the MB Register at TP2. The SKIP L signal is also tested during TS2. If the Skip logic has produced a 1, SKIP L signal is applied to the Carry In logic, and signal CAR IN L becomes a 1*. This is applied to the adders and added to the content of the PC. The result is then applied to the MAJOR REGISTERS BUS and loaded into the MB at TP2. At TP2, the SKIP flip-flop is also cleared. (This condition can occur only when an interrupt is honored immediately after an OPR, IOT, or ISZ instruction.)
(6)	A CAR IN L signal is asserted and a 1 is placed in the adders. The content of the CPMA Register is gated through the Register Input Multiplexer to the adders. The result is applied to the MAJOR REGISTERS BUS and loaded into the PC Register at TP3.

*AC signal line is pulled low.

Flow Reference	Explanation
(7)	For all instructions, if there is no INTERRUPT IN PROGRESS, the SKIP L signal line is tested. If SKIP L does not equal 1, no CAR IN L signal is developed and the content of the PC Register is gated through the Register Input Multiplexer and then applied to the MAJOR REGISTERS BUS. At TP4, the content of the BUS is loaded into the CPMA Register. If the SKIP L signal equals 1 (because of ISZ and CARRY OUT), a CAR IN L signal is developed and applied to the adders. This signal is added to the PC and loaded into the CPMA at TP4. In both cases, F SET L is asserted and the next major state is FETCH.
(8)	If there is an INTERRUPT IN PROGRESS, a JMS instruction is forced into the Instruction Register and the Register Input Multiplexer is enabled so that 0s are applied to the MAJOR REGISTERS BUS. During TP4, the content of the BUS is loaded into the CPMA and EXECUTE is clocked into the Major States Register.

SECTION 3 – TIMING GENERATOR

3.12 TIMING GENERATOR, GENERAL DESCRIPTION

The M8330 Timing Generator provides synchronizing signals for memory and processor operations. Eight basic processor timing signals and five basic memory timing signals are generated.

3.13 TIMING GENERATOR, FUNCTIONAL DESCRIPTION

Figure 3-19 shows the functional sections of the PDP-8/E Timing Generator. At the heart of the timing operation is a chain of 4-bit shift registers, designated the Timing Shift Register. A preset combination of logic 1s and 0s is repetitively cycled through the chain. Selected outputs of the Timing Shift Register are used to control flip-flops that produce the basic timing signals. Think of the chain of shift registers as a tapped delay line; in this way the concept of shift register timing might be more easily understood. A control signal is placed on the input of this delay line at time 0. This signal flows along the delay line and is sampled at selected taps, where it is used to set or reset flip-flops. Thus, consecutive timing signals can be produced. When the signal reaches the end of the delay line it can be returned to the beginning to start another timing cycle.

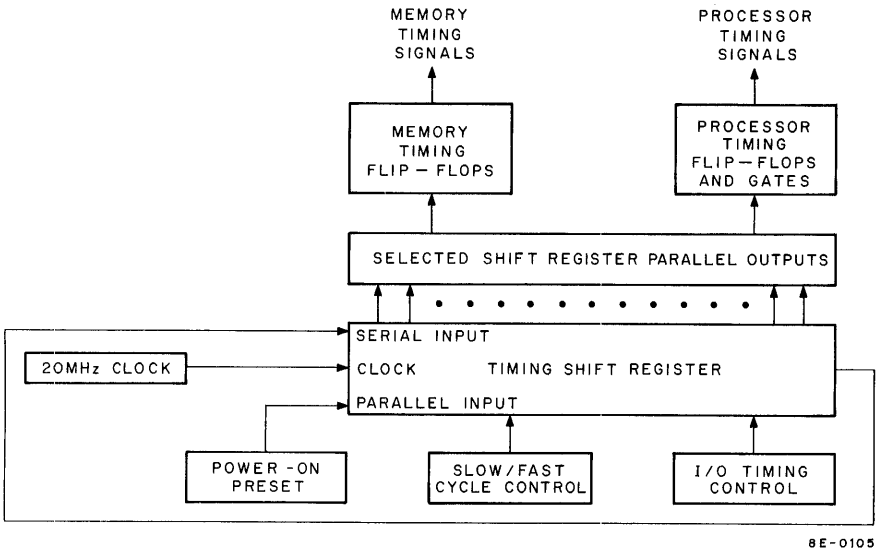


Figure 3-19 Timing Generator, Block Diagram

The delay line concept is easily understood; however, the PDP-8/E features a variable timing cycle. A delay line does not provide the necessary balance between flexibility and simplicity of design, nor does it provide a stable cycle time. Balance and stability are achieved by using a chain of shift registers to produce the timing signals. In its simplest form, the Timing Shift Register is a 28-bit shift register that is right-shifted by clock pulses derived from a 20 MHz, crystal-controlled transistor oscillator.

3.14 BASIC TIMING OPERATION

Figure 3-20 is a simplified representation of the Timing Shift Register; it illustrates the basic timing operation. Assume a method exists for presetting a 0 voltage level in the first stage of this register and also presetting positive voltage levels in every other stage. After this initial condition has been established, the clock is turned on. The first clock pulse shifts the 0 level to stage 2; simultaneously, the positive level from stage 28 is shifted into stage 1. Clock pulse 2 shifts the 0 level into stage 3 and simultaneously shifts a positive level into both stages 1 and 2. Each pulse moves the 0 level to the right by 1 bit, replacing it with a positive level. When the clock shifts the level into stage 5, the flip-flop is cleared by the negative-going edge of the pulse. The flip-flop remains in this reset state until clock pulse 8 shifts the level into stage 9, thereby setting the flip-flop. The signal produced at the 0 side of the flip-flop is a 200 ns gate. Pulses can also be generated, as shown by the AND gate connected to stage 12. When the level is shifted into the stage by clock pulse 11, the gate is enabled and the desired output is produced.

The actual operation is more detailed than the example given, although the basic shifting process remains the same. As the block diagram indicates, the shift register is preset by a circuit that operates the moment power is turned on. Each clock pulse shifts the preset control signal to the right; the register is recycled by connecting the last stage back to the first. In the simplest arrangement, a complete cycle requires 28 clock pulses, or 1.4 μs; this is the "slow" cycle. If a "fast" cycle is called for, the slow/fast cycle control decreases the cycle time by 200 ns. Another control network that modifies the basic shifting operation is shown as I/O timing control on Figure 3-19. This control is used to interrupt the timing cycle while certain I/O transfers are carried out. All of these control circuits are discussed in detail in the following sections.

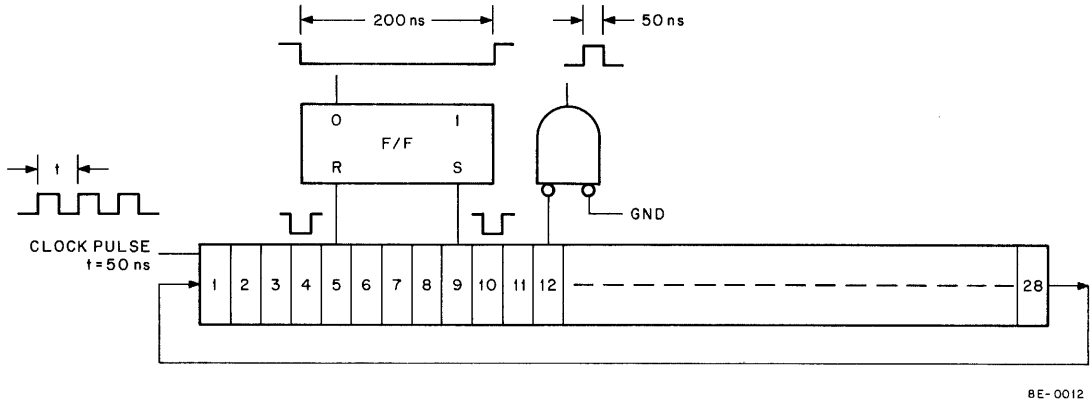


Figure 3-20 Simplified Timing Shift Register Operation

3.15 TIMING SHIFT REGISTER

As previously noted, the shift register is the key to the timing operation. The shift register comprises ten DEC 74194, 4-bit shift registers. A logic representation of the DEC 74194 integrated circuit (IC) is shown in Figure 3-21. The circles at the outputs of each bit (pins 15, 14, 13, and 12), at the corresponding parallel-entry inputs (pins 3, 4, 5, and 6, respectively), and at the serial-in (S) line, indicate that ground level signals represent logic 1s. If the mode (M) input is taken to a positive voltage, the DEC 74194 IC is programmed for parallel loading. Those signals present at the parallel-entry inputs are transferred to the corresponding outputs by a clock pulse at C. Thus, the logic 1 at pin 3 is transferred to output pin 15. The same clock pulse transfers a logic 1 from pin 4 to pin 14 and logic 0s from pins 5 and 6 to pins 13 and 12, respectively.

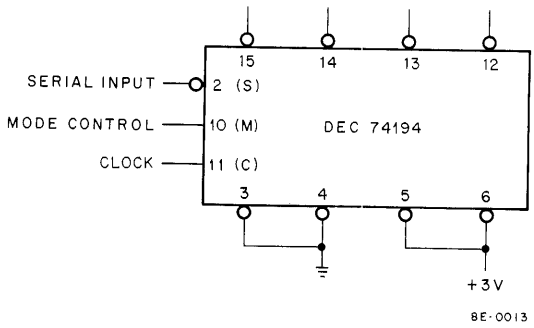


Figure 3-21 DEC 74194 Shift Register Logic

If the M input is taken to ground, rather than to a positive voltage, the DEC 74194 IC is programmed for shifting operation and the parallel-entry inputs are disabled. Information at the S input is shifted to the right one bit each time a clock pulse is applied at C. Thus, a logic 1 at S is shifted to pin 15 by the first clock pulse, to pin 14 by the second, etc. Refer to Appendix A for a detailed discussion of DEC 74194.

Ten shift register ICs are connected to form the Timing Shift Register referred to in Figure 3-19. This arrangement is presented in detail in Figure 3-22. For the moment, all ICs, with the exception of the first, E43, are shown programmed for serial-shift operation; i.e., the M inputs are grounded. Outputs that are used to produce the timing signals are identified according to function. Parallel-entry inputs are shown only on E43.

The discussion of the 28-stage shift register (Figure 3-20) assumed that the register could be preset so that stage 1 contained a 0-voltage level, while all other stages contained positive voltage levels. Essentially, this is accomplished by the power-on preset control. This control operates when the power is first turned on and ensures that, before a timing cycle is initiated, bits 1 and 2 of E43 (represented by output pins 15 and 14, respectively) contain logic 1s, while all other bits of the Timing Shift Register contain logic 0s. The control takes the M input of E43 to a positive voltage and maintains this voltage for a predetermined delay period. Thus, during this time period E43 is programmed for parallel-entry, while the remaining ICs of the register are programmed for serial shifting (the delay period is required to offset the indeterminate state of individual bits at power turn-on; because a bit can assume either a 0 or a 1 level at power-on, the delay period is used to shift out of the register any logic 1s that may be present). The first clock pulse that occurs transfers the logic levels at the parallel-entry inputs of E43 to the outputs. Pins 15 and 14 go to ground (logic 1), and pins 13 and 12 go to +3V (logic 0). The logic 0 at pin 12 is applied to the S input of E38. Thus, the next clock pulse shifts the logic 0 into E38. Each succeeding clock pulse does the same, while also right-shifting the register. During the shifting operation, a signal from the control holds the timing flip-flops in the reset state. This action ensures that the logic 1s being shifted through the register have no affect on the flip-flops. All logic 1s are shifted out of the register in approximately 1.2 μs (25 clock pulses). The register is then in the preset condition.

When the predetermined delay period has ended, E43 must be placed in the right-shift mode by activating a key on the operator's console, thereby asserting the OMNIBUS MEM START L signal. This signal causes the power-on preset control to bring the M input of E43 to ground, programming E43 for shifting operation. Clock pulses at C begin shifting the logic 1s of bits 1 and 2 to the right. A negative pulse moves through the shift register (see Figure 3-23 for a graphic representation of this pulse). The negative-going edge is used to set and reset flip-flops, thereby producing timing gates, while the entire pulse is used to produce timing pulses. Note that 28 clock pulses return the register to the initial condition; thus, a timing cycle of 1.4 μs results (28 clock pulses $\times$ 50 ns per clock pulse).

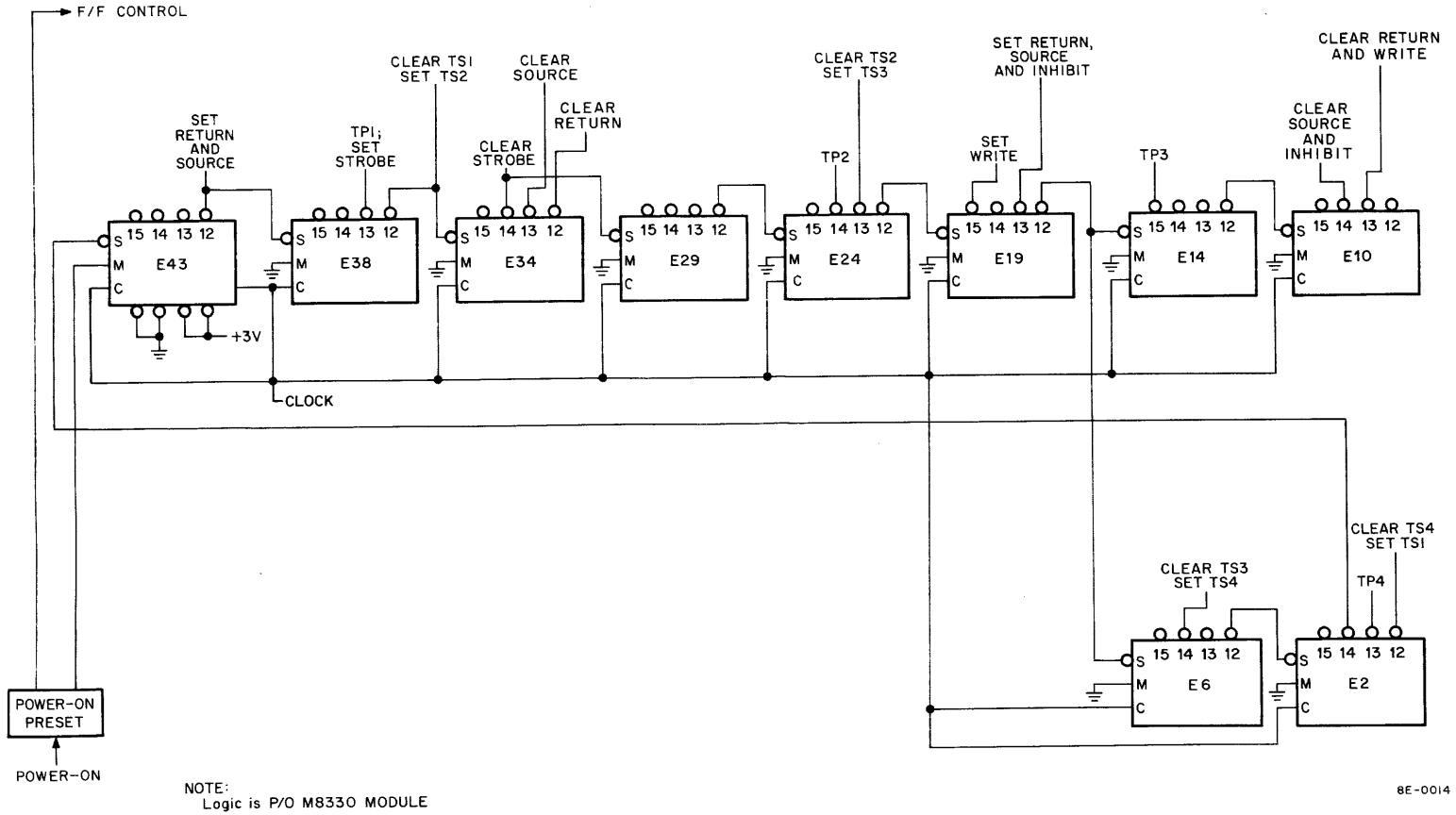


Figure 3-22 Timing Shift Register, Simplified Version

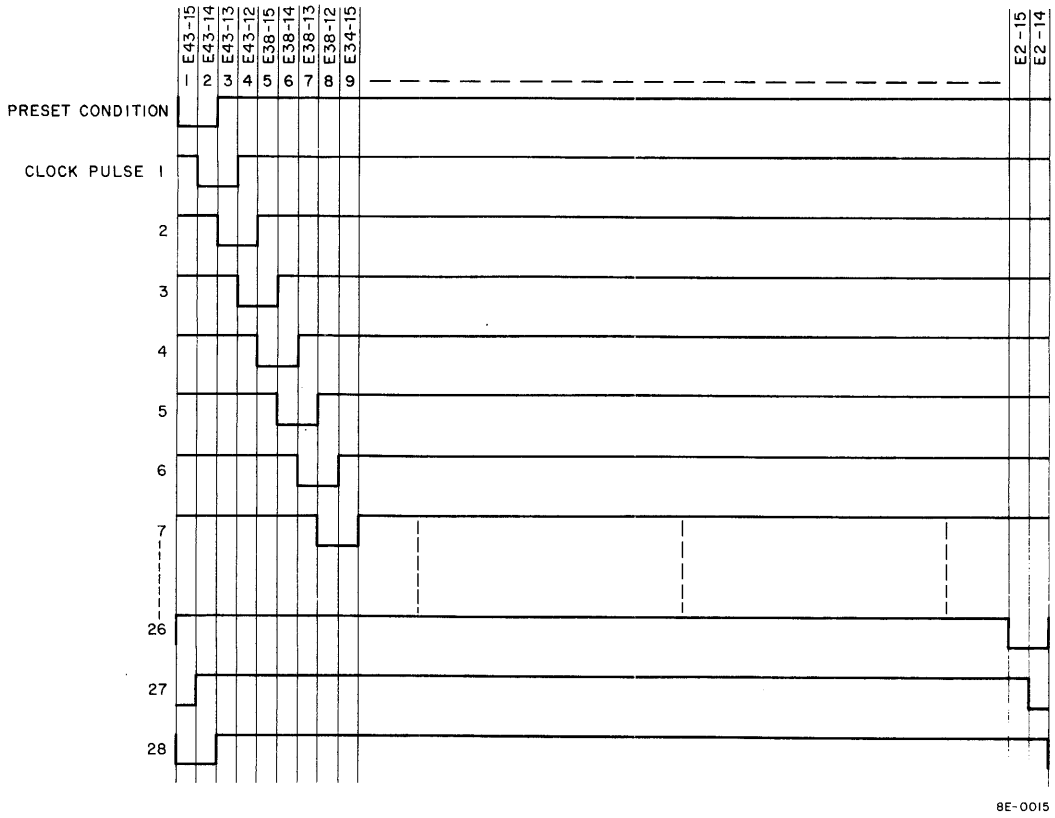


Figure 3-23 Register Composite Logic Signal Timing Diagram

3.16 POWER-ON PRESET CONTROL

The power-on preset control logic is shown in Figure 3-24. Remember that this logic determines the operating mode of IC E43 in the Timing Shift Register. At power-on, the control holds E43 in the parallel-entry mode while all logic 1s are shifted out of the remainder of the register. To carry out this function, the control logic monitors the OMNIBUS POWER OK signal that originates in the power supply (Paragraph 3.47.6).

When power is turned on, POWER OK is negated (grounded). This signal is negated when power supply voltages are below a predetermined level, which is the case at power-on. Power supply voltages do not reach this predetermined level instantaneously at power-on; rather, there is a delay of perhaps hundreds of microseconds before POWER OK is asserted. However, at some time during this delay, the voltages reach a level that is sufficient to start the clock and begin loading and/or shifting the Timing Shift Register. Note that when POWER OK is low, both flip-flop E39B and flip-flop E39A (RUN) are held in the clear state by the asserted POWER PRESET L signal. The 0 output of E39B is high; this signal keeps E43 in the parallel-entry mode. Thus, the conditions for presetting the register are met, viz., E43 is held in the parallel-entry mode, clock pulses shift out the remaining register bits, and the POWER PRESET L signal holds the timing flip-flops in the reset state.

Long after the register has been preset, POWER OK is asserted. After a delay introduced by the delay circuit shown in Figure 3-24, POWER PRESET L is negated (the delay circuit has major significance only at power-off; this is explained shortly). The operator can activate either the DEP, CONT, or EXAM key (Paragraph 3.32.2.1), causing MEM START L to be asserted. This signal sets the RUN flip-flop; the 1 output of the flip-flop causes RUN L to be asserted and provides a high level at the D-input of flip-flop E39B. The next clock pulse sets E39B; the 0-output of the flip-flop places IC E43 in the right-shift mode, and the timing cycle begins.

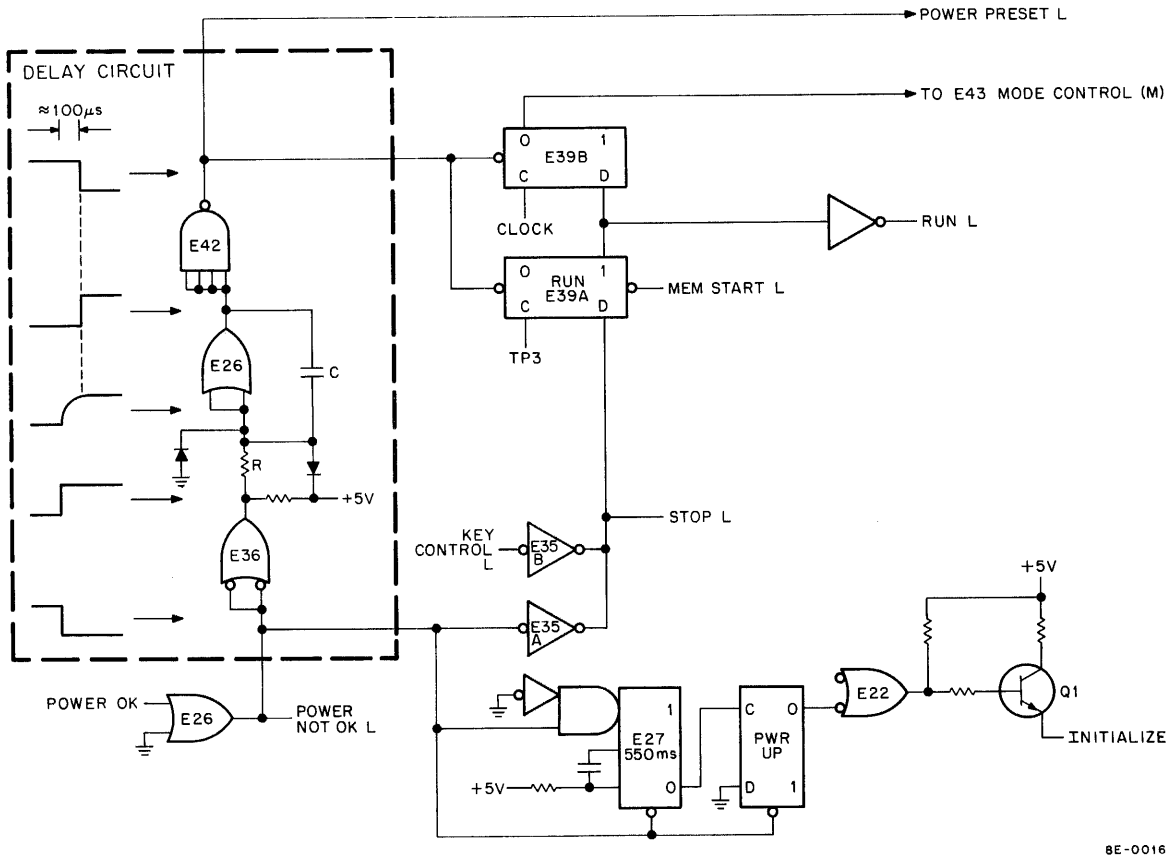


Figure 3-24 Power-On Preset Control Logic

The power-on preset control has an important function at power-off as well. If the operator turns off the power, or a low power supply voltage is detected, POWER OK is negated. To ensure that both processor and memory complete the current timing cycle, the assertion of POWER PRESET L is delayed by approximately 100 μs. This delay is accomplished by the circuit shown within the dashed line; the method is illustrated by the waveforms shown.

When POWER OK is negated, POWER NOT OK L is asserted. The next occurring TP3 pulse resets the RUN flip-flop, thereby negating the RUN L signal and enabling the clock to reset flip-flop E39B. The current timing cycle proceeds to its conclusion and, because IC E43 of the Timing Shift Register is in the parallel-entry mode, the register halts in the preset state. When the POWER PRESET L signal goes low after the delay, it holds E39A, E39B, and the timing flip-flops in the clear state. Timing can be restarted only if the operator activates one of the keys mentioned earlier.

Note that when POWER OK is negated, the STOP L signal is asserted by gate E35A. The STOP L signal can be asserted in a number of other ways as well:

a. A HLT instruction in the program can assert STOP L.

b. The HALT switch or the SING STEP switch on the operator's console can be closed, asserting STOP L.

c. The DEP key, the EXAM key, or the EXTD ADDR LOAD key can be activated, asserting KEY CONTROL L that causes STOP L to be asserted.

That part of the logic in the lower right portion of Figure 3-24 is used to generate the INITIALIZE signal at power-on. At some time before POWER OK goes high, the power supply voltages become sufficiently high for transistor Q1 to conduct, asserting the INITIALIZE signal (note that 1-shot E27 is held in the clear state and the PWR UP flip-flop is held in the set state, both by POWER NOT OK L). When POWER OK goes high, the 1-shot is triggered. 550 ms later, E27 times out; its 0-output clears the PWR UP flip-flop; this causes the INITIALIZE signal to be negated. The long-duration INITIALIZE signal allows all system equipment to complete the operations initiated by the leading edge of the signal.

3.17 SLOW/FAST CONTROL

Figure 3-22 shows only the intermodule connections required for a slow cycle of operation. Other connections, necessary for normal timing operation, are omitted for clarity. The PDP-8/E uses a fast timing cycle (1.2 μs) in normal operation; to produce this fast cycle, five additional connections are necessary (Figure 3-25). The connections are:

a. a connection between E34, pin 14 and E24, pin 3

b. three connections on E24 itself

c. a connection from the slow/fast control to the mode input of E24.

The key to the difference between a fast and slow cycle can be found in IC E24. The mode control signal of E24 is controlled by the 0 side of flip-flop E30. This flip-flop is reset each time either a FETCH state or a non-autoindex DEFER state, both requiring a fast cycle, is entered. Thus, a fast cycle puts E24 in the parallel-entry mode. The outputs of E24 are connected to the parallel-entry inputs; consequently, parallel loading of E24 accomplishes the same result as serial shifting, e.g., four clock pulses shift the signal in E24, pin 15 into E19, pin 15. The difference between fast and slow cycles occurs because of the number of clock pulses needed to shift a signal from E34, pin 14 into E24, pin 15. During a slow cycle, when the parallel-entry inputs of E24 are disabled, five clock pulses shift a signal from E34, pin 14, through E29 and into E24, pin 15. During the fast cycle, however, with the parallel-entry at E24, pin 3 enabled, E29 is bypassed and only one clock pulse is needed to shift the signal from E34, pin 14 into E24, pin 15. TP2 and all subsequent timing signals are generated four clock pulses earlier than during the slow cycle. Therefore, the fast cycle shortens both the memory and processor timing cycles by 200 ns.

NOTE

E30 can be held in the set state by connecting jumper W1 from the "dc set" input to ground. The SLOW CYCLE ONLY feature facilitates troubleshooting by keeping the timing cycle at a constant 1.4 μs.

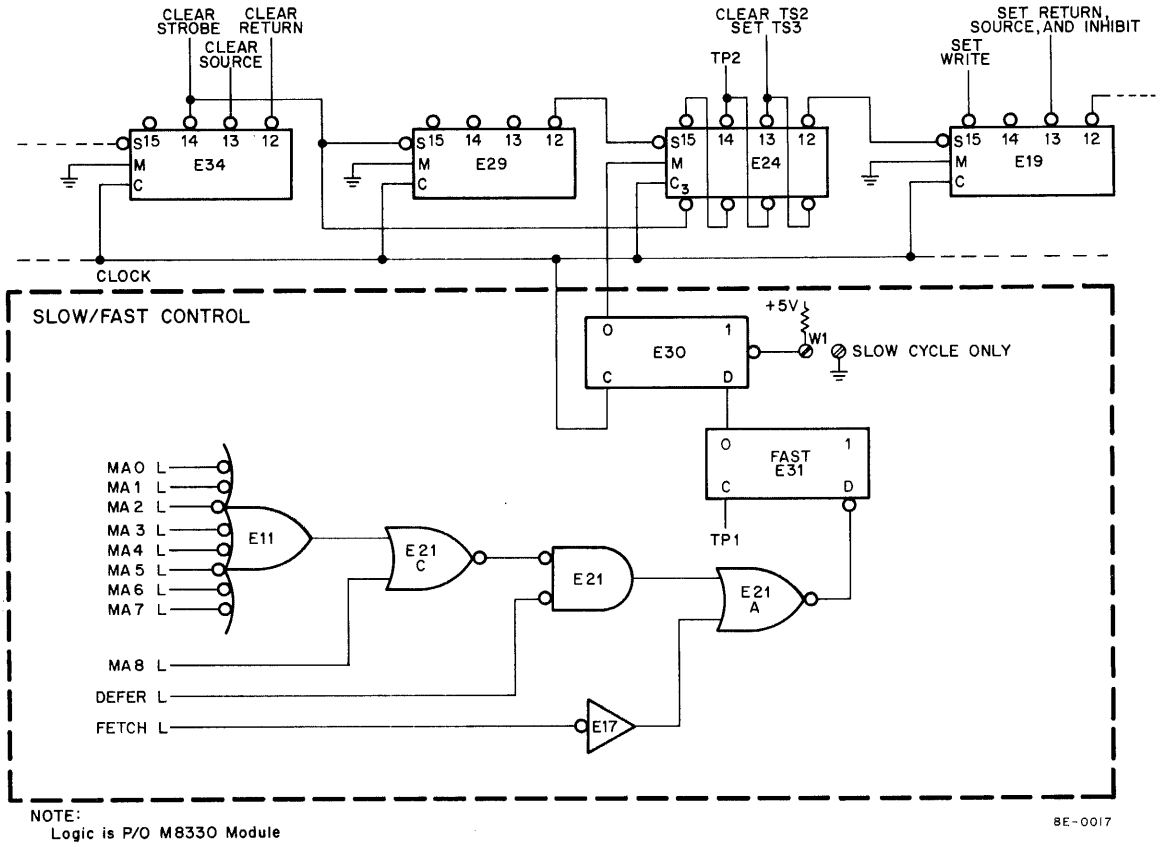


Figure 3-25 Slow/Fast Control Logic

3.18 TIMING DIAGRAM

Timing diagrams of the two cycles of operation are shown in Figure 3-26. The slow cycle is taken as the base and is shown for one timing cycle with TS1 as the initial signal. Processor time states (TS1, etc.) are entered successively, and the timing pulses (TP1, etc.) bracket the trailing edges of their corresponding time state signals.

Note that the time duration of each timing signal, except TS2, remains constant whether the cycle is slow or fast. The 200 ns difference between the slow and fast cycle is accomplished by varying the time duration of TS2 alone and, thus, the amount of time between the read and write portions of a memory cycle is variable. The slow cycle is used when data is read from memory, taken to the processor for modification, and returned to memory. If the data is to be read and then rewritten, as in a FETCH cycle, less cycle time is required; thus, the fast cycle is provided.

3.19 PROCESSOR TIMING

Figure 3-27 shows the logic that provides processor timing signals. Time state signals are provided by four R/S flip-flops; each flip-flop consists of two cross-coupled NOR gates and is controlled by selected pins of the Timing Shift Register. Timing pulse signals are provided by four NOR gates connected to the register. The POWER PRESET L signal from the power-on preset controls the flip-flops at both power-on and power-off (or at some condition of low power supply voltage). The signal clears the TS2, TS3, and TS4 flip-flops and sets the TS1 flip-flop. Thus, the processor is clamped in TS1 if a timing cycle is not in progress.

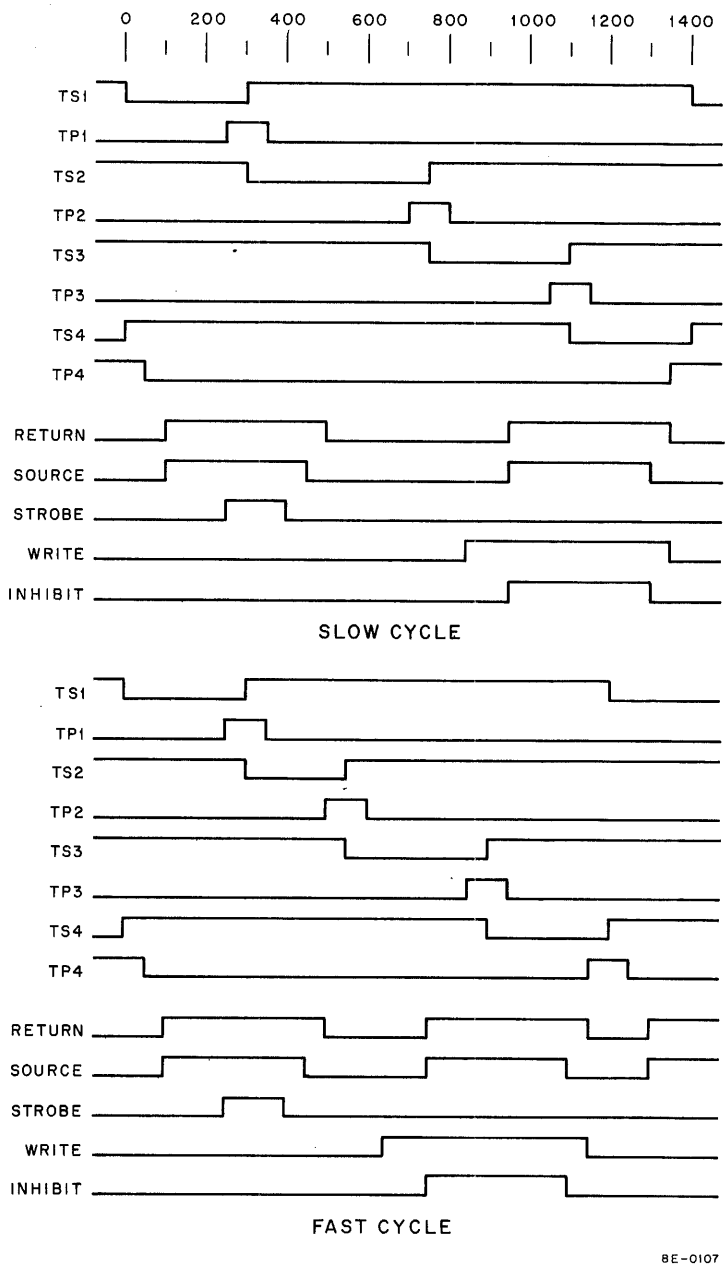


Figure 3-26 Memory and Processor Signals, Timing Diagram

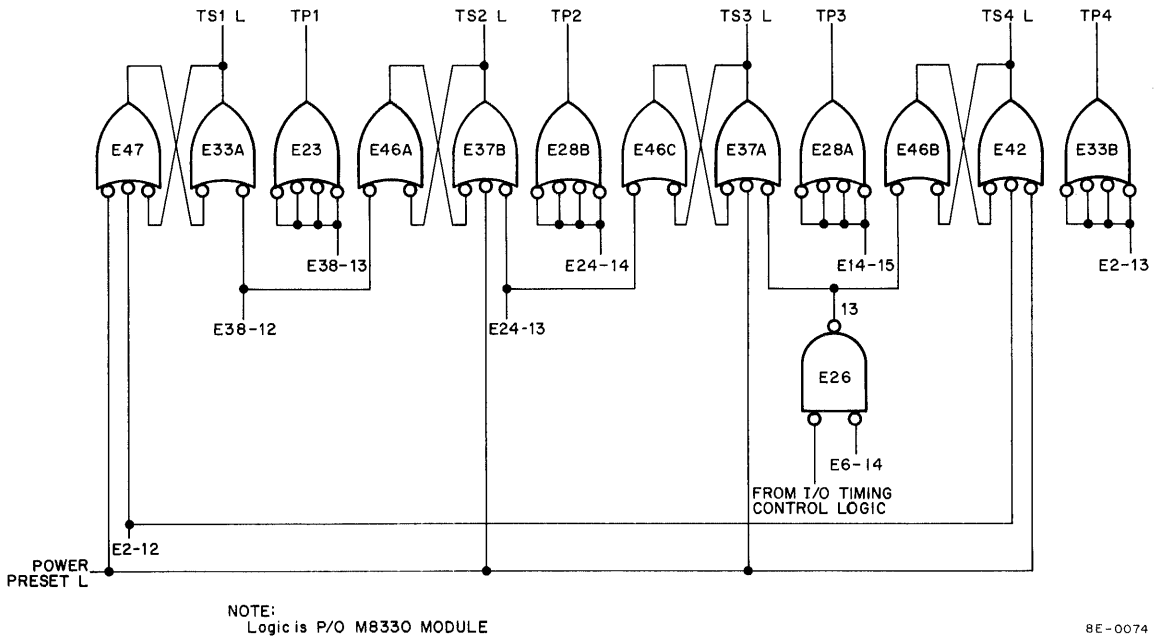


Figure 3-27 Processor Timing Signal Logic

The processor timing signals are used primarily in the CPU, where they generate signals for major register gating and control. Timing pulses have two major functions within the CPU: to sample processor control lines, and to generate "load" signals for the major registers. The time state signals generally provide enabling levels, during which major register outputs are processed.

3.20 MEMORY TIMING

Figure 3-28 shows the logic that provides the memory timing signals. Each signal is generated by an R/S flip-flop of two cross-coupled NOR gates and is controlled by the indicated shift register output pins. The POWER PRESET L signal resets all flip-flops at power-on and power-off.

These timing signals are used in the memory to control the read and write portions of the timing cycle. RETURN and SOURCE are generated during both halves of the cycle, thereby turning on memory current. The conjunction of these two signals determines the width of the current pulse. Note on the timing diagram that return and source are asserted at the same time, but that return is negated 50 ns later than source; this ensures that the memory stack does not remain capacitively charged. STROBE is generated only during the read half of the memory cycle and is used to provide a time reference from which the outputs of the sense amplifiers are sampled. WRITE and INHIBIT are generated only during the write half of the memory cycle. WRITE enables the proper Read/Write switches, thereby providing write currents to the memory stack. INHIBIT is asserted 100 ns later than WRITE and gates the Inhibit Drivers associated with memory control. Details regarding the function of these signals are presented in Section 4, Memory System.

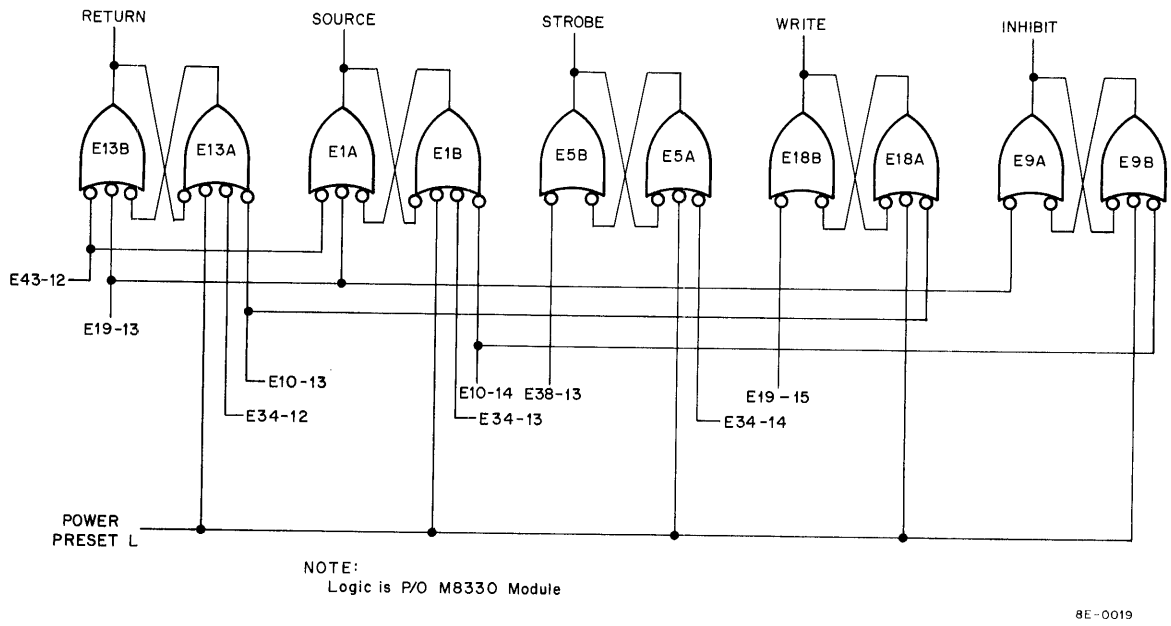


Figure 3-28 Memory Timing Signal Logic

3.21 I/O TIMING CONTROL

The connection between the I/O Timing Control and the mode input of IC E6, omitted from Figure 3-22, is illustrated in Figure 3-29. This control network is used when a peripheral is making more than one I/O transfer during a single IOT instruction and when, because of gating delays, the peripheral needs more time for a transfer than is allowed with normal timing. In either case, the peripheral takes the NOT LAST TRANSFER line to ground, and at the next TP3 time the timing cycle is interrupted and stalled in TS3. The peripheral transfers the information, issuing a BUS STROBE L signal with each transfer. Transfers continue until the peripheral negates the NOT LAST TRANSFER L signal, signifying that the next BUS STROBE L issued by the peripheral is the last of the I/O transfer. This last BUS STROBE L signal restarts the timing cycle, allowing TS3 to end and TS4 to begin.

The last five shift register ICs of the chain are shown in Figure 3-29. Note that all but E6 are programmed for serial shifting. The mode input of E6 is controlled by flip-flop E20B, which is, in turn, controlled by flip-flop E20A. This mode input is normally at a ground level, and the timing signals are generated in the normal way, i.e., the 100 ns negative pulse is shifted from E19 through E14 and E6 to E10 and E2, respectively (Figure 3-23). Note that when E6, pin 14 goes low NAND gate E26 is enabled, provided flip-flop E20A is set; the TS3 L signal is negated, and TS4 is entered.

However, if the peripheral has caused the NOT LAST TRANSFER L signal to be asserted, E20A is cleared at TP3 time, and NAND gate E26 cannot be enabled (the timing diagram in Figure 3-30 visualizes the process). This action prevents both the TS3 L signal from being negated and the TS4 L signal from being asserted. In order to complete the interruption of the timing cycle, the shifting process must be halted. This is done at the next clock pulse time, when flip-flop E20B is cleared. The 0 output of the flip-flop places E6 in the parallel-entry mode. The 100 ns negative pulse is stalled in E6, pins 15 and 14 staying low until the I/O transfer has ended (the state of the parallel-entry inputs of E6 ensures that the state of the outputs remains constant). Note that IC E14 is allowed to continue shifting the negative pulse down the line. This path of the shift register deals with the write half of the memory timing signals. Because I/O transfer data is not transferred directly to memory, the memory timing signals need not be altered in any way.

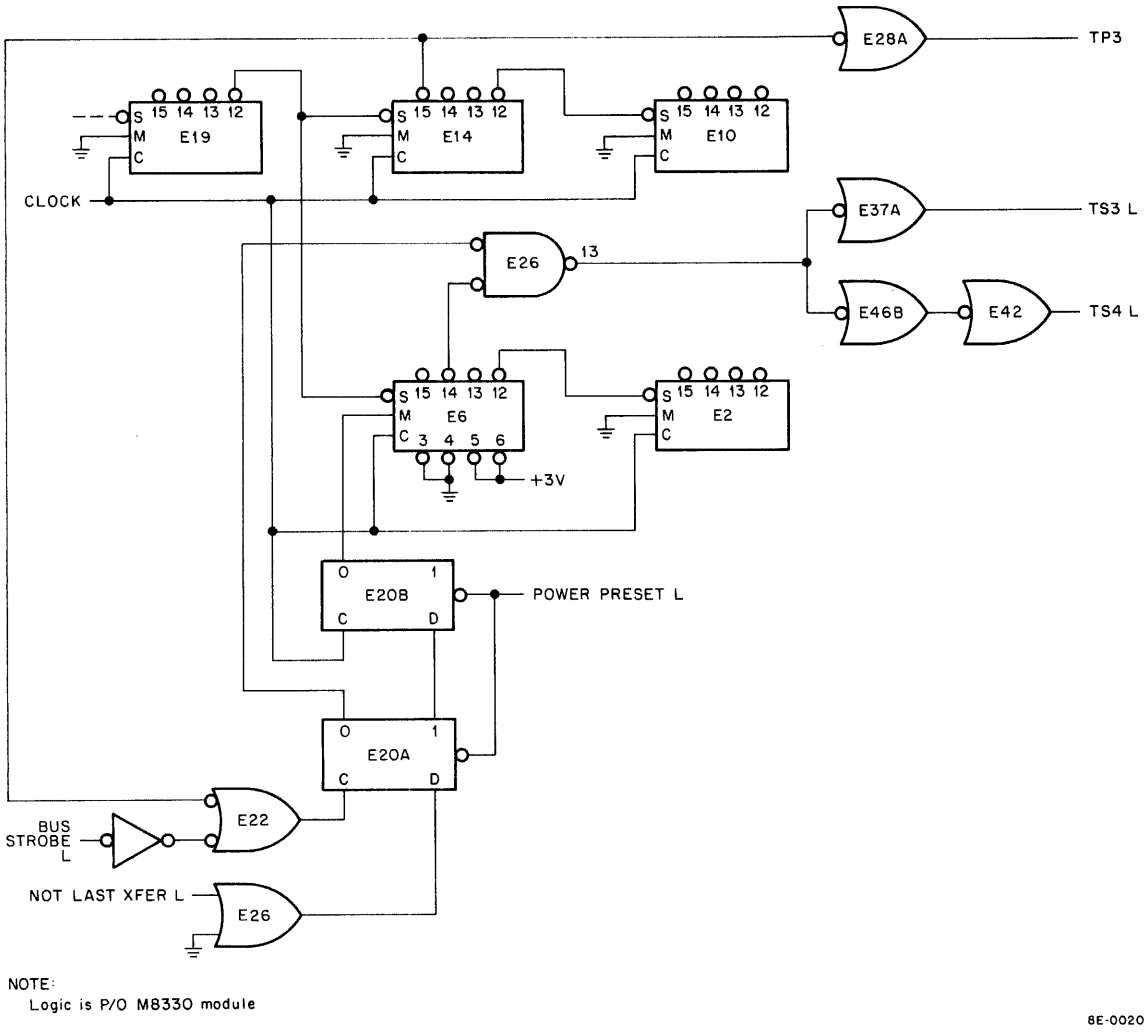


Figure 3-29 I/O Timing Control Logic

When the I/O transfer is complete, the NOT LAST TRANSFER L signal is negated and the peripheral generates a BUS STROBE L signal that sets E20A. NAND gate E26 is enabled, causing the TS3 L signal to be negated and the TS4 L signal to be asserted. The first clock pulse to occur after E20A is set, sets E20B, and E6 is returned to the right-shift mode. The next clock pulse begins shifting the negative pulse through E6 and the timing returns to normal.

Figure 3-30 illustrates an I/O timing interrupt. The cycle time is arbitrarily shown as 1550 ns. Note that the timing, before interruption, is that of a fast cycle. This is always true, because I/O transfers are accomplished while the processor is in the FETCH state, which uses a fast timing cycle.

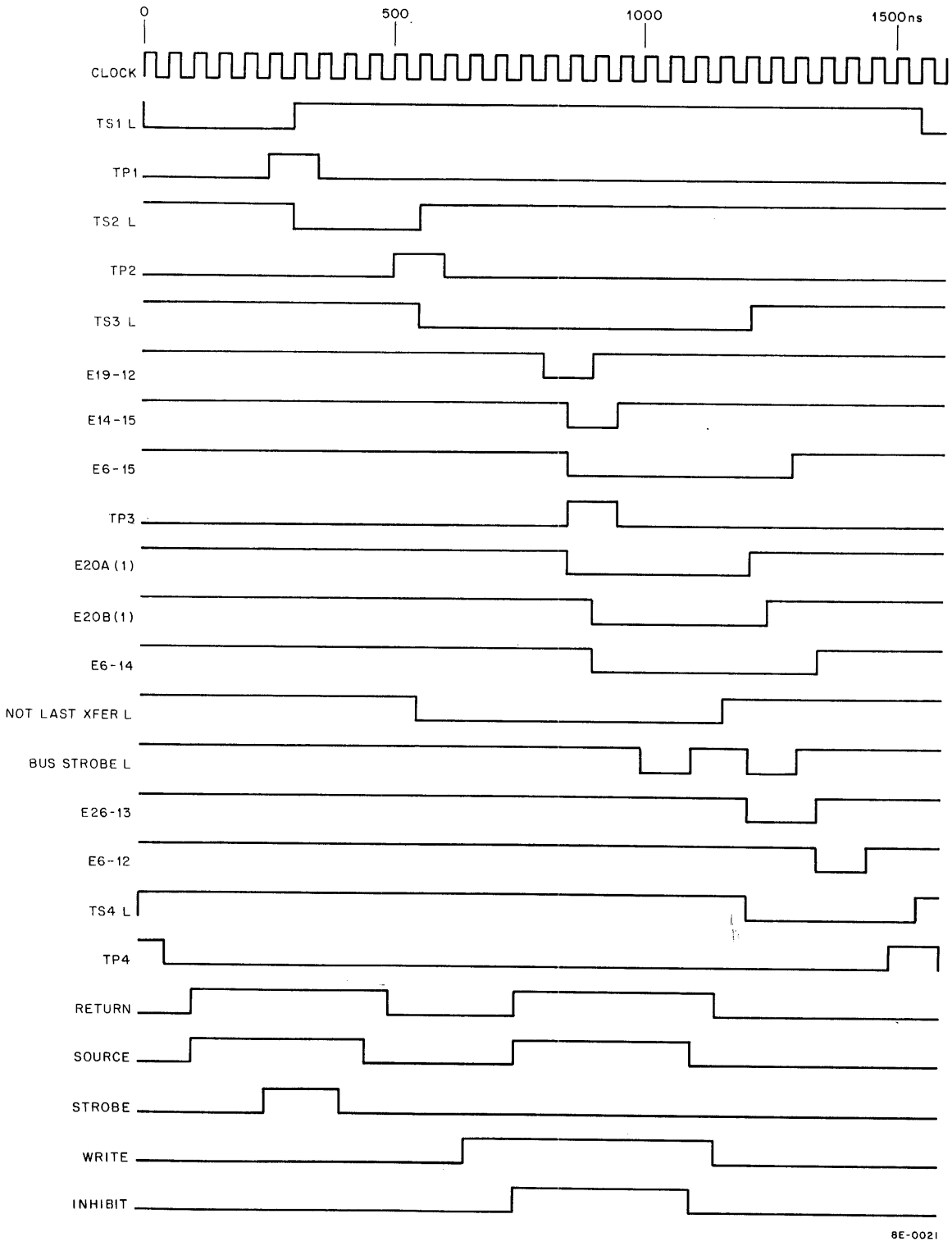


Figure 3-30 Memory and Processor Timing I/O Interrupt

SECTION 4 – MEMORY SYSTEM

3.22 MEMORY SYSTEM, GENERAL DESCRIPTION

The standard PDP-8/E core memory (designated MM8-E) is a random access, coincident-current, magnetic READ/WRITE core memory with cycle times of 1.2 μs and 1.4 μs. The memory comprises ferrite cores wired in a 3-D, 3-wire, planar configuration. The basic unit can store up to 4096 (4K) 12-bit words. The memory can be expanded to 32K words in 4K increments.

3.23 MEMORY SYSTEM, FUNCTIONAL DESCRIPTION

The memory system performs three basic functions for the PDP-8/E processor:

a. It decodes and selects the desired core location in which a 12-bit word is stored or will be stored.

b. It reads a 12-bit word from the selected location.

c. It writes a 12-bit word into the same selected location.

These functions are illustrated in Figures 3-31 and 3-32, for which one memory cycle is represented. The processor must first supply the address (refer to Chapter 4, Section 1, Memory Addressing, of the *PDP-8/E & PDP-8/M Small Computer Handbook)* before a read or write operation can be considered. The CPMA Register (Paragraph 3.34) is loaded at TP4; the content of the CPMA is placed on the MA lines. Memory address decoders receive the MA bits and turn the corresponding Read current switch on when control signals RETURN, SOURCE, and WRITE L (not) are present. The Memory Register is cleared when RETURN and NOT WRITE L become active (WRITE L is high and RETURN is high).

The outputs from the 12 selected cores are fed to their respective sense amplifiers. A strobe signal is used to gate the Sense Amplifier into the local Memory Register. If MD DIR L is low (as it always is during the READ portion of the memory cycle), the output of the Memory Register is placed on the MD lines. During the WRITE portion of the memory cycle, the memory selection system uses the same address inputs and control signals; however, control signal WRITE L will change states, causing the write current switches to be activated. To write the content of the Memory Register back into core, MD DIR L will be low (active). Otherwise, the content of the MB Register will be placed on the MD lines, and the word in the MB Register will be written into core. The INHIBIT L signal controls the gating circuits, and only when INHIBIT L is active will the Inhibit Drivers be activated. A 0 received from the MD lines and INHIBIT L causes the corresponding Inhibit Driver to produce inhibit current.

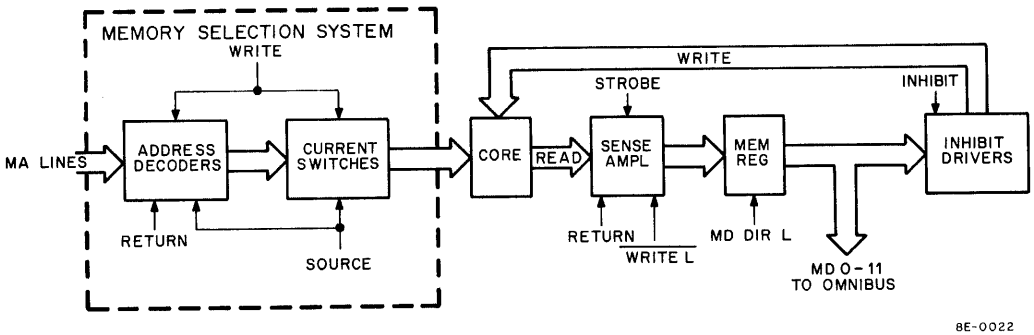


Figure 3-31 Memory System Functional Flow Diagram

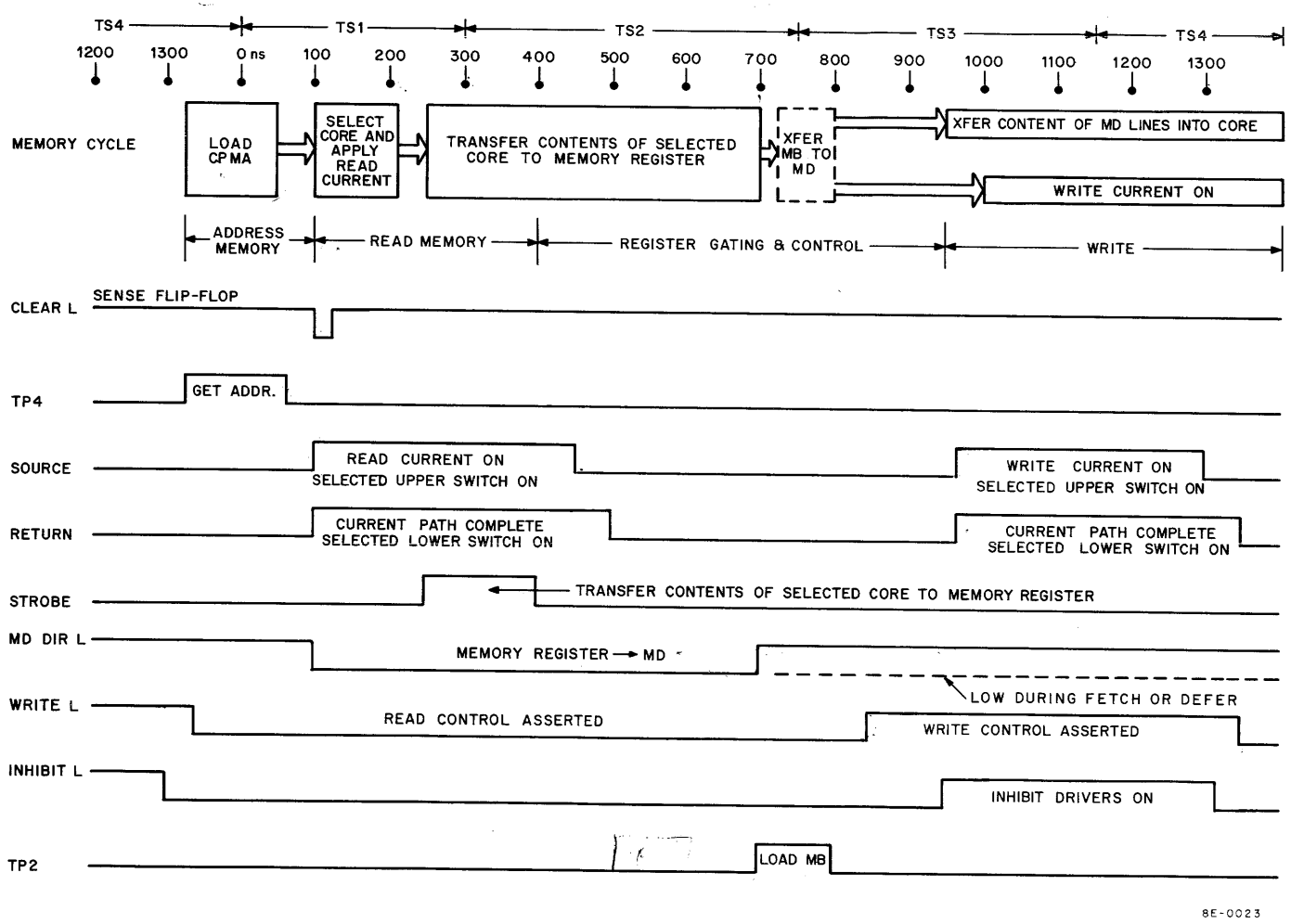


Figure 3-32 Memory Cycle Timing

3.24 MEMORY SYSTEM, DETAILED THEORY

The organization of the memory system is illustrated in Figure 3-33. Three quad-size boards are used to contain the memory system as follows:

a. G104 Sense/Inhibit contains 12 Sense Amplifiers, Memory Registers, and Inhibit Drivers with the corresponding control logic, slice control, -6V supply and current control;

b. G619 Memory Stack contains 12 mats of 4096 cores per mat, and X/Y diode selection matrix;

c. X/Y Driver and Current Source contains address decoding and selection switches, X-current source, Y-current source, and stack discharge switch-power ON/OFF protection circuit.

The detailed theory of core memory, memory selection system, and the memory sense/inhibit function is described in the following paragraphs.

3.25 CORE MEMORY

The basic storage element in the MM8-E Memory System is a small toroidal (ring-shaped) piece of magnetic material, called a magnetic core. A single core, mounted on a ground plane, is illustrated in Figure 3-34. Three wires pass through each core to accommodate the X- and Y-selection and the sense/inhibit function. A primary difference between the PDP-8/E and its predecessors is the combination of the SENSE line with the INHIBIT line to form a three-wire system instead of a four-wire system.

3.25.1 Hysteresis Loop

The characteristics of the magnetic core can be shown by a graph, plotting the current (the magnetizing force) versus flux-density (the resulting magnetism) hysteresis loop as illustrated in Figure 3-35. This hysteresis loop illustrates the magnetizing current, I, produced by the current contained in the three wires plotted along the horizontal axis, and the resulting flux density, B, through the core along the vertical axis. Two directions of current are shown. READ current, with respect to the graph, is directed from right to left. If a logic 1 is stored in the core, B will move from the remanent point ($+B_r$) down to saturation at $-B_m$ when the READ current is turned on. When the magnetizing current is removed, the flux density settles down to the remanent point at $-B_r$. WRITE current is directed from left to right with respect to the graph. If a 1 is to be written into core, the flux density will move the point $-B_r$ to point $+B_m$ on the graph and then settle down to $+B_r$ when the magnetizing current is removed. Thus, points $-B_m$ and $+B_m$ are the extreme saturation points, and points $-B_r$ and $+B_r$ are the extreme points in the normal logic states.

3.25.2 X/Y Select Lines

Core saturation occurs only when both the X- and Y-select lines each contain half the amount of current required to reach saturation. This is called the coincident current technique and results in a fully selected core. If either X- or Y-line contains no current, there is no significant change in flux density. For example, for a READ, if the core is in logic 1 state, the flux change is from point $+B_r$ to H on the graph and then reverts back to point $+B_r$. For a WRITE, the flux change is from point $-B_r$ to point J and then reverts back to $-B_r$.

3.25.3 READ Operation

READ occurs during the first half of the memory cycle. Its function is to sample either a logic 1 or logic 0 in a fully selected core. Thus, both the X- and Y-Read half-select currents must be applied for the Sense/Inhibit line to receive a pulse resulting from a change in flux density if the core is in the logic 1 state. If the core is in the logic 0 state, no change in flux density occurs and, therefore, no pulse appears on the Sense/Inhibit line.

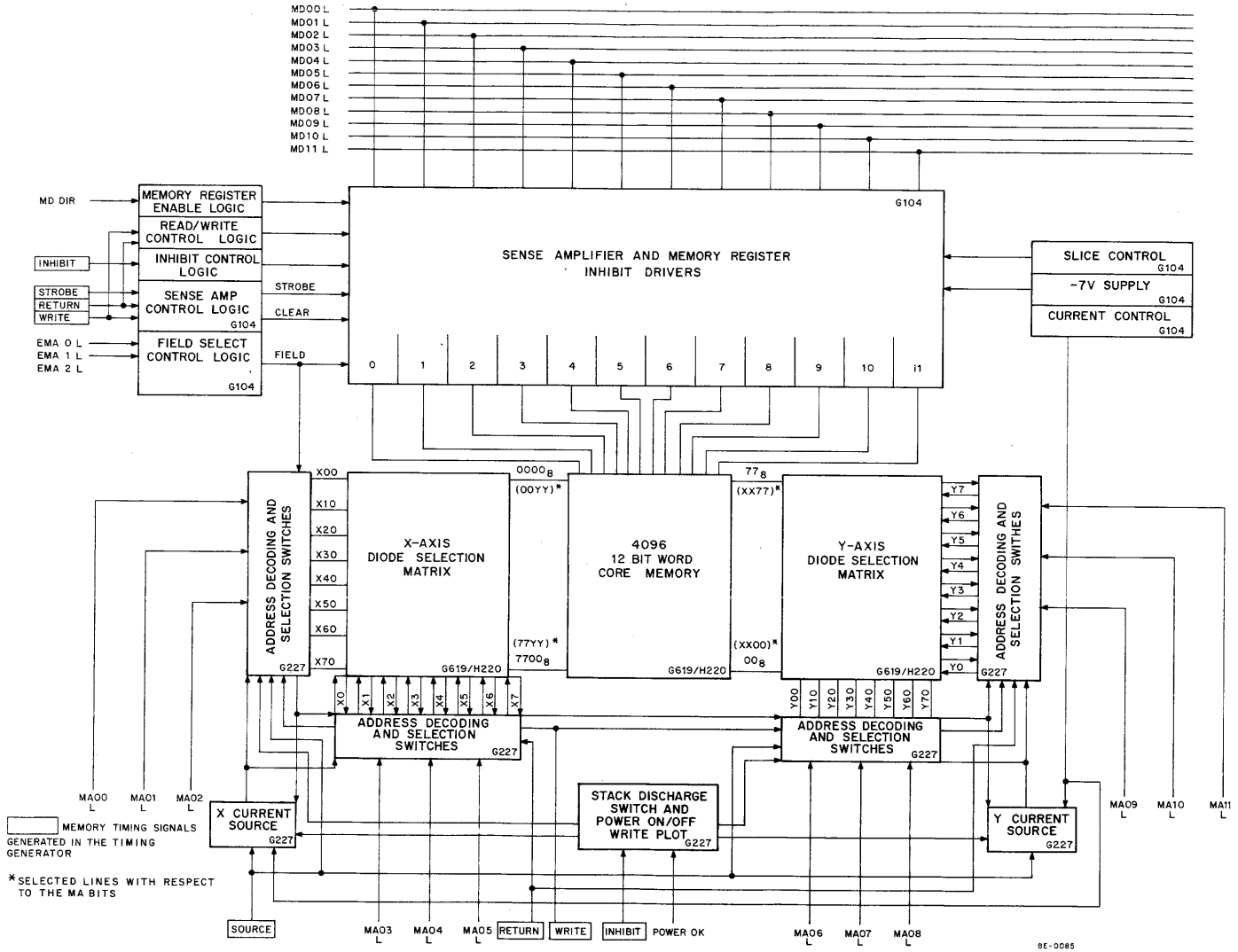


Figure 3-33 Memory System Block Diagram

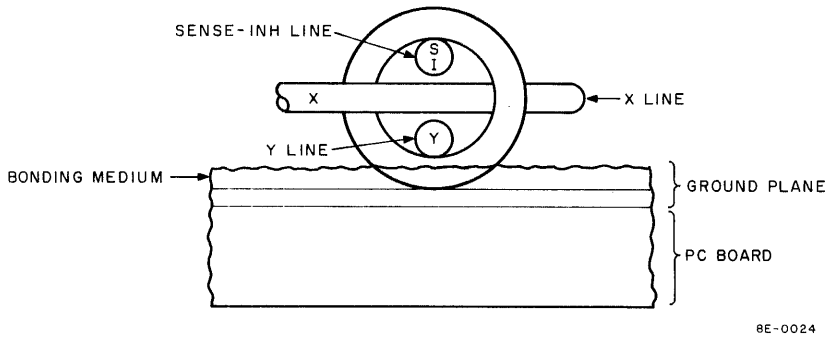


Figure 3-34 Magnetic Core

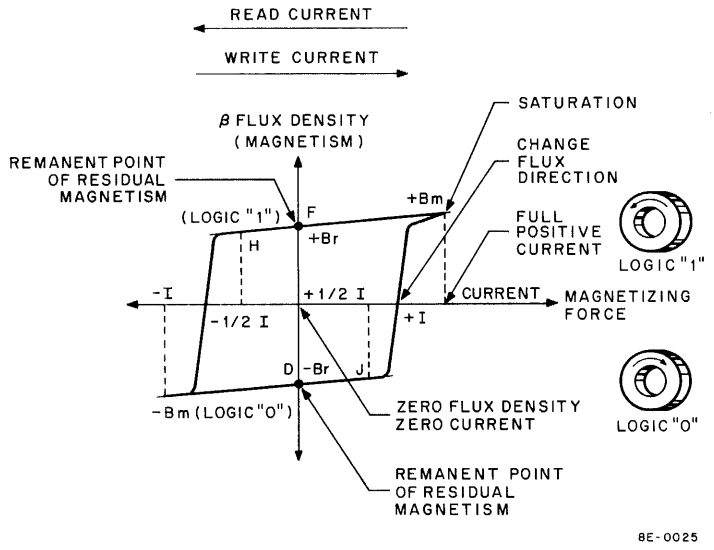


Figure 3-35 Magnetic Core Hysteresis Loop

3.25.4 WRITE Operation

WRITE occurs during the second half of the memory cycle. Because WRITE follows READ, the cores at the selected address have been cleared to a logic 0 state. If the fully selected core (X- and Y-currents) is not inhibited, the magnetic flux moves from point $-B_r$ to $+B_r$ on the graph, and a 1 is stored in core. However, to store a 0 in core, it is necessary to cause a less than fully selected condition. This can be achieved by generating an inhibit current and applying this current to the Sense/Inhibit line. If this inhibit current is in the opposite direction to the X- and Y-current, the net result of the change in flux will be from point $-B_r$ to point J on the graph. When all currents are removed, the flux density reverts back to $-B_r$ on the graph.

3.25.5 Magnetic Core In Two-Dimensional Array

A partial three-wire memory configuration is illustrated in Figure 3-36. Half-select currents are produced for one X-line and one Y-line. If, for example, the core at X3, Y2 is selected, the corresponding wires going through each row would contain half-select current. For the X3 row, X3, Y1 core would contain only half-select current, and X3, Y2 core would contain full-select current. All other cores in row Y2 would contain half-select current. The Sense/Inhibit line terminates at the Sense Amplifier and the Inhibit Driver in the manner shown in Figure 3-36. There are two termination points on the Sense Amplifier side, and one termination point at the Inhibit Drivers.

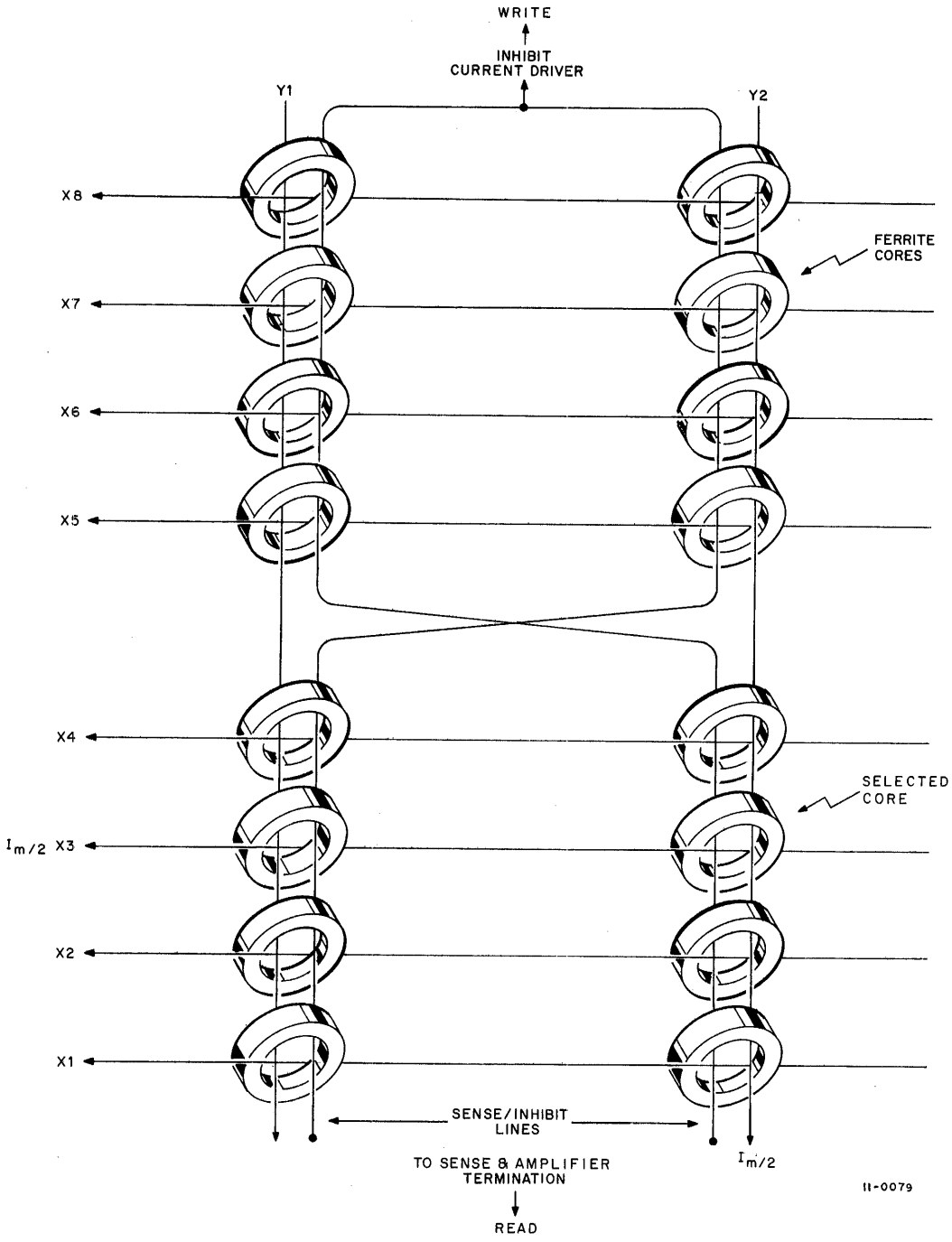


Figure 3-36 Three-Wire Memory Configuration

The third wire (the Sense/Inhibit line) receives the resulting signal at the coincident-current points during READ. Current direction is from the top of the illustration down to the Sense Amplifier. For WRITE, current direction is from the bottom of the illustration to the top to the Inhibit Current Driver. This direction opposes the current in the Y-selection line and, therefore, causes a half-select condition. This half-select procedure is only required where a 0 is to be written into core.

3.25.6 Assembly of 12-Stacked Core Mats

The MM8-E Memory is a 64 X 64 configuration (64 X-rows and 64 Y-rows). This configuration provides 4096 cores per mat, for which one core can be selected during any one memory cycle and, therefore, one bit of information per mat.

The MM8-E is a 12-bit word memory system; thus, 12 mats are used. Each mat stores one unique bit of information, which is deposited and sensed by one unique line called the Sense/Inhibit line. Thus, 12 Sense/Inhibit lines are used to deposit and sense 12 unique bits of information. The arrangement of the selection lines is quite different. All 12 mats contain 64 X-lines and 64 Y-lines. The threading of each of the X- and Y-lines continues from one mat to the next through all 12 mats. For example, row X31 of mat 0 is common to row X31 of mat 1, which is common to all subsequent mats at row X31. The common factor to each mat is the selection line that is threaded through 12 X 64 cores or 768 cores. The intersection of X31 and Y29, therefore, occurs 12 times in the 12 mats. Because each mat contains a unique Sense/Inhibit line, 12 unique bits of information can be stored to form a 12-bit word.

3.25.7 Physical Orientation of Core Memory

The memory stack layout is illustrated in Figure 3-37. Figure 3-38 illustrates the X- and Y-windings within the memory stacks.

3.26 CORE SELECTION SYSTEM

Core selection is accomplished by enabling the desired X-line and the desired Y-line and allowing current to pass through the selected lines. To accomplish the selection of the X- and Y-lines, a decoding network that receives the MA bits and decodes for line selection is required. An X- and Y-current source is also required so that each line is half-selected.

A selection system functional block diagram illustrating the parts of the memory system involved in core selection is given in Figure 3-39. The primary components involved are:

a. the memory address decoder, which receives memory address bits and control signals to select (enable) the corresponding switch and driver,

b. a current source to provide the necessary select current,

c. a driver and switch to apply current to the selected row and forward-bias the selection diode,

d. one read or write diode, which becomes forward-biased by the driver and switch while all other diodes are back-biased,

e. one selected row containing 768 cores.

The driver and switch shown in Figure 3-39 are one of 16 drivers and one of 16 switches. A WRITE operation for row X13 is illustrated to show the current path.

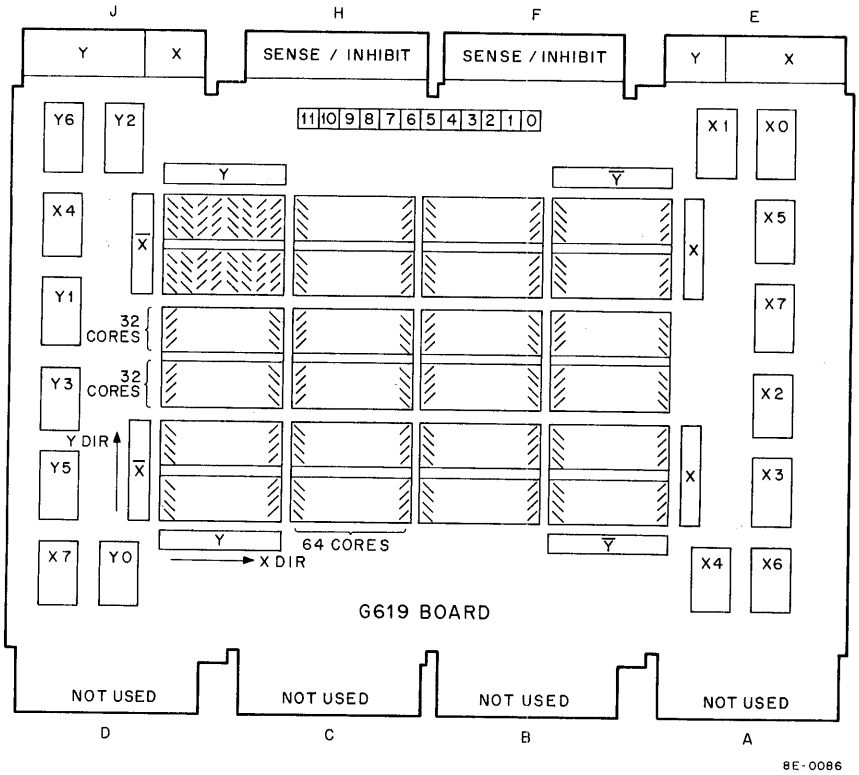


Figure 3-37 Memory Stack Layout (Core Orientation)

Both the READ and WRITE current paths are illustrated in Figure 3-40. Although not all of the circuitry is shown, the current path relationship between a READ and WRITE operation (Figures 3-40a and 3-40b) illustrates how the direction of current for WRITE is opposite to the direction for READ. The illustration also shows how the unselected components are interconnected but passive.

NOTE

Electron current flow is presented in this manual. The reader should consider current originating at a more negative voltage level and taking the path to a more positive voltage level. A forward-biased diode results when the current takes the direction opposite to the diode arrow.

3.26.1 Organization of X/Y Drivers and Current Source

Figure 3-41 illustrates the organization of the X/Y drivers and current source, and the primary signals required to make line selection and current switching possible. Eight decoders are used to select one of 64 X-lines and one of 64 Y-lines as determined by the content of bits MA0 through MA11 L. X-current and Y-current, provided by the X- and Y-current source, are applied to the drivers. The READ signal is applied to both the decoder control gates and the Bias Driver. When a READ operation is to be performed, the selected READ switches and drivers are enabled and the READ/WRITE current switch changes its output signal from ground to -15V. The negated READ signal acts to enable the WRITE function in a similar manner.

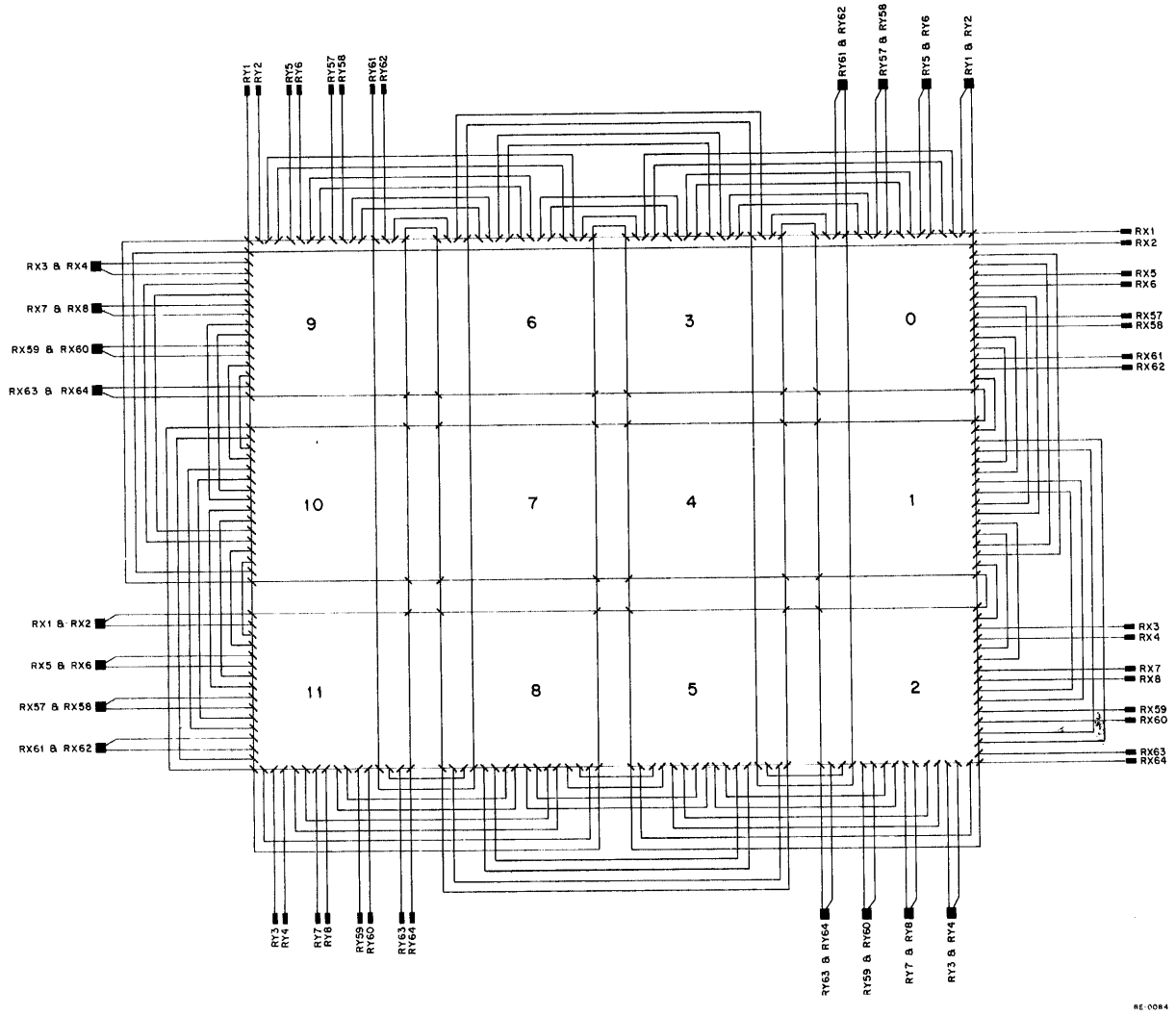


Figure 3-38 Memory Stack X, Y Windings

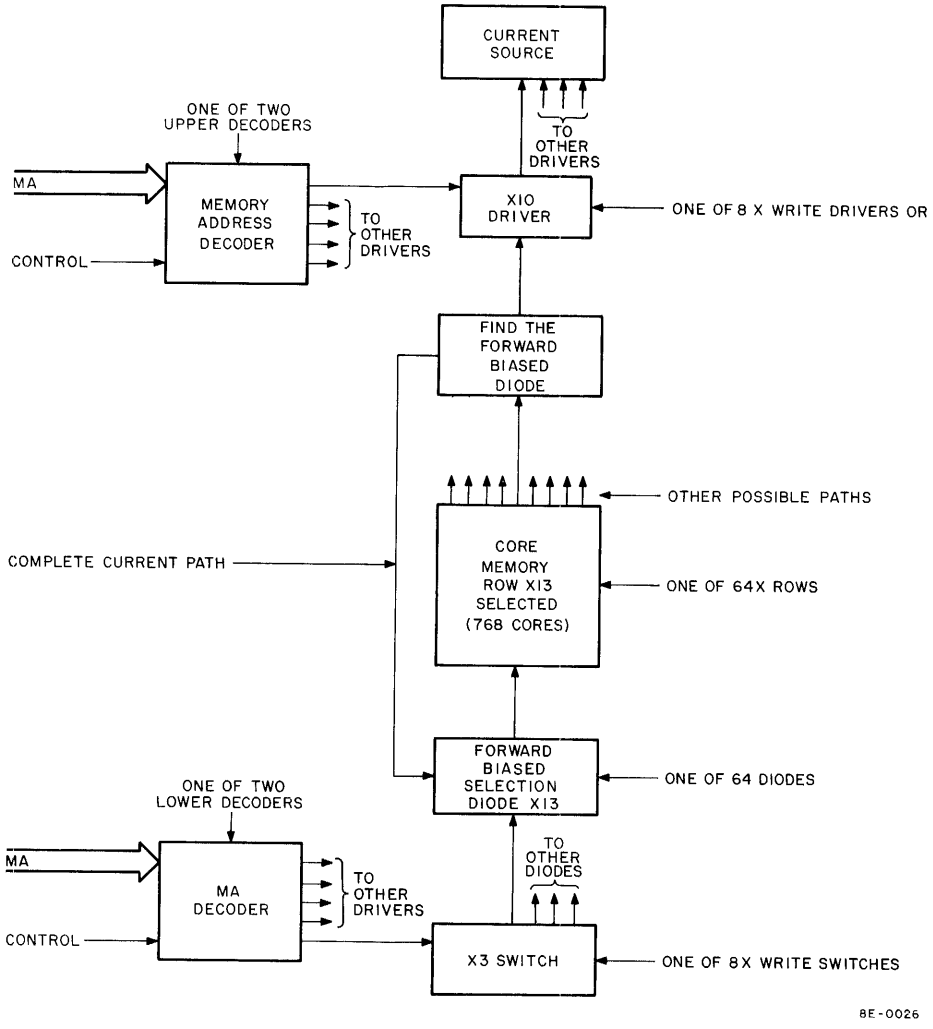
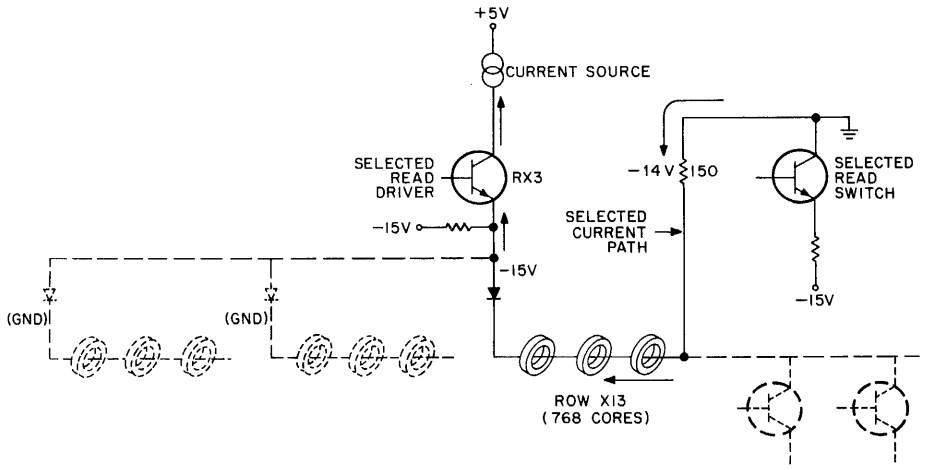
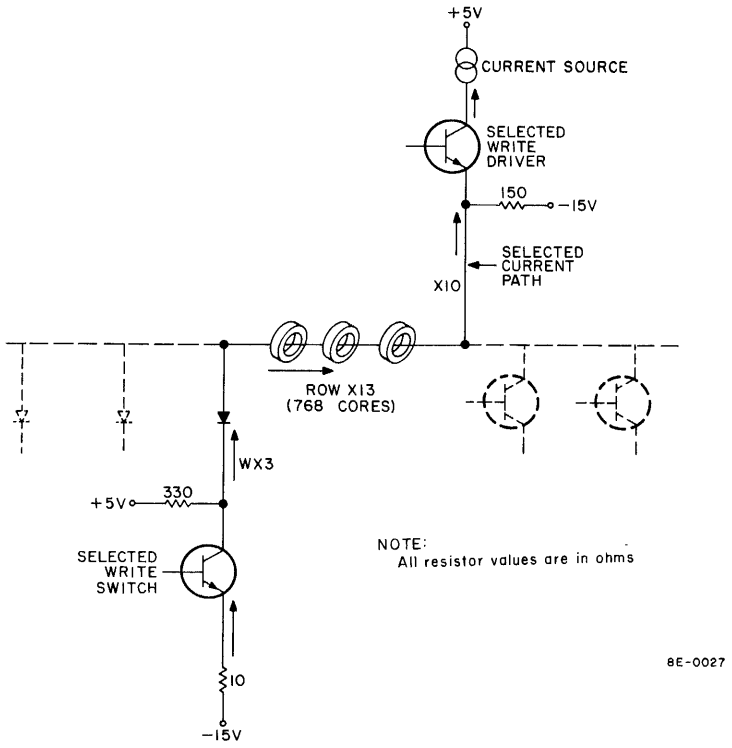


Figure 3-39 Selection System Functional Block Diagram for Write Current of X Rows



a. Current Path for Read Current



b. Current Path for Write Current

Figure 3-40 Read/Write Current Paths

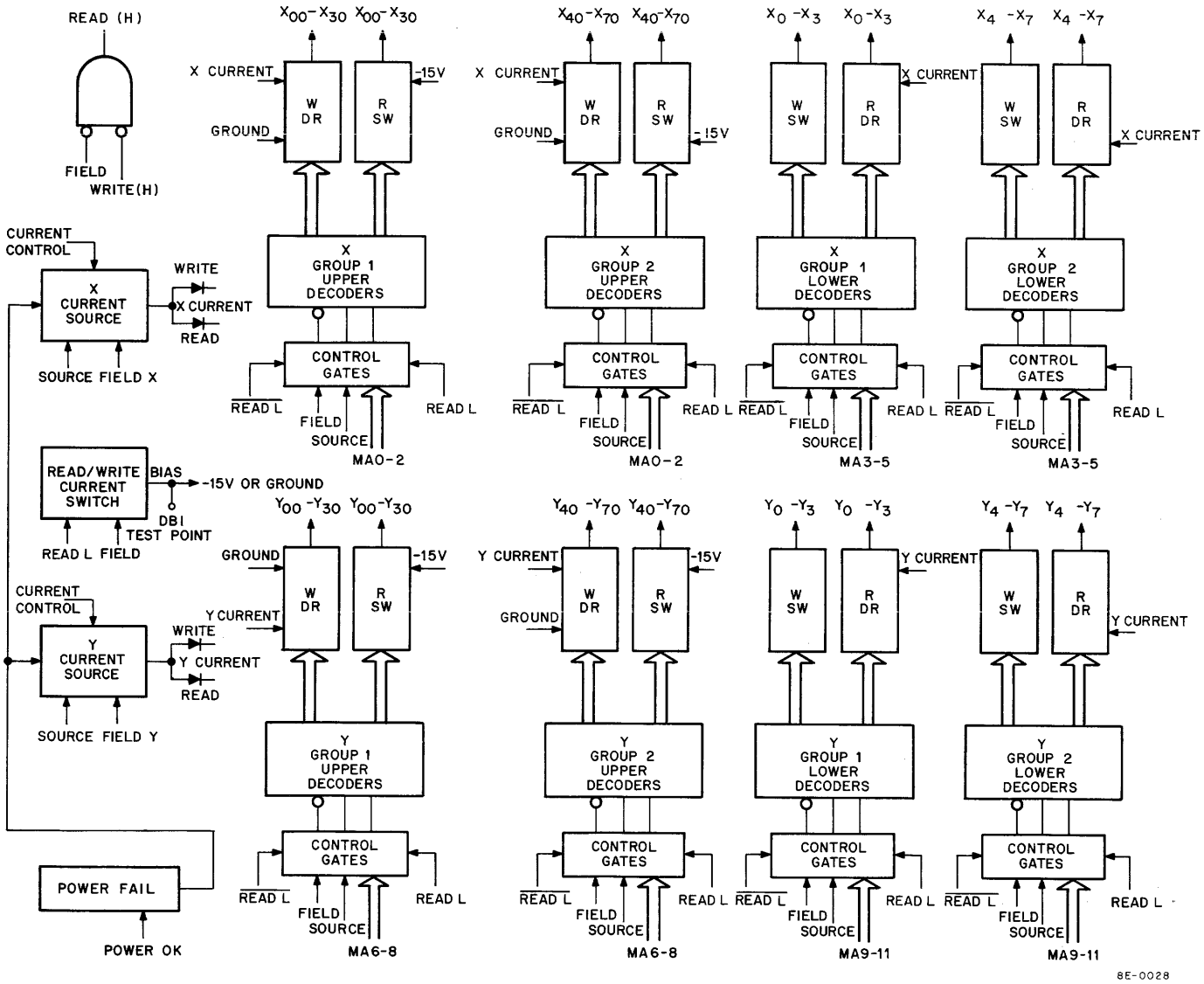


Figure 3-41 X- and Y-Drivers and Current Source
(Block Diagram Representation of G227 Circuit Schematic)

3.26.2 X- and Y-Current Sources

The X- and Y-current sources supply constant current to the READ and WRITE drivers (Figures 3-42 and 3-43). The READ and WRITE drivers receive bias voltage from the current control circuit located on the sense/inhibit board and are turned on when both FIELD and SOURCE are active. They have a slow turn-on rate and a fast turn-off characteristic due to the capacitor in the circuitry. A fast turn-off is achieved by the interaction between the capacitor and two transistors. When SOURCE is negated, one of the transistors is turned on, causing the capacitor to discharge, which causes the output transistor to be biased off. The slow turn-on time reduces the coupling effects within the core stack. Furthermore, the slow turn-on time also means that the READ current is completely controlled by the current source. Because the current source is controlled, the position of the sense output voltage relative to the drive currents is constant.

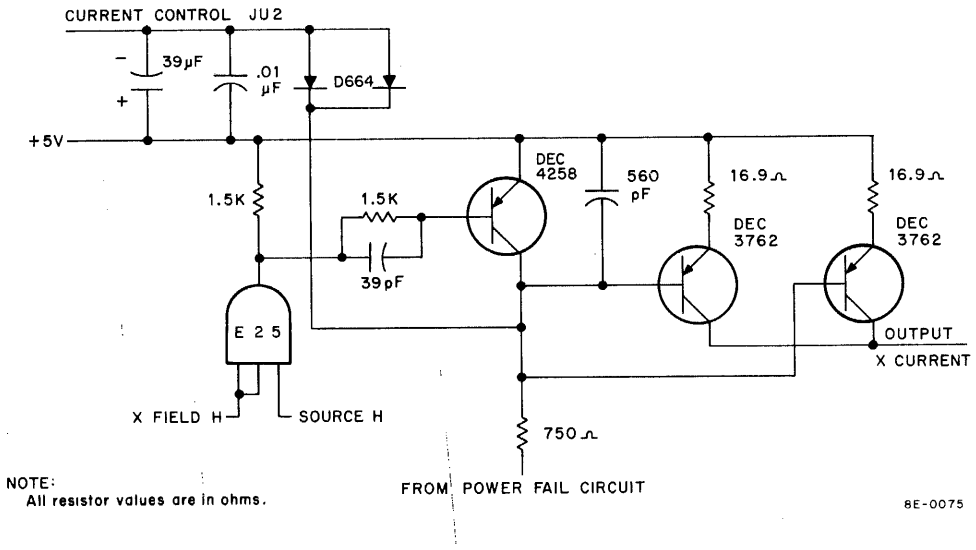


Figure 3-42 X-Current Source

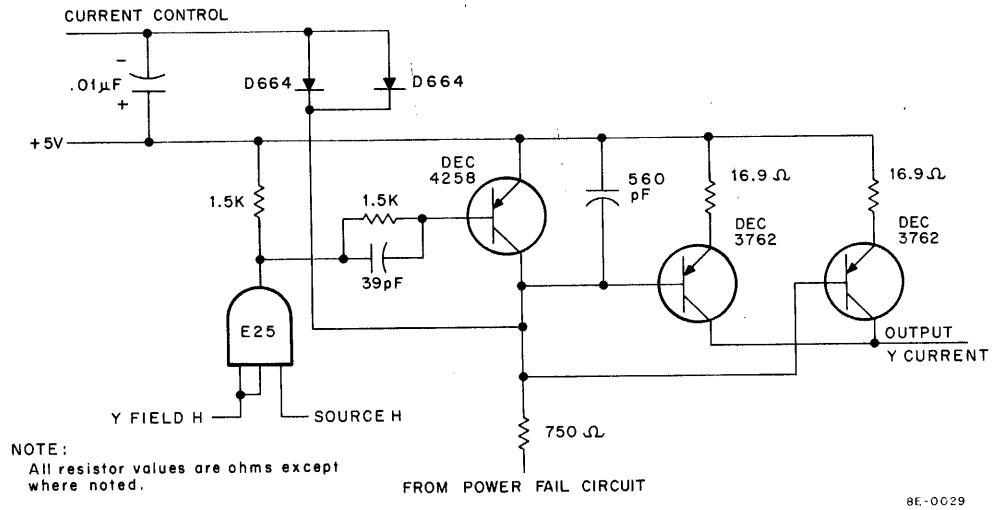


Figure 3-43 Y-Current Source

3.26.3 Bias Driver

The Bias Driver (Figure 3-44) switches the bias voltage from ground for a READ operation to -15V for a WRITE operation. When control signals READ and X FIELD are both active, level shifting circuits along with an output transistor switch the output to ground. When READ is not asserted, the output switches to -15V. The Bias Driver provides the reverse bias condition on the nonselected diodes in the memory stack. Reverse biasing the diodes reduces capacitance and, therefore, reduces "sneak currents" that might be on the line. Refer to Paragraph 3.26.7 for the organization of the planar stack diode matrix.

3.26.4 Power Fail Circuitry

The power fail circuitry (Figure 3-45) responds to the POWER OK signal from the power supply. Its primary function is to ensure that selected memory locations are not changed due to a power failure. The power supply senses a voltage change when the dc voltage drops and grounds the POWER OK line when the voltage is too low. This shuts off the timing chain but ensures that the memory cycle is completed. The memory power fail circuitry turns off the X- and Y-current source after a delay sufficient to complete the WRITE operation. When the machine is turned on initially and the POWER OK signal is asserted, the current source is activated immediately. Thus, the memory power fail circuit has a characteristic of a fast-on/slow-off switch.

3.26.5 Core Selection Decoders

Eight decoders (IC 8251) (Figure 3-41) are used to decode MA0 L through MA11 L from the Memory Address Register (refer to Appendix A for circuit description of 8251). These bits are combined with READ L, FIELD, SOURCE, and RETURN signals to enable the appropriate switch and driver. Signal READ L is generated when WRITE L is not asserted, or negated READ L results when WRITE L is active. The WRITE L signal is developed in the Timing Generator during the last half of the memory cycle. SOURCE is necessary to turn on the selected driver or switches corresponding to the upper X- and Y-select lines, and RETURN is necessary to turn on the selected drivers or switches corresponding to the lower X- and Y-select lines. Both RETURN and SOURCE are developed in the Timing Generator. RETURN remains on for 50 ns longer than SOURCE so that the lines completely discharge. FIELD is developed in the Sense Inhibit circuitry (Figure 3-47). If Extended Memory has not been addressed, this signal will be active.

3.26.6 Address Decoding Scheme

The block diagram in Figure 3-41 illustrates the method through which the MA bits are decoded; the results enable either a WRITE driver or READ switch and the corresponding driver or switch counterpart required to complete the current path. The decoder is arranged as follows: the upper select line decoders are on the left side and the lower select line decoders are on the right side of the illustration. The upper X-select line decoders decode bits MA0–2 L, while the lower X-select line decoders decode bits MA3–5 L. The upper Y-select line decoders decode bits MA6–8 L, while the lower Y-select line decoders decode bits MA9–11 L. There are a total of eight upper X-select lines, eight upper Y-select lines, eight lower X-select lines, and eight lower Y-select lines. The decoder outputs are applied to the selected switches. The outputs of the selected switches connect to the X-selection diodes (Paragraph 3.26.7) which, in turn, are connected to a line that is threaded through 768 memory cores. The arrangement of the illustration (Figure 3-41) is such that each component corresponds to the approximate location on the engineering drawing schematic (G227). This arrangement allows a quick reference to the circuits of interest.

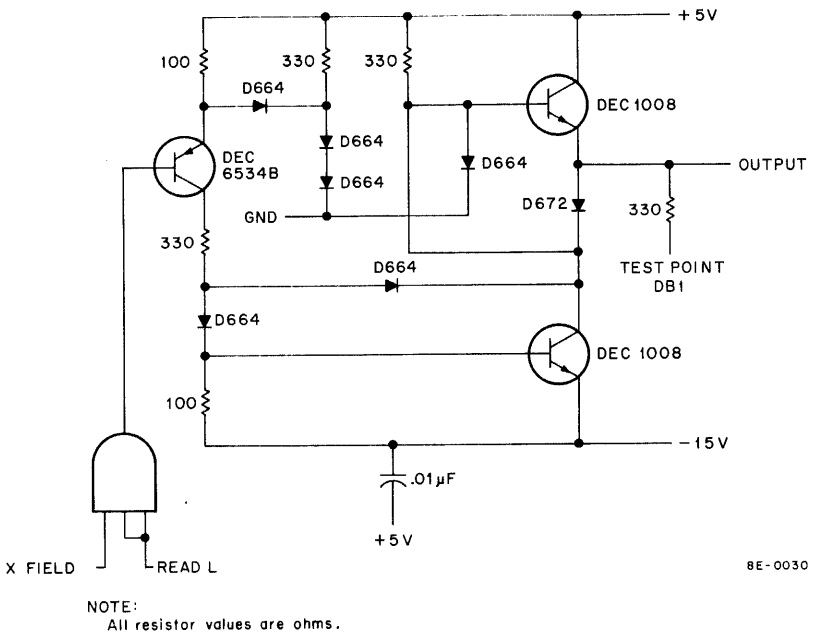


Figure 3-44 Bias Driver

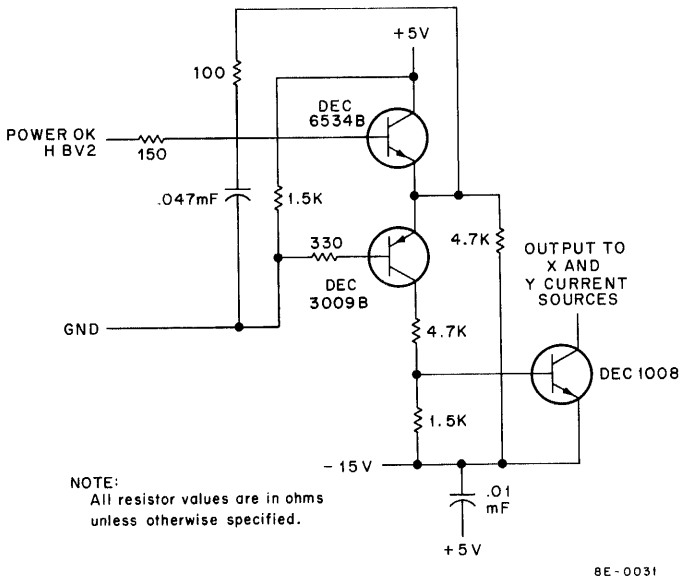


Figure 3-45 Power Fail Circuit

The decoding scheme of the MA bits is illustrated in Figure 3-46. The illustration shows the five parts of the memory address, what is decoded, and where in the field of the drawing the decoders are located. Table 3-3 lists the necessary input control signals, the content of the memory address, the input pins, the output pins, and the selected X- or Y-line. With this information, the user can easily trace through all of the components on any signal/current path to find the selected components.

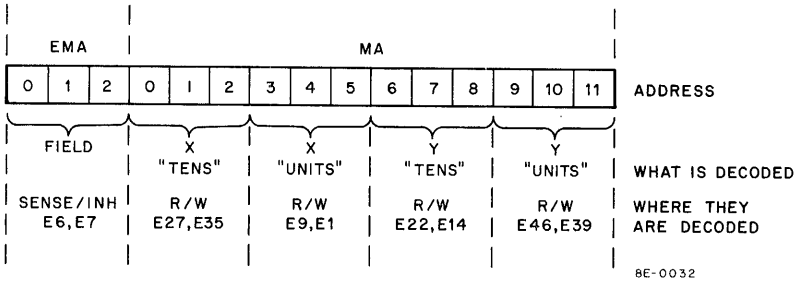


Figure 3-46 Decoding Relationships

3.26.7 Operation of Diodes

Each of the X- and Y-select lines are connected to a corresponding string of diodes (Figure 3-47). Selection is such that any one of the eight upper select lines will pass current in a path determined by whether it is a READ or WRITE operation. In the illustration given in Figure 3-47, for X-selection, the example illustrates line X_{12} being selected. The current passes through 768 cores and back through one of the diodes. The path the current takes from this point is determined by the diode that is forward-biased. The forward-biasing of a diode is accomplished by operating the switch and driver. If it is a WRITE operation, WX2 is forward-biased and the current takes the path from WX2 to X10. If it is a READ operation, RX2 is forward-biased and the current takes the path from RX10 to RX2.

NOTE

The READ and WRITE currents are opposite in direction. This is accomplished by READ L, which controls the Bias Driver circuit.

In both cases, the selection diodes are instrumental in determining the current path. All diodes except the selected diode are reverse-biased.

3.26.8 Operation of Selection Switches

Figure 3-48 illustrates the switching operation of the currents through X12 select line. On the upper side, a pair of transistors are used to either drive or switch current, depending on whether the operation is READ or WRITE. A complementary pair of transistors on the lower side are used to either drive or switch the current. Between the upper and lower side is a line that is threaded through 768 cores. The READ operation begins with the decoders. When an X-line such as X12 is to be selected, the READ driver and READ switch must first be turned on. To turn on the READ driver and READ switch, the base of each transistor must be positive with respect to the emitter. This occurs only when the output of the decoder is low (active). Otherwise, +5V is applied to the emitter side of the transformer as illustrated by S = open.

Table 3-3
Core Selection Decoding Scheme

Groups 1 and 2 – Upper X- and Y-Decoders

READ (SOURCE-)

FUNCTION	FIELD	SOURCE	WRITE L	MA 0–2 (X) MA 6–8 (Y)	Group 1 Input Pins	Group 1 Output Pins	Group 2 Input Pins	Group 2 Output Pins	Selected Line
Turn on Read Switch	L ↕ H	H ↕ L	L ↕ H		DBA				
				000	LLL	4L	– – – – – –		X or Y 00
				001	LLH	5L	– – – – – –		X or Y 10
				010	LHL	6L	– – – – – –		X or Y 20
				011	LHH	7L	– – – – – –		X or Y 30
							DBA		
				100	– – – – – –		LLL	4L	X or Y 40
				101	– – – – – –		LLH	5L	X or Y 50
				110	– – – – – –		LHL	6L	X or Y 60
				111	– – – – – –		LHH	7L	X or Y 70

Table 3-3 (Cont)
Core Selection Decoding Scheme

Groups 1 and 2 – Upper X- and Y-Decoders

WRITE (SOURCE-)

FUNCTION	FIELD	SOURCE	WRITE L	MA3–5 L MA9–11 L	Group 1 Input Pins	Group 1 Output Pins	Group 2 Input Pins	Group 2 Output Pins	Selected Line
Turn on Write Switch	L ↕ H	H ↕ L	H ↕ H		DBA				
				000	LLL	0L	– – – – – –		WX0 or WY0
				001	LLH	1L	– – – – – –		WX1 or WY1
				010	LHL	2L	– – – – – –		WX2 or WY2
				011	LHH	3L	– – – – – –		WX3 or WY3
							DBA		
				100	– – – – – –		LLL	0L	WX4 or WY4
				101	– – – – – –		LLH	1L	WX5 or WY5
				110	– – – – – –		LHL	2L	WX6 or WY6
				111	– – – – – –		LHH	3L	WX7 or WY7

Table 3-3 (Cont)
Core Selection Decoding Scheme

Groups 1 and 2 – Upper X- and Y-Decoders

WRITE
(RETURN+)

FUNCTION	FIELD	SOURCE	WRITE L	MA0–2 L MA6–8 L	Group 1		Group 2		Selected Line
					Input Pins	Output Pins	Input Pins	Output Pins	
	L	H	H		DBA				
Turn	↑	↑	↑	000	LLL	0L	– – – – – –		X or Y 00
on				001	LLH	1L	– – – – – –		X or Y 10
Write				010	LHL	2L	– – – – – –		X or Y 20
Drivers				011	LHH	3L	– – – – – –		X or Y 30
							DBA		
				100	– – – – – –		LLL	0L	X or Y 40
				101	– – – – – –		LLH	1L	X or Y 50
				110	– – – – – –		LHL	2L	X or Y 60
	L	H	H						
				111	– – – – – –		LHH	3L	X or Y 70

Table 3-3 (Cont)
Core Selection Decoding Scheme

Groups 1 and 2 – Upper X- and Y-Decoders

READ
(RETURN+)

FUNCTION	FIELD	SOURCE	WRITE L	MA3–5 L MA9–11 L	Group 1		Group 2		Selected Line
					Input Pins	Output Pins	Input Pins	Output Pins	
	L	H	L		DBA				
Turn	↑	↑	↑	000	LLL	4L	– – – – – –		RX 0 or RY 0
on				001	LLH	5L	– – – – – –		RX 1 or RY 1
Read				010	LHL	6L	– – – – – –		RX 2 or RY 2
Drivers				011	LHH	7L	– – – – – –		RX 3 or RY 3
							DBA		
				100	– – – – – –		LLL	4L	RX 4 or RY 4
				101	– – – – – –		LLH	5L	RX 5 or RY 5
				110	– – – – – –		LHL	6L	RX 6 or RY 6
				111	– – – – – –		LHL	7L	RX 7 or RY 7
	L	H	L						

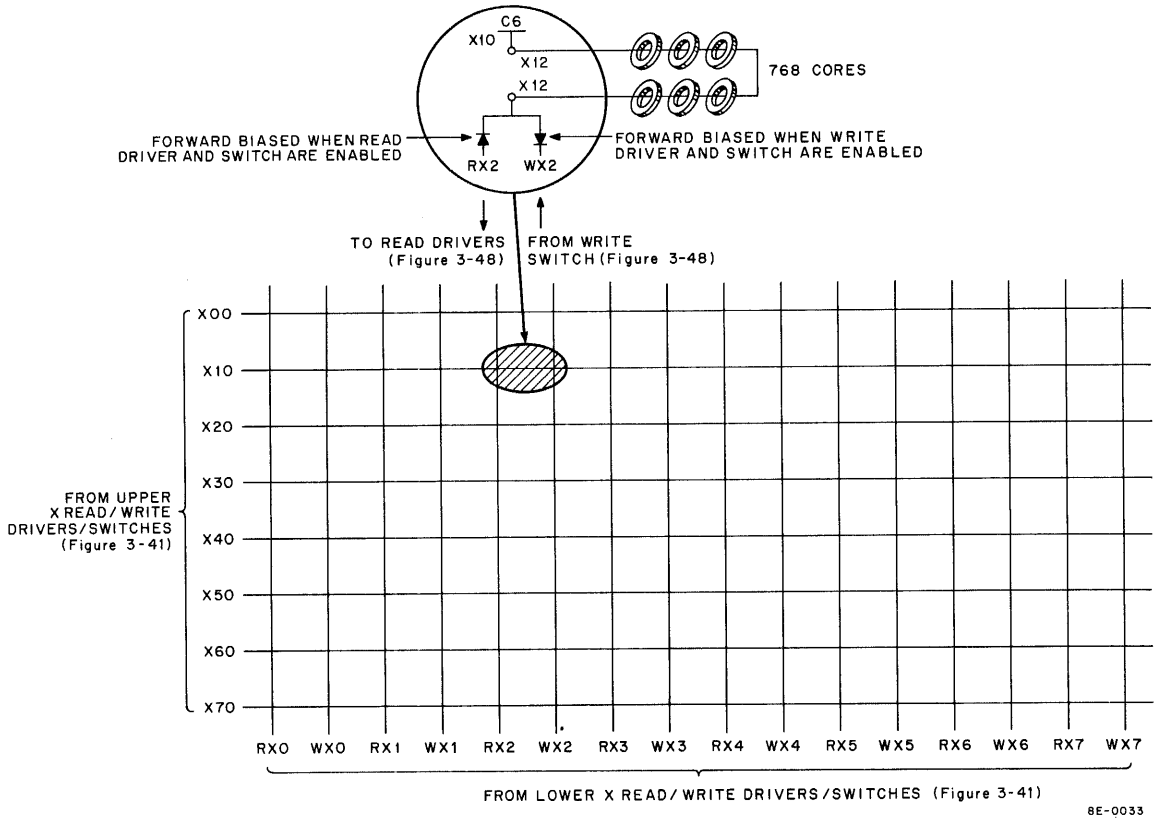


Figure 3-47 Organization of Planar Stack Diode Matrix for X Select Lines

When the READ driver is off, the +5V causes the READ diode at the current source to be reverse-biased. As soon as the READ driver is turned on, the READ diode immediately becomes forward-biased, allowing regulated current to be applied to the READ driver. The driver serves as a high-gain current amplifier, which supplies the required current to half-select any given core. A second requirement to pass READ current through core is to forward-bias the READ diode in the diode matrix. Current then passes through the READ driver, through the READ diode, through 768 cores, and back to the READ switch.

The WRITE operation is similar to READ and begins with the decoder. To select line X12, the decoder causes the WRITE driver transformer to reverse polarity, which then turns on the WRITE driver. The WRITE diode at the current source becomes forward-biased and current begins flowing through the diode, the WRITE diode of the matrix, and through 768 cores.

3.26.9 Operation of the Core Selection System

The cores that contain a selected X-line and selected Y-line define the location for which a 1 or 0 will be either written in or read out. Figure 3-49 illustrates a small portion of memory and the corresponding selection devices. Using Table 3-3, the selection of any given core can be traced from the Memory Address Register, through the decoders and switches, to the selected core.

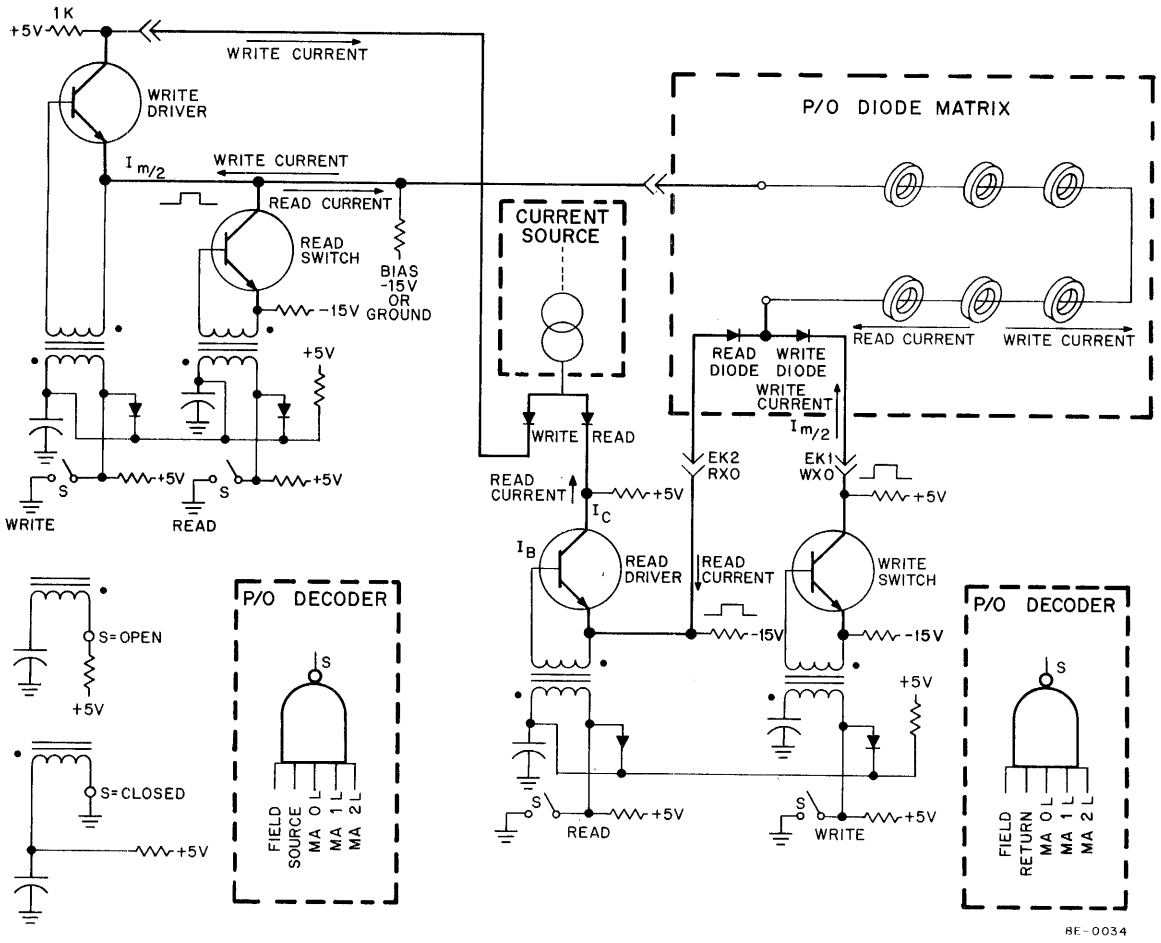


Figure 3-48 Operation of Selection Switches

3.27 SENSE/INHIBIT FUNCTION

The previous paragraphs have described the memory core, the selection of memory core, and the selection of memory core in terms of the READ/WRITE operation. However, to perform a READ or a WRITE operation, sense amplifiers are necessary to sense the state of the selected cores, and Inhibit Drivers are necessary to write 0s into core. Control logic and data registers are also required to control the data flow to and from memory. These necessary circuits are illustrated in a simplified diagram (Figure 3-50). The circuitry corresponding to the READ operation is shown on the lower portion of the illustration; the circuitry corresponding to the WRITE operation is illustrated in the upper portion of the illustration.

3.27.1 Sense/Inhibit Line

The line that is used to sense a 1 during READ is used to transmit current when a 0 is to be written during the WRITE portion of the memory cycle. The Sense/Inhibit line passes through 4096 cores of a corresponding mat. Both ends of this line are terminated at the input to the Sense Amplifier; a terminal connection is made so that the Inhibit Driver output joins this same line.

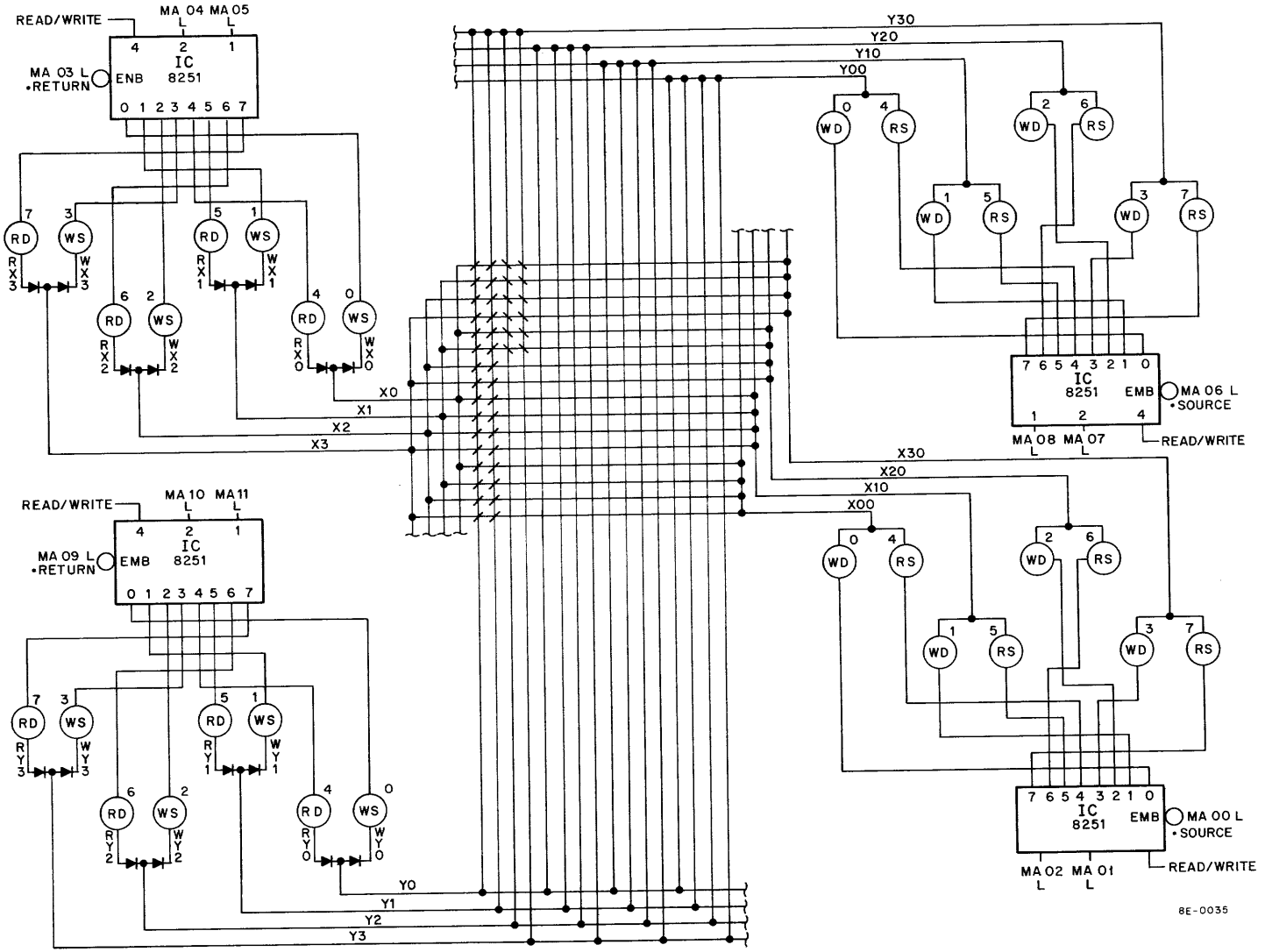


Figure 3-49 Operation of X/Y Selection Switches

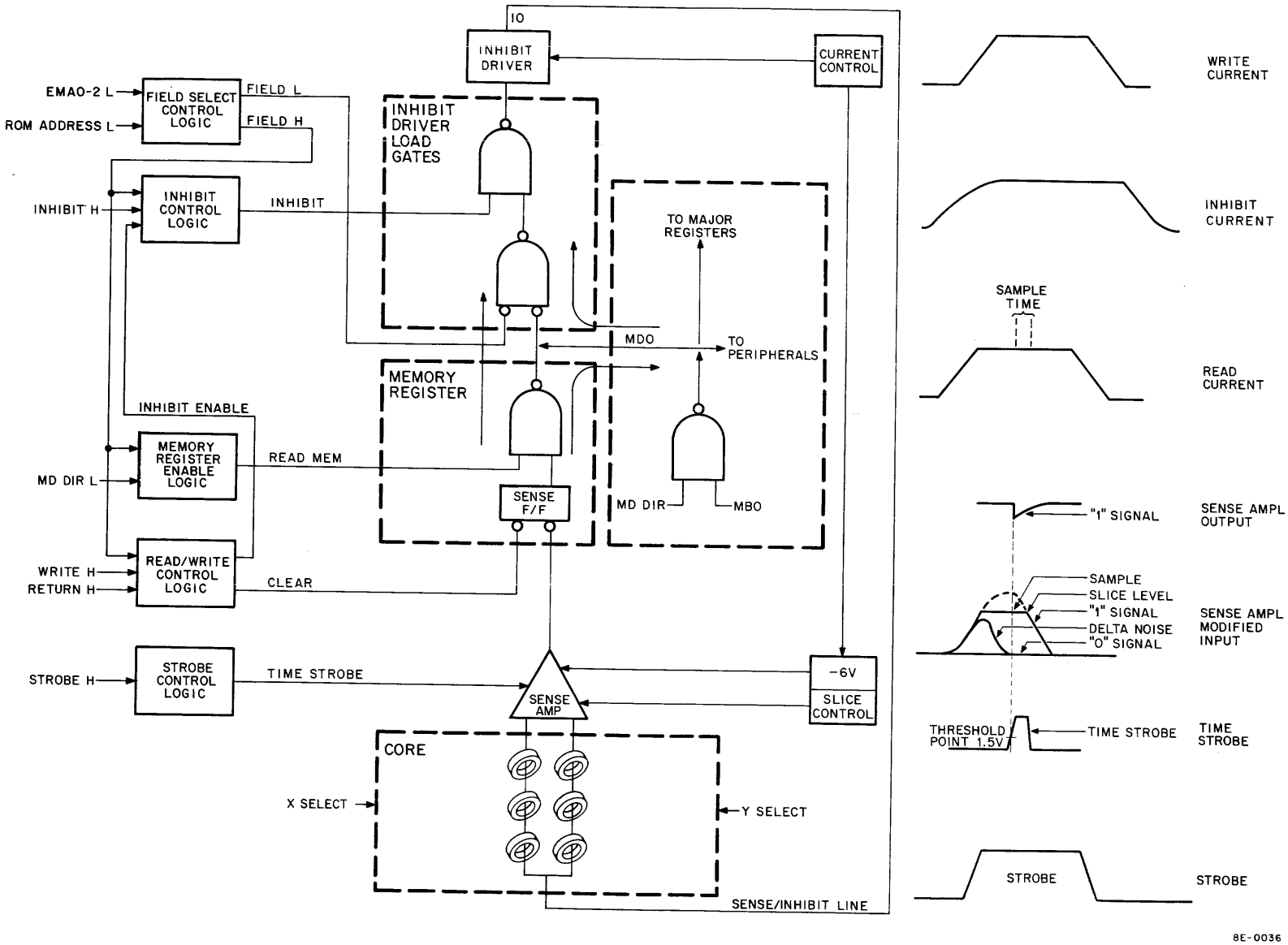


Figure 3-50 READ/WRITE Operation, Simplified Diagram (Bit 0)

3.27.2 READ Operation

The READ operation involves the Sense Amplifier, Memory Register, and the necessary control logic in conjunction with the selection system. During the READ portion of the memory cycle, the selected core develops a signal on the Sense/Inhibit line only if a 1 was previously stored in core. The SENSE flip-flops are cleared and TIME STROBE gates either a 1 or 0 out of the Sense Amplifiers and applies a corresponding pulse (if it is a 1) to the Memory Register. When a 1 is sensed, the Sense Amplifier applies a negative-going pulse to the SENSE flip-flop. The Memory Register output gate receives the SENSE flip-flop signal and gates the 1 or 0 out to the MD line. Note that the Memory Register outputs are gated onto the MD lines only when MD DIR L is low; consequently, the only requirement to write the contents of the Memory Register back into memory is to keep MD DIR L low during the WRITE portion of the memory cycle. The output of the Memory Register can be applied, therefore, to the inhibit circuits for a rewrite; or because the data is first applied to the MD BUS, the output of the Memory Register can be loaded into one of the major registers or a peripheral.

When the Memory Register applies data to the MD lines (Figure 3-2), the data can be loaded into any one of the Major Registers, as well as applied to the Inhibit Drivers for re-deposit into core. Conversely, the data contained in the Memory Buffer (MB) Register can be applied to the MD lines and to the Inhibit Drivers.

3.27.3 WRITE Operation

The WRITE operation involves the Inhibit Drivers, load gates, Memory Register, and the necessary control logic in conjunction with the selection system. The Inhibit Driver load gates receive 1s and 0s via the MD lines from either the MB Register in the processor or the Memory Register. Control gating signals for the Inhibit Driver load gates are:

a. FIELD, which indicates that field 0 has been selected,

b. INHIBIT from the Timing Generator. Inhibit current is generated by the Inhibit Drivers only when a 0 is to be written into core.

3.27.4 Field Select Control Logic

The field select control logic (Figure 3-51) determines if the basic memory has been selected. When field 0 is selected, the logic develops a signal, called FIELD, for gating other control logic and the Inhibit Driver load gates. The logic receives extended address memory bits EMA0 L through EMA2 L.

A comparison circuit compares the bits on the EMA lines with the EMA jumpers. If the two are equal and if ROM ADDRESS L is high, the field is selected. Bank 0 is always selected with all jumpers in. The Exclusive-OR gate provides a high output only when one input is high.

3.27.5 Inhibit Control Logic

The Inhibit Control logic (Figure 3-52) provides a gating control signal to the Inhibit Driver load gates during the WRITE portion of the memory cycle. The logic receives INHIBIT from timing, RETURN from the Timing Generator, FIELD from the Field Select Control logic, and WRITE ENABLE from the READ/WRITE control logic.

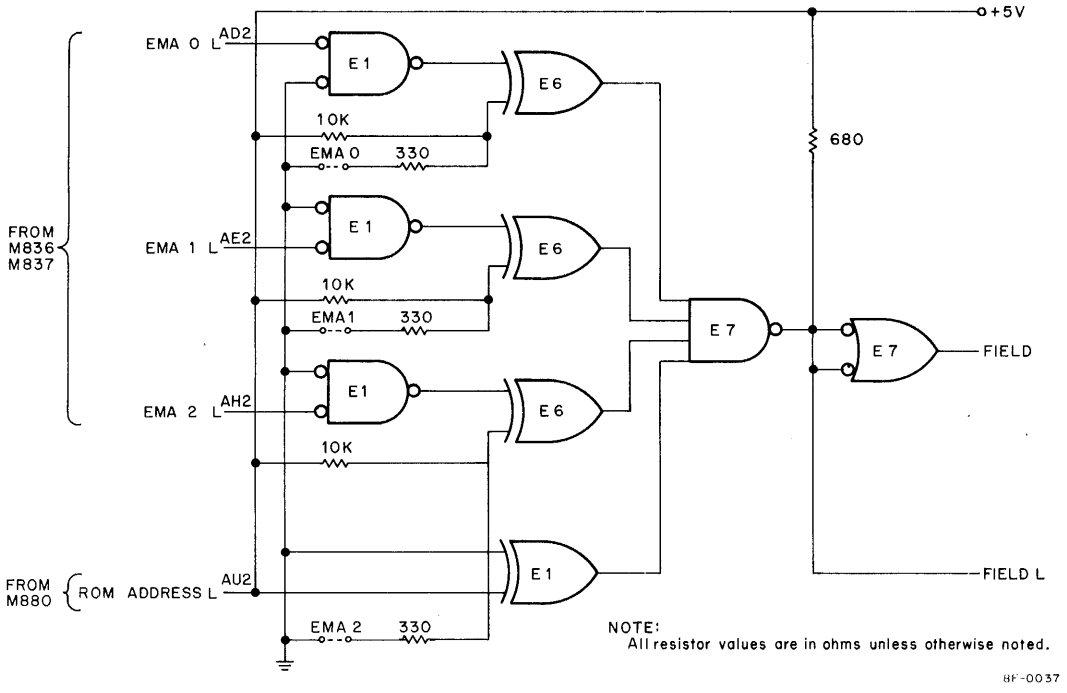


Figure 3-51 Field Select Control Logic

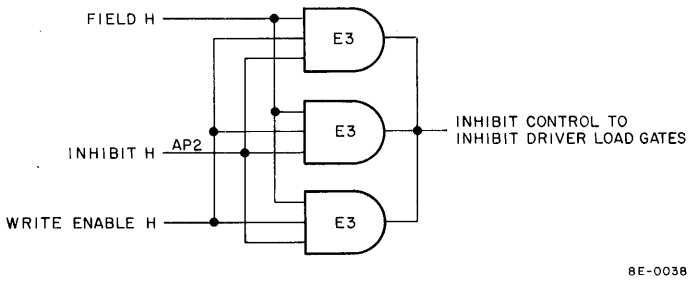


Figure 3-52 Inhibit Control Logic

3.27.6 Memory Register Enable Logic

The Memory Register Enable logic (Figure 3-53) functions when the contents of the Memory Register are to be gated onto the Inhibit Drivers and MD lines. When MD DIR L is low, the output of the control logic (READ) gates the content of the SENSE flip-flops to the MD BUS.

3.27.7 READ/WRITE Control Logic

The READ/WRITE Control logic (Figure 3-54) clears all SENSE flip-flops and enables the Inhibit Control logic.

The CLEAR L signal only becomes active when WRITE H is not active and RETURN H is asserted. This begins at the start of the READ portion of the memory cycle and continues for a period of approximately 50 ns. The CLEAR L signal becomes inactive when the E4 flip-flop is reset by the CLEAR L signal input.

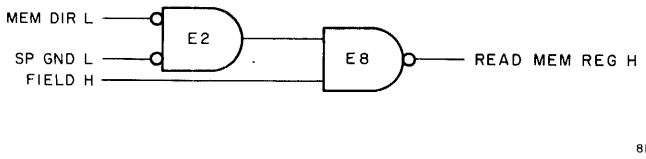


Figure 3-53 Memory Register Enable Logic

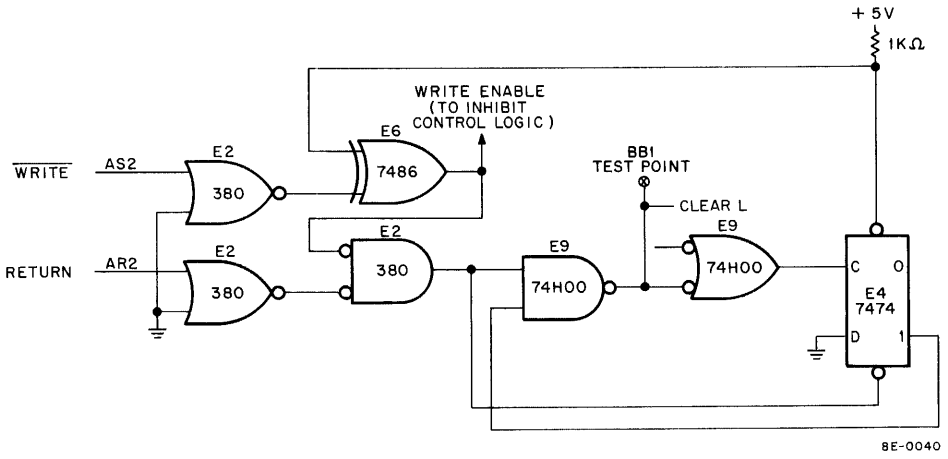


Figure 3-54 READ/WRITE Control Logic

3.27.8 Strobe Control Logic

The Strobe Control logic (Figure 3-55) is used to control the sample time of the Sense Amplifiers during the READ portion of the memory cycle. TIME STROBE occurs when WRITE L is not asserted, FIELD has been selected, and the STROBE timing signal from the Timing Generator has been received. STROBE is gated in and passed through an adjustable time-delay circuit. The flip-flop (7474) senses the rise and fall times of the strobe pulse and enables the output gate. The signal can be observed at test point CA1 (using a module extender).

3.27.9 Sense Amplifiers

Twelve Sense Amplifiers (Figure 3-56) are required to sense signals on the twelve sense lines. If the selected core in a given mat contains a 1, a pulse is received on the Sense/Inhibit winding. This pulse is amplified by the Sense Amplifier and then used to set a 1 into the Memory Register. If the selected core contains a 0, the signal received by the Sense Amplifier is small, and no pulse appears at the output of the Sense Amplifier; the Memory Register remains in the 0 state. The Sense Amplifier is "strobed" with a narrow pulse to ensure that the content of the sense lines is sampled at the proper time. This timing is necessary because the cores in the 0 state produce a small signal when "sensed" and because many of the cores in each mat receive half-selected pulses. The total sum of the noise can be considered a "delta noise", which appears at the early portion of the core selection time. The noise, generated by the half-selected cores, ceases shortly after the half-select pulses are started. Therefore, the Sense Amplifier is strobed during the latter part of the READ time, when the output resulting from a selected core-reversing state is highest in proportion to the noise from half-selected cores (maximum signal-to-noise ratio). Because the delta noise is confined to a smaller amplitude with respect to ground, the slice control ensures that any sampling of the 1 state occurs beyond the noise level amplitude. Thus, there are two methods of avoiding

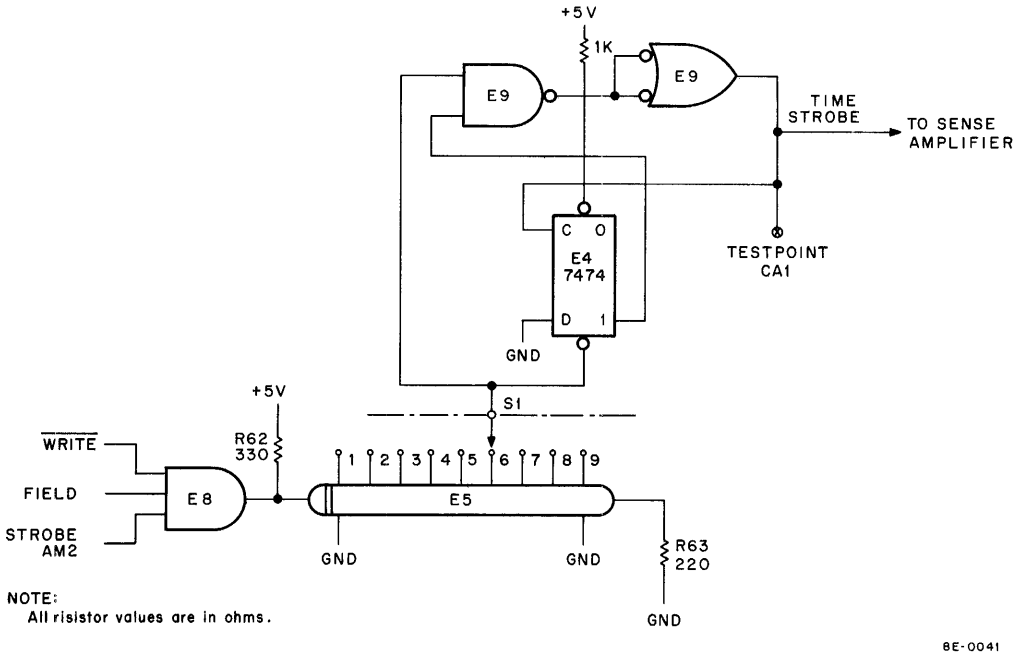
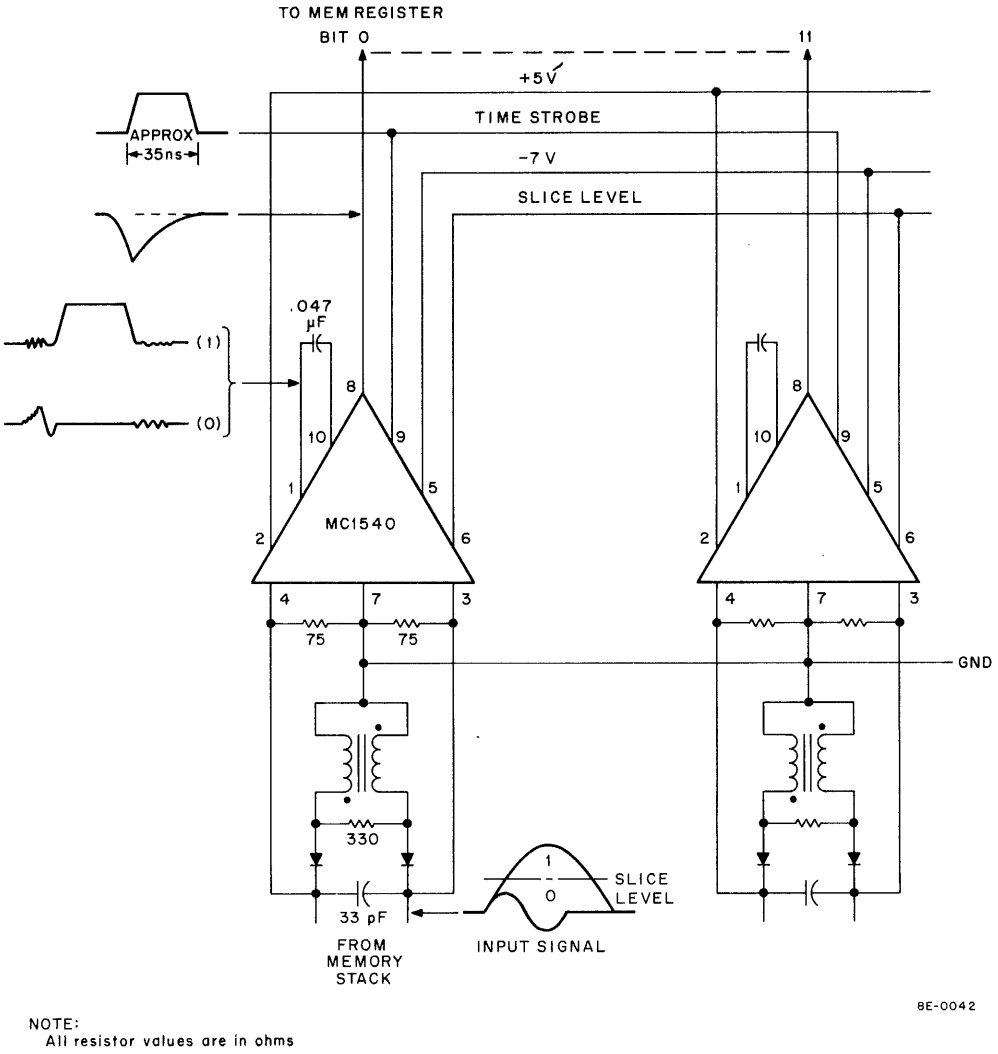


Figure 3-55 Strobe Control Circuit

the delta noise: (a) sample beyond the noise level amplitude, and (b) sample after the noise pulse. The delta noise is a direct function of the switching of the cores. For a 0, the Sense Amplifier senses a negligible change; a delta noise occurs but is not sensed, because STROBE is applied after the noise has settled down. STROBE is factory adjusted so that sampling clears the delta noise pulse, but does not clear it so far that the amplitude of a 1 is missed. This adjustment is in increments of 10 ns in a range of 30 to 40 ns. STROBE can be adjusted at the time-delay switch shown in Figure 3-55. However, the switch positions should not be changed until the diagnostic procedures indicate that STROBE timing is not properly synchronized. There are six distinct values on this switch in 10 ns increments. The switch is connected to a tapped delay line located on the Sense/Inhibit board. At CA1, a test point is available if any troubleshooting is necessary. The waveform is illustrated in Figure 3-56, corresponding to pin 9 of the Sense Amplifier; the sense line waveform at pin 10 is also shown. During the 1 state, the top portion is sliced off by the slice control input.

The balun transformer shown in Figure 3-56 performs an equalizing function for the inhibit currents during a WRITE operation. The Sense/Inhibit line is constructed so that one end of the wire is connected to one leg of the balun transformer, and the other end of the wire is connected to the other leg of the transformer. The inhibit output is tapped in the middle of this wire, thus forming a Y-type of connection. During the WRITE portion of the memory cycle, it is necessary to apply an equal amount of current through both legs of the Sense/Inhibit line. However, because the resistance on each leg is not exact (approximately 3Ω), it is possible to have 20 percent more current on one leg than the other. The balun transformer functions to make up the difference in current so that both legs are equalized. When the inhibit current is removed, a voltage backswing is prevented from entering the amplifier by the presence of the diodes. During the READ portion of the memory cycle, both ends of the diodes are at ground level and, therefore, back-biased. During the WRITE portion of the memory cycle, these diodes are forward-biased and, therefore, the transformer immediately begins balancing the currents.



NOTE:
All resistor values are in ohms

Figure 3-56 Sense Amplifiers

3.27.10 Memory Register

The Memory Registers (Figure 3-57) retain the information strobed out of the Sense Amplifiers until a CLEAR L signal is received during the first 50 ns of the next READ operation. The output gates, controlled by the READ MEM signal, drive 1s and 0s into the Inhibit Driver load gates. The flip-flops are termed "Sense flip-flops" and are set when there is a 1 (negative-going pulse) on the output of the corresponding Sense Amplifier. READ MEM is enabled only when MD DIR L is low.

3.27.11 Inhibit Driver Load Gates

The Inhibit Driver Load Gates (Figure 3-58) control the WRITE operation. During READ, the contents of the sense lines are placed on the MD lines. With FIELD (active) and INHIBIT (active), the contents of the MD lines are gated into the Inhibit Drivers. INHIBIT is generated in the Timing Generator only during the WRITE portion of the memory cycle.

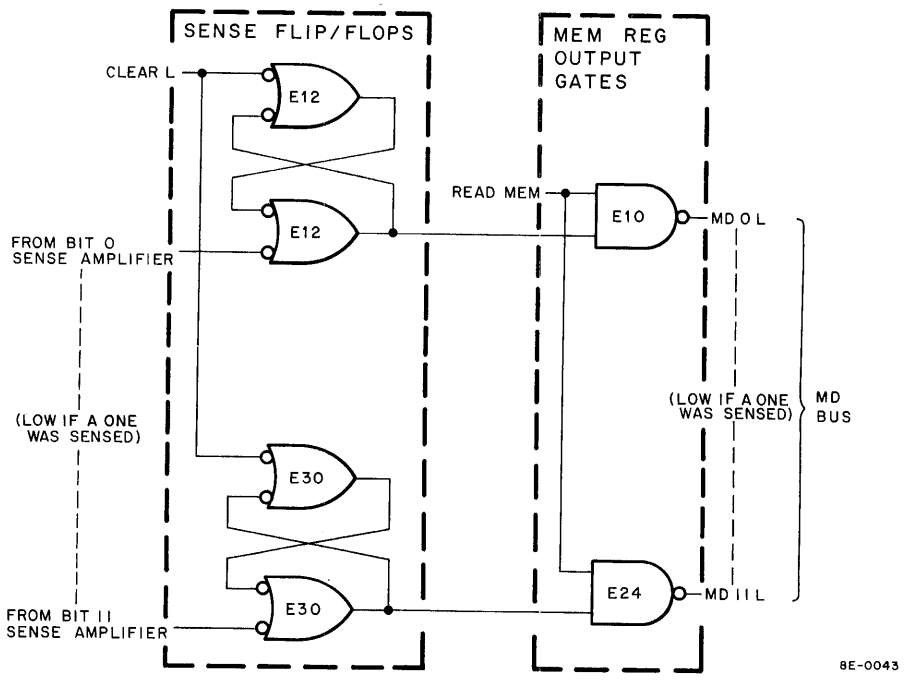


Figure 3-57 Memory Register

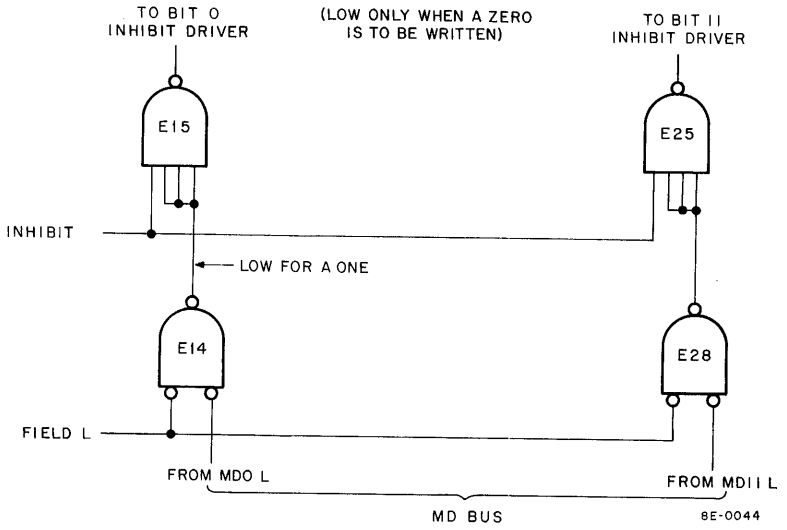


Figure 3-58 Inhibit Driver Load Gates

The MD lines receive data from the Sense flip-flops. When a FETCH or DEFER state is being processed, MD DIR L is made low and the memory cycle is a fast cycle (1.2 μs). This allows the content of the Sense flip-flops to be gated out to the Inhibit Driver load gates during WRITE and, subsequently, applied to the Inhibit Drivers. When data is to be written into memory from the MB Register, memory cycle timing is 1.4 μs and MD DIR L is high during the WRITE portion of the memory cycle. The Sense flip-flops are then made inactive, and the Inhibit Driver input gates look at only the MB Register. If data break is used, data is transferred immediately from a peripheral to the MB Register and gated into memory during the current memory cycle. During most other types of transfer operation, data must be transferred from the AC Register to the MB Register and applied to the Inhibit Driver input gates.

3.27.12 Inhibit Drivers

Inhibit Drivers (Figure 3-59) apply inhibit current to the selected core when a 0 is to be written. Each of the 12 drivers receives either a positive level (for a 1) or a ground input (for a 0) at the 1:1 input transformer. During a 0 output of any Inhibit Driver load gate, the transistor-base side of the transformer secondary is positive with respect to the emitter side. This forward bias turns the transistor on, allowing inhibit current to pass through and be applied to the selected core. Because the inhibit current direction is opposite to the write select current, a half-select condition results and the core remains in the 0 state. During a 1 output of any one Inhibit Driver input gate, the transistor-emitter at the same potential as the base and the transistor does not conduct. The full select current is then applied to the corresponding core, which results in a 1 state. The Inhibit Driver acts as a relay solenoid driver. It consists of an inductor, a resistor, and a switching transistor. When the transistor is turned on, the Inhibit line current is determined by the transistor emitter circuit. When the switch turns off, the energy stored in the inductor creates a back EMF that can damage the transistor circuit. The diode-to-ground at the collector output is used to protect the transistor from this unwanted backswing condition.

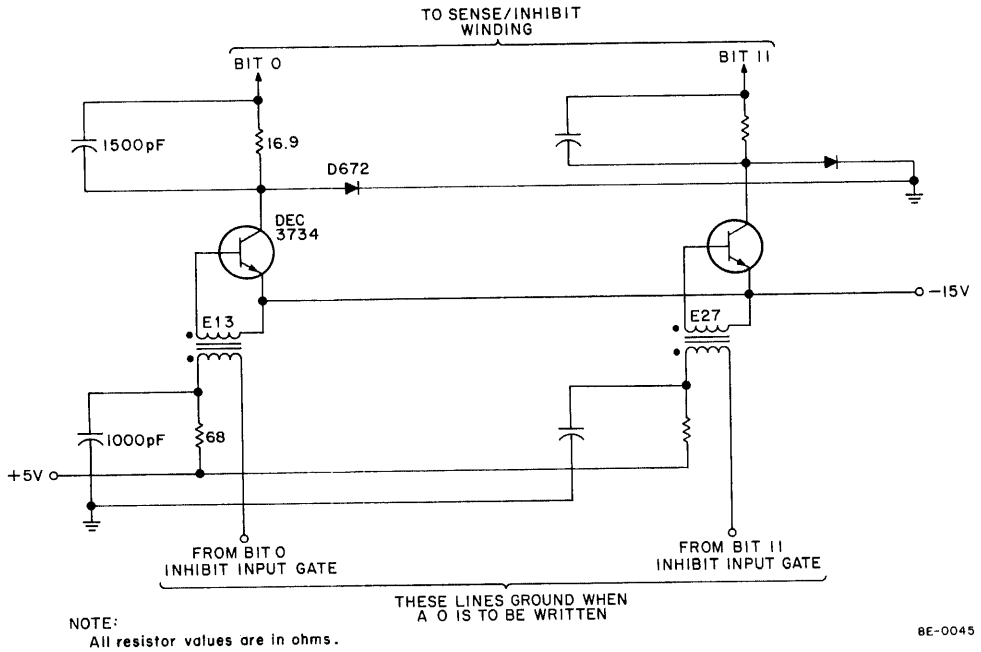


Figure 3-59 Inhibit Drivers

3.27.13 Current Control Circuit

The Current Control circuit (Figure 3-60) controls the current level in the X- and Y-select lines. The control circuit operates on a +5V and -15V supply. The output of the X- and Y-current sources (Figures 3-42 and 3-43) is a voltage-regulated supply that varies with temperature changes. The temperature sensing is accomplished by the thermistor, located on the memory stack board. The two jumpers are factory installed to control the preset X- and Y-current reference point.

3.27.14 -7V Supply and Slice Control Circuits

The -7V Supply and Slice Control circuits (Figure 3-61) provide a voltage slice level to the Sense Amplifier (Figure 3-56) and a regulated -5 Vdc output to the Sense Amplifier. The slice level is controlled by jumpers SLA and SLB, which are factory installed.

3.28 MEMORY TRANSFER CONTROL LOGIC

Memory transfer control is accomplished by signal MD DIR L. When MD DIR L is low, the content of the Memory Register, containing information from the READ operation, is gated out to the MD BUS. When MD DIR L is high, the content of the MB Register is gated out to the MD BUS for deposit in memory during the WRITE operation. When the processor directs memory to write back into memory the word retrieved during READ (manipulating signal MD DIR L), MD DIR L remains low during the WRITE operation. The content of the Memory Register is on the MD BUS; consequently, the same word is written back into memory. This procedure always applies during FETCH and DEFER (NON-AUTOINDEX).

3.28.1 Transfer Control During FETCH, DEFER, or EXECUTE States

The memory transfer control logic for FETCH, DEFER, or EXECUTE states is illustrated in Figure 3-62. A CLEAR L signal is generated by timing 100 ns after the start of TS1. This resets E19, which asserts MD DIR L. The flip-flop remains unchanged until TP2 is received as a clock input. If the major state is FETCH, a low will be clocked into the data input of the flip-flop, and E19 remains unchanged until TP2 of the next cycle. If the major state is DEFER (NON-AUTOINDEX), a low will be clocked into the data input of the flip-flop, and E19 remains unchanged. Thus, in both cases, the data from the Memory Register is re-deposited in memory.

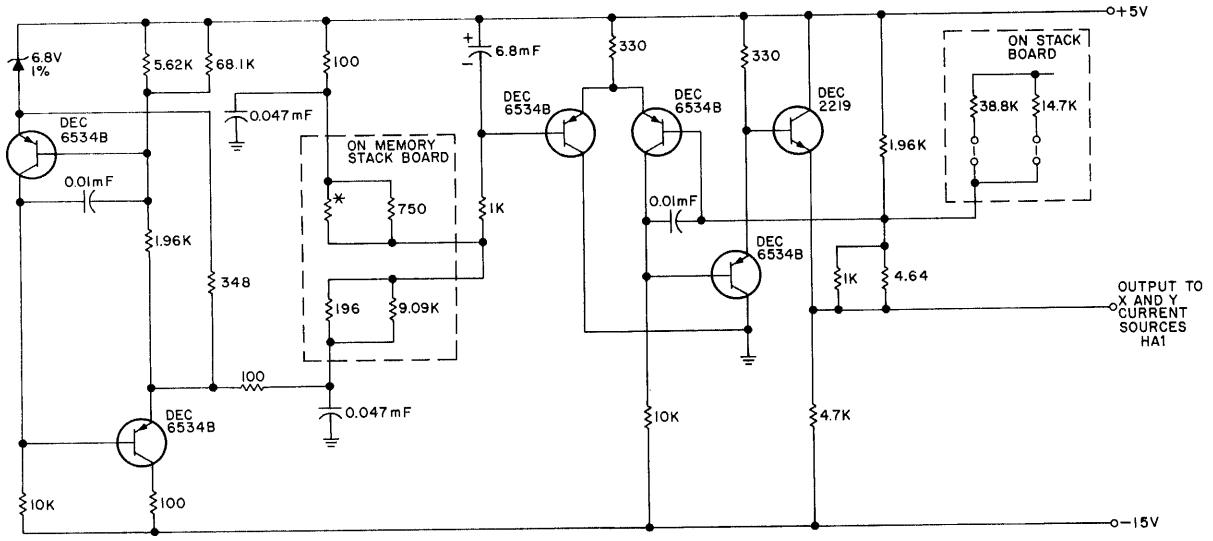
If the major state is DEFER and AUTOINDEX (MA0–7 L equals 0 and MA8 L equals 1), a high is clocked into the flip-flop, and E19 is set. A low into E27 causes MD DIR L to go high, and memory receives the data from the MB Register.

If the major state is EXECUTE, a high is clocked into the data input of the flip-flop, and E19 is set; this condition, as in the previous case, causes MD DIR L to be high.

3.28.2 DMA State, Manual Operation Transfer Control

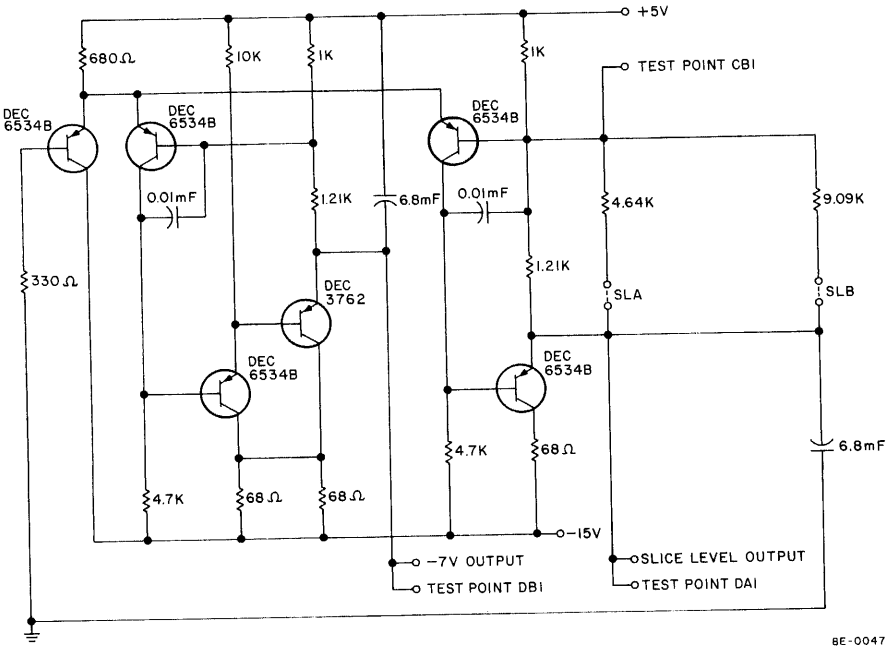
MD DIR L is high at TP2 unless pulled low by the Memory Transfer Control logic in the Programmer's Console (Figure 3-63).

Because FETCH or DEFER is not asserted, due to the DMA state, the Memory Transfer Control logic in the Timing Generator remains high, because no reset pulse is generated by timing. Either the LOAD ADDR or EXAM key, when depressed, will generate MD DIR L, which places the content of the Memory Register onto the MD BUS.



NOTE:
* Thermistor. 1K @ 25°C
All resistor values are in unless otherwise noted.

Figure 3-60 Current Control



NOTE:
Resistor values are in ohms unless otherwise noted.

Figure 3-61 -7V Supply and Slice Control Circuits

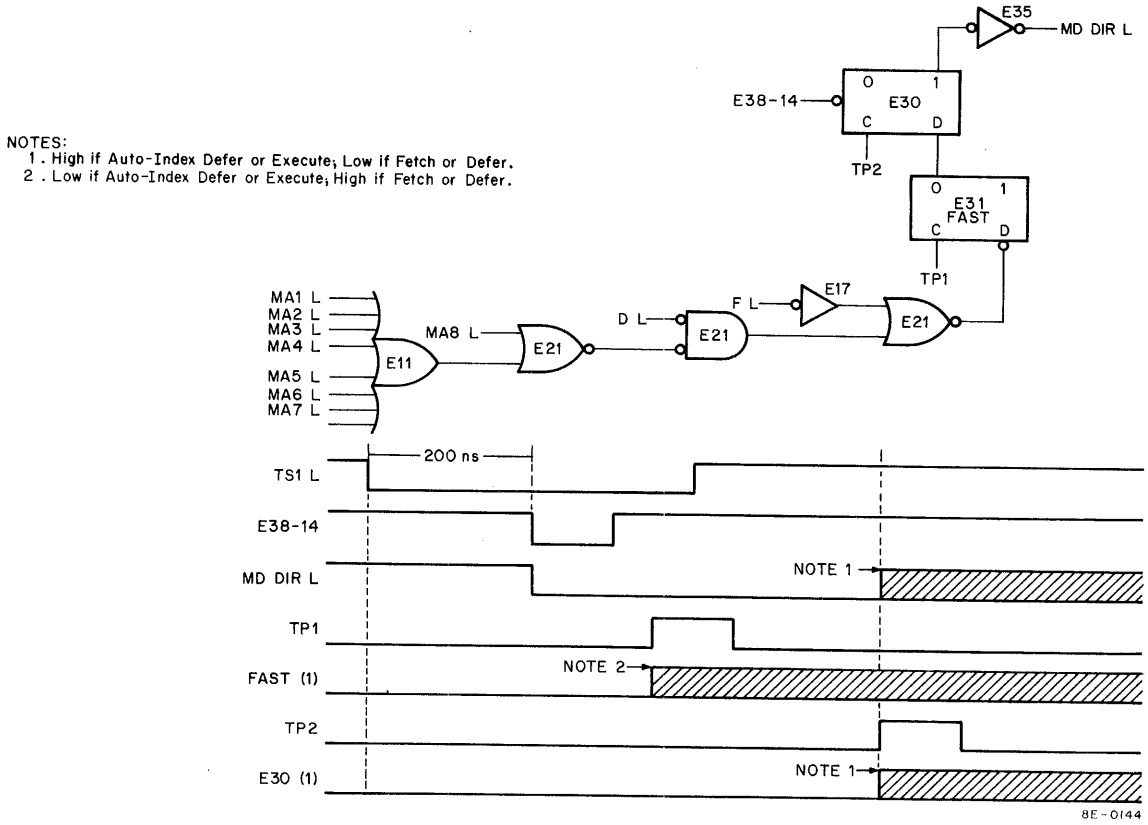


Figure 3-62 Memory Transfer Control Logic (FETCH, DEFER, or EXECUTE)

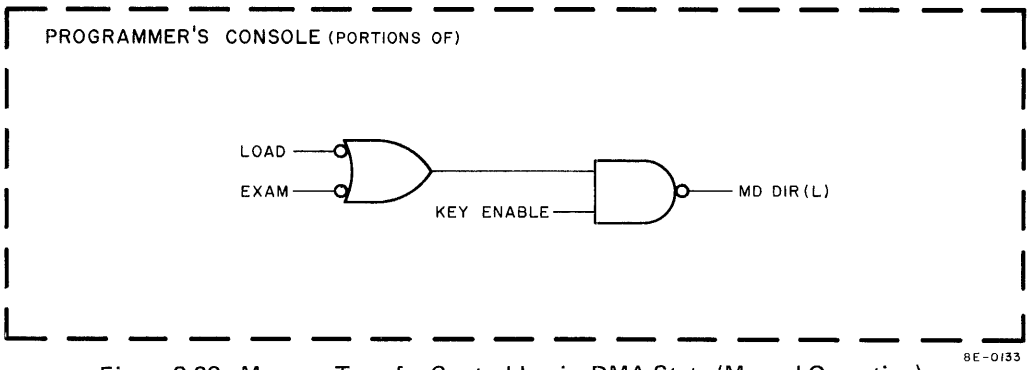


Figure 3-63 Memory Transfer Control Logic, DMA State (Manual Operation)

When data is deposited into memory, the data path is from the DATA BUS to the MB Register to memory. Thus, MD DIR L must go high so that the content of the MB Register can be gated out to the MD BUS.

3.28.3 DMA State, Data Break Operation

Each data break device contains Memory Transfer Control logic. MD DIR L will always be low except when:

a. Incrementing the word count (3-cycle data break device)

b. Incrementing the current address (3-cycle data break device)

c. Transferring data from the device to memory, or incrementing memory.

Refer to Volume 2, Chapter 10 of this manual for a detailed discussion of data break transfers.

SECTION 5 – CENTRAL PROCESSOR

3.29 CENTRAL PROCESSOR, GENERAL DESCRIPTION

The central processor unit (CPU) manipulates data in response to a predetermined sequence of instructions. In the PDP-8/E, both the data to be manipulated and the instructions are stored in memory. An instruction is brought from memory to the processor where it is decoded to determine, first, what to do to the data, and, second, what data is affected. When the data has been manipulated, the result is stored within the processor, transferred to a memory location, or transferred to some peripheral equipment. The CPU consists of the M8300 Major Registers module, and the M8310 Major Register Control module.

3.30 CENTRAL PROCESSOR, FUNCTIONAL DESCRIPTION

Figure 3-64 shows the functional breakdown of the CPU and should aid in understanding processor operation. To perform all the operations involved in retrieving, storing, and modifying information, the CPU utilizes the major registers, previously introduced. Data is transferred between registers, between registers and memory (via the OMNIBUS MD lines), between registers and peripherals (via the OMNIBUS DATA lines), and between registers and internal options. Transfers are accomplished by a major register gating network, which selects the particular register that takes part in the transfer and performs some operation on the data being transferred. The selection and operation performed are determined by control signals developed within the Major Register Control logic. This logic also provides control signals that determine the destination of the transferred data.

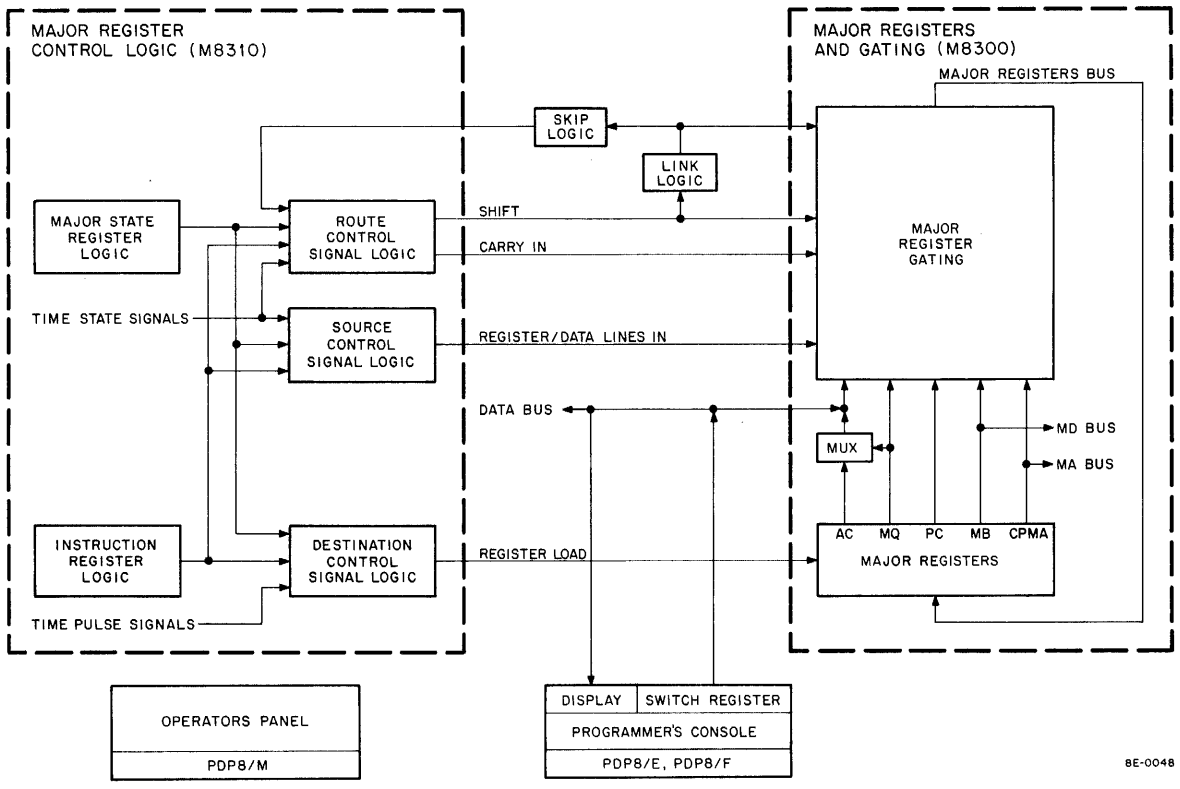


Figure 3-64 Block Diagram, Central Processor Unit

The signals that control the registers and their gating are developed within the Major Register Control logic. The signals are developed largely in response to three variables: (a) basic instructions (as decoded by the Instruction Register logic), (b) processor major states (as determined by the Major State Register logic), and (c) time states and time pulses. These variables are combined to produce control signals that make the major register gating network function. For convenience, these signals are grouped according to function. Thus, source control signals select the register that contains the data to be operated on; route control signals determine what is done to the data, and then place the result on the MAJOR REGISTERS BUS; finally, destination control signals load the result into the selected register.

Two other logic groupings are the Skip logic and the Link logic. Both logic blocks utilize timing signals, major state signals, and instruction signals, among others, to carry out operate microinstructions. The LINK, itself, is used to extend AC Register arithmetic capability. As shown, the LINK can be applied to the major register gating in response to shift signals. It is also used to initiate Skip logic in response to certain operate microinstructions. The Skip logic, in carrying out various microinstructions, is used primarily to generate the Carry In route control signals.

The Programmer's Console, although not physically part of the CPU, is functionally inseparable. The operator can communicate with the major registers and cause data transfers to occur by operating various front panel keys. Data is transferred between the console and the processor on the DATA lines, in response to control signals generated within the console logic (Figure 3-64). If an Operator's Panel is used instead of the Programmer's Console, the operator has no control over the processor. He can turn power on at the front panel, and he can cause memory and processor timing to begin, provided certain options are connected to the OMNIBUS.

Each functional group is discussed, in detail, in succeeding sections. Expressions of the form PC → MA were introduced earlier. The quantities to the left of the arrow represent the source data. This data is transferred to the destination indicated on the right of the arrow. Source data is produced during a time state, either by a time state signal itself (TS3) or by a composite that includes the time state signal (DCA•E•TS3). Source data is loaded into the destination by the time pulse that corresponds to this time state signal, or by a composite that includes the time pulse. Thus, source data produced during TS3 is loaded into its destination at TP3. This information will aid in understanding processor operation.

3.31 FRONT PANEL OPERATIONS

The front panel of the basic computer can incorporate a Programmer's Console or an Operator's Panel, the latter usually finding greater application with OEMs. In either case, the respective module contains keys and switches, indicating devices, and the logic that drives the controls and indicators. The controls protrude through slots in the silk-screened front panel; the indicators are visible at designated spots on the panel.

The PDP-8/M Operator's Panel, KC8-M, is described in Paragraph 3.32. The PDP-8/E and the PDP-8/F Programmer's Consoles, KC8-EA and KC8-FL, respectively, are described in Paragraph 3.33. Information concerning the types of front panels available with each system can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

3.32 KC8-M OPERATOR'S PANEL

The Operator's Panel is used with the PDP-8/M (Figure 1-4). Unlike the Programmer's Console, the Operator's Panel printed circuit board does not plug into the OMNIBUS. Instead, it is hardware-mounted to the front panel and connected to the OMNIBUS by a connector/harness assembly. Only the SW switch, an integrated circuit, two resistors, and a capacitor are mounted on the printed circuit board. The light-emitting diodes (LEDs) that indicate POWER and RUN are mounted directly on the front panel.

Figure 3-65 represents the Operator's Panel printed circuit board and the connections to the OMNIBUS. Part of the ON/OFF microswitch wiring is also shown. P1 of the OMNIBUS harness assembly connects to J1 of the printed circuit board. When the power is on, the POWER LED will glow. When the RUN L signal is low, indicating that the Timing Generator is producing memory and CPU timing signals, the RUN LED will glow. When a KC8-M Operator's Panel is used, the Timing Generator cannot be turned on at the front panel unless an MI8-E Bootstrap Loader option is included in the system. If such a module is plugged into the OMNIBUS, the operator can start the Timing Generator by depressing and lifting the SW switch. If a KP8-E Power Fail and Auto-Restart option is included in the system, the Timing Generator can be turned on merely by turning the microswitch to ON.

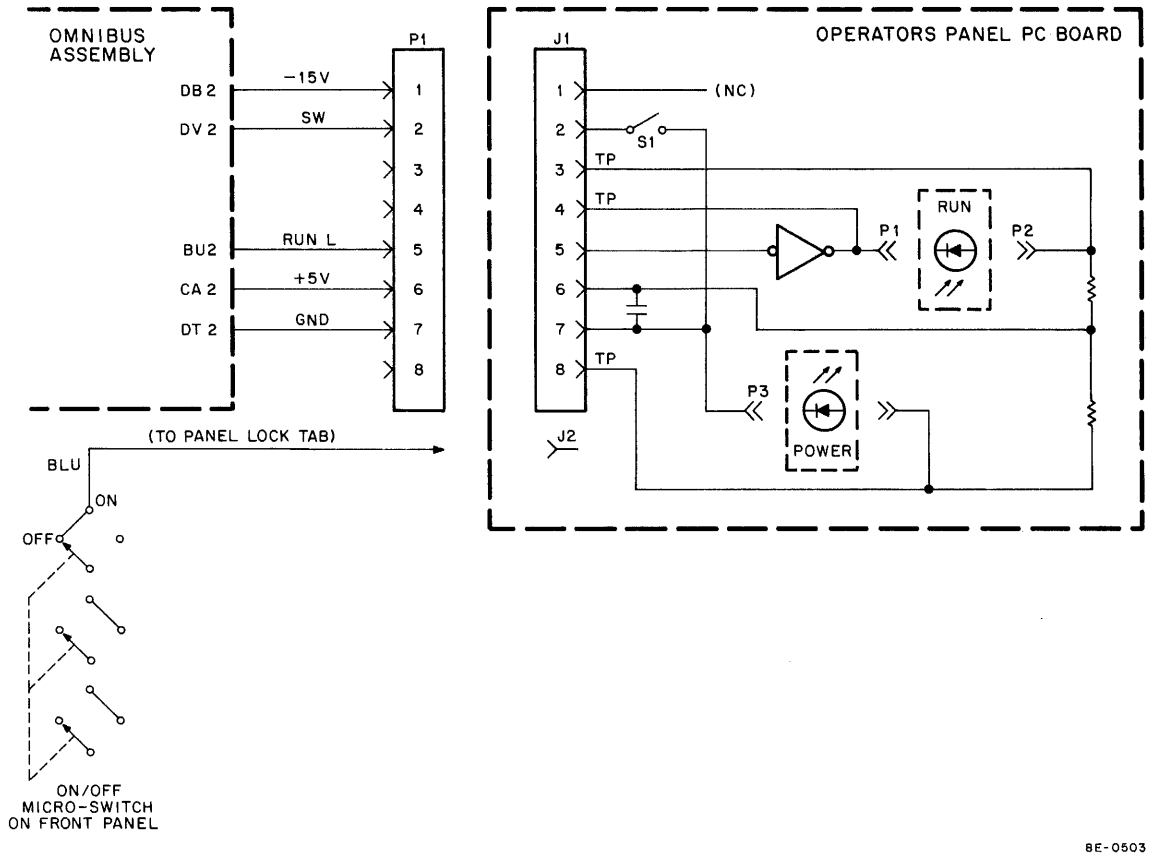


Figure 3-65 KC8-M Operator's Panel Logic

Note that a tab, labeled J2, is included on the Operator's Panel printed circuit board. This tab accommodates a spade lug that is connected by a wire to one section of the ON/OFF microswitch. This wire has no significance to a KC8-M and J2 is provided only in the interest of good housekeeping. However, a PDP-8/M can be equipped with a KC8—ML Programmer's Console (identical to the KC8-FL). In this case, the wire referred to is quite important. Figure 3-66 shows the OMNIBUS harness assembly and P1. When the KC8-ML is used, J1 of the microswitch harness assembly connects to P1. The spade lug on the end of the blue wire connects to the panel lock tab on the Programmer's Console. When the OFF/POWER/PANEL LOCK microswitch is in the POWER position, the - 15V supply is connected to the console. In the PANEL LOCK position, the voltage is removed from the console, and switches, controls, and indicators (except the RUN indicator) are inoperative.

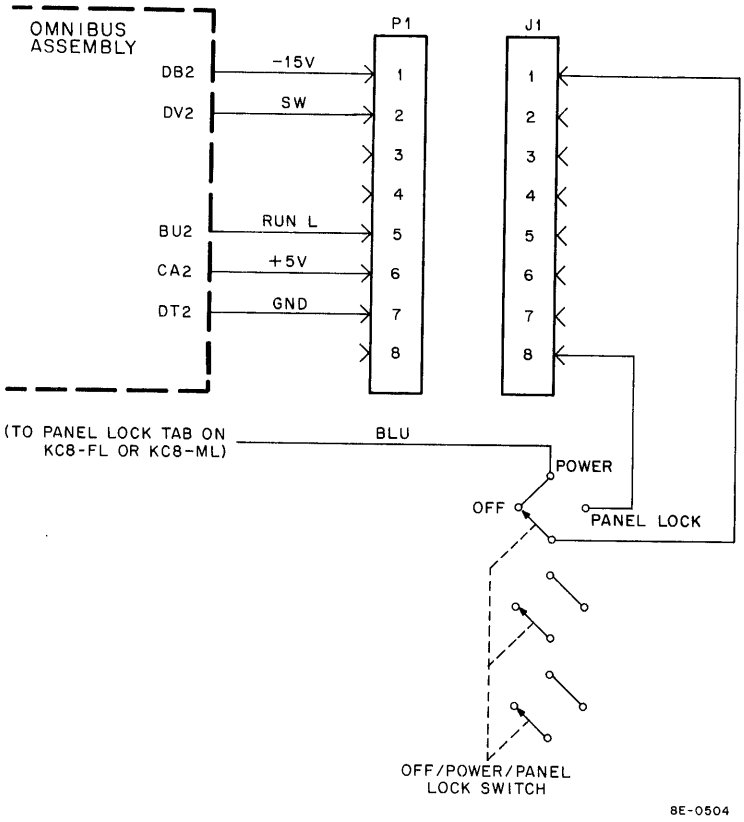


Figure 3-66 PDP-8/M Panel Lock Wiring

3.33 PROGRAMMER'S CONSOLE, GENERAL DESCRIPTION

Figure 3-67 is a block diagram of the two major functions of the KC8 Programmer's Console: manual operation and display. The display enables the operator to monitor the content of certain processor major registers, as well as the state of many of the OMNIBUS signal lines. Manual operation enables the operator to load programs into memory, initiate and halt automatic operation of the computer, and perform specialized tasks, which are discussed in subsequent sections.

As shown in Figure 3-67, the manual operations can be divided into a number of subordinate functions for convenience. Thus, several keys are grouped under the heading "manual start" to indicate that these keys initiate a timing cycle. Two switches, SING STEP and HALT, can be used to stop operation and are grouped under the heading "manual stop". The flow diagram, Figure 3-68, relates the manual functions to the processor time states.

The logic that makes manual operation and display possible is contained on the Programmer's Console module. The logic of the PDP-8/F Programmer's Console, KC8-FL, is simpler than that of the PDP-8/E Programmer's Console, KC8-EA (an earlier version of the KC8-FL uses logic that is similar to that of the KC8-EA; this version, which is not detailed in this manual, has been improved on the current model). The KC8-EA is described in Paragraph 3.33.1; the KC8-FL is described in Paragraph 3.33.2.

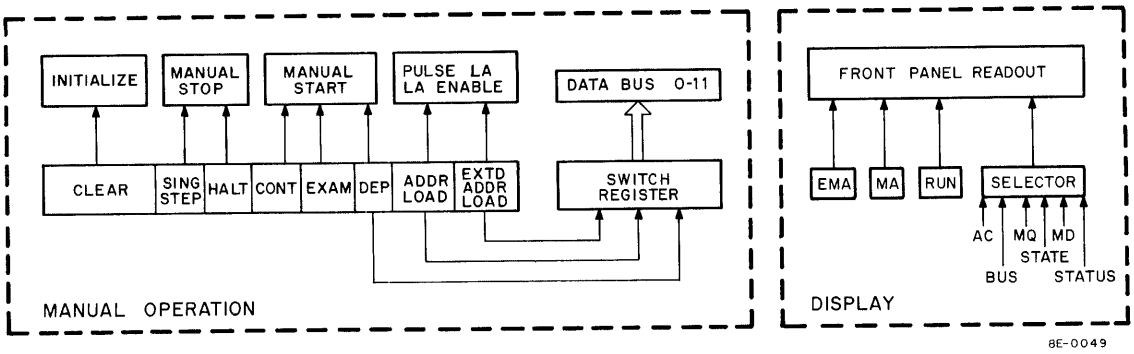


Figure 3-67 Programmer's Console, Block Diagram

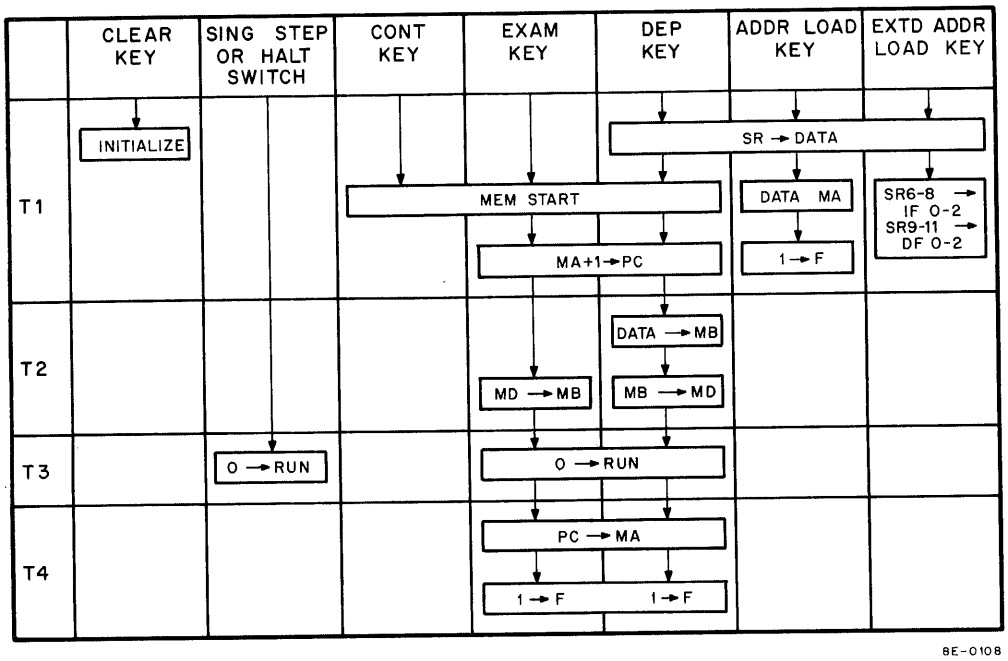


Figure 3-68 Manual Operation Function, Flow Diagram

3.33.1 KC8-EA Programmer's Console

3.33.1.1 Manual Operation

Switch Register — The switch register consists of 12 switches that enable the operator to load the processor CPMA Register with a 12-bit memory address, to deposit a 12-bit data word in a selected memory location, and to load the extended address bits, if more than 4K of memory is used. To carry out these functions, the switch register is operated in conjunction with the DEP, ADDR LOAD, and EXTD ADDR LOAD keys, as indicated on the block diagram.

Figure 3-69 illustrates the logic and circuits used to set data into the switch register and to place it on the DATA 0–11 lines; the circuit used with switch register bit 0 is shown in detail. If switch S11 is open (in the up position on the front panel), a positive voltage is applied to one input of NAND gate E25. If a positive enabling voltage is

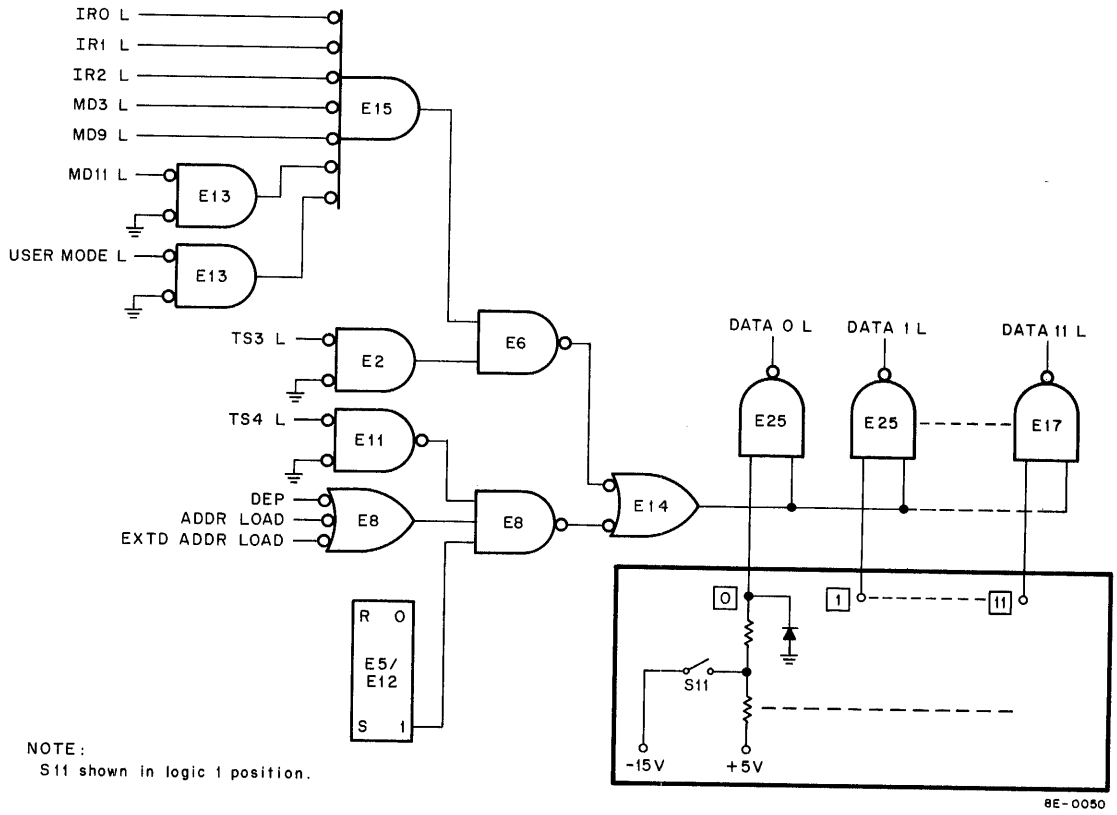


Figure 3-69 Switch Register Control Logic

applied at the other input, the DATA 0 line will go to ground, thereby indicating a logic 1. When the switch is closed, the diode in the circuit begins conducting. The resulting voltage drop across the diode takes the diode cathode below ground potential, inhibiting the NAND operation. The DATA 0 line remains at a positive voltage level, indicating a logic 0.

The NAND operation of E25 can be enabled by NOR gate E14 in either of two ways: (a) If the machine is stopped, the DEP, LOAD, or EXTD ADDR LOAD key can be activated. This action enables gate E25 and all of the other enable gates. (The DATA lines are reserved during TS4 for priority checking by peripherals; NANDing TS4 L ensures that no switch register information appears on the DATA lines during this time state.) (b) The OSR (inclusive OR, switch register with AC) instruction or the LAS (load AC with switch register) instruction can be issued, thereby enabling the gates at TS3, provided the USER MODE line has not been asserted by the KM8-E Memory Extension and Time Share option.

ADDR LOAD Key and EXTD ADDR LOAD Key – The ADDR LOAD key is used to load the CPMA Register with the memory address specified by the switch register. When the operator depresses this key, switch register information is placed on the DATA 0–11 lines. At the same time, LA ENABLE L and MS, IR DISABLE L are asserted. These two control signals enable a path for the DATA lines through the adder network to the MAJOR REGISTERS BUS. The PULSE LA signal is then asserted. This signal produces the CPMA LOAD L pulse, which loads the CPMA Register with the information on the DATA 0–11 lines. The memory location specified by the CPMA Register can then be operated on by the DEP key or the EXAM key.

Note, in Figure 3-68, that the ADDR LOAD key does not initiate a timing cycle. The purpose of this key is to establish a memory location at which some operation will take place. If a timing cycle is initiated, the CPMA address is incremented, and the operation takes place at the desired address plus 1. Thus, to avoid confusion, ADDR LOAD does not initiate a timing cycle.

The EXTD ADDR LOAD key, likewise, does not initiate a timing cycle. This key is used to load switch registers bits 6–11 into the Instruction Field (IF) and Data Field (DF) Registers of the KM8-E Memory Extension and Time Share option (bits 0–5 of the switch register are used for IOT designation and device selection code). When the operator depresses the EXTD ADDR LOAD key, the switch register information is placed on the DATA 0–11 lines. The LA ENABLE L and KEY CONTROL L signals are asserted, providing a path to the KM8-E option for the DATA 6–11 lines. The PULSE LA signal is then asserted, and the DF and IF Registers are loaded with the extended address information. The address specified by the CPMA Register and the DF and IF Registers can then be operated on by other keys.

Figure 3-70 shows the logic used by the ADDR LOAD and EXTD ADDR LOAD keys. When either key is depressed, NOR gate E14A is enabled. If the RUN L signal is negated, NAND E12A is also enabled (if RUN L is asserted, the computer is in automatic operation; E12A ensures that this operation is not inadvertently interrupted by key action). R/S flip-flop E5/E12, which is reset by INITIALIZE or by a previous TP4 pulse, is set when NAND E12B is enabled. The 1-side of the flip-flop is NANDed with positive voltage levels produced by key closure. Thus, LA ENABLE L, MS, IR DISABLE L, KEY CONTROL L, and SR → DATA are produced (note that LA ENABLE L asserts IND1 L and negates IND2 L, removing AC, MQ, or STATUS words from the DATA lines).

When NAND E12A is enabled, the block designated "pulse processor and delay network" also receives an initiating signal. This block, representing a noise filter, a differentiator, and a delay circuit, is discussed in detail in Paragraph 3.33.1.2. Essentially, the network generates a noise-free logic gate of 400 ns duration when activated. The start of the gate is delayed approximately 20 ms from the time the key is depressed, thus filtering out contact noise and allowing preliminary operations to be completed before PULSE LA is generated. The gate is NANDed with the positive voltage level that results from key closure. The amount of time that the key remains closed is indeterminate, being a result of operator action; however, it is much longer than the gate duration. Thus, PULSE LA is asserted for 400 ns.

DEP Key – If the operator wants to deposit data in a particular location of the basic 4K memory, he first loads the address into the CPMA, as described above. Then he sets the switch register switches to correspond to the data to be deposited, and lifts the DEP key. As the flow diagram in Figure 3-68 shows, the switch register data is placed on the DATA 0–11 lines. At the same time two control signals, MS, IR DISABLE L and KEY CONTROL L, are asserted. KEY CONTROL L selects the MA lines for gating into one leg of the adder network, while MS, IR DISABLE L provides an arithmetic 0 at the other adder input. KEY CONTROL L also asserts the CAR IN L signal, thus incrementing the CPMA Register. Some milliseconds later, MEM START L is asserted, the RUN flip-flop is set, and a timing cycle begins. At TP1 time the PC Register is loaded with the next consecutive memory address (note that the nonincremented address remains in the CPMA Register until TP4 of the cycle).

During TS2 of the timing cycle, the adder control signals enable a path through the adder network for the DATA 0–11 lines, adding an arithmetic 0 to each DATA bit. The switch register information is placed on the MAJOR REGISTERS BUS and loaded into the MB Register at TP2 time. This same TP2 pulse causes the MD DIR L signal to be negated, placing the MB Register data on the MD 0–11 lines. The data is then read into the memory location specified by the content of the CPMA.

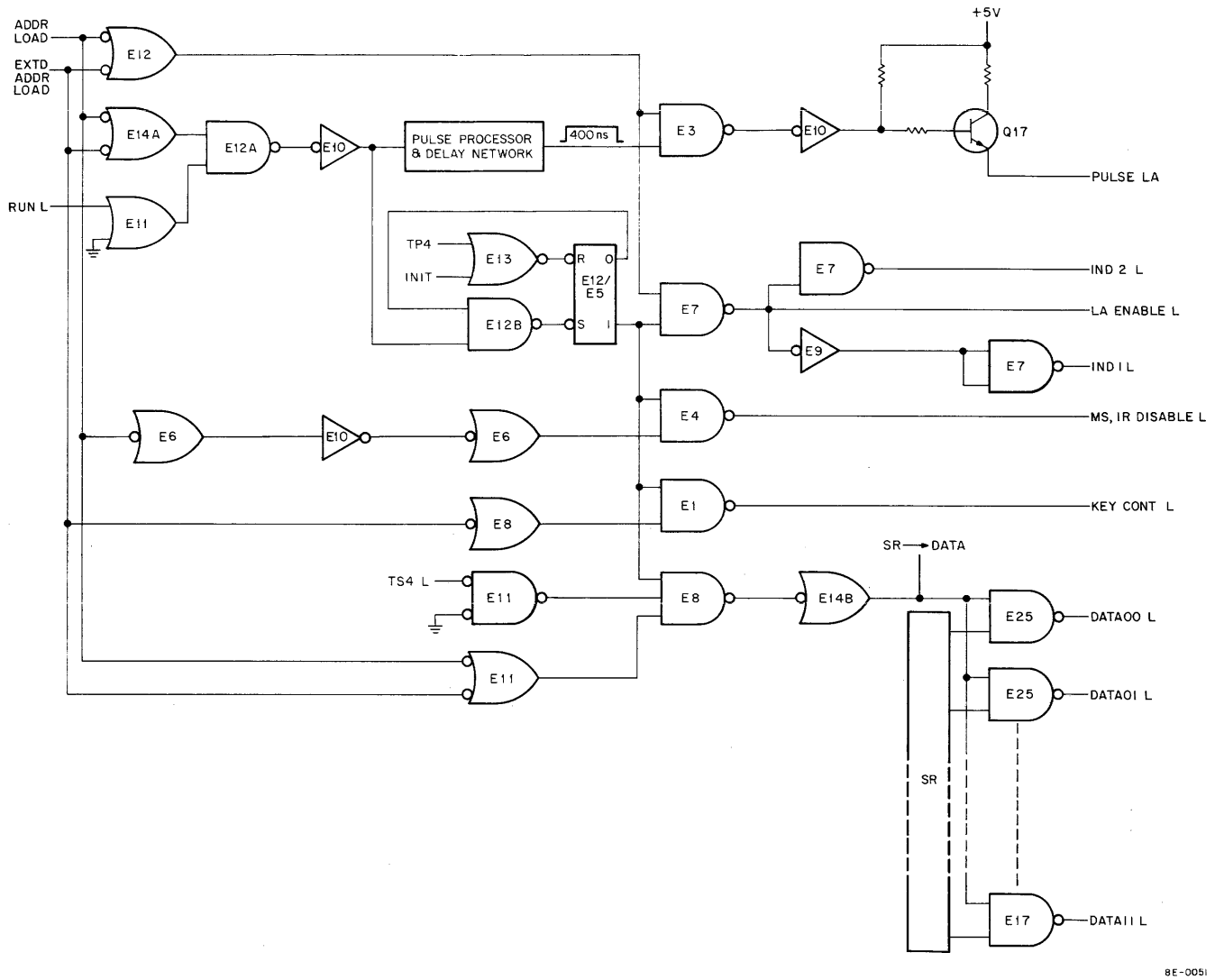


Figure 3-70 LOAD and EXTD LOAD Keys

At TP3 time, the KEY CONTROL L signal generates a STOP L signal, which resets the RUN flip-flop. The timing continues through TS4 and TP4 to halt in TS1 of some as yet unspecified cycle. Before completion of the cycle, one other operation is performed. The consecutive address must be transferred from the PC Register to the CPMA Register. Thus, the PC is gated to one leg of the adder, a 0 is added to each bit, and the new address is placed on the MAJOR REGISTERS BUS and loaded into the CPMA Register at TP4. The cycle then ends.

Figure 3-71 shows the logic used when a timing cycle is initiated by the DEP key. Again, flip-flop E5/E12 is set, provided that the RUN L signal is negated. The 1 side of E5/E12 is NANDed with positive voltage levels produced by the key closure, thereby asserting KEY CONTROL L, MS, IR DISABLE L, and SR → DATA. After the 20 ms delay, a 400 ns MEM START L signal is produced, which sets the RUN flip-flop. KEY CONTROL L enables TP3 to reset the RUN flip-flop; thus, only one cycle is produced.

EXAM Key – The EXAM key also initiates a timing cycle. By depressing this key, the operator can cause the contents of a selected memory location to be brought from memory and loaded into the MB Register. Except for the absence of SR → DATA, TS1 operations are identical to those of the DEP key. KEY CONTROL L and MS, IR DISABLE L are asserted. However, the EXAM key asserts two signals that are not needed by the DEP key and, therefore, TS2 operation is different. MD DIR L and BRK DATA CONT L are the additional signals. BRK DATA CONT L gates the MD lines to the adder network, where a 0 is added to the data being brought from the memory location. The MD bits are placed on the MAJOR REGISTERS BUS and loaded into the MB Register at TP2 time. The operator can monitor the contents of the MD lines by selecting the MD position with the front panel function selector switch. The data in the examined location can be modified by using the switch register and the DEP key. However, the EXAM cycle increments the PC Register to set up the next sequential memory address; therefore, to modify the data in an examined location, the switch register and ADDR LOAD key must be used to return to the correct address.

Figure 3-72 shows the EXAM key logic. This logic differs from the DEP logic only in the deletion of the SR → DATA enabling gate and the addition of enabling gates for MD DIR L and BRK DATA CONT L.

CONT Key – The CONT key also initiates a timing cycle by generating MEM START L. This is an important function because this is the only key that initiates repetitive timing cycles. Thus, the operator can begin automatic operation only by depressing the CONT key. Figure 3-73 shows the logic used to implement this function.

CLEAR Key – The last key on the Programmer's Console is the CLEAR key. As the flow diagram indicates, a timing cycle is not initiated. The logic diagram, Figure 3-74, shows that this key generates a 400 ns INITIALIZE signal. This signal clears the AC, LINK, and all peripheral flags.

SING STEP Switch and HALT Switch – The PDP-8/E can be stopped manually by either the SING STEP switch or the HALT switch. The logic is shown in Figure 3-75. Either switch enables TP3 to reset the RUN flip-flop, ending the generation of timing cycles. Both switches produce the STOP L signal, which is NANDed with TP3 in the timing logic. The resulting pulse resets the RUN flip-flop. If the SING STEP switch is used, the timing cycle halts at the beginning of the next TS1. However, the HALT switch produces the STOP L signal only when F SET L is asserted. Because F SET L is asserted only when the next machine cycle is to be a FETCH cycle, the processor completes an entire instruction before halting in TS1. The operator can use these switches, with the CONT key, to step a program one cycle or one instruction at a time.

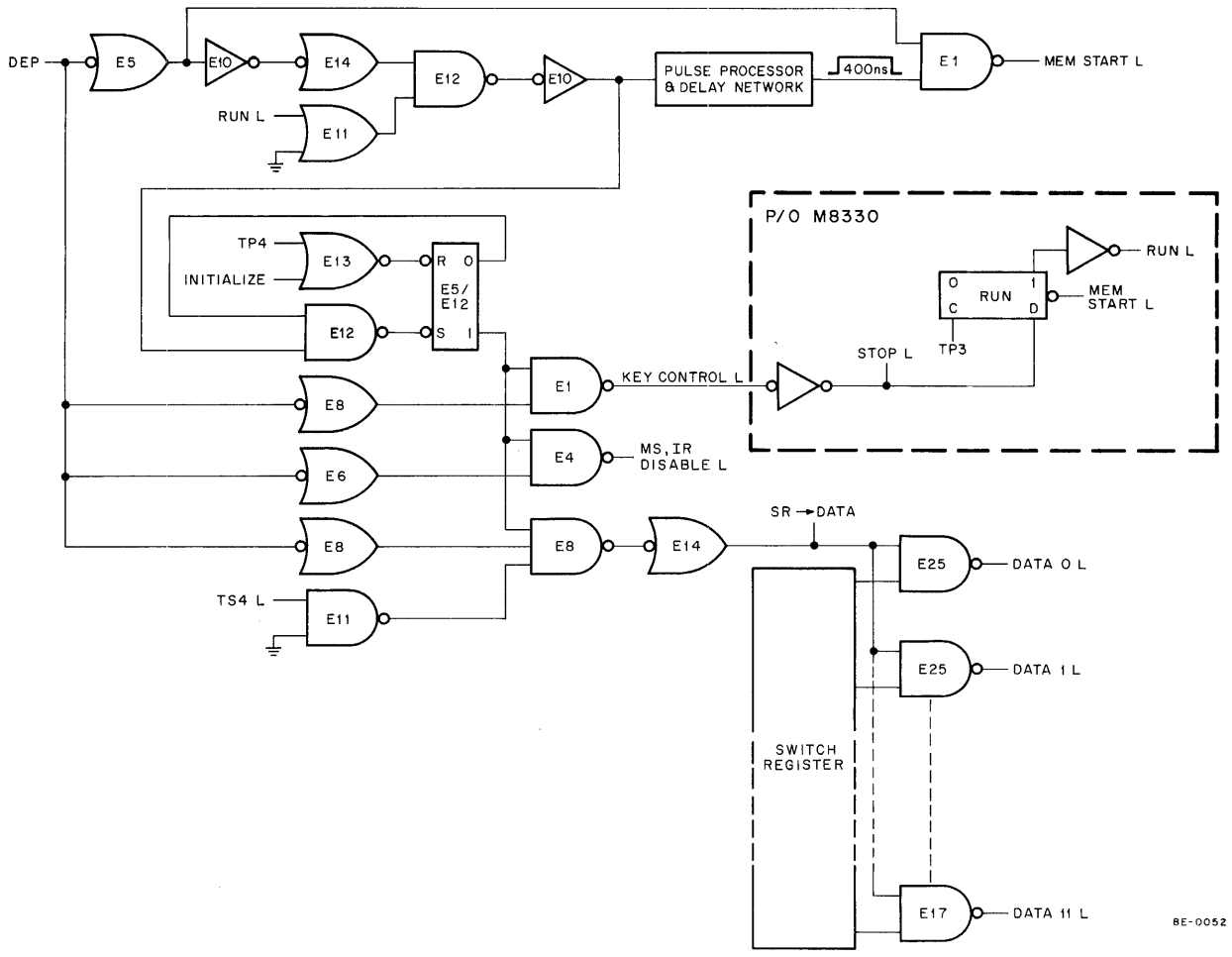


Figure 3-71 DEP Key Logic

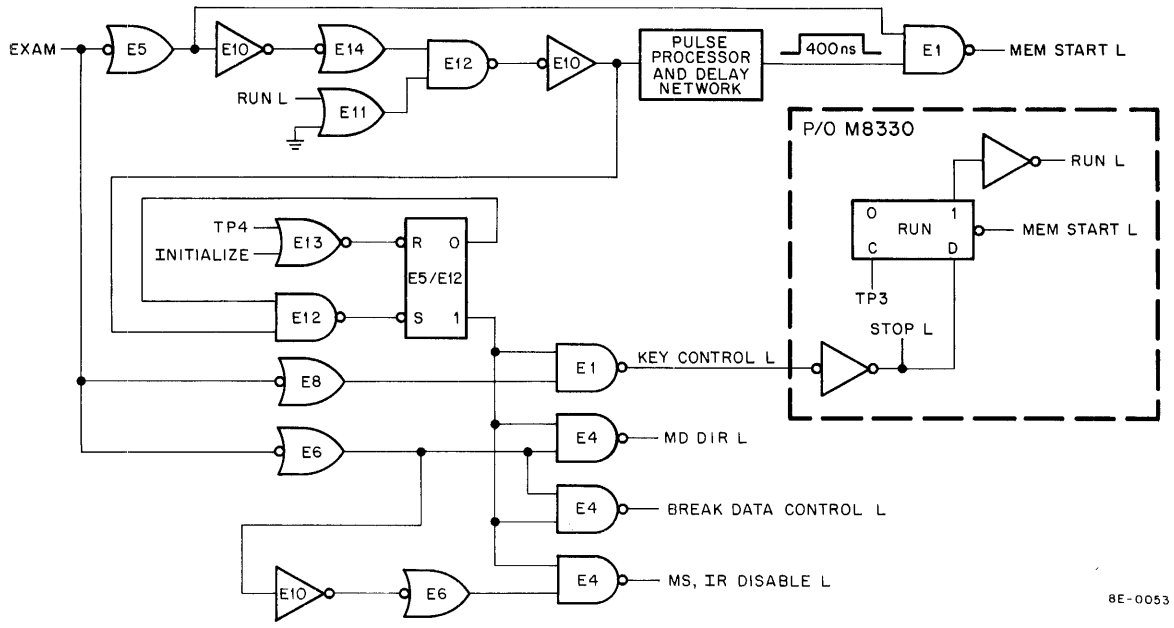


Figure 3-72 EXAM Key Logic

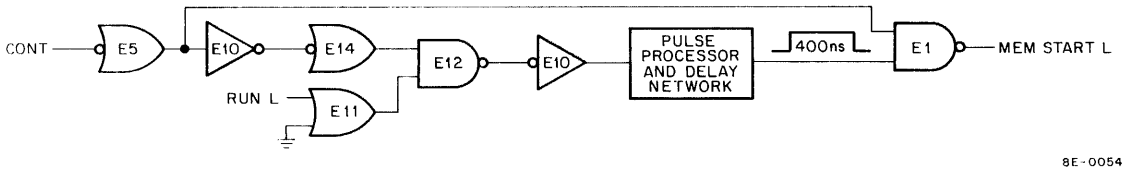


Figure 3-73 CONT Key Logic

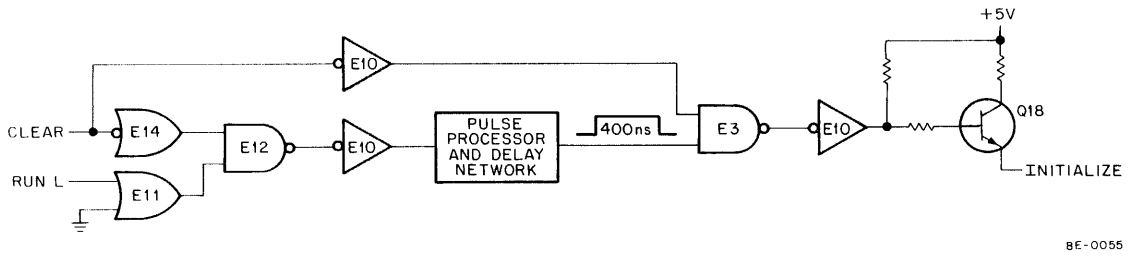


Figure 3-74 CLEAR Key Logic

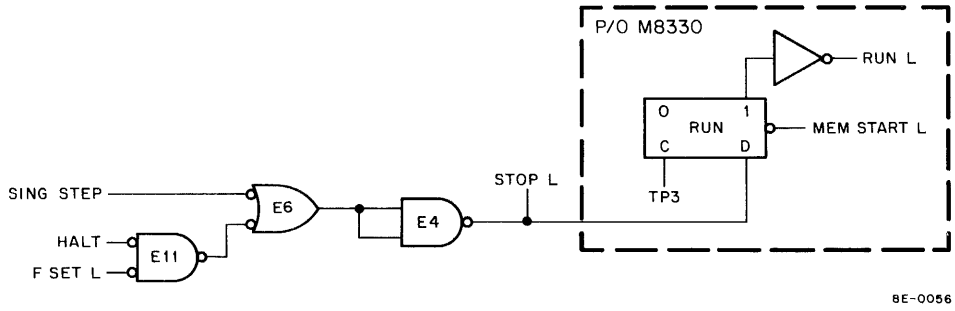
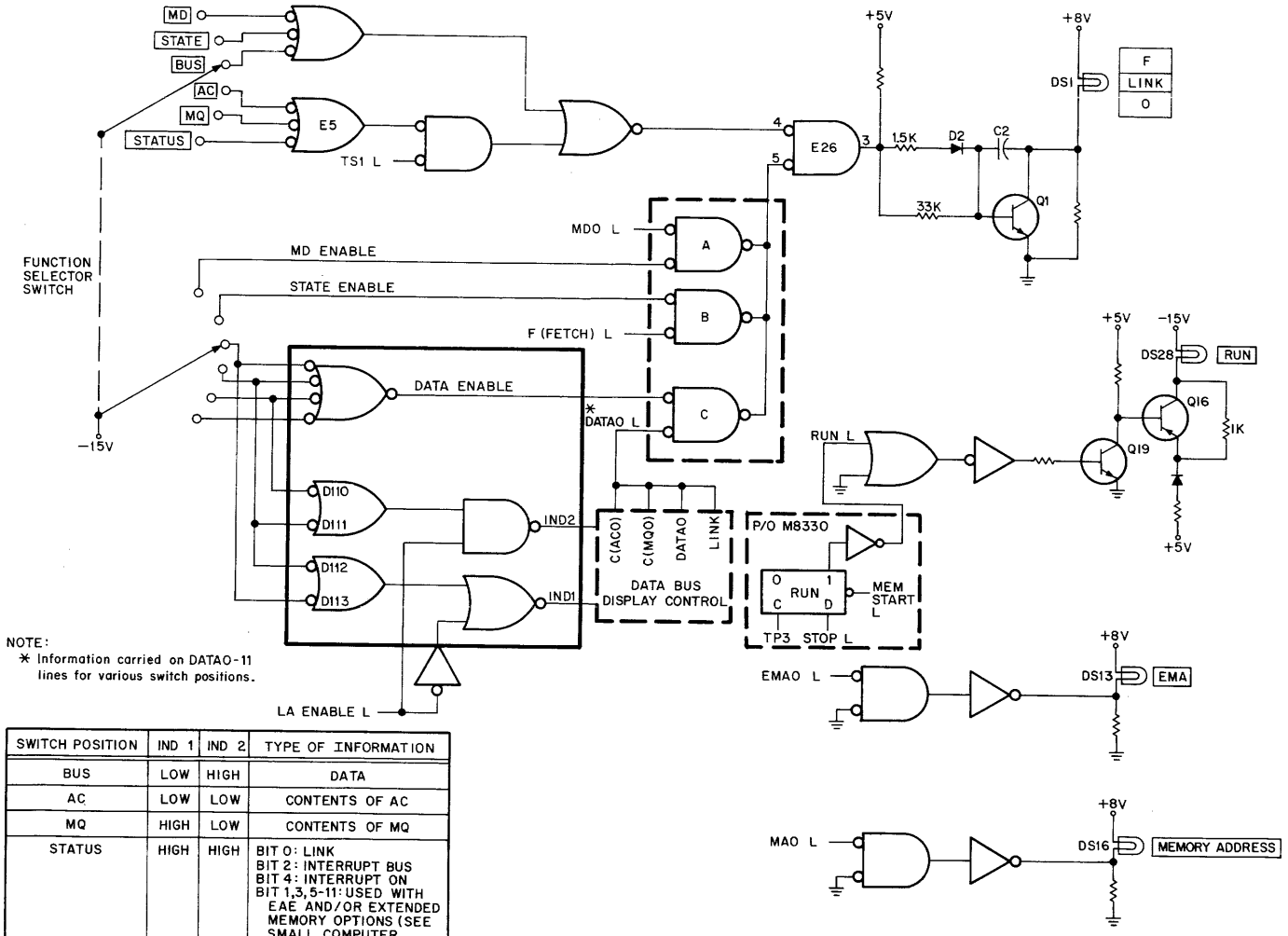


Figure 3-75 SING STEP and HALT Switch Logic

3.33.1.2 Display – The display logic and circuits are shown in Figure 3-76. There are three groups of indicator lamps and a single lamp (RUN) which, when lit, indicates that timing cycles are being generated. Each of the three groups is represented by its 0 bit, e.g., EMA0 L, MA0 L, LINK. The circuits used to display EMA and MEMORY ADDRESS are relatively simple; for example, if MA0 L is a logic 1, the NAND gate is enabled. The output of the inverter drops to a ground level. The full 8V supply voltage appears across the lamp and causes it to light. The lamp has a small voltage across it when MA0 L is a logic 0 (this condition extends the life of the lamp by eliminating the full-on/full-off cycle that often burns out lamp filaments). Consequently, it is lit at this time; however, the lamp is so dim that it is not visible from the front panel.

The circuit used to display RUN is shown above the EMA display circuit. When timing cycles are not being generated, the RUN flip-flop in the Timing Generator is cleared. Q19 and Q16 are in the nonconducting state. The conducting path for the lamp voltage includes the 1000Ω resistor; thus, a small voltage appears across DS28, causing it to be dimly lit. When RUN L is asserted by MEM START L, Q19 and Q16, in turn, are turned on. The conducting path from +5V to -15V takes the low impedance route through Q16 (from emitter to collector), rather than through the 1000Ω resistor. Thus, the RUN lamp is brightly lit, indicating that timing cycles are being generated.



SWITCH POSITION	IND 1	IND 2	TYPE OF INFORMATION
BUS	LOW	HIGH	DATA
AC	LOW	LOW	CONTENTS OF AC
MQ	HIGH	LOW	CONTENTS OF MQ
STATUS	HIGH	HIGH	BIT 0: LINK BIT 2: INTERRUPT BUS BIT 4: INTERRUPT ON BIT 1,3,5-11: USED WITH EAE AND/OR EXTENDED MEMORY OPTIONS (SEE SMALL COMPUTER HANDBOOK-1972)

Figure 3-76 Display Logic

The RUN indicator uses - 15V and +5V, rather than +8V, to operate the lamp. The +8V supply is removed from the display panel, thus extending the lamp life, when the panel is locked. The - 15V supply is not removed; thus, there is an indication of whether or not the computer is running.

The last group of indicators uses the greatest amount of the display logic and circuitry. This group reflects the data appearing on the MD 00–11 lines, the data appearing on the DATA 00–11 lines, and the state of selected registers and OMNIBUS control lines.

The type of information displayed by this group of indicators is selected at the front panel by a six-position rotary switch, labeled "Function Selector Switch" on Figure 3-76. Note that this switch produces one of three enable signals, depending on its position. If MD ENABLE is asserted, data on the MD 00–11 lines is displayed on the front panel; if STATE ENABLE is asserted, data on selected OMNIBUS signal lines is displayed; if DATA ENABLE is asserted, data on the DATA 00–11 lines is displayed.

If the operator wants to monitor the information on the MD lines, he selects the MD position of the rotary switch. This action asserts MD ENABLE, which is ANDed with MD0 L (the actual circuits within this dashed line are presented in a following paragraph of this section). If MD0 L is a logic 1, the AND gate brings pin 5 of NAND gate E26 to a virtual ground. Because pin 4 is also at ground, E26 is enabled, and pin 3 goes to +5V. Transistor Q1 turns on rapidly because its base drive is supplied through the low-impedance diode path. The switching action of Q1 places a ground on its collector; thus, approximately 8V appear across DS1, causing it to be brightly lit. When E26 is again disabled, pin 3 goes to ground, and diode D2 is reversed-biased. Capacitor C2 begins to discharge through the 33 kΩ resistor. This long RC time constant ensures that Q1 turns off slowly, increasing the visibility of DS1.

If the operator wants to monitor the content of the AC Register, he selects the AC position; the DATA ENABLE signal is then asserted. In addition, NOR gates D110/D111 and D112/D113 are enabled (the actual circuit within this solid line is presented in a following paragraph). When these gates are enabled, both IND1 and IND2 are asserted, provided that LA ENABLE L is not asserted. These control lines cause the content of the AC Register to be placed on the DATA 00–11 lines. If DATA 0 is a logic 1, E26, pin 5 is grounded; pin 4 is also grounded, but only during TS1, and the content of DATA 0 is displayed on DS1.

Similarly, the content of the MQ Register, STATUS information, and BUS data can be displayed. The relationship between IND1/IND2 and the type of information displayed is indicated on Figure 3-76. Figure 3-77 shows the logic used to generate control signals in response to IND1 and IND2. This logic is contained within the block designated DATA BUS DISPLAY CONTROL in Figure 3-76.

Figure 3-78 shows the circuit represented by AND gate C, enclosed within the dashed line in Figure 3-76 (gate C was arbitrarily selected for discussion; the following can apply to gates A and B, if the signal names and component designations are changed accordingly). Both the DATA ENABLE line and the DATA 0 line must be asserted if pin 5 of E26 is to be true (logic 1, or 0V). If the DATA ENABLE line is not asserted, it is at +5V. The junction of diodes D61 and D36 is +5V; neither diode conducts current; thus, pin 5 is +5V. When the DATA ENABLE line is asserted, both diodes can conduct current. If the DATA 0 line is negated (at 3V), the diode junction goes to approximately 2.3V. Pin 5 then goes to 3V, and E26 remains disabled. When DATA 0 becomes true (0V), the junction goes to -0.7V, pin 5 goes to ground, and E26 is enabled.

Figure 3-79 shows the circuit represented by the logic gates and enclosed within the solid line in Figure 3-76. Each of the four switch positions asserts DATA ENABLE by switching the DATA ENABLE line to - 15V through a diode. Thus, the line, when asserted, is at approximately - 14V.

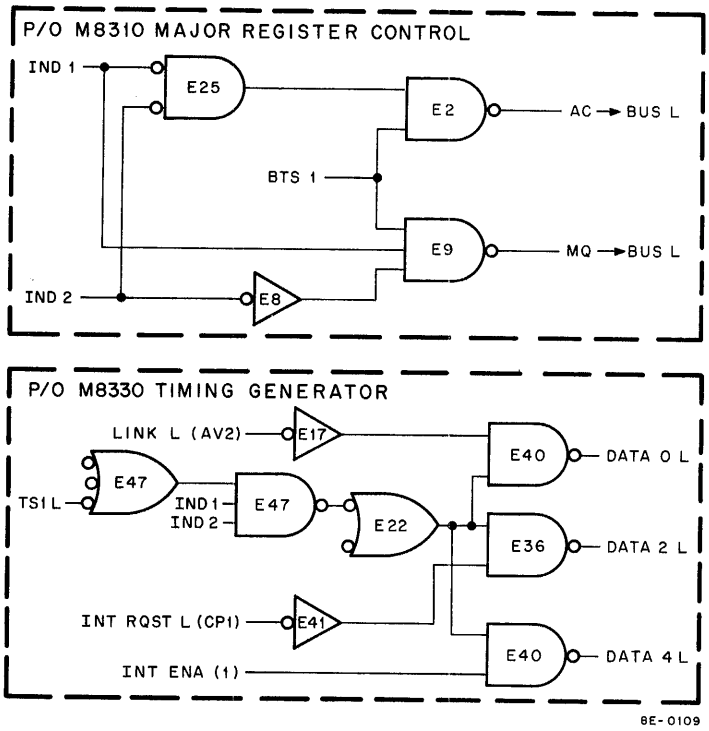


Figure 3-77 Data Bus Display Control Signals

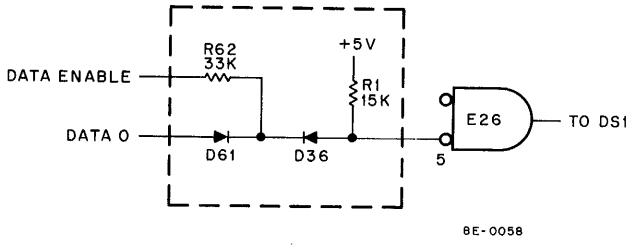


Figure 3-78 Enable Circuit

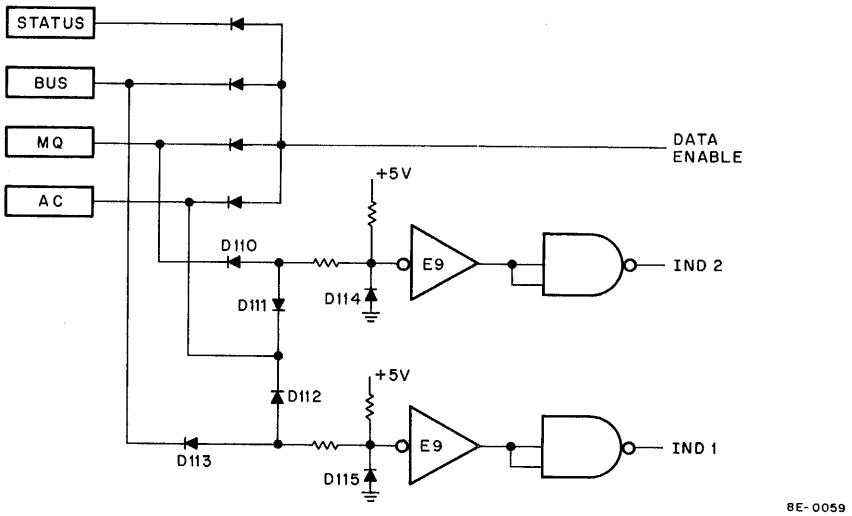


Figure 3-79 DATA ENABLE/IND SELECT

Only STATUS asserts DATA ENABLE without affecting either the IND1 or IND2 control lines. Each of the remaining three positions causes one or both of these control lines to be asserted. For example, if BUS is selected, the junction of diodes D113 and D112 goes to approximately -14V. D115 has a conduction path and, thus, clamps the input of E9 at -0.7V. The resulting positive voltage at the output of E9 enables the following NAND gate to assert IND1. If neither D112 nor D113 conducts, D115 remains in the nonconducting state. The input to E9 remains at +5V, and IND1 is negated.

The pulse processor and delay network is shown in Figure 3-80. The input to the network, from inverter E10, is a positive-going level that results from closure of a front panel key. The output from the network is a noise-free, 400 ns gate that is used to assert either MEM START L, PULSE LA, or INITIALIZE.

When a front panel key, EXAM, is depressed, the resulting negative-going edge at the input to inverter E10 may appear as shown in Figure 3-80; i.e., noise spikes appear because of contact bounce. The integrator at the output of E10 is designed to remove the noise spikes. The large capacitance is unresponsive to noise, and, therefore, smooths the edge, while also greatly increasing its rise time. The integrating action, along with the shaping and filtering accomplished by the three transistors, which comprise a Schmitt trigger, produces a positive transition at the collector of Q15. This transition is delayed approximately 20 ms from the negative transition at the input of E10.

The differentiator converts the transition to a positive spike, which triggers a one-shot. This spike is inverted by NOR gate E2; the leading edge of the negative spike is coupled through the 330 pF capacitor and enables NAND gate E2. Simultaneously, the leading edge enables a charging path for the capacitor. This path is sustained by bringing the NAND gate output back to keep the NOR gate enabled. The capacitor charges toward +5V on a long time constant, keeping the NAND gate enabled for approximately 400 ns. When the capacitor has charged to a voltage sufficiently high to disable NAND gate E2, the charging path is removed. Thus, the output of E2 is a 400 ns positive gate and, in this instance, asserts MEM START L for that length of time.

3.33.2 KC8-FL Programmer's Console

3.33.2.1 Manual Operation

Switch Register – The switch register comprises 12 switches that allow the operator to load the CPMA Register with a 12-bit memory address; to load the extended address bits, if more than 4K of memory is used; to deposit a 12-bit data word in a selected memory location; and to change the content of the AC Register. To carry out these functions, the switch register is operated in conjunction with the DEP, ADDR LOAD, and EXTD ADDR LOAD keys (Figure 3-67).

Figure 3-81 illustrates the logic used to set data into the switch register and to place it on the DATA 0–11 lines. The operator selectively closes switches S11 through S22 (designated "0" through "11", respectively, on the front panel). He then causes NOR gate E20 to assert SR → DATA; this signal gates the information represented by the switch register keys onto the DATA lines.

There are three ways for the operator to assert SR → DATA. If he wants to load the CPMA Register, he depresses ADDR LOAD, causing NAND gate E13A to be enabled. (The signals designated A0 L, A1 L, A2 L, and E4 (1) are enable signals that are selectively generated when the operating keys are activated; these signals are described in the *Operating Keys* section.) If he wants to load the extended address bits, he depresses EXTD ADDR LOAD, again causing E13A to be enabled. If he wants to deposit data in a memory location, he raises the DEP key, causing NAND gate E9C to be enabled during TS2 (a variety of information must be carried by the DATA lines;

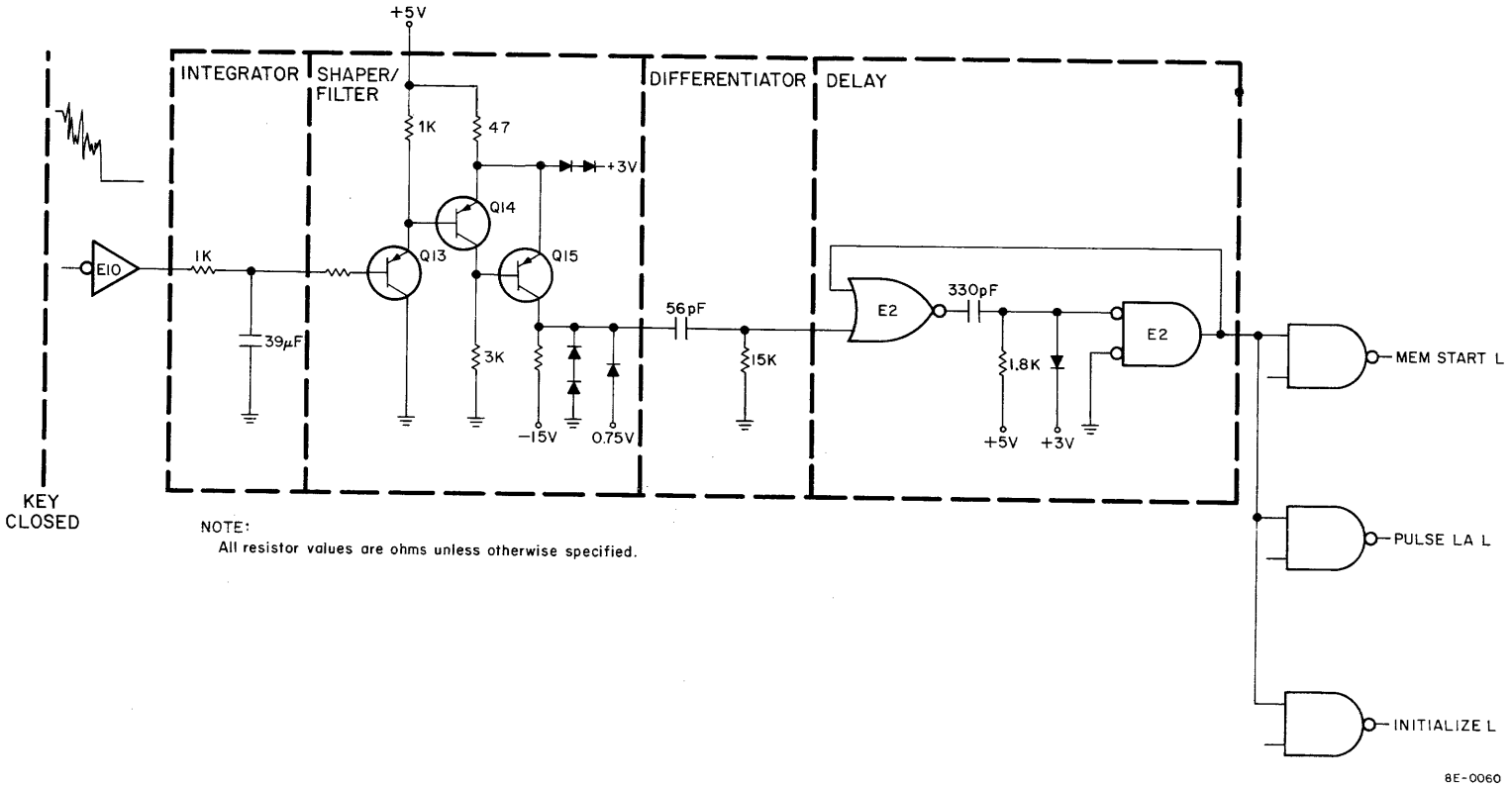


Figure 3-80 Pulse Processor and Delay Network, Schematic

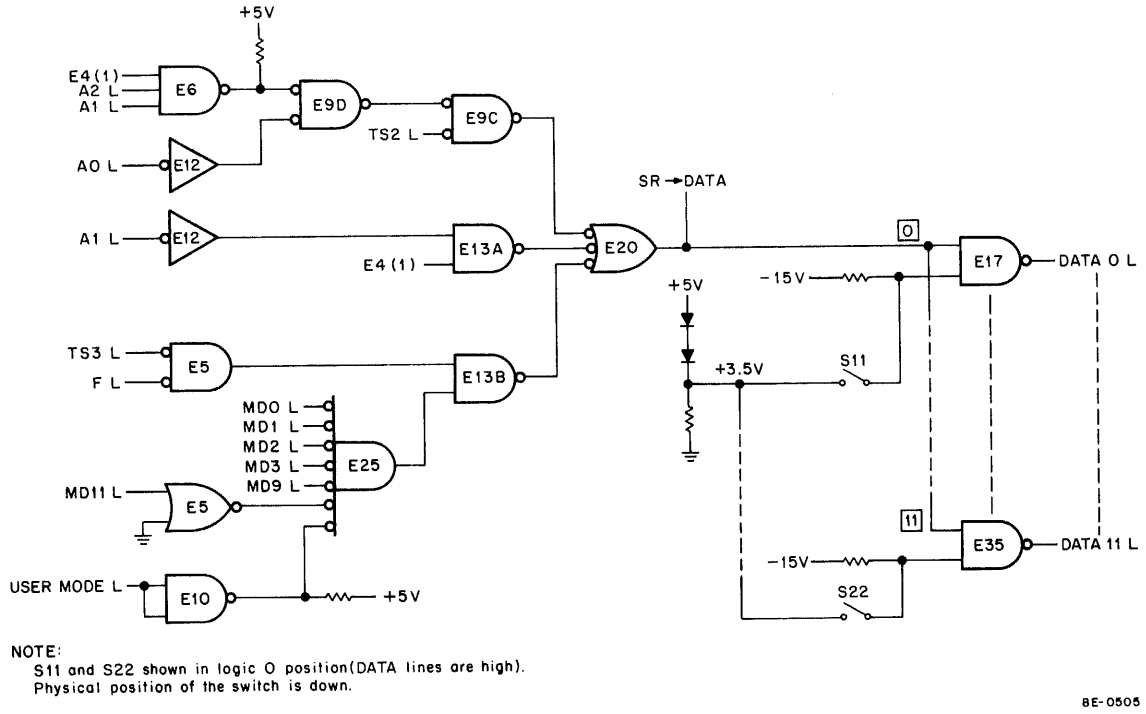
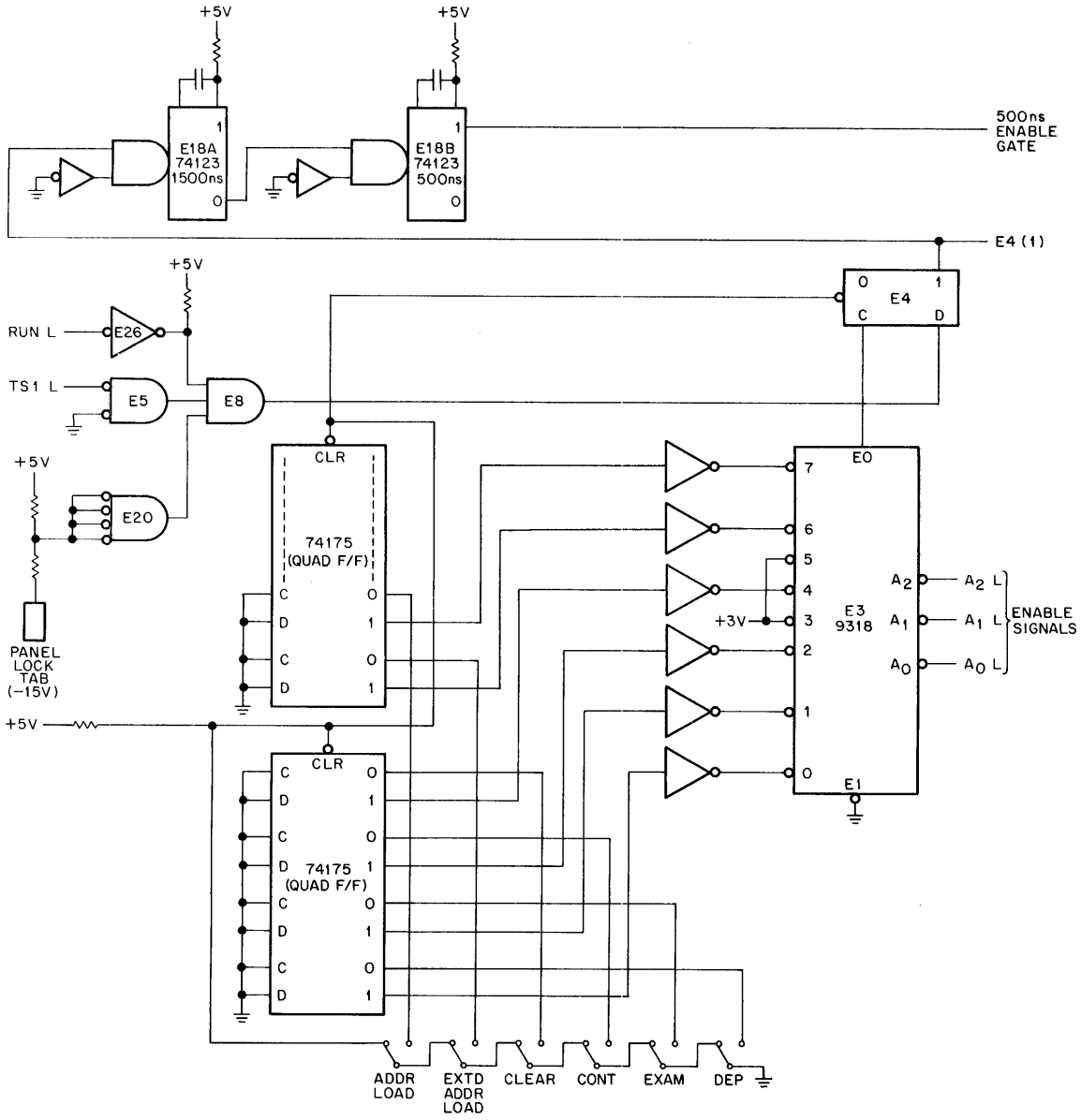


Figure 3-81 Switch Register Control Logic

time sharing of the lines must be employed to maintain the identity of each type of information). Finally, if the operator wants to change the content of the AC Register under program control, he can program either the OSR instruction (inclusive OR, switch register with AC) or the LAS instruction (load AC with switch register). Either instruction causes gate E25 to be enabled, provided USER MODE L is not asserted by the KM8-E option. When NAND gate E5 is enabled during TS3, E13B is enabled, in turn, and the SR → DATA signal is asserted. NANDing the F L signal in gate E5 ensures that E13B is not enabled during the DEFER or EXECUTE cycle of a multicycle instruction.

Operating Keys – The operating keys selectively generate enable signals when they are activated. The enable signals, in turn, selectively assert control signals that cause the processor to carry out the intended key function (all but one of the control signals, SR → DATA, are on the OMNIBUS). The logic used to generate the enable signals is shown in Figure 3-82.

Each key controls one of the D-type flip-flops of a DEC 74175 quad flip-flop IC. The normally open contact of each key is connected to the 0 output of a flip-flop. When a key is activated, the ground placed on the 0 output of the associated flip-flop forces the flip-flop to the set state. The 1 output is applied through an inverter to a DEC 9318 8-input priority encoder. Each input of the encoder is assigned a value from 0 to 7. When an input line is activated, the 9318 encoder provides a binary representation on the active low outputs A0, A1, and A2 (A0 is the LSB). At the same time, the 9318 active high output, EO, goes high, clocking flip-flop E4. If the computer is stopped (power is on but timing has not been initiated), the RUN L signal is high and the D input of E4 is high. Thus, E4 is set and the E4 (1) signal is asserted (if the front panel OFF/POWER/PANEL LOCK switch is in the PANEL LOCK position, the -15V supply voltage is removed from the panel lock tab, and NAND gate E8 cannot be enabled; this effectively disables the operating keys and switches and prevents manual operation of the switch register). The E4 (1) signal triggers 1-shot E18A; 1500 ns later the 500 ns enable gate is generated when E18B is triggered.



7	6	5	4	3	2	1	0	E0	A_2	A_1	A_0	KEY
H	H	H	H	H	H	H	H	L	H	H	H	—
L	X	X	X	X	X	X	X	H	L	L	L	ADDR LOAD
H	L	X	X	X	X	X	X	H	L	L	H	EXTD ADDR LOAD
H	H	H	L	X	X	X	X	H	L	H	H	CLEAR
H	H	H	H	H	L	X	X	H	H	L	H	CONT
H	H	H	H	H	H	L	X	H	H	H	L	EXAM
H	H	H	H	H	H	H	L	H	H	H	H	DEP

H = High voltage level
L = Low voltage level
X = Dont care

8E-0506

Figure 3-82 Operating Keys, Enable Signal Logic

The table in Figure 3-82 relates the keys and the 9318 inputs and outputs. The table reflects the dominant feature of the 9318 priority encoder, viz., if two or more inputs are simultaneously active, the input with the highest priority is represented by the binary output. Input 7 is assigned highest priority; thus, the ADDR LOAD key takes precedence over all other keys. If the operator depresses the ADDR LOAD key, for example, the 9318 IC asserts the A0 L, A1 L, A2 L, and EO signals. Until this key is released, no other key can affect the enable signals. When the key is released, the 74175 CLR input is returned to ground, clearing the flip-flop that was set by the ADDR LOAD key. Now, the flip-flop associated with a key of lower priority causes the 9318 output to change. Note that flip-flop E4 is also cleared when a key is released. Thus, the enable signals and, as a result, the control signals are asserted only as long as the operator depresses a key. Manual operation with the KC8-FL is, therefore, as fast as the operator can make it.

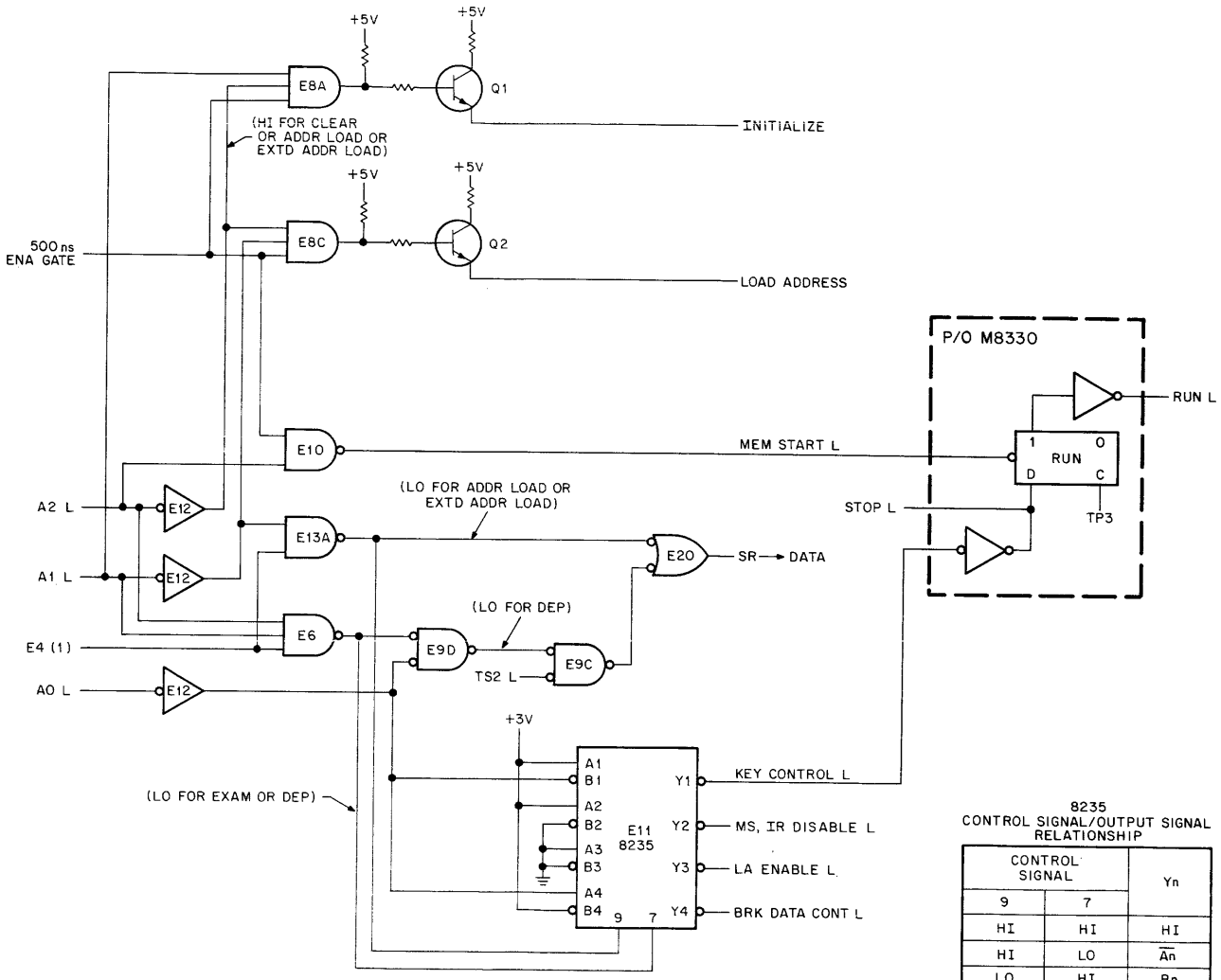
The logic used to generate the control signals is shown in Figure 3-83. The gating of the logic in response to the enable signals is not discussed; this task is left to the reader. Table 3-4, which will facilitate this task, relates the control signals, the enable signals, and the keys. The state of each of the control inputs of the 8235 IC is also tabulated. A functional description of each of the keys follows. Refer to the flow diagram, the logic diagrams, and the tables while reading the functional descriptions.

ADDR LOAD Key and EXTD ADDR LOAD Key – The ADDR LOAD key is used to load the CPMA Register with the memory address specified by the switch register. When the operator depresses this key, switch register information is placed on the DATA 0–11 lines. At the same time, LA ENABLE L and MS, IR DISABLE L are asserted. These two control signals enable a path for the DATA lines through the adder network to the MAJOR REGISTERS BUS. The LOAD ADDRESS signal is then asserted. This signal produces the CPMA LOAD L pulse, which loads the CPMA Register with the information on the DATA 0–11 lines. The memory location specified by the CPMA Register can now be operated on by the DEP key or the EXAM key.

Note that the ADDR LOAD key does not initiate a timing cycle. The purpose of this key is to establish a memory location at which some operation will take place. If a timing cycle were to be initiated, the CPMA address would be incremented, and the operation would take place at the desired address, plus 1. Therefore, to avoid confusion, ADDR LOAD does not initiate a timing cycle.

The EXTD ADDR LOAD key, likewise, does not initiate a timing cycle. This key is used to load switch register bits 6–11 into the Instruction Field (IF) and Data Field (DF) Registers of the KM8-E Memory Extension and Time Share option (bits 0–5 of the switch register are used for IOT designation and device selection code). When the operator depresses the EXTD ADDR LOAD key, the switch register information is placed on the DATA 0–11 lines. The LA ENABLE L and KEY CONTROL L signals are asserted, providing a path to the KM8-E option for the DATA 6–11 lines. The LOAD ADDRESS signal is then asserted and the DF and IF Registers are loaded with the extended address information. The address specified by the CPMA Register and the DF and IF Registers can now be operated on by other keys.

DEP Key – The DEP key is used to deposit the data represented by the switch register in a specified memory location. When the DEP key is lifted, two control signals, MS, IR DISABLE L and KEY CONTROL L, are asserted. KEY CONTROL L selects the MA lines for gating into one leg of the adder network, while MS, IR DISABLE L provides an arithmetic 0 at the other adder input. KEY CONTROL L also asserts a processor signal that increments the CPMA Register. 1500 ns later, the MEM START L signal is asserted, the RUN flip-flop is set, and a timing cycle begins. At TP1 time the PC Register is loaded with the next consecutive memory address (note that the nonincremented address remains in the CPMA Register until TP4 time of the cycle).



8235
CONTROL SIGNAL/OUTPUT SIGNAL RELATIONSHIP

CONTROL SIGNAL		Yn
9	7	
HI	HI	HI
HI	LO	$\overline{An}$
LO	HI	Bn

8E-0507

Figure 3-83 Operating Keys, Control Signal Logic

Table 3-4
KC8-FL CONTROL/ENABLE Signals

Key	ENABLE Signals					E11		CONTROL Signals
	A0 L	A1 L	A2 L	E4 (1)	500 ns ENA Gate	9	7	
ADDR LOAD	LO	LO	LO	HI	HI	LO	HI	LOAD ADDRESS, SR → DATA, MS, IR DISABLE L, LA ENABLE L
EXTD ADDR LOAD	HI	LO	LO	HI	HI	LO	HI	LOAD ADDRESS, SR → DATA, MS, IR DISABLE L, LA ENABLE L, KEY CONTROL L
CLEAR	HI	HI	LO	HI	HI	HI	HI	INITIALIZE
CONT	HI	LO	HI	HI	HI	HI	HI	MEM START L
EXAM	LO	HI	HI	HI	HI	HI	LO	MEM START L, KEY CONTROL L, MS, IR DISABLE L, BRK DATA CONT L
DEP	HI	HI	HI	HI	HI	HI	LO	MEM START L, KEY CONTROL L, MS, IR DISABLE L, SR → DATA

During TS2 of the timing cycle, the switch register data is gated onto the DATA 0–11 lines and the adder control signals enable a path through the adder network, adding an arithmetic 0 to each DATA bit. The switch register information is placed on the MAJOR REGISTERS BUS and loaded into the MB Register at TP2 time. At the same time, the MD DIR L signal is negated causing the content of the MB Register to be placed on the MD 0–11 lines. The data is then read into the memory location specified by the content of the CPMA Register.

At TP3 time the RUN flip-flop is reset (the STOP L signal is asserted when KEY CONTROL L is generated). The timing continues through TS4 and TP4 to halt in TS1 of some as yet unspecified cycle. Before the cycle is completed, one other operation is performed. The next consecutive address must be transferred from the PC Register to the CPMA Register. Therefore, the information in the PC Register is gated to one leg of the adder, and a 0 is added to each bit; the new address is placed on the MAJOR REGISTERS BUS and loaded into the CPMA Register at TP4 time. The cycle then ends.

EXAM Key – The EXAM key also initiates a timing cycle. By depressing this key the operator causes the content of a selected memory location to be brought from memory and loaded into the MB Register. Except for the absence of the SR → DATA signal, the TS1 operations are the same for the EXAM key as for the DEP key. The MS, IR DISABLE L, KEY CONTROL L, and MEM START L signals are asserted and function as described. However, the EXAM key also causes the BRK DATA CONT L signal to be asserted; this signal causes the TS2 operations to differ from those of the DEP key.

The BRK DATA CONT L signal gates the MD lines to the adder network, where a 0 is added to the data being brought from the memory location. The MD bits are placed on the MAJOR REGISTERS BUS and loaded into the MB Register at TP2 time (at the same time, the MD DIR L signal is negated, causing the register content to be again placed on the MD lines; thus, the content of the memory location can be re-written during the write half of the timing cycle). The operator can view the content of the MB Register by selecting the MD position on the front panel function selector switch. The operator can modify the data in the examined location by using the switch register and the DEP key. However, the EXAM cycle increments the PC Register to set up the next sequential memory address; therefore, to modify the data in the examined location, the switch register and ADDR LOAD key must be used to get back to the correct address.

CONT Key – The CONT key initiates a timing cycle by causing the MEM START L signal to be asserted. This is an important function because this is the *only* key that initiates repetitive timing cycles. Thus, the operator can begin automatic operation only by depressing the CONT key.

CLEAR Key – The CLEAR key generates the INITIALIZE signal. This signal clears the AC Register, the LINK, the Interrupt system, all peripheral flags, and various flip-flops within the basic system.

SING STEP Switch and HALT Switch – The operator can stop the PDP-8/E by closing either the SING STEP or the HALT switch. The logic is shown in Figure 3-84. If the SING STEP switch is used, the STOP L signal is generated and the first TP3 pulse clears the RUN flip-flop. The RUN L signal is negated, and the machine stops at the beginning of the next TS1 period. If the HALT switch is used, the STOP L signal is generated only when the F SET L signal is asserted. Because F SET L is asserted only when the next timing cycle is to be a FETCH cycle, the processor completes an entire instruction before halting in TS1. The operator can use these two switches and the CONT key to step a program one cycle or one instruction at a time.

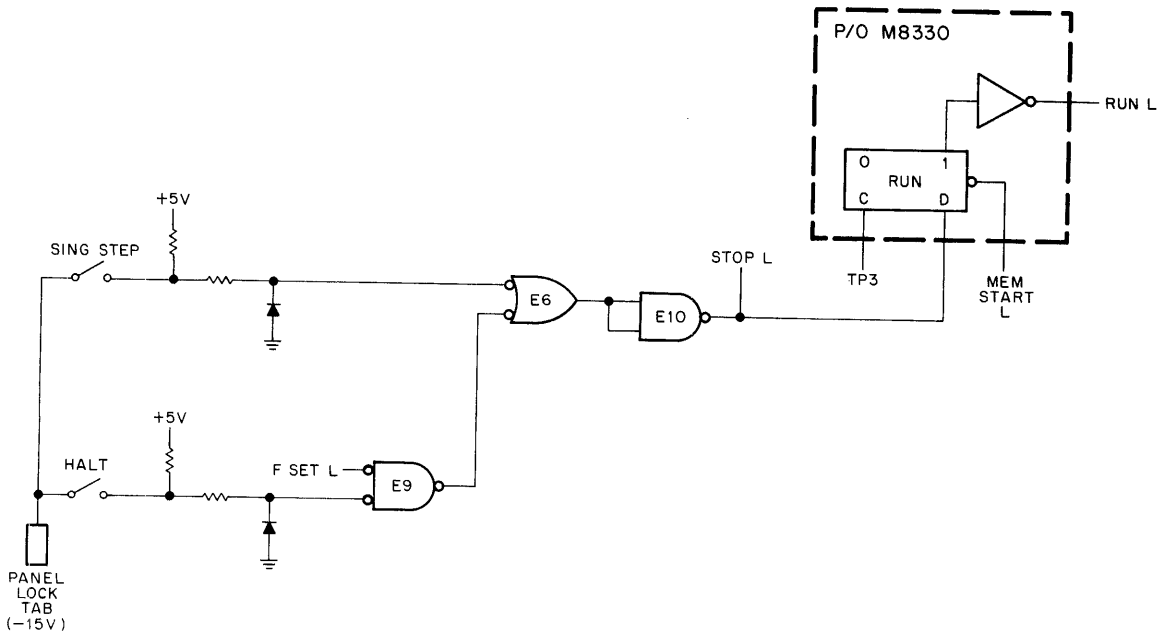


Figure 3-84 SING STEP and HALT Switches

3.33.2.2 Display – The KC8-FL Programmer's Console uses solid-state devices rather than filament-type lamps to indicate the state of various PDP-8/F (PDP-8/M) major registers and OMNIBUS signals. These indicators, light-emitting diodes (LEDs), are more durable than lamps and help to promote maintenance-free operation. LEDs differ from incandescent lamps in another important way. As the name implies, LEDs are diodes. Consequently, they exhibit the usual nearly constant forward voltage when conducting. A series resistor to define the forward current through the diode is necessary. In the KC8-FL, the resistor value of 330Ω establishes the LED on-current at about 10 mA. At currents of less than 500 μA, the diode does not emit detectable amounts of light.

A single indicator, designated RUN, emits light when timing cycles are being generated. The light from this and all other indicators, is visible on the front panel (Figure 1-1). The other indicators are divided into two groups. One group, comprising 15 LEDs, displays the current memory address. This group is represented by the designations MEMORY ADDRESS and EMA. The other group, comprising 12 LEDs, displays the contents of selected registers and important OMNIBUS signals. A front panel switch enables the operator to select the register or type of OMNIBUS signal that he wishes displayed.

The display logic is represented in Figure 3-85. The RUN indicator is shown in the lower right of the figure. When the timing generator logic (M8330) asserts the RUN L signal, LED D35 emits light, indicating that the computer is running (power is on and timing cycles are being generated).

The two groups of indicators are represented by the 0 bit logic. For example, a complete 15-bit memory address has two 0 bits, EMA0 and MA0. Both bits are shown in the logic. When either the EMA0 L signal or the MA0 L signal is asserted, the +V voltage appears across the corresponding LED and its current determining resistor, causing it to light. The +V voltage, approximately +4.5V, is taken from the circuit that includes Q3 and Q4. When the front panel OFF/POWER/PANEL LOCK switch is in the PANEL LOCK position, the -15V supply is removed from the panel lock tab, thereby removing the +V voltage. Consequently, only the RUN indicator is lit with the switch in this position.

The majority of the logic in Figure 3-85 is used with the group of indicators that displays OMNIBUS signals and major register contents. Again, only the 0 bit logic is represented. The type of information displayed is selected on the front panel by a 6-position rotary switch, labeled S1 in Figure 3-85. This switch causes one of three signals to be asserted, depending on its position: in the MD position, MD IND is asserted; in the STATE position, STATE IND is asserted; in all other positions, DATA IND is asserted.

If the operator wants to monitor the MD lines, he switches to the MD position, causing the MD IND signal to be asserted. This signal is ANDed with the MD0 L signal in AND/NOR gate E15. The three other AND gates of E15 are disabled when S1 is in the MD position. If the MD0 L signal is asserted, E15 is disabled. Therefore, the output of inverter E22 is low. The +V voltage appears across LED D23, causing it to emit light that is visible on the front panel. The same analysis can be repeated for the F L signal when S1 is in the STATE position. However, the logic gating is more complicated when any of the other four switch positions is selected. The reason for this is that the four different types of signals must be carried on only the DATA lines; furthermore, remember that the DATA lines are time-shared and display information has access to these lines only during TS1.

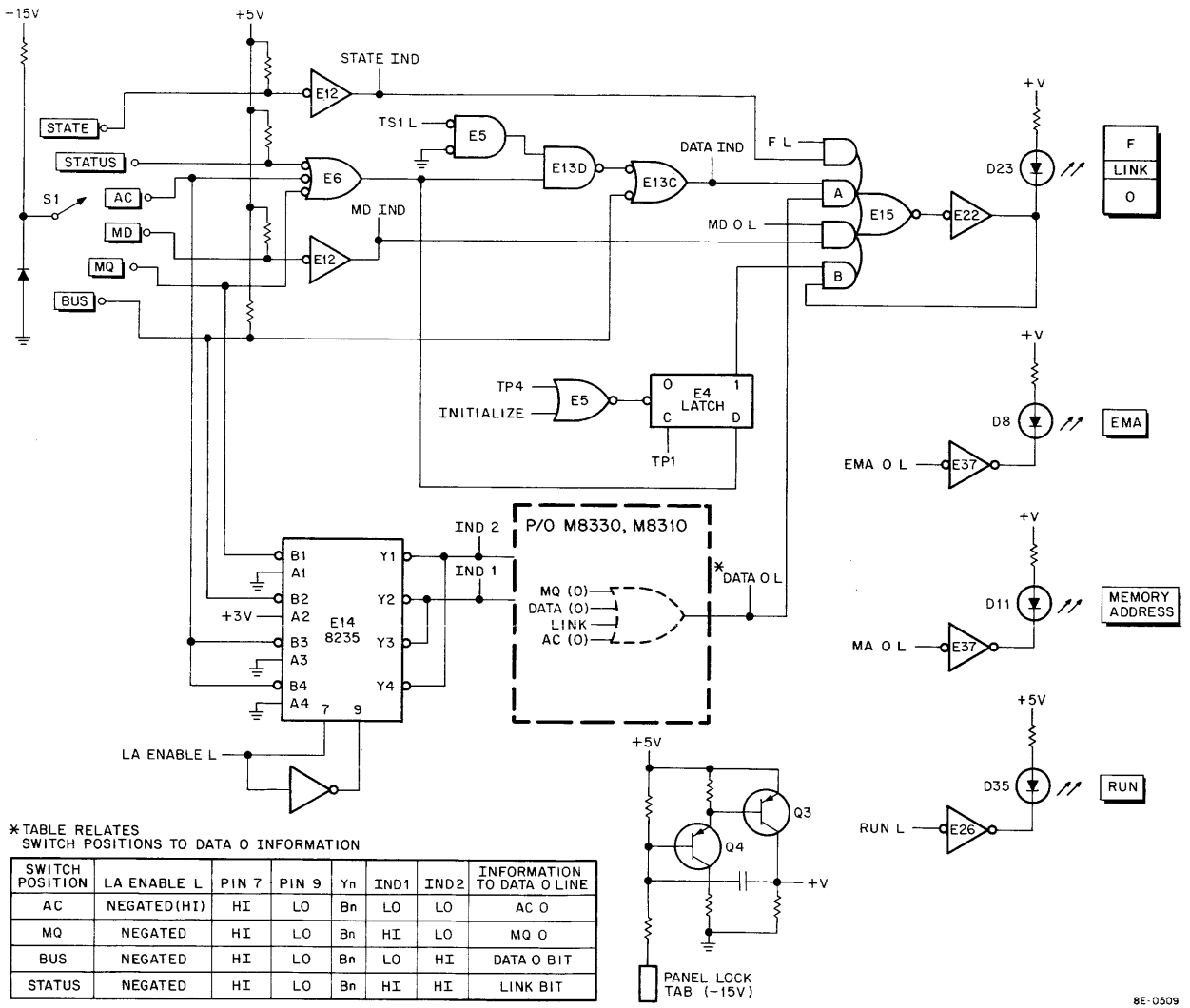


*TABLE RELATES SWITCH POSITIONS TO DATA O INFORMATION

SWITCH POSITION	LA ENABLE L	PIN 7	PIN 9	Yn	IND1	IND2	INFORMATION TO DATA O LINE
AC	NEGATED(HI)	HI	LO	Bn	LO	LO	AC O
MQ	NEGATED	HI	LO	Bn	HI	LO	MQ O
BUS	NEGATED	HI	LO	Bn	LO	HI	DATA O BIT
STATUS	NEGATED	HI	LO	Bn	HI	HI	LINK BIT

Figure 3-85 Display Logic

Assume that the operator positions S1 at AC. The DATA IND signal is asserted during TS1. The AC0 bit must be gated to the DATA 0 line so that its state can be displayed. The table in Figure 3-85 shows that when the AC position is selected, the 8235 IC takes both IND1 and IND2 low. This combination of IND1 and IND2 causes the logic within the broken line (the actual logic is shown in Figure 3-86) to assert the AC → BUS L signal. Thus, the AC0 bit is gated to the DATA 0 line. If the AC0 bit is logic 1, AND gate A of E15 is disabled, the output of E15 stays high, and D23 emits light.

If the AC0 bit is logic 0, the LATCH flip-flop performs an important function. To illustrate, assume that the operator, while stepping the computer through a series of timing cycles (with the SINGLE STEP switch closed), causes a TAD instruction to be executed. The computer stops in TS1 of the cycle following the TAD instruction. The operator wants to check the result and switches to the AC position. D23 indicates logic 0. When the CONT key is depressed, AND gate A of E15 is disabled as soon as TS2 of the new timing cycle is entered. Therefore, if AND gate B and the LATCH flip-flop were not present, D23 would emit light for most of the timing cycle following the TAD execute cycle. Instead, the LATCH flip-flop is set at TP1 time (the D-input is high when the AC position is selected). The 1 output of the flip-flop and the high at the output of E22 keep E15 enabled; D23 remains dark throughout the timing cycle. At TP1 time the LATCH flip-flop is cleared.

Similarly, the content of the MQ Register, STATUS information, and BUS data can be displayed. The relationship between IND1/IND2 and the type of information displayed is indicated on Figure 3-85. Figure 3-86 shows the logic used to generate control signals in response to IND1 and IND2.

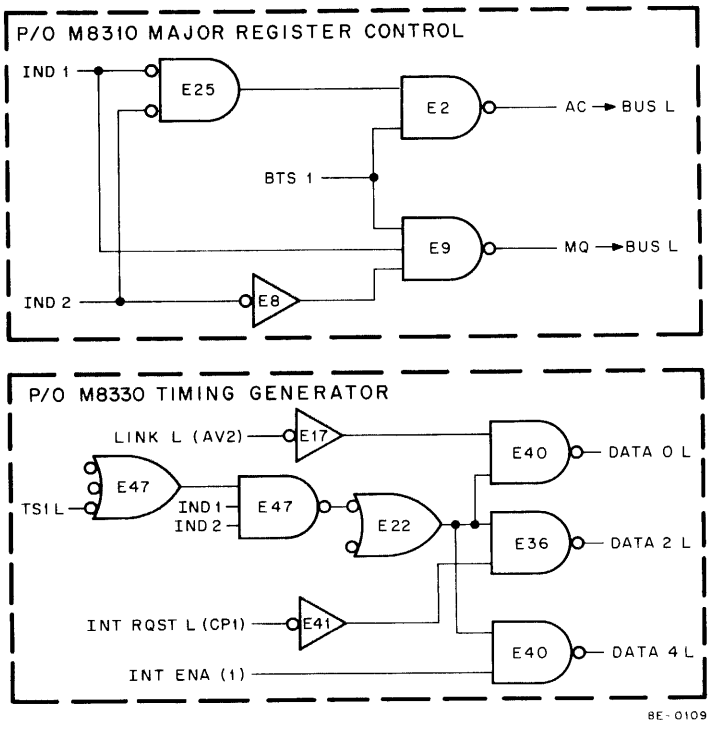


Figure 3-86 Data Bus Display Control Signals

3.34 MAJOR REGISTER GATING, BLOCK DIAGRAM DESCRIPTION

The major registers of the PDP-8/E perform all the operations required to implement program instructions. In retrospect, the PC Register keeps track of the program steps, the CPMA Register selects the memory location provided by the PC, and the AC Register uses the data in the selected memory location to carry out arithmetic operations. Information of one type or another (data, addresses, etc.) is continuously exchanged by the major registers. To effect these exchanges, the major register gating network is required. The major registers and the gating network are illustrated in the block diagram of Figure 3-87. This diagram presents the register flip-flops and the gating for one bit, bit 0, of the PDP-8/E 12-bit data word. All 12 data bits have similar gating networks; when differences exist, they will be noted in the discussion.

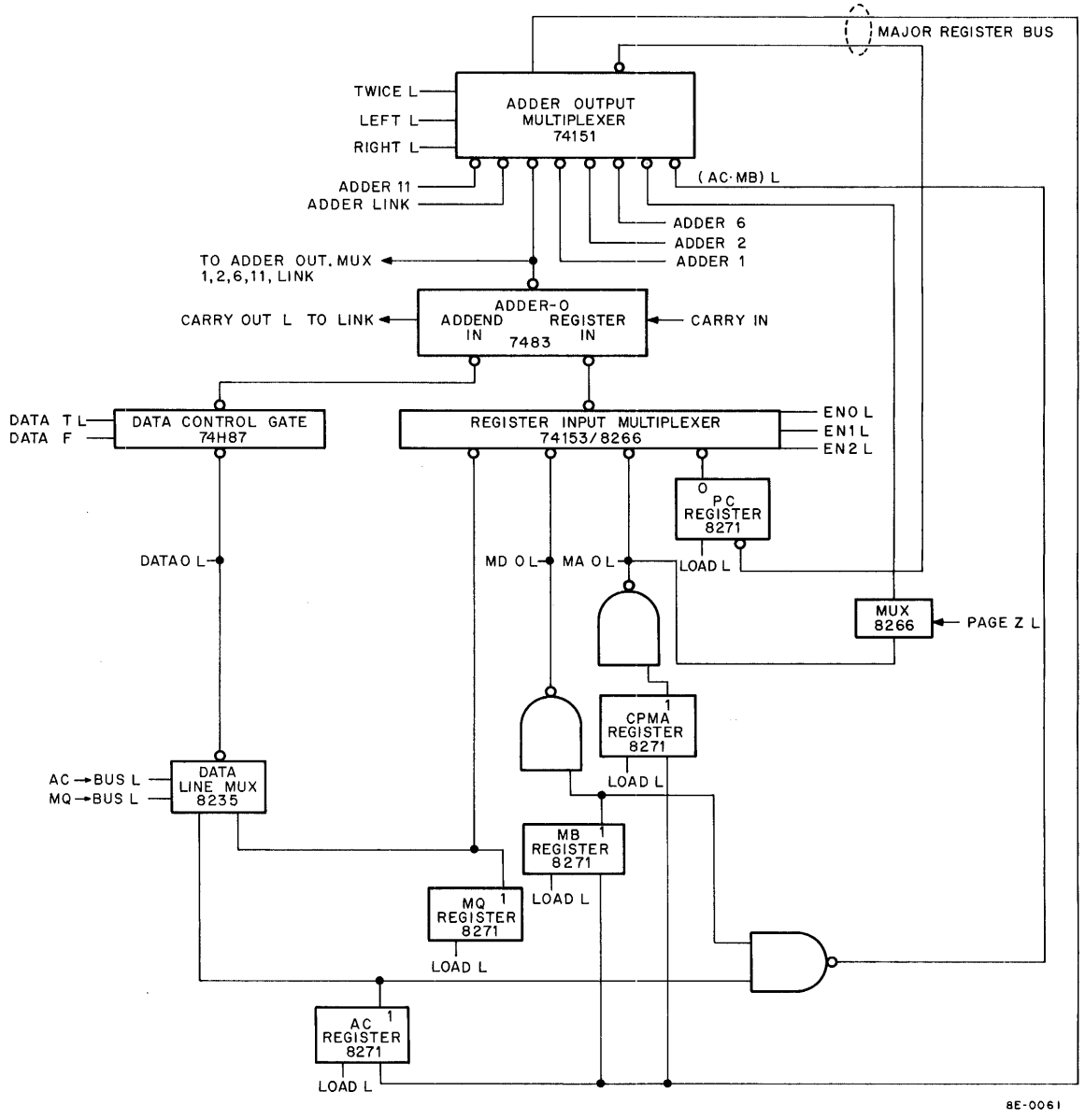


Figure 3-87 Major Registers and Gating, Block Diagram

Each major register is loaded with data that is transferred to the 0 bit flip-flop by the MAJOR REGISTERS BUS. The source of the data on this bus is the adder network. This network consists of the adder itself, a Register Input Multiplexer, an Adder Output Multiplexer, and a Data Control Gate which supplies an addend to the adder. The Register Input Multiplexer gates the output from a selected register flip-flop to the "register in" line of the adder. The data to be added to the 0 bit of this register is supplied by the Data Control Gate. The sum for the adder is transferred to the MAJOR REGISTERS BUS by the Output Multiplexer. A timing pulse then provides a load signal, which clocks the data into the desired register.

Note that the Adder Output Multiplexer can select any one of eight inputs for transfer to the register bus. Consider only the adder 0 input. Bit 0 of any register can be transferred to bit 0 of any other register. This is the case when the memory address in the PC Register is transferred to the CPMA Register at the completion of an instruction (PC → CPMA). Bit 0 of the PC is gated by the Register Input Multiplexer to the adder "register in" line. Because the bit must be transferred unaltered, an arithmetic 0 is supplied at the "addend in" line by the DATA T/DATA F control signals. The Adder Output Multiplexer places the unaltered bit on the MAJOR REGISTERS BUS; a load signal clocks the data into the 0 bit of the CPMA Register.

A similar operation takes place when the 0 bit is modified before transfer. For example, during an IOT instruction a peripheral can effect a relative jump of the program count (DATA + PC → PC). In this case, the "addend in" line must represent the state of the DATA 0 line and can be either a 0 or a 1. The sum of DATA 0 and PC0 is transferred to the MAJOR REGISTERS BUS; a load signal clocks the data into the 0 bit flip-flop of the PC.

If the Adder Output Multiplexer control signals (TWICE L, LEFT L, RIGHT L) select the "adder 1" input for transfer to the 0 bit MAJOR REGISTERS BUS, the RAL microinstruction (rotate AC and LINK left one place) is being implemented. Bit 1 of the AC Register is transferred to bit 0 of the AC Register (at the same time, AC bit 0 is transferred to the LINK). AC transfers are accomplished differently from the transfers of the other major registers. AC bit 0 is gated onto the DATA 0 L line by an AC → BUS signal, and through the data control gate to the adder. In this case, the Register Input Multiplexer provides an arithmetic 0 at the "register in" line. Bit 0 is then gated through the Adder Output Multiplexer that is associated with the LINK. Simultaneously, the output from adder 1 is gated onto the 0 bit MAJOR REGISTERS BUS. The AC LOAD L signal then clocks the data into the 0 bit of the AC Register.

Similarly, AC bits 11, 2, and 6, and the LINK bit can be transferred into bit 0 of the AC. The microinstructions implemented by those transfers are RTR, RTL, BSW, and RAR, respectively.

In addition to adder outputs, the Adder Output Multiplexer can gate two other signals onto the MAJOR REGISTERS BUS. One of these signals is (AC·MB) L, which is active when both MD0 L and AC0 L are at a positive voltage level (logic 1). When the basic AND instruction is implemented, the signal is gated through the Adder Output Multiplexer by the control signals. The logic 1 or 0 represented by the signal is then clocked into AC0.

The other signal that can be gated by the multiplexer is encountered during implementation of a Memory Reference Instruction (MRI). As the block diagram shows, this input is taken from a multiplexer that is controlled by the PAGE Z L signal. If the page address of the operand of the MRI is the same as that of the MRI, itself, the multiplexer output reflects the state of the MA0 line; however, if the operand is located on the 0 page, the multiplexer output is an arithmetic 0. In either case, the page data is placed on the MAJOR REGISTERS

BUS and loaded into CPMA0. This gating procedure only applies to register bits 0 through 4. If register bits 5 through 11 are considered, only a relative address must be considered. Therefore, the input to the Adder Output Multiplexer is taken directly from the appropriate MD line, rather than from the MA line via the PAGE Z multiplexer. A further discussion is presented when the logic diagrams are considered in detail.

3.34.1 Major State Register

PDP-8/E operations are grouped functionally into the four major states already introduced. FETCH (F), DEFER (D), and EXECUTE (E) are entered actively by setting flip-flop in the Major State Register. The fourth state, Direct Memory Access (DMA), results when none of the other three has been entered.

The Major State Register logic is shown in Figure 3-88. Flip-flops E45 and E50 are used to generate the F, D, and E states. The outputs of E45 and E50 are NANDed with a control signal called MS, IR DISABLE L. When this signal is negated (at +3V), one of the NAND gates (only one major state flip-flop may be active at any given time) is enabled; either F, D, or E is asserted. On the other hand, if MS, IR DISABLE L is asserted, none of these three states is entered. Thus, the computer is in the Direct Memory Access (DMA) state. This state is entered when data is to be transferred between memory and a data break peripheral, or between memory and the front panel. In either case, this state bypasses the processor logic that is normally used to access memory.

The major state flip-flops, E45 and E50, are clocked by the inverted CPMA LOAD L signal. This signal is produced when the front panel LOAD key is depressed during manual operation. In addition, the signal is generated by each TP4 pulse during automatic operation. Some type of manual operation always precedes automatic operation; for example, to initiate automatic operation of a stored program, the operator must load the CPMA with the starting address of the program. This address is loaded by depressing the LOAD key, an action that produces the CPMA LOAD pulse. However, this action also produces MS, IR DISABLE L. In fact, MS, IR DISABLE L is produced some 20 ms before CPMA LOAD. MS, IR DISABLE L causes the logic to generate a control signal, F SET L, which is applied to the data (D) input of the FETCH state flip-flop. Thus, when CPMA LOAD is produced, it clocks the flip-flop to its reset state, and the next cycle of operation will be a FETCH state. If the operator now depresses the CONT key, the computer begins the FETCH operation specified by the instruction just addressed.

The F SET L signal is asserted when computer operation requires that the FETCH state be entered. As previously indicated, FETCH is always entered on completion of manual operation. FETCH can also be entered on completion of a data break operation. Both manual and data break operations take place in the DMA state. Entry to and exit from this state is discussed fully in a following paragraph; a third method of entering the FETCH state is discussed in the following paragraph.

All instructions start in the FETCH state; consequently, this state can be entered from any state that completes an instruction. FETCH is entered from the EXECUTE state at the completion of a two- or three-cycle instruction; FETCH is entered from the DEFER state at the completion of a two-cycle instruction; finally, FETCH is entered from FETCH, itself, at the completion of a one-cycle instruction.

Figure 3-88 shows that F SET L is asserted when both inputs to NAND gate E49 are logic 0 (positive voltage level). Note that this condition arises only if NAND gates E30, E31, and E35 are disabled (ignore FE SET L and FD SET L for this discussion). If the computer is entering the EXECUTE state of a two- or three-cycle instruction, E is asserted at pin 4 of NAND gate E49, while both BD and BF are negated. E30, E31 and E35 are disabled, and CPMA LOAD L (produced by TP4) sets the FETCH flip-flop. If the computer is in the DEFER state of a two-cycle instruction, BF is negated, and E30 and E31 are disabled. E35 is likewise disabled in this

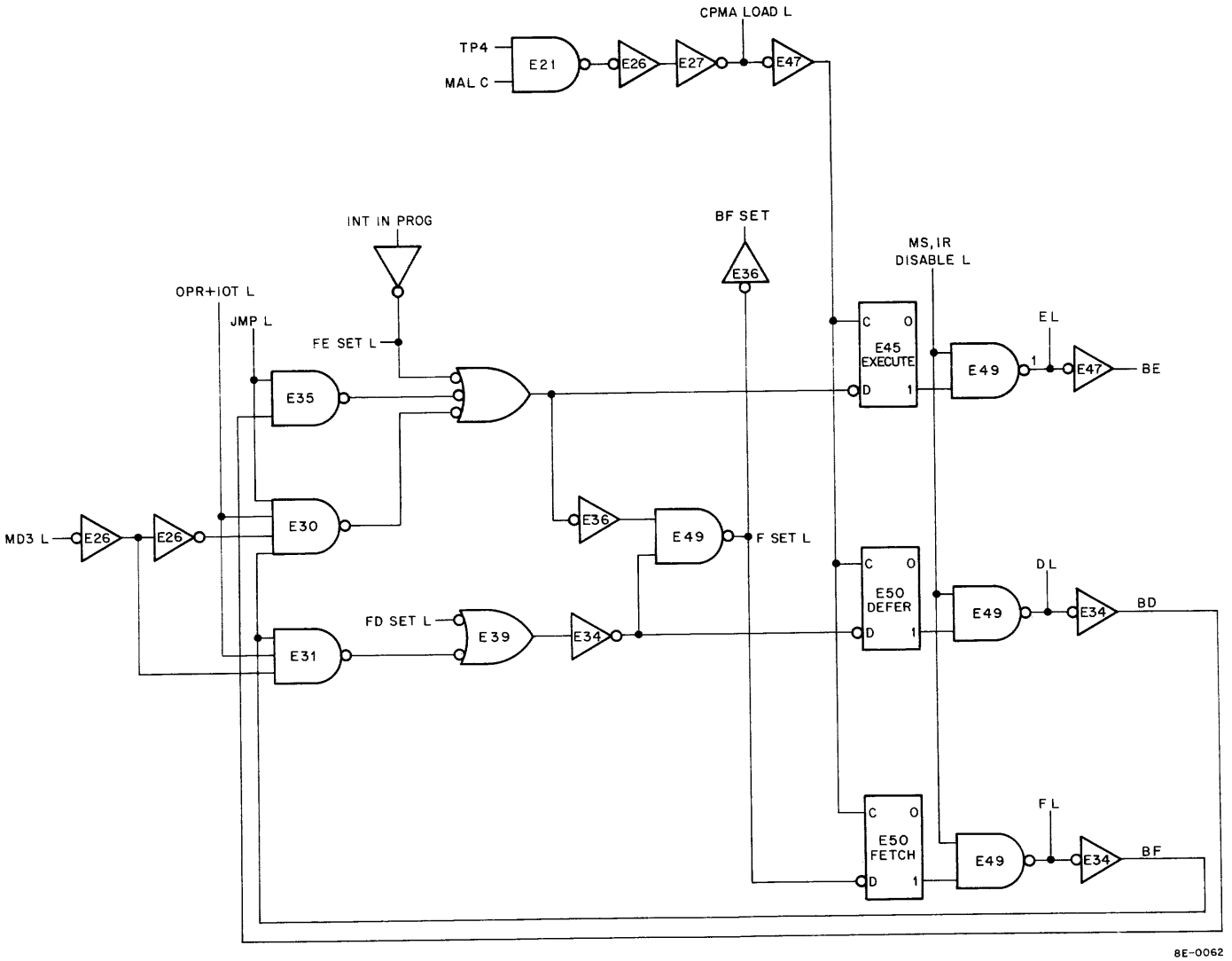


Figure 3-88 Major State Register Logic

case, because a two-cycle instruction involving the DEFER state can only be a JMP instruction. Therefore, the JMP line is asserted low and, again, all three NAND gates are disabled. Finally, if the computer is performing a one-cycle instruction (a FETCH state), BD is negated, thereby disabling E35. A one-cycle instruction can be an OPR microinstruction, an IOT instruction, or a directly addressed JMP instruction. If the instruction is either of the first two, the OPR + IOT line is grounded to disable gates E30 and E31. However, if the instruction is a directly addressed JMP, the JMP line is grounded to disable E30, while the negated MD3 L signal disables E31.

When the FETCH state of a multicycle instruction has been completed, either a DEFER or EXECUTE state follows, unless the operator depresses the SING STEP key or a data break device causes suspension of program control. Either circumstance can cause a halt or interruption when the FETCH state is completed; then the DMA state is entered. When the operations in this state have been carried out, control is returned to the program, and the multicycle instruction can be completed.

Consider, at this time, normal operation under program control, and assume that the instruction being processed is either a two-cycle instruction involving the DEFER state, or a three-cycle instruction. Operations are being carried out in the FETCH state. The DEFER state is the next state to be entered. The data line of the DEFER flip-flop must be asserted low, if the flip-flop is to be set at TP4 of FETCH; thus, NAND gate E35 must be enabled (again, disregard FD SET L). Because the FETCH state of a multicycle instruction is being performed, BF is high and OPR + IOT L is high. The DEFER state is entered when indirect addressing is required by the memory location of the operand. Such addressing is indicated when MD3 L is asserted, thereby providing the third high level for NAND gate E31. TP4 sets the DEFER flip-flop, and operations are then carried out in the DEFER state.

If the instruction is complete at the end of the DEFER state, the FETCH state is entered; however, a three-cycle instruction requires that EXECUTE be entered after DEFER. This requirement is met if NAND gate E35 is enabled. With BD asserted high and JMP negated (some instruction other than JMP is being performed and FE SET L is disregarded), E35 is enabled and TP4 sets the EXECUTE flip-flop. When EXECUTE is complete, the FETCH state is again entered. If the multicycle instruction being carried out does not require indirect addressing, the computer goes directly from FETCH to EXECUTE; in this event, NAND gate E30 is enabled, because MD3 L is negated high.

The preceding discussion disregarded the signals FD SET L and FE SET L. These signals are asserted by the EAE option; their functions are discussed in Volume 2 of this manual. However, note that the INT IN PROG L signal also can assert the FE SET line. The INT IN PROG L signal is asserted high when an interrupt request is honored by the interrupt logic of the timing generator module. The data line of the EXECUTE state flip-flop is then high, and TP4 forces the EXECUTE state to be entered next. FE SET can be asserted in this manner during either a FETCH, DEFER, or EXECUTE state, provided that the particular state is the final state of an instruction.

FETCH can be entered from the DMA state. The DMA state is used during manual operation and for data breaks. This state is entered when the MS, IR DISABLE L line is asserted. If this line is asserted because manual operations are being performed, the FETCH state always follows the DMA state. MS, IR DISABLE L disables NAND gates E49, thereby asserting F SET L (Figure 3-88). If the EXAM or DEP key has been depressed, TP4 and MA, MS LOAD CONT L (the latter is negated during manual operations) produce CPMA LOAD L. If the LOAD key has been depressed, PULSE LA H produces CPMA LOAD L. In either case, the FETCH flip-flop is reset and automatic operation begins in the FETCH state.

If MS, IR DISABLE L has been asserted by a data break peripheral, the FETCH state may or may not follow the DMA state. A data break operation can begin at the end of any major state. Program control is halted for one timing cycle (control may be halted for three cycles, as well; for convenience, a halt of one cycle is considered). When the data transfer has been completed, program control is re-established and the previously interrupted operation continues. An example of the interrupting processor is given in the following paragraph.

If operations are being carried out in the FETCH state of a two-cycle DCA instruction, the data line of the EXECUTE flip-flop is at a positive voltage level. If a peripheral initiates a data break during this FETCH state, MS, IR DISABLE L is asserted at TP4. At the same time, CPMA LOAD L is produced by TP4 and MA, MS LOAD CONT L and the EXECUTE flip-flop is set, but E, at the output of E49, remains negated. The DMA state is entered, instead of the EXECUTE state, and data transfer begins. Because the E49 NAND gates are disabled, F SET L is asserted. It could be assumed that the next TP4 pulse (of the DMA state) would reset the FETCH flip-flop; however, at TP1 of the DMA state the peripheral asserts MA, MS LOAD CONT L, thereby preventing the TP4 pulse in question from resetting the FETCH flip-flop. Instead, this TP4 negates MS, IR DISABLE L. The EXECUTE flip-flop is still set and, thus, E is asserted. Operations begin in the EXECUTE state of the interrupted instruction. At TP1 of this state, MA, MS LOAD CONT L is negated, completing the return to uninterrupted operation.

Consequently, because a data break can occur at the end of any major state, either FETCH, DEFER, or EXECUTE can be entered directly from the DMA state. The following section describes how the DMA state is used to suspend operation of the Instruction Register and decoder network during a data break operation.

3.34.2 Instruction Register

Operations within each major state are determined by the type of instruction that is contained in the addressed memory location. This instruction is placed on the MD lines, near the beginning of a FETCH cycle. MD bits 0, 1, and 2 are decoded by a network consisting, primarily, of an Instruction Register (IR) and a decoder IC. The decoder IC provides an output in response to the octal number represented by IR0 L, IR1 L, and IR2 L (MD0 L, MD1 L, and MD2 L, respectively). For example, the TAD instruction is represented as 1000 octal. Therefore, MD bits 0, 1, and 2 are 0, 0, and 1, respectively. The decimal 1 line is asserted by the decoder, causing TAD operations to begin. Other basic operations are initiated in the same manner. For a detailed presentation of the decoder integrated circuit, see Appendix A.

The decoding network, referred to as the IR decoder, is shown in Figure 3-89. Each of the IR decoder flip-flops, E40 and E45, is clocked by TP2 of the FETCH state. When the data (D) input of a flip-flop is grounded, indicating a logic 1 on the MD line in question, TP2 resets the flip-flop. When a flip-flop is reset, its corresponding IR line (0, 1, or 2) is asserted (grounded), provided that the MS, IR DISABLE L signal is negated. The eight possible combinations of the IR lines are decoded by the decoder module to produce one of the eight basic instructions shown.

If MS, IR DISABLE L is asserted (grounded), it removes the IR flip-flop outputs from the IR0 L, IR1 L, and IR2 L lines (it also causes the decoder to assert the AND L line; however, MS, IR DISABLE L forces the processor into the DMA state, and the basic instructions are not implemented during this major state). When MS, IR DISABLE L is negated, the IR lines return to their former state, and the interrupted instruction is again asserted.

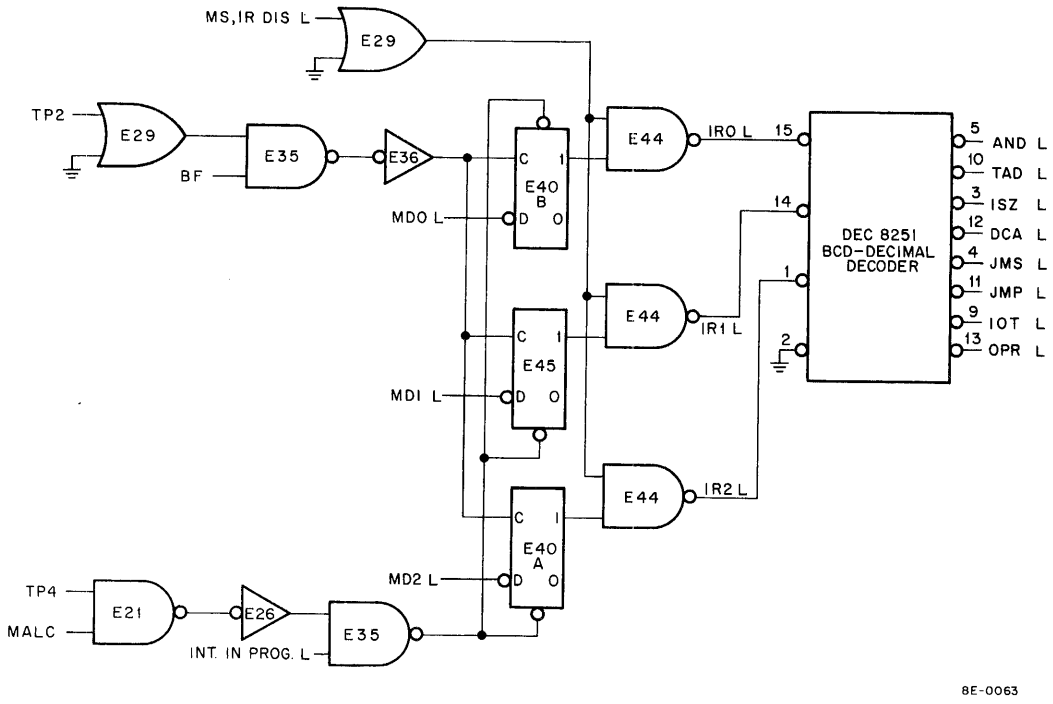


Figure 3-89 IR Decoder Logic

Note that flip-flop E40B can be dc-set and flip-flops E40A and E45 can be dc-cleared by a negative transition at the output of NAND gate E35. This transition occurs at TP4 time, if the INT IN PROG L signal has been asserted. This action forces the IR to 4 (JMS) and causes the decoder to assert the JMS line. Remember that INT IN PROG L also enables the data input of the EXECUTE flip-flop; thus, TP4 also sets the EXECUTE flip-flop. The processor enters the EXECUTE state and performs the JMS instruction, storing the program count in memory location 0, and entering the interrupt servicing routine. When the subroutine has been completed, the main program is resumed at the program count specified by memory location 0.

A data break device can request a break by asserting MS, IR DISABLE L at the same time (TP4) the IR flip-flops are dc-clocked to the JMS state. In this case, the data break device assumes control, and the processor enters the DMA state. On completion of the data break, the processor enters the EXECUTE state, performs the JMS instruction, and services the interrupting device, as outlined.

3.35 SOURCE CONTROL SIGNALS

3.35.1 Register In Enable Signals

The EN0 L, EN1 L, and EN2 L control signals are used to gate the 12 bits of the desired major register to the adder "register in" lines. Table 3-5 lists the usable combinations of these signals (in terms of voltage levels) and the register selected by each combination. The last entry of Table 3-5, which has EN0 L as a positive voltage level, gates an arithmetic 0 to the register in line. This condition occurs during TS3, when an OPR microinstruction or an IOT instruction is being carried out by the processor; in addition, a data break peripheral can cause such a condition to occur during TS2 of the DMA state.

Table 3-5
Register In Enable Signals

EN0 L	EN1 L	EN2 L	Input to Adder Register In Line
Low	Low	Low	PC Register
Low	Low	High	MD Lines
Low	High	Low	MQ Register (can be effected only by EAE option)
Low	High	High	CPMA Register
High	X	X	Arithmetic Zero

Note: X represents a "do not care" condition.

The logic gates used to generate the EN control signals are shown in Figure 3-90. To better understand processor operation, consider the logic diagrams as a means for understanding why a particular register is brought into the adder. For example, when all three signals are at a 0V level, the PC Register is gated to the adder. The processor flow diagram shows that the PC is transferred to the CPMA during TS4 of every major state. Thus, signals involved with TS4 should be examined.

The TS4 signal is the signal most likely to be used in gating the PC. This signal is applied to three separate NAND gates, E1A, E1B, and E3B. However, only E1B or E3B can, alone, cause all three EN signals to go to a ground level. E3B uses KEY CONTROL L as an enabling signal; KEY CONTROL L is asserted by the EXAM and DEP keys, both of which initiate a timing cycle. Thus, E3B produces the signals that gate the PC to the adder, thereby establishing a path from the PC to the CPMA during manual operation. E1B performs a NAND operation with two signals. One signal is a composite consisting of TS4, F SET L, and MS, IR DISABLE L. The F SET L signal indicates that the instruction is complete; MS, IR DISABLE L ensures that the current cycle is not a DMA state caused by a data break (if this is the case, the interrupted instruction may not have been completed prior to the data break; consequently, the PC must not be transferred to the CPMA). The other signal NANDed in E1B is (FE+FD) L. This signal is asserted either by the KE8-E option (operation in this circumstance is discussed in Volume 2), or by the INT IN PROG L signal. In the event that (FE+FD) L is negated, E1B produces the signals that establish a path from the PC to the CPMA during automatic operation.

If (FE+FD) L is asserted by INT IN PROG L, the PC is not transferred to the CPMA. Rather, the 0 location is loaded into the CPMA, and the processor goes into the EXECUTE state to carry out the JMS operation. During TS4 of this EXECUTE state, the PC is transferred to the CPMA.

In the process of carrying out the above JMS instruction, the processor must deposit the program count in location 0 (the PC must be transferred to the MB). Thus, the PC is gated to the adder. Inverter E8D causes the EN signals to be asserted during TS2 of the EXECUTE state of a JMS instruction. TS2 ensures that the PC data is on the MAJOR REGISTERS BUS before MB LOAD L is generated at TP2 time.

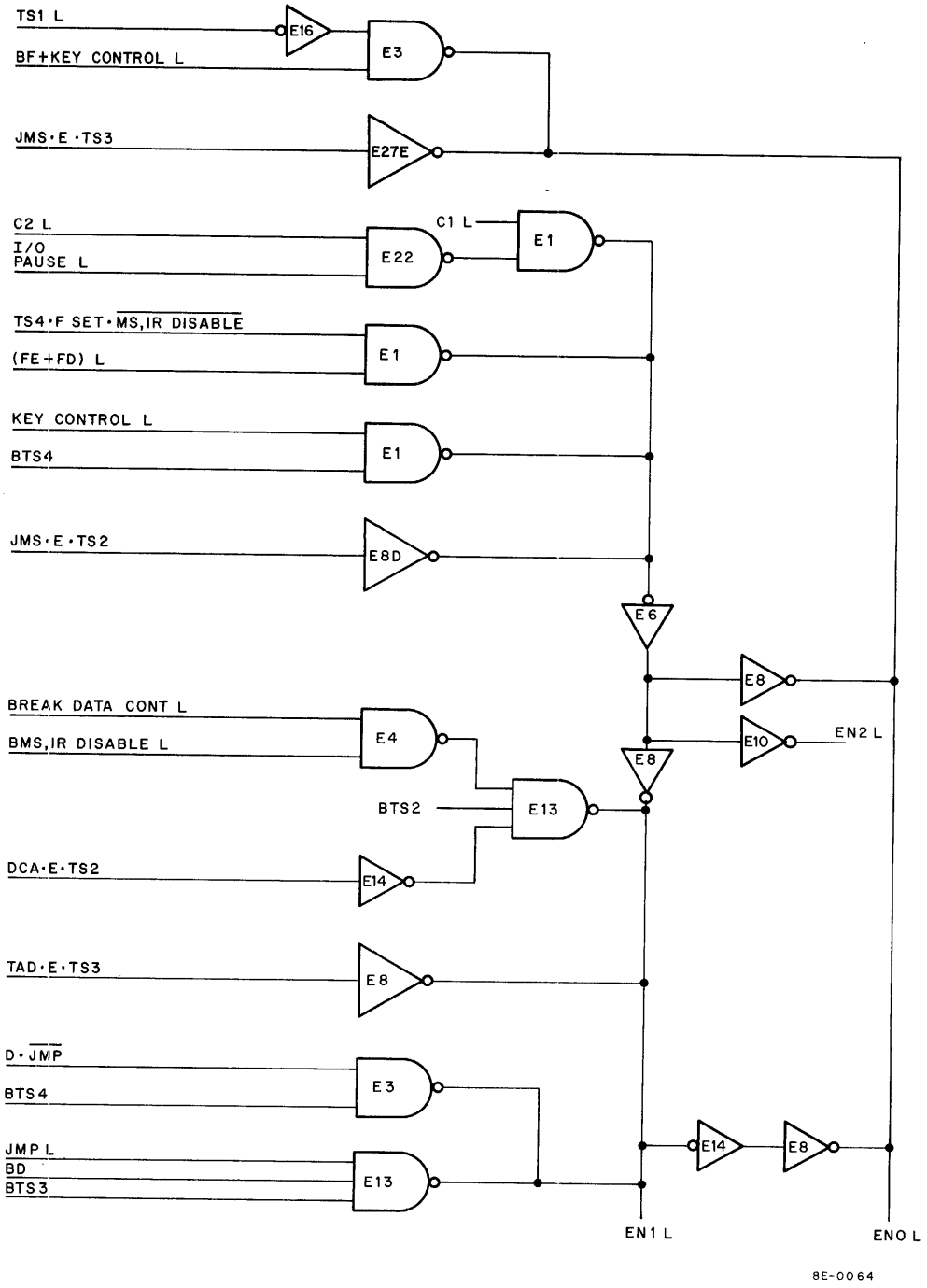


Figure 3-90 Register In Enable Logic

One remaining operation calls for the PC to be gated to the adder. A peripheral, through an IOT instruction, can change the program count in the PC Register by causing DATA+PC to the PC. NAND gates E22 and E1D assert the EN signals for this purpose. Further discussion of the C0 L, C1 L, C2 L, and I/O PAUSE L signal is presented in Section 6, I/O Transfer Logic.

If only EN0 is asserted, the CPMA Register is gated to the adder network (Table 3-5). As the logic indicates (Figure 3-90), the only way the processor can assert EN0, alone, is by enabling the wired-NOR consisting of NAND gate E3D and inverter E27. The signals used by this wired-NOR for gating the CPMA to the adder are described in the following paragraphs.

E3D is enabled during TS1 of the FETCH cycle or during TS1 when KEY CONTROL L is asserted (remember that the EXAM and DEP keys assert KEY CONTROL L). Thus, the CPMA is gated to the adder, making possible CPMA+1 to the PC during automatic and manual operation.

E27 asserts EN0 during TS3 of the EXECUTE state of a JMS instruction. The program count is stored in memory location 0000 when a JMS is forced by the INT IN PROG L signal. This sequence occurs during TS2 of the EXECUTE cycle. During TS3, the address in the CPMA, 0000, is incremented and sent to the PC. The new count, 0001, represents the address of the next instruction to be performed, and this instruction directs the processor to the starting address of the subroutine. Thus, when E27 asserts EN0, it allows CPMA+1 to be transferred to the PC during TS3 of the JMS instruction.

Table 3-5 indicates that the MQ Register can be gated to the "register in" line of the adder if EN0 and EN2 are brought to ground together. Note on the logic diagram (Figure 3-90) that this cannot be accomplished by any of the processor signals. MQ can be gated onto this line only by the KE8-E option (this feature is used by the SMA instruction). Thus, the remaining gates on the logic diagram are used to gate the MD lines to the adder, which is done by asserting both EN0 and EN1, while negating EN2. The MD lines are usually gated to the adder during TS2. The data from a memory location is transferred, either with or without modification, to the MAJOR REGISTERS BUS and loaded into the MB by TP2. NAND gate E13B causes EN1 and EN0 to be asserted during TS2 of all major states, with two exceptions. One of these exceptions occurs when the DCA instruction is being executed. To execute DCA, the processor must load the MB with the contents of the AC; thus, only the AC contents must be on the MAJOR REGISGERS BUS during TS2. The MB is loaded by TP2, the MD DIR L signal is negated, and the AC contents are written into the memory location. The other exception occurs during the DMA state (MS, IR DISABLE L is asserted), when the BRK DATA CONT L signal has not been asserted by a data break peripheral. Under these conditions, data is transferred by a peripheral to the DATA0 L–DATA11 L lines during TS2 and gated unchanged through the adder to the MAJOR REGISTERS BUS. At TP2 time, the data is loaded into the MB and then placed on the MD lines.

The processor flow diagram (Section 2) illustrates the operations that require the MD lines to be gated to the adder. MD to the MB is carried out during the FETCH state and during the non-autoindexed DEFER state, though the operation is meaningless. Because MD to the MB does not disrupt processor operations, it is more convenient to allow, rather than inhibit, its occurrence.

The MD lines are gated to the adder in three other instances: (a) During TS3, when a TAD instruction is being executed, both the MD lines and the contents of the AC are gated to the adder. The resulting sum is then placed on the MAJOR REGISTERS BUS and loaded into the AC by TP3. Inverter E8E allows EN0 and EN1 to be asserted in response to the (TAD·E·TS3) L signal. (b) When the processor is in the DEFER state of an indirectly addressed JMP instruction, the contents of the PC Register are changed to address the location of the next instruction to be performed. This address, the effective address of the JMP instruction, is placed on the MD lines.

The MD lines are gated through the adder to the MAJOR REGISTERS BUS during TS3, and then loaded into the PC by TP3. NAND gate E13A allows EN0 and EN1 to be asserted by the BTS3, BD, and JMP L signals. (c) MD → ADDER occurs also during the DEFER state; however, this instance specifically excludes the JMP instruction. If an AND, TAD, ISZ, DCA, or a JMS instruction has been indirectly addressed, the effective address is loaded in the CPMA, rather than the PC. The processor then goes to the EXECUTE state to operate on the data in the effective address. Thus, NAND gate E3B is enabled during TS4, thereby placing the effective address, contained on the MD lines, on the MAJOR REGISTERS BUS. TP4 then loads the address into the CPMA.

3.35.2 Data Line Enable Signals

The AC → BUS and MQ → BUS control signals are used to gate the 12 bits of the AC or MQ Registers to the DATA lines. The selected register can then be gated through the Data Control Gate to the "addend in" line of the adder.

The logic elements that produce MQ → BUS are shown in Figure 3-91. NAND gate E9A is used when the function select switch on the Programmer's Console is set to the MQ position. The console logic takes the IND2 line to ground and the IND1 line to a positive voltage. During TS1, the contents of the MQ are placed on the DATA 0 – DATA 11 lines and displayed on the Programmer's Console.

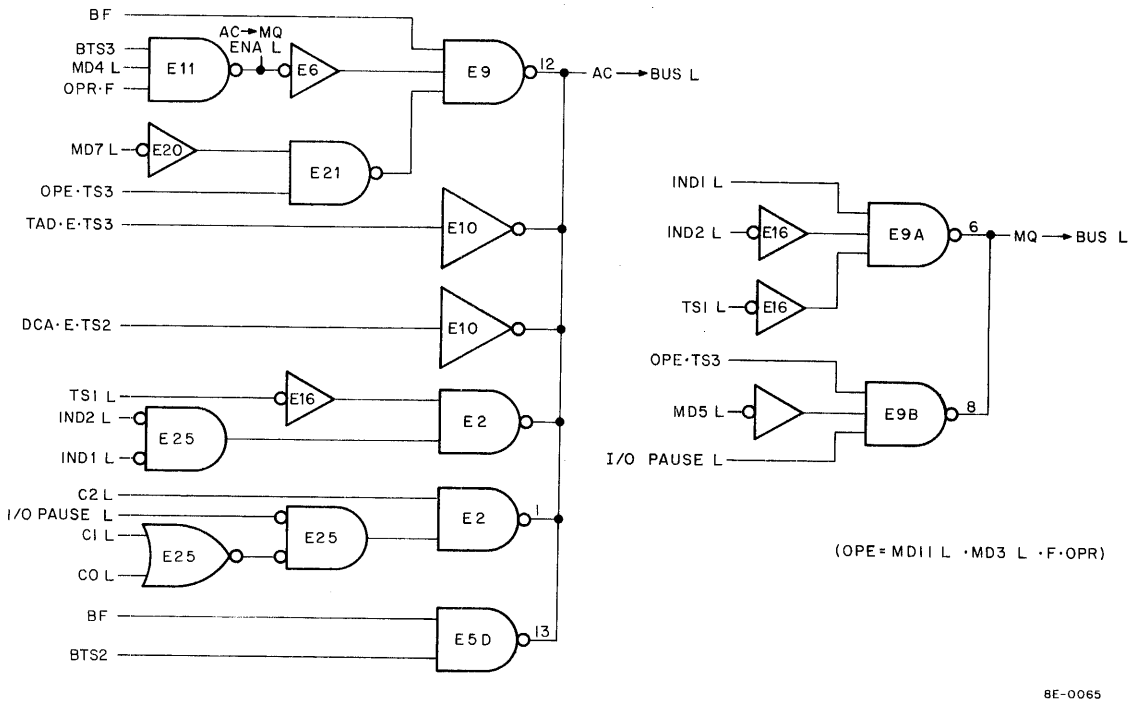


Figure 3-91 Data Line Enable Logic

NAND gate E9B is used to gate the MQ to the DATA lines for certain MQ microinstructions. Thus, this gate is enabled, provided the MQ BUS INH L signal is negated, for the following instructions: MQA, SWP, ACL, and CLA, SWP. The MQA instruction asserts both MQ → BUS and AC → BUS, a condition which causes an inclusive-OR to be performed by the Data Line Multiplexer. Each of the other MQ microinstructions asserts only MQ → BUS. The MQ contents are then gated through the data control gate to the adder, placed on the MAJOR REGISTERS BUS, and loaded into the AC by TP3.

The logic that produces AC → BUS is also shown in Figure 3-91. NAND gate E9C is used to gate the AC to the DATA lines during operate microinstructions. The AC contents are then gated to the adder, and the result of the arithmetic operation is loaded into the AC by TP3.

Inverters E10A and E10F assert AC → BUS during the EXECUTE state. E10A allows the AC to be gated to the adder during TS3 of a TAD instruction; also during TS3, the contents of the MD lines are gated to the adder by the Register In Enable logic. Thus, the 2's complement adding operation is effected, and the result is stored in the AC. E10F is used during TS2 of a DCA instruction. The contents of the AC are to be deposited in a memory location. To accomplish this, the contents of the AC must be placed on the MAJOR REGISTERS BUS before TP2. At TP2 time, the MB is loaded and the MD DIR L signal is negated, placing the AC contents on the MD lines in preparation for the WRITE operation.

NAND gate E5 asserts AC → BUS during TS2 of each FETCH cycle. This condition is not required by an instruction; however, it establishes the state of the AC lines at the positive I/O interface early in the FETCH cycle in order to maintain timing compatability with some older peripherals.

NAND gate E2C is used when the operator wishes to monitor the contents of the AC Register. During TS1, this information is placed on the DATA lines and used by the Programmer's Console logic.

E2B asserts AC → BUS when an IOT instruction directs a data transfer to a peripheral. In this case, I/O PAUSE L is asserted by the processor, the correct C lines are asserted by the peripheral, and the information on the DATA lines is strobed into a peripheral Buffer Register.

3.35.3 Data Enable Signals

The data enable signals, DATA T and DATA F, are used to determine the input for the addend in line of the adder. As indicated in the discussion of the data line enable signals, this input can be AC information, MQ information, or a combination of the two. The input can also be information that is being transferred from a peripheral to either the AC, PC, or MB. One other possibility exists: some operations require that the addend in line be an arithmetic 0. Therefore, the DATA T/DATA F signals are used to gate, to the adder, either the information carried on the DATA lines or an arithmetic 0. Table 3-6 is a truth table of these two signals (in terms of voltage levels); Figure 3-92 shows the logic that implements the truth table.

Table 3-6
Data Enable Signals

Signal		Explanation
DATA T	DATA F	Input to Adder "addend in" line
Low	Low	DATA LINES (complement of contents of AC or MQ Registers, I/O XFER DATA)
Low	High	DATA LINES (contents of AC or MQ Registers, I/O TRANSFER DATA)
High	High	7777 (not used)
High	Low	Arithmetic 0

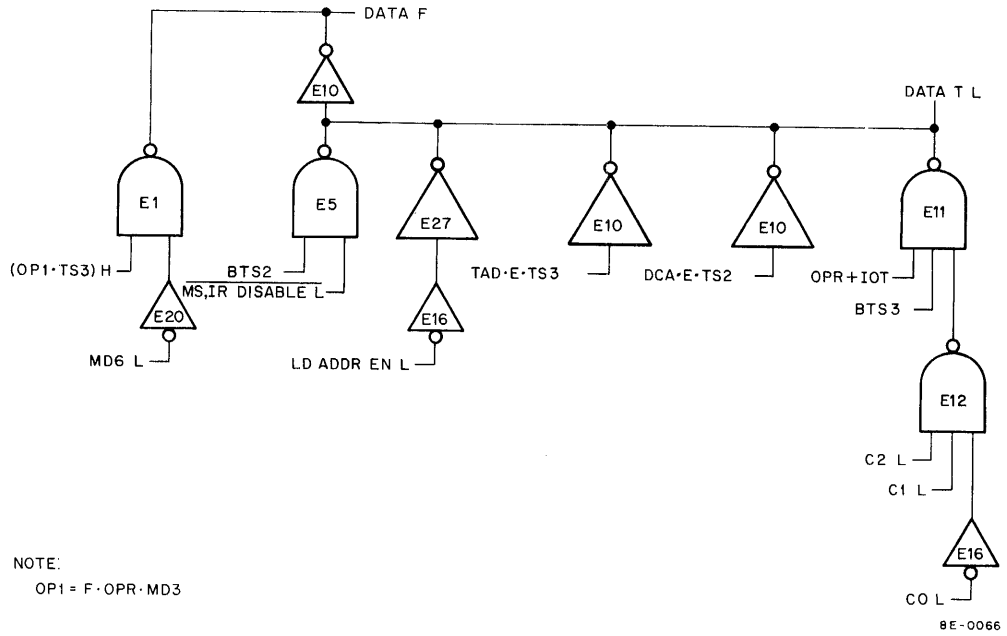


Figure 3-92 Data Enable Logic

Information on the DATA lines is often a result of implementation of an OPR or an IOT instruction. NAND gate E11 is used to assert DATA T in either case. If an IOT instruction has been decoded, DATA T is asserted, and DATA F remains negated. The transfer can be either into or out of the processor, depending on which C control line, if any, is asserted by the peripheral. If the C lines specify a transfer into the processor, the information is placed on the DATA lines by the peripheral, gated through the adder, and placed on the MAJOR REGISTERS BUS; the information is loaded into either the AC or the PC at TP3. If the transfer is out of the processor, the AC information on the DATA lines is gated into the peripheral's Buffer Register. However, the information must also be retained in the AC and, therefore, it is gated through the MAJOR REGISTERS BUS and again loaded into the AC by TP3.

In one case, an IOT instruction does not cause DATA T to be asserted via E11. If the peripheral asserts the CO L line, and leaves C1 L and C2 L negated, NAND gate E12 is enabled. Thus E11 is disabled, and, because no other gate enables DATA T under these circumstances, an arithmetic 0 is gated to the addend in line of the adder. This action results in an output data transfer and also a clearing of the AC, because 0s are loaded at TP3.

If an OPR microinstruction has been decoded, E11 is again used to assert DATA T, while DATA F is left negated. However, several OPR microinstructions (CMA, for example) are implemented by gating the complement of the signal on the DATA lines to the adder. This can be done if the DATA F signal is grounded along with DATA T. As Figure 3-92 shows, NAND gate E1 grounds DATA F; it does this only for those OPR microinstructions (CMA, CIA, CLA, CMA) that require the AC to be complemented.

DATA T can be asserted by any one of four other signals. One signal is (DCA·E·TS2) L, which asserts both AC → BUS and DATA T. Thus, the AC information is gated to the MAJOR REGISTERS BUS and loaded into the MB by TP2. After the AC information is transferred, the AC must be cleared by negating DATA T and, thereby, placing a 0 on the "addend line" line. Because a 0 is also placed on the "register in" line during TS3 of a DCA instruction, a 0 is placed on the MAJOR REGISTERS BUS. This is then loaded into the AC by TP3.

Another signal group that asserts both AC → BUS and DATA T is TAD•E•TS3. Thus, the AC information is gated to the adder, where it is added to the contents of a memory location; the result is then loaded into the AC by TP3.

The LOAD ADDR EN L signal asserts DATA T during manual loading of an address. The operator sets an address on the console switch register and depresses the LOAD ADDR key. This action places the address on the DATA lines, and DATA T gates it to the MAJOR REGISTERS BUS. The address is then loaded into the CPMA by the CPMA LOAD L signal.

The last method of asserting DATA T is with NAND gate E35. This gate provides a path to the adder for data that is being transferred to the MB, either from a data break peripheral or from the console switch register. TP2 then loads the data from the MAJOR REGISTERS BUS into the MB.

3.36 ROUTE CONTROL SIGNALS

3.36.1 Carry In Logic

The Carry In logic is shown in Figure 3-93. The CARRY IN L control signal enables the processor to increment data. The block diagram in Figure 3-87 shows that a CARRY IN L signal is applied to the adder IC (DEC 7483). This IC is a full adder and, therefore, can perform a complete addition by adding three inputs: an augend, an addend, and a carry from a previous order. In the PDP-8/E, the CARRY IN line of Figure 3-93 is applied directly to the carry input of adder 11, the LSB of the 12-bit data word. The carry from adder 11 is applied to adder 10, and so on, until the carry from adder 0 is applied to the LINK adder (Link logic is discussed in Paragraph 3.39).

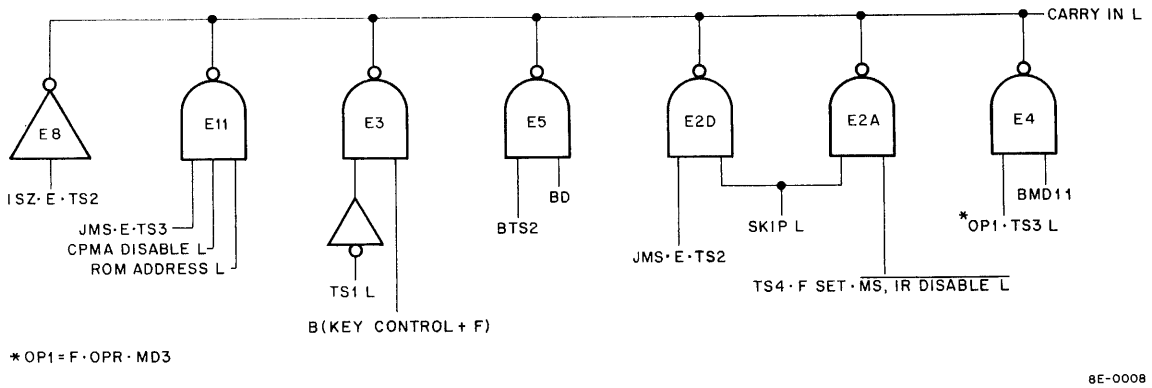


Figure 3-93 Carry In Logic

Data is incremented during various operations which were introduced in the discussion of the source control signals. For example, the address carried on the MA lines is incremented during TS1 of the FETCH cycle. This new address is then loaded into the PC Register at TP1, thereby updating the program counter. The operation is represented symbolically as MA+1 → PC and is carried out as follows: (a) the data on the MA lines is gated to the register in line of the adder (the augend); (b) a 0 is gated to the addend in line of the adder (the addend); and (c) a 1 is gated to the CARRY IN line of the adder by NAND gate E3. The result, MA+1, is placed on the MAJOR REGISTERS BUS and loaded into the PC by TP1; because this must happen at the beginning of each instruction, E3 is enabled by TS1 L and F L.

NAND gate E3 asserts CARRY IN L during automatic operation and during those manual operations that cause the KEY CONTROL L signal to be generated (Paragraph 3.33). Remember that KEY CONTROL L can be asserted by three Programmer's Console keys: DEP, EXAM, and EXTD ADDR LOAD. Because both DEP and EXAM initiate a single timing cycle, the PC is updated by 1 (MA+1 → PC) each time either of these keys is activated. The EXTD ADDR LOAD key also asserts KEY CONTROL L and, thus, CARRY IN L; however, both assertions are meaningless in the present application, because no timing cycle is initiated by EXTD ADDR LOAD L.

The program count must also be incremented during the EXECUTE cycle of a JMS instruction. The program count is stored in the memory location specified by the operand of the JMS instruction, e.g., location Y. The processor then proceeds to the first instruction of the subroutine. The address of this first instruction is contained in location Y+1; thus, the PC must be incremented and, as in the last example, the operation is represented symbolically as MA+1 → PC. This operation is accomplished during TS3 by NAND gate E11. The ROM ADDRESS L and CPMA DISABLE L signals are asserted if the MR8-E (Read-Only Memory) option is included in the system. Use of CARRY IN L with this option or with any option designed to assert CPMA DISABLE L only is discussed in Volume 2.

Inverter E8 asserts CARRY IN L in response to the signal ISZ•E•TS2. The ISZ instruction directs the processor to increment the data in the specified location and then skip the next instruction if the result of the incrementation is 0000. To increment the data, the processor performs the operation MD+1 → MB. The CARRY IN L line is asserted during TS2 of the EXECUTE cycle so that MD+1 can be loaded into the MB at TP2 time. The second portion of the ISZ instruction is carried out as described in Paragraph 3.38.

NAND gate E5 also asserts CARRY IN L. E5 does this during TS2 of a DEFER cycle and as part of the operation MD+1 → MB. Remember that this operation has significance during the DEFER cycle only if an Autoindex Register (locations 0010–0017) has been referenced by the instruction being performed. When this is the case, the content of this register is incremented before it is used as the operand. Autoindexing is discussed fully in Chapter 4 of the *PDP-8/E & PDP-8/M Small Computer Handbook.*

NAND gates E2A and E2D are used with the Skip logic (Paragraph 3.38) to assert CARRY IN L. Gate E2A asserts CARRY IN L when a skip of one program instruction (symbolized as PC+1 → CPMA) is required. This requirement arises if: (a) a Group 2 operate microinstruction such as SKP (skip unconditionally) is programmed; (b) if an IOT instruction causes a peripheral to assert the OMNIBUS SKIP L signal; and (c) as a result of the ISZ instruction. In each of these circumstances, TP3 sets the SKIP flip-flop, E13 (Paragraph 3.38), thereby asserting the SKIP (1) line high. During TS4, CARRY IN L is asserted, the PC is gated to the adder and incremented, and the result is placed on the MAJOR REGISTERS BUS and loaded into the CPMA at TP4. The F SET L portion of the enabling signal at E2A ensures that CARRY IN L is asserted only during the last cycle of the instruction. MS, IR DISABLE L is high and ensures that CARRY IN L is not asserted during TS4 of a DMA state. For example, if the program is stopped by the HALT key, the SKIP flip-flop can remain set. Then, if the operator pushes the EXAM key, CARRY IN L is asserted and PC+1, rather than PC only, is loaded into the CPMA at TP4 time of the memory cycle. MS, IR DISABLE L prevents this error from occurring because it is high.

NAND gate E2D is used to assert CARRY IN L if a program interrupt prevents gate E2A from asserting it. For example, if a Group 2 OPR microinstruction causes the SKIP flip-flop to be set at TP3, the PC should be incremented during TS4. However, if the interrupt system logic located in the Timing Generator has honored a peripheral's interrupt request, the OMNIBUS INT IN PROG H signal is also asserted at TP3. The assertion of INT IN PROG H prevents the PC from being gated to the adder network during TS4 (Paragraph 3.35.1). The CPMA is

loaded with 0s, rather than being loaded with the incremented PC contents at TP4. The processor then enters the EXECUTE state. During TS2, CARRY IN L is asserted by E2D, and the PC is gated to the adder and incremented. At TP2 the result (PC+1) is stored in location 0, and the SKIP flip-flop is reset. When the interrupt has been serviced, a JMP I to location 0 causes the main program to be resumed at location PC+1 (the original location if the interrupt had not been requested).

The last gate to consider in the Carry In logic is NAND gate E4. This gate is used during TS3 of a FETCH cycle to carry out operate instructions involving the IAC command. If IAC has been programmed, the contents of the AC are placed on the DATA lines during TS3 and gated through the Data Control Gate to the adder. A 0 is gated to the adder's register in line. E4 asserts CARRY IN L; the result, AC+1, is placed on the MAJOR REGISTERS BUS and loaded into the AC by TP3.

If CIA has been programmed, the operation is similar to that just outlined. However, the data in the AC is complemented by the Data Control Gate before it is applied to the addend in line of the adder. Thus, the result, $AC_{complement}+1$, is loaded into the AC at TP3.

When CLA IAC is programmed, 0s are provided at the addend in and register in lines of the adder. When CARRY IN L is asserted, the resulting output from the adder is 0001_8. This is loaded into the AC at TP3, setting AC=1. Similar operations occur when the IAC command is microprogrammed with other Group 1 operate instructions.

3.36.2 Shift Control Signals

The shift logic is shown in Figure 3-94. The control signals produced by this logic, RIGHT L, LEFT L, TWICE L, and PAGE Z L, gate data to the MAJOR REGISTERS BUS. This data can be taken from an adder, from a NAND gate, or from the PAGE Z multiplexer, as illustrated by the block diagram of Figure 3-87.

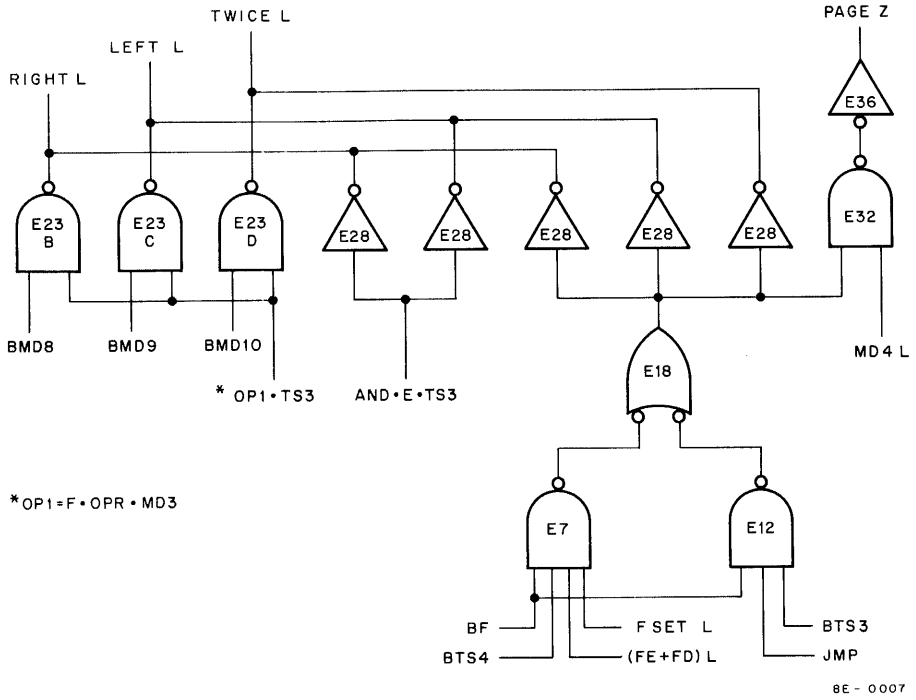


Figure 3-94 Shift Logic

A data bit can be transferred from one major register to another major register (Paragraph 3.34 where bit 0 was considered). To transfer bit 0 from one register to another, a "no shift" condition is needed by the Adder Output Multiplexer. As shown in Table 3-7, this condition arises when RIGHT L, LEFT L, and TWICE L are high, and PAGE Z L is low. Because most processor operations involve no shifting, this combination of signals normally prevails. A different combination can arise during either TS3 or TS4 of a FETCH cycle, with one exception. This exception, as shown on the logic diagram (Figure 3-94), occurs during TS3 of the EXECUTE cycle of an AND instruction and is discussed in the following paragraph. Thus, unless the program specifically requires a shifting operation, the shift signals remain as shown above. Shifting is a consequence of any one of five operate microinstructions (Paragraph 3.34). These microinstructions, RAR, RAL, RTR, RTL, and BSW, enable NAND gates E23B, E23C, and E23D in combinations that cause the desired shifting to occur. For example, if RAR (7010_8) (rotate AC and LINK right one) is programmed, NAND gate E23B is enabled during TS3 of the FETCH cycle. Bit X of the AC Register is placed on the DATA X line at the beginning of TS3, and gated through Data Control Gate X to adder X. A 0 is gated to the register in line of the adder. The adder CARRY IN line is negated. The adder X output is selected by Adder Output Multiplexer X+1, in response to the RIGHT L signal, and placed on MAJOR REGISTERS BUS X+1. At TP3 time, the data is loaded into bit X+1 of the AC Register. In the same manner, AC bit X can be shifted to the right twice (RTR) to AC bit X+2, to the right by six (BSW), or to the left in response to RTL, for example. All this shifting is accomplished by NAND gate E23.

RIGHT L, LEFT L, and TWICE L signals are used in operations other than shifting. Both RIGHT L and LEFT L are asserted by the composite signal AND•E•TS3, as illustrated in Figure 3-94. This combination enables each Adder Output Multiplexer to select the output of a NAND gate for transfer to the MAJOR REGISTERS BUS. This NAND gate is used to implement the basic AND instruction. During the EXECUTE cycle of this instruction, data in the addressed memory location is brought from memory and loaded into the MB Register at TP2 time. The MB Register output is logically NANDed with the AC Register output. During TS3, the logical result is gated through the Adder Output Multiplexer by RIGHT L and LEFT L signals to the MAJOR REGISTERS BUS and loaded into the AC at TP3 time.

Seven of the eight inputs to the Adder Output Multiplexer have been considered with respect to the shift signals. The eighth input is taken from the PAGE Z multiplexer (Figure 3-87). The gating networks for bits 0 through 4 use this multiplexer to provide the page address of the operand of either an MRI or an indirectly addressed JMP instruction. If this address is on the current page, the PAGE Z multiplexer output gates the data on MA lines 0 through 4 to the Adder Output Multiplexers. RIGHT L, LEFT L, and TWICE L signals gate these (0–4) bits to the MAJOR REGISTERS BUS. They are then loaded into CPMA 0 through 4, respectively, at TP4 time (this applies to an MRI; they are loaded into PC 0–4 and CPMA 0–4 for the JMP I instruction). Table 3-7, entry 8, lists the signal levels required to carry out this operation. This condition is implemented by gates E7, E13, E28, E32, and E36, shown in Figure 3-94. NAND E7 is enabled only during TS4 of a FETCH cycle. F SET L must be negated, ensuring that the instruction is either a JMP I or an MRI (if F SET L is negated, either a DEFER or an EXECUTE cycle follows the FETCH). The (FE+FD) L signal must also be negated. If the KE8-E option is not in the system, (FE+FD) L can be asserted only if the INT IN PROG H signal is asserted. Because INT IN PROG H is asserted only if F SET L is asserted, (FE+FD) L and F SET L are negated as a pair. The KE8-E option, by asserting FE SET L or FD SET L, can cause (FE+FD) L to be asserted even though F SET L is negated. Refer to Volume 2 for a further discussion.

Table 3-7
Shift Control Operations

RIGHT L	LEFT L	TWICE L	PAGE Z L	Input To Adder Output Multiplexer	Used For
HI	HI	HI	LO	ADDER X	No-Shift Operations
HI	LO	HI	LO	ADDER (X+1)	Rotate and Byte Swap Instructions
HI	LO	LO	LO	ADDER (X+2)	
LO	HI	HI	LO	ADDER (X-1)	
LO	HI	LO	LO	ADDER (X-2)	
HI	HI	LO	LO	ADDER (X+6)	
LO	LO	HI	LO	ACX, MBX → ACX·MBX	Logical AND Instruction (0000)
LO	LO	LO	LO	PAGE Z Multiplexer 0–4 to Adder Output Multiplexers 0–4. MA 0–4 loaded into CPMA 0–4 (or into PC 0–4).	Providing Page Address of operand of either an MRI or an indirectly addressed JMP instruction.
				MD Lines 0–11 to Adder Output Multiplexers 5–11, loaded into CPMA 5–11 (or PC 5–11).	Providing Relative Address of either of above.
LO	LO	LO	HI	PAGE Z Multiplexer 0–4 to Adder Output Multiplexer 0–4. 0s loaded into CPMA 0–4 (or into PC 0–4).	Providing Page Address
				MD lines 5–11 to Adder Output Multiplexer 5–11, loaded into CPMA 5–11 (or PC 5–11).	Providing Relative Address

NOR gate E18 is enabled, and the high level at its output causes inverter E28 to assert RIGHT L, LEFT L, and TWICE L. This high level is also applied to E32, where it is NANDed with the signal representing the state of MD4 L. If MD4 L is asserted (the address of the operand is on the current page) PAGE Z L is negated. The data on MA lines 0–4 is loaded into CPMA 0–4 at TP4 time. However, if MD4 L is negated (the address of the operand is on page 0), PAGE Z L is asserted. In this case, the PAGE Z multiplexer provides arithmetic 0s for the Adder Output Multiplexer; these 0s are loaded into CPMA 0–4 at TP4 time.

The PAGE Z multiplexer is also used to provide the page address of an indirectly addressed JMP instruction. This operation is carried out in the same manner as described for the MRI. If the JMP instruction is directly addressed, it is carried out in one cycle of operation. Thus, NAND gate E12 is used to assert the RIGHT L, LEFT L, and TWICE L signal lines. As before, MD4 L can be asserted or negated. If this line is asserted, the data on MA lines 0–4 is placed on the MAJOR REGISTERS BUS and loaded into the PC Register (bits 0–4, respectively) at TP3 time. If MD4 L is negated, 0s are loaded into PC 0–4.

To specify the complete address to which the program must jump, the relative address specified by bits 5 through 11 of the JMP instruction must be loaded into PC 5–11. Bits 5 through 11 of the major register gating do not use a PAGE Z multiplexer. Instead, MD lines 5–11 are connected directly to Adder Output Multiplexers 5–11. Whenever RIGHT L, LEFT L, and TWICE L are asserted by the JMP instruction, the data carried on MD lines 5–11 is selected by the Adder Output Multiplexer, placed on the MAJOR REGISTERS BUS, and loaded into PC 5–11 by TP3. The program control is then transferred to this new location, if the JMP instruction is directly addressed. If it is indirectly addressed, the data on MD lines 5–11 is gated to the MAJOR REGISTERS BUS during TS4 and loaded into CPMA 5–11 at TP4 time.

Similarly, when the instruction is an MRI, the data on MD lines 5–11 is placed on the MAJOR REGISTERS BUS during TS4. It is then loaded into CPMA 5–11 at TP4, providing the CPMA with the absolute address of the operand.

3.37 DESTINATION CONTROL SIGNALS

The destination control signals load data into the major registers. Data is placed on the MAJOR REGISTERS BUS during time states and loaded into a specific major register by a specific time pulse. Thus, TP1 loads only the PC Register, TP2 loads only the MB Register, TP3 loads the AC Register, primarily (it also loads the PC, if certain conditions are met), and TP4 loads only the CPMA Register. The fifth major register, MQ, is also loaded by TP3, but not from the MAJOR REGISTERS BUS. Because of the unique manner in which data is transferred to the MQ, Paragraph 3.40 is devoted to this major register; the MQ LOAD L signal is also discussed there.

3.37.1 MB LOAD L

The logic used to provide the MB LOAD L signal is shown in Figure 3-95. The MB is loaded only at TP2 time, but at *every* TP2. Thus, data placed on the MAJOR REGISTERS BUS during TS2 of any cycle is loaded into the MB Register by inverter E48.

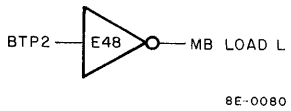


Figure 3-95 MB LOAD L Logic

3.37.2 AC LOAD L

The logic used to provide the AC LOAD L signal is shown in Figure 3-96. NAND gate E15D is used to provide the AC LOAD L signal during an IOT transfer. A detailed discussion of the use of AC LOAD L during an IOT transfer can be found in Section 6 of this chapter. The remainder of this discussion is concerned with how NAND gate E15C is used to assert AC LOAD L.

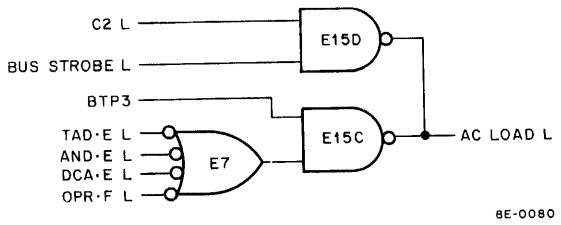


Figure 3-96 AC LOAD L Logic

Note that this load signal is generated at TP3 time. Thus, data that is to be loaded into the AC must be placed on the MAJOR REGISTERS BUS during TS3 time. If a TAD instruction is being executed, data in the AC is gated to the addend in line of the adder, while data on the MD lines is gated to the register in line of the adder (remember all gating is accomplished by the composite signal TAD·E·TS3). The result from the adder is a 2's complement sum of the two quantities. This sum is placed on the MAJOR REGISTERS BUS (all the shift signals are negated) and loaded into the AC at TP3 time.

If an AND instruction is being executed, the RIGHT L and LEFT L shift signals are asserted by AND·E·TS3, as described in Paragraph 3.36.2. The result obtained by NANDing the AC and the MB is gated to the MAJOR REGISTERS BUS and, again, the AC is loaded at TP3 time.

When a DCA instruction is being executed, the source control signals gate 0s to the adders during TS3. The 0 from the adder is placed on the MAJOR REGISTERS BUS and loaded by TP3.

Finally, all operate microinstructions cause the AC to be loaded at TP3 time, which occurs even when the microinstruction does not involve the AC (CML, for example). In this case, the AC is loaded at TP3 time with the same word that it contained prior to TP3 (the operation can be represented as AC → AC).

3.37.3 PC LOAD L

The logic used to provide the PC LOAD L signal is shown in Figure 3-97. NAND gate E15 is used during an IOT transfer and is discussed fully in Section 6 of this chapter. Note that PC LOAD L can be asserted at either TP1 or TP3 time. E53B is enabled by TP1 of a FETCH cycle or by TP1 of a key-initiated DMA cycle (KEY CONTROL is asserted by the DEP key and by the EXAM key; each key initiates a single DMA cycle). During TS1 of a FETCH cycle or of a key-initiated DMA cycle, the data on the MA lines is gated to the adder. The CAR IN L signal is asserted, and the output from the adder, MA+1, is gated through the Adder Output Multiplexer by the no-shift condition. TP1 then enables E53B to assert PC LOAD L, and MA+1 is loaded into the PC, updating the program count. NAND gates E53A and C assert PC LOAD L at TP3 time. E53A is used with the JMP housekeeping instruction. During TS3 of the FETCH cycle of a JMP instruction, an absolute address is gated onto the MAJOR REGISTERS BUS by the shift signals (Paragraph 3.36.2). This address gives the memory location from which the next program instruction is to be taken. At TP3 time, E53A asserts PC LOAD L, and the new program count is loaded into the PC Register.

NAND gate E53C asserts PC LOAD L at TP3 to load either MA+1 or MA into the PC. The address that is loaded into the PC is that of the first instruction of the subroutine to which program control is being transferred (Paragraph 3.36.1).

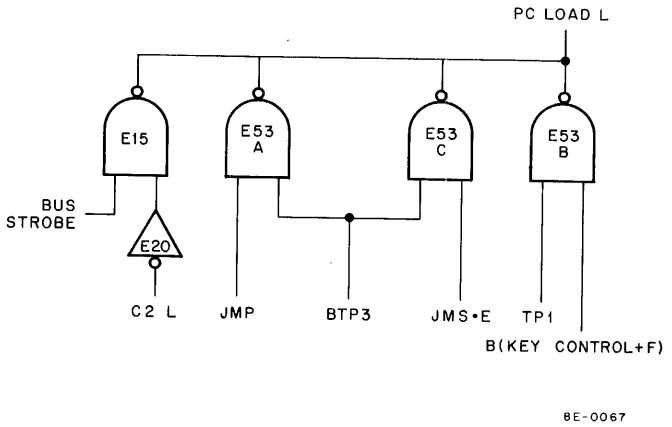


Figure 3-97 PC LOAD Logic

3.37.4 CPMA LOAD L

The logic used to provide the CPMA LOAD L signal is shown in Figure 3-98. Although only two gates are used, a variety of operations are involved. NAND gate E52 is used with the ADDR LOAD key. When the key is depressed, the address represented by the console switch register keys is gated to the MAJOR REGISTERS BUS. PULSE LA then enables E52, and the address is loaded into the CPMA.

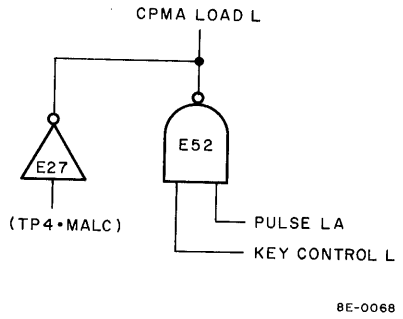


Figure 3-98 CPMA LOAD Logic

Inverter E27 asserts CPMA LOAD L when signal TP4•MA,MS LOAD CONTROL L is high. Thus, CPMA LOAD L is asserted by each TP4 pulse, with only one exception. This exception is the TP4 pulse that occurs during a peripheral-induced DMA state. The MA,MS LOAD CONTROL L signal is grounded by the peripheral to ensure that the processor returns to the correct major state at the end of the data break (see Paragraph 3.34.1 for more details).

The data loaded into the CPMA at TP4 time is always an address. If the instruction being performed is in its concluding cycle, or if the cycle is a DMA state, this address specifies the succeeding memory location. Because this address is being transferred from the PC Register, the operation is represented as PC → CPMA (it can also be represented as PC+1 → CPMA, an operation that involves the Carry In logic and the Skip logic; this operation is detailed in subsequent paragraphs).

If the request of a peripheral for a program interrupt has resulted in the INT IN PROG signal being asserted, the address loaded into the CPMA at TP4 time is 0000. The PC address is then stored in this memory location while the interrupting peripheral is serviced (Paragraph 3.35.1).

If the processor is in the FETCH state of either an MRI or an indirectly addressed JMP instruction, or is in the DEFER state of an indirectly addressed MRI, the address loaded into the CPMA at TP4 time specifies the memory location of the operand. If the processor is in the DEFER state, the operation is represented as MD → CPMA (Paragraph 3.35.1). If the processor is in the FETCH state, the operation is represented as either MA 0–4 → CPMA 0–4, MD 5–11 → CPMA 5–11, or 0 → CPMA 0–4, MD 5–11 → CPMA 5–11 (Paragraph 3.36.2).

3.38 SKIP LOGIC

The Skip logic, shown in Figure 3-99, is used to sample the contents of the AC Register and/or LINK, and the state of the OMNIBUS SKIP line. If the sampled data satisfies specified conditions, the program count is incremented before it is transferred to the CPMA at TP4 time. Thus, the next program instruction is skipped.

The Skip operation is used primarily during the implementation of operate microinstructions. As the PDP-8/E instruction list indicates, the majority of the Group 2 operate microinstructions, and nearly half of the combined operate microinstructions, involve the Skip instruction. Thus, the greater part of the logic shown in Figure 3-99 is devoted to implementation of these Skip microinstructions.

Consider the Group 2 microinstruction SMA (7500) (skip on minus AC). Remember that minus numbers in the PDP-8/E are those between 4000_8 and 7777_8, bit 0 is a 1. The AC0 bit is sampled by NAND gate E5. Therefore, when the AC contains a minus number, E5 is enabled by the SMA microinstruction (BMD5 H is asserted by SMA). The exclusive-OR gate E38 provides a high output because only one of its input signals, MD8 L (which is negated by SMA), is high. Because (OP2·TS3) is always high for the operate Skip microinstructions, NAND gate E3 is enabled, and the data (D) input of flip-flop E17 is high. At TP3 time, E17 is set, and the SKIP L (1) signal is applied to the Carry In logic. The Carry In logic causes the program count to be incremented before being transferred to the CPMA at TP4 time (Paragraph 3.36.1).

If the program specifies SPA (skip on plus AC), E5 is disabled because AC0 L is now low; E4 and E43 are also disabled. However, E38 still provides a high output, because MD8 L is now asserted. The D input of flip-flop E17 is again high, and BTP3 sets the flip-flop. Each operate Skip microinstruction that involves sampling of the AC and/or LINK, as well as the unconditional Skip microinstruction, SKP, is implemented in a manner similar to that outlined for SMA and SPA. In all cases, exclusive-OR E38 provides a high output signal if the SKIP condition is met, thereby enabling E3. NOR gate E12 provides a high input at the D line of E17, and BTP3 sets the flip-flop.

The Skip logic is also used to sample the state of the OMNIBUS SKIP line. During an I/O transfer (IOT L is asserted), a peripheral may assert the SKIP L signal. This action enables NAND gate E22, causing E17 to be set at TP3 time. This ultimately results in a skip of the next program instruction (the procedure is explained in detail in Paragraph 3.41.3). The SKIP L signal can also be asserted by the KE8-E option, as discussed in Volume 2.

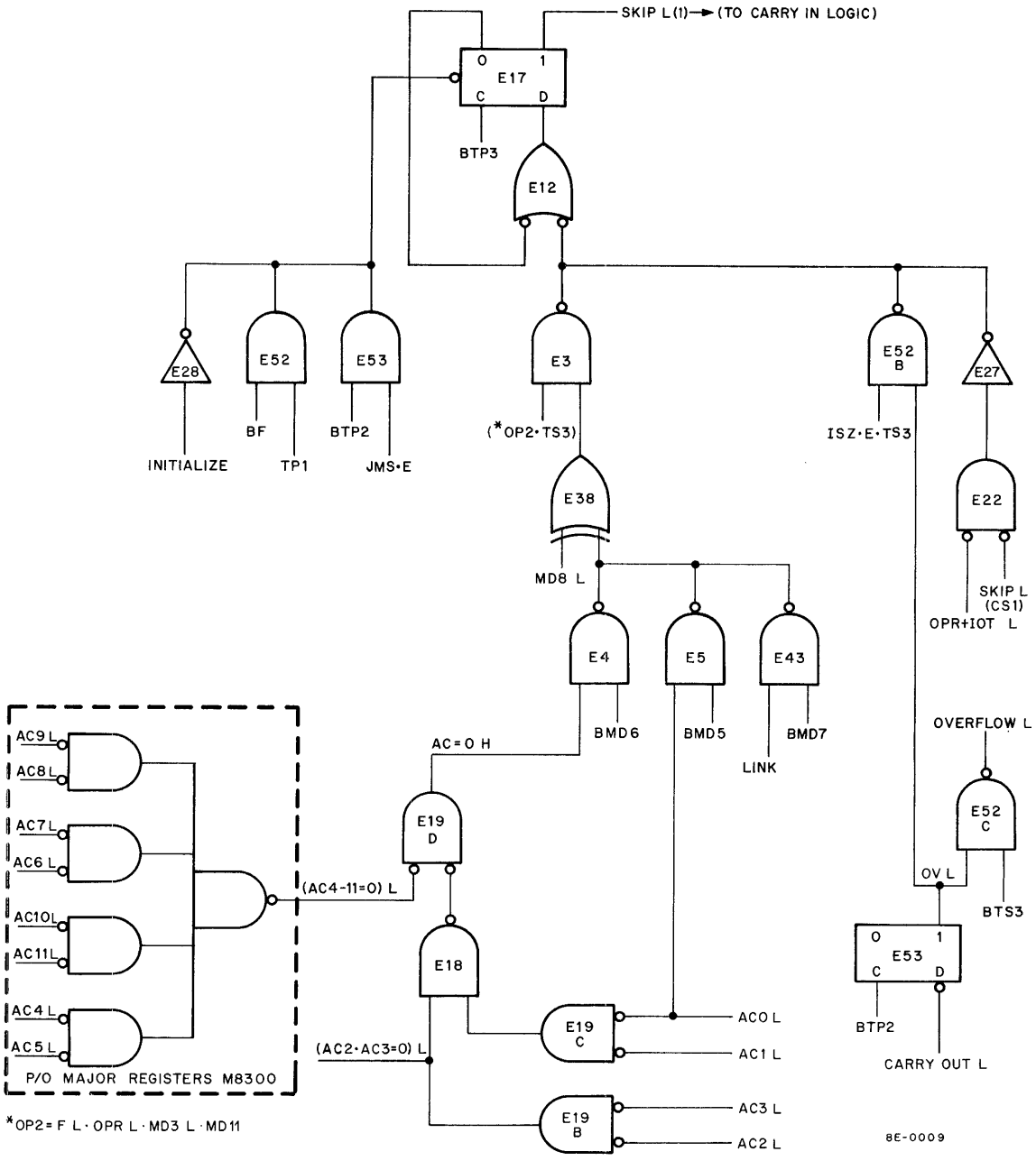


Figure 3-99 Skip Logic

Only one MRI (the ISZ instruction) causes the SKIP flip-flop, E17, to be set. The composite signal (ISZ·E·TS3) enables NAND gate E52B if E33, the OVERFLOW flip-flop, is active (Figure 3-99). The signal (ISZ·E·TS2) causes the CARRY IN L signal to be asserted, incrementing the operand of the MRI (Paragraph 3.36.1). If the result of this incrementation is 0000_8 (the operand must have been 7777_8), a carry out from adder 0 is generated. The CAR OUT L signal is applied to flip-flop E33, as shown in the logic diagram. BTP2 then sets E33. During TS3, E52B is enabled; thus, flip-flop E17 can be set by BTP3. SKIP(1) causes the CARRY IN L signal to again be asserted and to increment the program count. Thus, the ISZ instruction causes CARRY IN L to be asserted twice during the EXECUTE cycle.

Note that the 1 output of E33 is also applied to NAND gate E52C. During TS3, this gate is enabled, thereby grounding the OMNIBUS OVERFLOW line. This line is used by peripherals, and a further description can be found in Section 6 of this chapter.

Note that the SKIP flip-flop, E17, can be dc-reset in three ways: (a) it is reset whenever the INITIALIZE signal is asserted. This occurs when power is turned on or off, when the CLEAR key is depressed, or when the CAF instruction is programmed; (b) TP1 of each FETCH state resets it; (c) TP2 resets it when a JMS instruction is being executed (for details on the need for this reset see Paragraph 3.36.1, under the discussion of NAND gates E2A and E2D, see Figure 3-93).

3.39 LINK LOGIC

The Link is used with a TAD instruction or with Group 1 operate and combined operate microinstructions. The TAD instruction causes the content of the AC, a binary number, to be added to the content of a specified memory location, another binary number. Both binary numbers may be negative numbers (the MSB is a 1). Therefore, the addition may result in a carry from adder 0. Because this carry is significant to the result of the addition, it is gated to, and complements, the LINK flip-flop. The flip-flop can then be manipulated by the Group 1 operate microinstructions and used in other AC operations.

The Group 1 microinstructions can be used to clear and complement the LINK independently of the AC, or to rotate the LINK bit right or left along with the contents of the AC. In addition, the LINK can be complemented in response to the IAC microinstruction, providing the number in the AC is 7777 (−1) before incrementation.

The Link logic is shown in Figure 3-100. Note that the LINK flip-flop, E33, can be clocked if either NAND gate E43C or NAND gate E43D is enabled. The gate E43D is enabled if LINK LOAD L is asserted. LINK LOAD L and LINK DATA L are controlled by the RTF (restore interrupt flags) IOT instruction. RTF and its companion instruction, GTF (get interrupt flags), are designed primarily for use with the KE8-E and/or KM8-E options. These instructions are discussed only as they pertain to the loading of the LINK flip-flop.

The GTF instruction causes the state of the LINK bit to be placed on the DATA 0 L line. This data, and the information that is placed on DATA lines 1–11, is then loaded into the AC at TP3 time. The contents of the AC can be stored in some location until it is needed. At this later time, an RTF instruction can be issued. As the Link logic shows, the previous state of the LINK bit is placed on the Link Data line and gated through E32A to the D input of E33 (note that because RTF is an IOT instruction, NAND gate E30, at the Link Multiplexer output, is disabled). At TP3 time, LINK LOAD L is asserted and the previous LINK state is loaded back into E33.

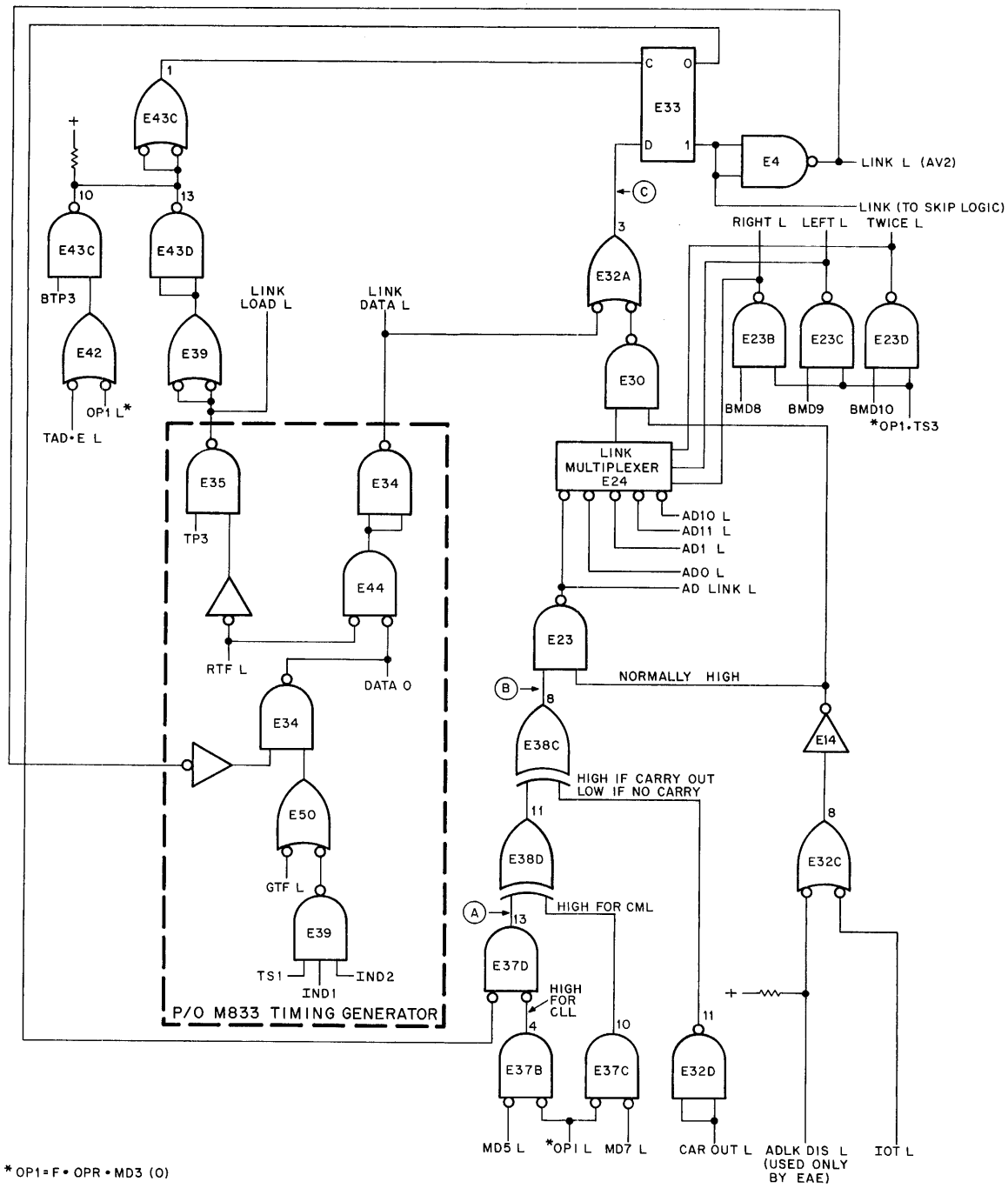


Figure 3-100 Link Logic

As previously discussed, the LINK is used with the TAD instruction and with Group 1 operate microinstructions (MD3 L is negated). Thus, when either (TAD•E) L or OP1 L is asserted, NAND gate E43C is enabled by BTP3, and E33 is clocked.

The Link can be rotated along with the AC. Therefore, the Link logic must contain a multiplexer similar to the Adder Output Multiplexers of the major register gating network. This required multiplexer is shown in Figure 3-100 as the Link Multiplexer, E24. Note that there are five distinct inputs to E24; four of these are from outputs of adders in the major register gating network. The fifth input is from the Link gating network (ICs E23, E32, E37, and E38), and is connected by the AD LINK L line to an input of Adder Output Multiplexers 0, 1, 10, and 11 in major register gating. When a rotate microinstruction is programmed, the shift signals, RIGHT L, LEFT L, and TWICE L, select only one of the four adder outputs, thereby enabling the logic level from this adder to be placed on the Link line. At the same time, the previous state of the Link line is selected by one of the Adder Output Multiplexers and placed on the MAJOR REGISTERS BUS for loading into the AC. For example, if RAR is programmed, the shift signals select the logic signal on the ADII L line (this signal reflects the contents of AC11). A signal representing this logic level is gated to the D input of the LINK flip-flop. When the LINK flip-flop is clocked, the logic level previously contained in AC11 is placed on the Link line. At the same time, the AD LINK input is selected by the shift signals at Adder Output Multiplexer. A signal representing the previous logic state of the Link line is placed on MAJOR REGISTERS BUS 0. At TP3 time, the AC is loaded and AC0 then contains the logic level previously carried on the Link line. Note that, because there is no connection between AD LINK L and Adder Output Multiplexer 5, and none between AD6 L and the Link Multiplexer, the Link line is unaffected by the BSW instruction.

To carry out the rotate instruction, the Link gating must place the state of the Link line on the AD LINK line. However, if a programmed microinstruction directs that the Link be cleared (the Link line negated), a high signal must be gated to the AD LINK line (E24's no-shift input). Finally, if a Group 1 microinstruction or a TAD instruction directs that the Link line be complemented, the complement must be placed at the AD LINK L input of E24. Because the Link gating must accomplish these tasks, the gating processes are relatively intricate. Three NAND gates, E37B, E37C, and E32D, are keys in the gating network. The various combinations of the enabled and disabled states of these gates determine whether the Link line is negated, complemented, or left unchanged. The output of E37B is low unless an operate instruction involving the CLL instruction is present; the output gate of E37C is high for the CML instruction; the output of E32D is low unless there is a carry from the adders; and the output of E14 is high for all except IOT and EAE instructions.

The outputs of the two exclusive OR gates E38C and E38D are low if their inputs are of the same logic level. If the inputs are different, the output is high. If there is no CML instruction, and no carry out from the adders, the logic level at point B is the same as the logic level at point A. If either a CML instruction or a carry out is present, $B \neq A$. If both CML and carry out are present (an extremely rare occurrence), $A = B$.

Table 3-8 is a learning aid and possible maintenance tool. This table lists the various gates of the Link gating network, along with the output to be expected from each under the conditions specified at the top of the table. For example, the CMA instruction should have no effect on the state of the Link line. However, the LINK flip-flop is clocked whenever the CMA instruction is programmed; therefore, the state of the flip-flop's D input must be such that the flip-flop is unchanged by the clock pulse. The level to be expected at the D input is found in the column headed BSW, etc. This level is the complement of the level on the Link line. If LINK L is asserted (a low level), the D input is high. At TP3 time, the flip-flop is set, as it was before TP3.

Table 3-8
Link Logic Gating Levels

Intended Operation / Gate State or Output	Complement Link (Group 1 Microinstruction)	Complement Link (CAR OUT L Asserted)	Rotate Link (Shift Signals Asserted)	Clear Link	BSW, CLA, NOP, CMA
E37B NAND	Disabled	Disabled	Disabled	Enabled	Disabled
E37C NAND	Enabled	Disabled	Disabled	Disabled	Disabled
E37D NAND	Output is complement of level on Link line	Output is complement of level on Link line	Output is complement of level on Link line	Output is LO regardless of level on Link line	Output is complement of level on Link line
E38D EXCLUSIVE-OR	Output is same as level on Link line	Output is complement of level on Link line	Output is complement of level on Link line	Output is LO regardless of level on Link line	Output is complement of level on Link line
E32D NAND	Enabled	Disabled	Enabled	Enabled	Enabled
E38C EXCLUSIVE-OR	Output is present level on Link line	Output is present level on Link line	Output is complement of level on Link line	Output is LO regardless of level on Link line	Output is complement of level on Link line
E32C NOR	Disabled	Disabled	Disabled	Disabled	Disabled
AD LINK LINE	Complement of level on Link line	Complement of level on Link line	Same as level on Link line	HI level regardless of level on Link line	Same as level on Link line
LINK F/F D INPUT	Same as level on Link line	Same as level on Link line	Complement of level on selected ADX line	LO level regardless of level on Link line	Complement of level on Link line
RESULT	Link line assumes, at TP3 the complement of its present level	Link line assumes, at TP3, the complement of its present level	Link line assumes level of selected ADX line at TP3	Link line assumes a HI level at TP3	Link line remains at same level

3.40 MQ REGISTER LOGIC

The MQ Register was briefly discussed in Paragraph 3.35. The MQ acts as an extension of the AC during Extended Arithmetic Element (EAE) operations. Only in this capacity does the MQ fulfill its potential. However, because the register is included in the basic machine, it provides the programmer with a temporary storage register and increases the processing power of the AC. Consequently, the eight MQ instructions, discussed in Paragraph 3.35.2, are included in the instruction repertoire of the basic PDP-8/E.

In carrying out these eight MQ instructions, the AC and MQ must transfer information from one to the other. The MQ is represented in the block diagram in Figure 3-87. Note that the MQ does not monitor the MAJOR REGISTERS BUS; therefore, to transfer the contents of the AC to the MQ, another data path must be provided as shown in the MQ logic gating for bit 0 (Figure 3-101). The AC data is transferred to the MQ via the MQ multiplexer, E12, and the right-shift gate, E17. Data to be transferred from the MQ to the AC is gated through the major register gating network to the MAJOR REGISTERS BUS. The logic used to generate the MQ control signals is shown in Figure 3-102. Some of these signals have been discussed in relation to other processor operations. The pecularities of this logic, when related to implementation of the MQ instructions, are discussed in this section.

Consider the MQ instruction CLA SWP, 7721 – transfer MQ to the AC, clear the MQ. The MQ data must be gated through the major register gating network to the MAJOR REGISTERS BUS during TS3 and loaded into the AC at TP3. There are two paths to the major register gating for the MQ (Figure 3-101). The path that goes to Register Input Multiplexer 0 is used only with the EAE option, during implementation of the SAM instruction. Thus, CLA SWP must cause the MQ data to be placed on the DATA 0 line for transfer to Data Control Gate 0. The MQ → BUS L control signal must be asserted, which is done by NAND gate E9B (I/O PAUSE L is asserted only during an IOT instruction). Note that at the same time AC → BUS L is negated by E9C (E21 is enabled, E11 is disabled). The MQ0 bit is gated to the MAJOR REGISTERS BUS and loaded into the AC at TP3. To complete the instruction, the MQ must now be cleared (0 → MQ), which is accomplished if SHL ENA L, RIGHT L, and AC → MQ ENA L are negated. The first two signals are asserted only by the EAE option, when considering the MQ. The last, AC → MQ ENA L, is controlled by NAND gate E11; as noted previously, this gate is disabled during CLA SWP (MD4 L is asserted). Therefore, AC → MQ ENA L is negated. These three control signals, when negated, cause a 0 (positive voltage) to be applied to the data (D) input of the MQ0 flip-flop. MQ LOAD L, at TP3, then clears the flip-flop.

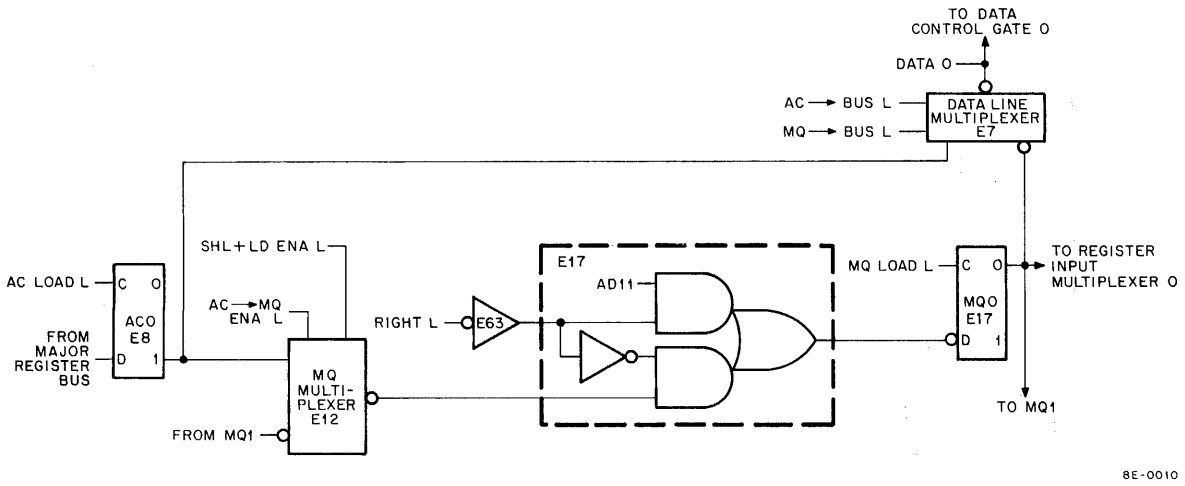


Figure 3-101 MQ Logic

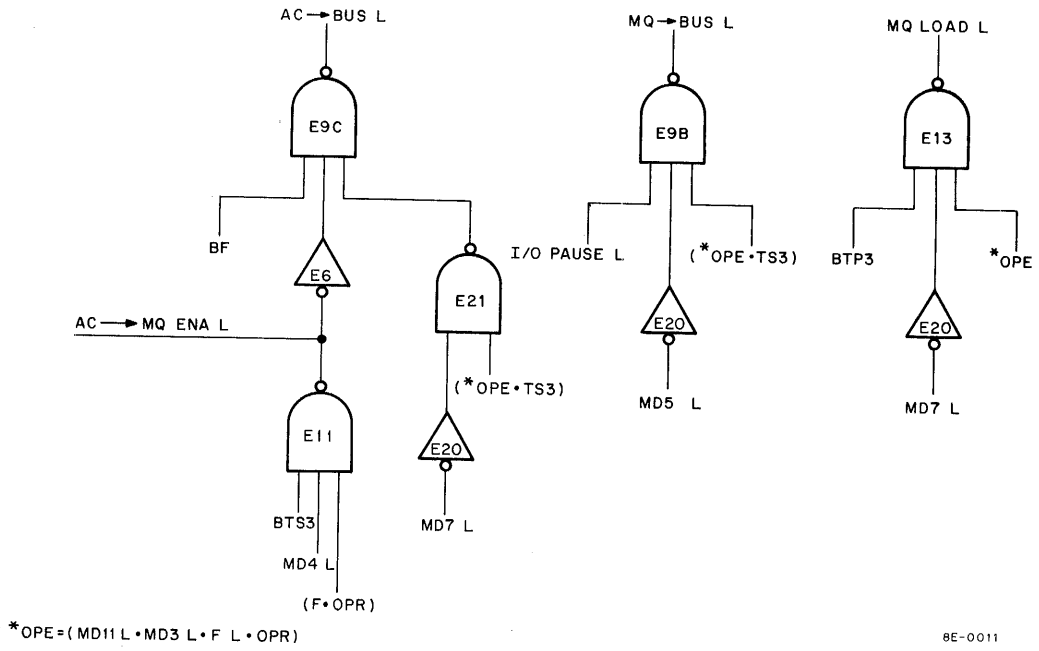


Figure 3-102 MQ Gating Control Logic

If ACL, 7701 (transfer MQ to the AC), is programmed, the operation is similar to CLA SWP. MQ → BUS L is asserted, and AC → BUS L is negated (E11 is disabled). MQ0 is loaded into AC0 at TP3. SHL ENA L, AC → MQ ENA L and RIGHT L are again negated. To prevent the MQ from being cleared, as it is during CLA SWP, the MQ LOAD L is negated (MD7 L is negated). Thus, the MQ retains the data, in addition to transferring it to the AC.

If SWP, 7521, is programmed, simultaneous transfers are required. Thus, the MQ is transferred to the AC as described, while the AC is transferred to the MQ via the MQ multiplexer, E12. This multiplexer gates the AC0 bit to E17, if AC → MQ ENA L is asserted and SHL ENA L is negated. The MQ transfer is negated unless asserted by the EAE. The AC transfer is asserted by NAND E11 in the AC → BUS L logic (AC → BUS L is negated by E21). If RIGHT L is negated (as it is, unless asserted by the EAE), the output of E17 reflects the state of the AC0 flip-flop. MQ LOAD then loads the MQ0 flip-flop with the AC0 data. At the same time, the AC0 flip-flop is being loaded with the MQ0 data.

The rest of the MQ instructions are implemented by carrying out one or another of the operations described in CLA, SWP, ACL, and SWP. These instructions are outlined in the following paragraph. The method through which the operations are implemented is not discussed.

The MQL instruction negates both AC → BUS L and MQ → BUS L, while asserting AC → MQ ENA L. The MQA instruction asserts both AC → BUS L and MQ → BUS L, while negating MQ LOAD (AC → MQ ENA L is asserted, but has no significance). The CAM instruction negates AC → BUS L, MQ → BUS L, and AC → MQ ENA L. The CLA instruction negates AC → BUS L, MQ → BUS L, AC → MQ ENA L, and MQ LOAD L.

The MQ logic is discussed in Volume 2 when the EAE option is described in detail. Signal destination and signal source notation, which were not discussed in this section, are fully explained in Volume 2.

SECTION 6 – I/O TRANSFER LOGIC

3.41 PROGRAMMED I/O TRANSFER LOGIC

3.41.1 Programmed I/O Transfer Gating and Control Logic

Programmed I/O transfers use IOT instructions to initiate data transfers between an option and the AC Register. Information is transferred from and to an option via the OMNIBUS DATA 0–11 lines. Figure 3-103 shows the major register gating for bit 0 and the programmed I/O control signal logic. The major register gating shows only the essential features of I/O transfer; thus, only the AC and the PC Registers are included in the diagram. Note that the route control signals of major register gating are always negated for I/O transfers. However, the source control signals and the two destination control signals are used in a manner similar to that encountered in transfers between major registers. These last two types of control signals are asserted during I/O transfers, largely by the signals present on three OMNIBUS control lines: C0 L, C1 L, and C2 L. The option asserts the C0 L, C1 L, and C2 L signals, thereby specifying the direction (from or to the CP) of data transfer. Two important signals that are used along with these C-line signals are asserted within the processor whenever an IOT instruction is programmed. These two signals are I/O PAUSE L, used in the source control signal logic, and BUS STROBE L, used in the destination control signal logic. These signals are discussed in detail in later paragraphs. For this discussion it is sufficient to know that I/O PAUSE L is asserted by the processor when an IOT instruction is programmed; BUS STROBE L is asserted at TP3 time of an I/O transfer.

Table 3-9 lists the six possible types of programmed I/O transfers, the C-line signal levels for each type, and the resulting source and destination control signal levels (signal levels are given in terms of HI and LO voltages). This table can be used with Figure 3-103 as both a learning aid and a maintenance tool. The following discussion is an introduction to the table, when applied to the gating diagram.

For example, consider the first entry under Type of Transfer: OUTPUT, AC UNCHANGED. The AC0 bit must be placed on the DATA 0 line (it is later strobed into a buffer register within the option). The option accomplishes this by negating the C lines. AC → BUS L is asserted and gates AC0 to the DATA 0 line. Now, the 0 bit must be gated to the MAJOR REGISTERS BUS. The DATA T/DATA F control signals gate the bit to adder 0 during TS3. A 0 is gated to the adder by Register Input Multiplexer 0; because the route control signals are negated, the unaltered AC0 bit is placed on the MAJOR REGISTERS BUS. At TP3, BUS STROBE L is asserted and the resulting AC LOAD L signal clocks AC0. Because the D input does not change states, the AC0 flip-flop does not change states. Thus, the output transfer leaves the AC unchanged. The major register gating should be examined with Table 3-9. Understanding each type of data transfer results in an excellent understanding of programmed I/O transfers.

3.41.2 I/O PAUSE L, BUS STROBE L, INT STROBE Logic

The logic used to assert the I/O PAUSE L, BUS STROBE L, and INT STROBE signals is shown in Figure 3-104. The I/O PAUSE L signal is asserted by NAND gate E7 whenever an IOT instruction is brought from memory, provided the OMNIBUS USER MODE L signal has not been asserted (this signal is asserted by the KM8-E option and is discussed in detail in Volume 2; for the present discussion, this signal is negated high). Gate E7 is enabled when bits MD0–2 indicate an IOT instruction ($6XXX_8$), the USER MODE L signal is high, and the I/O TIME flip-flop is set. This flip-flop is set during each FETCH cycle at the same time that the STROBE memory timing signal is negated, i.e., at TP1 time plus 150 ns (setting the flip-flop at this time allows the option maximum time to decode the IOT instruction and activate the necessary control lines).

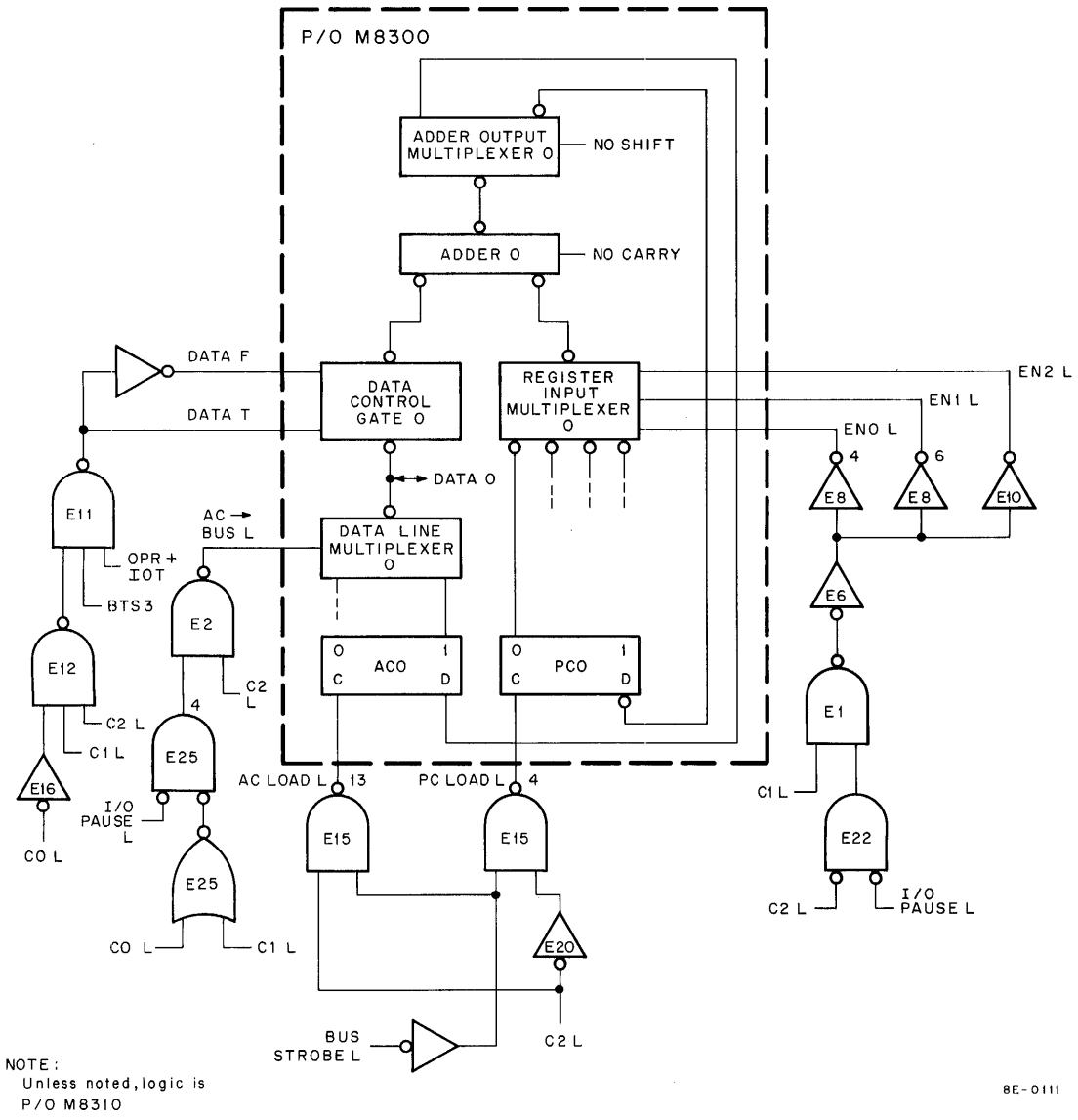


Figure 3-103 Major Register Gating (Bit 0) and Control Signal Logic, Programmed I/O Transfer

Table 3-9
Programmed I/O Transfer Control Signals,
Major Register Gating

Type of Transfer	C0 L	C1 L	C2 L	AC → BUS L	DATA T/F	EN0,1,2 L	AC LOAD L	PC LOAD L
OUTPUT, AC UNCHANGED	HI	HI	HI	LO	LO/HI	HI	LO	HI
OUTPUT, AC CLEARED	LO	HI	HI	LO	HI/LO	HI	LO	HI
INPUT, AC ORed with INPUT DATA	HI	LO	HI	LO	LO/HI	HI	LO	HI
JAM INPUT	LO	LO	HI	HI	LO/HI	HI	LO	HI
INPUT, DATA ADDED TO PC	LO	HI	LO	HI	LO/HI	LO	HI	LO
INPUT DATA TO PC	LO	LO	LO	HI	LO/HI	HI	HI	LO

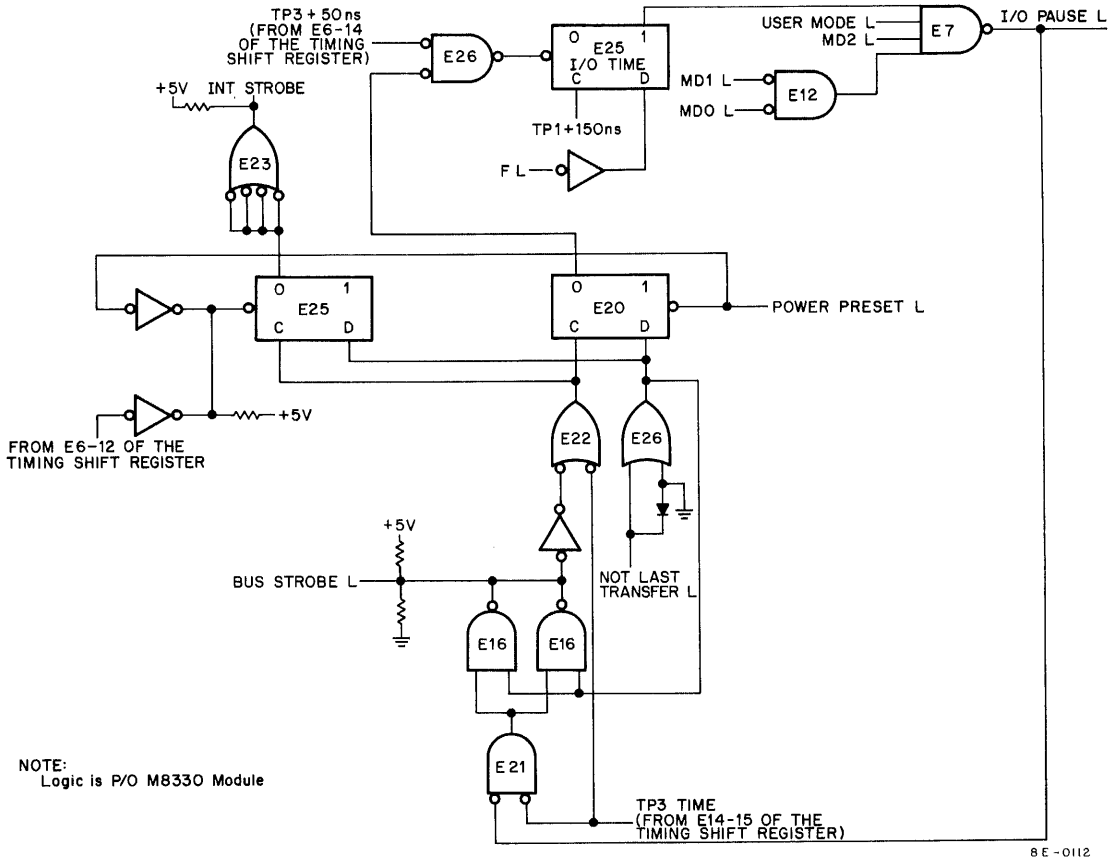


Figure 3-104 I/O PAUSE L, BUS STROBE L, and INT STROBE Logic

If the I/O transfer can be accomplished in a normal fast cycle (1.2 μs), the NOT LAST TRANSFER L signal remains high throughout the transfer (Paragraph 3.21 discusses the NOT LAST TRANSFER L signal and how the signal is used to interrupt normal processor timing). The BUS STROBE L signal is asserted at TP3 time by NAND gates E16 (the signal identified as TP3 TIME is a 100 ns negative pulse coinciding with the TP3 pulse). At the same time, flip-flop E20 is set. NAND gate E26 is enabled 50 ns later, clearing the I/O TIME flip-flop and causing the I/O PAUSE L signal to be negated. Note that the I/O TIME flip-flop is set during each FETCH cycle, even if the I/O PAUSE L signal is not asserted. Thus, the flip-flop must be cleared during each cycle; this is why the TP3 TIME signal is allowed to clock E20 via NOR gate E22.

If the option asserts the NOT LAST TRANSFER L signal, normal processor timing is interrupted. The timing of the logic in Figure 3-104 is also interrupted. The NOT LAST TRANSFER L signal prevents flip-flop E20 from being set by the TP3 TIME signal and ensures that NAND gates E16 do not assert BUS STROBE L. The option assumes responsibility for generating BUS STROBE L and clearing the I/O TIME flip-flop.

After the option negates the NOT LAST TRANSFER L signal, it issues a BUS STROBE L signal that sets flip-flop E20. The processor timing resumes, NAND gate E26 is enabled, and the I/O TIME flip-flop is cleared.

The INT STROBE signal synchronizes the program interrupt logic (Paragraph 3.42) and is used by data break devices to synchronize device and processor timing. It is normally asserted at TP3 time, when flip-flop E25 is set. When normal timing is interrupted for an I/O transfer, the INT STROBE signal is not generated until the peripheral negates the NOT LAST TRANSFER L signal and then issues BUS STROBE L. The INT STROBE signal remains high until E25 is cleared by a signal from E6, pin 12, of the Timing Shift Register (this results in an INT STROBE pulse of 100 to 150 ns duration).

3.41.3 IOT Skip Logic

The IOT Skip logic is shown in Figure 3-105. An option can assert the OMNIBUS Skip line in response to directions contained in the IOT instruction. When this occurs, flip-flop E17 is set at TP3 time. At TP4 of the FETCH cycle (B F SET L and (MS, IR DISABLE L) H ensure that this occurs only during FETCH), CARRY IN L is asserted and PC + 1 → CPMA is carried out by the processor (refer to Paragraph 3.34 for the discussion concerning the F SET L and IOT L signals).

3.41.4 Processor IOT Logic

A number of internal IOT instructions are designated processor IOT instructions. They are represented as $600X_8$ and are concerned, in general, with program interrupts. This paragraph discusses only the assertion of signals representing the processor IOTs, except in the case of the CAF instruction.

The appropriate logic is shown in Figure 3-106. NAND gate E15 is enabled whenever an internal IOT instruction is brought from memory (the signal at pin 2 of E49 represents an instruction of the form $600X_8$). The INTERNAL I/O L signal is asserted so that peripherals interfaced to the OMNIBUS via the KA8-E option (Positive I/O Bus Interface) will ignore the IOT instruction. The eight possible combinations of bits MD9–11 are decoded by E49 to provide the eight processor IOTs shown. These IOTs, with the exception of CAF, are used with program interrupt and with the KE8-E (EAE) and/or the KM8-E (Memory Extension) options. The IOTs that deal with program interrupts are discussed in Paragraph 3.42; refer to Volume 2 for information concerning those instructions relating to the KE8-E and KM8-E. The CAF IOT instruction causes the one-shot, E27, to be triggered at TP3 time. Transistor Q1 is turned on, asserting the OMNIBUS INITIALIZE signal. The one-shot is cleared at TP2 time of the next timing cycle; if the processor timing ends after the CAF instruction (the operator is single-stepping, for example), the one-shot times out after 3 μs, ensuring that the INITIALIZE signal is not asserted for an inordinate amount of time.

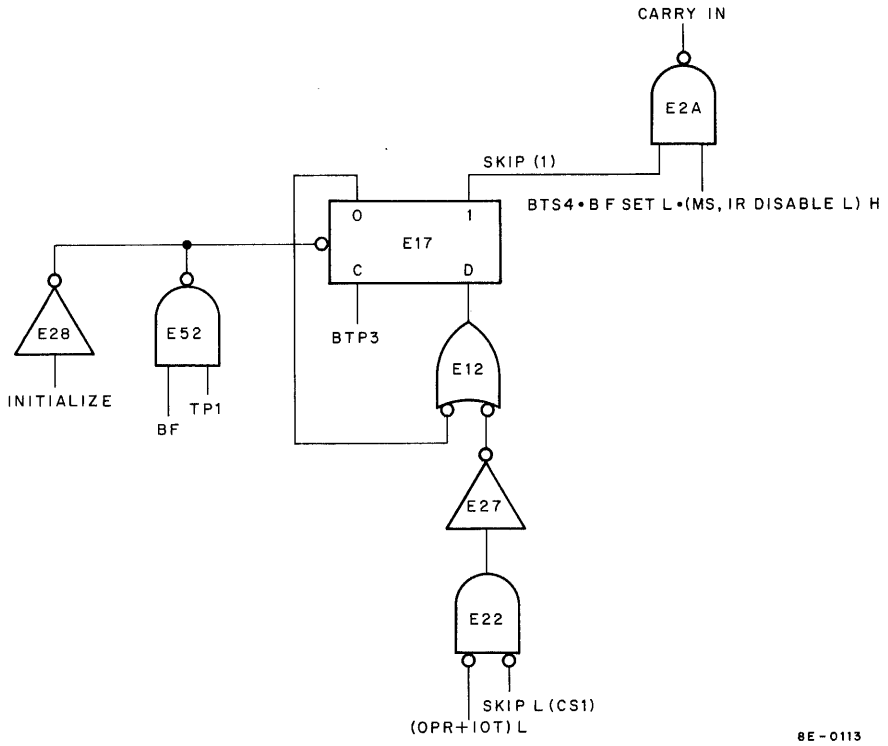
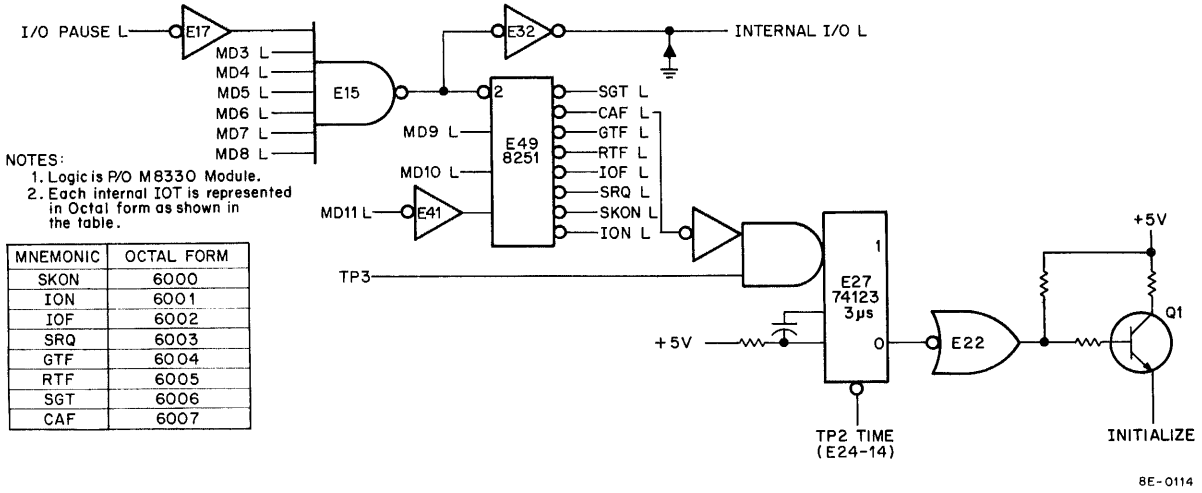


Figure 3-105 IOT Skip Logic (M8310)



NOTES:
1. Logic is P/O M8330 Module.
2. Each internal IOT is represented in Octal form as shown in the table.

MNEMONIC	OCTAL FORM
SKON	6000
ION	6001
IOF	6002
SRQ	6003
GTF	6004
RTF	6005
SGT	6006
CAF	6007

Figure 3-106 Processor IOT Logic

3.42 PROGRAM INTERRUPT LOGIC

3.42.1 Interrupt On/Off Logic

Program interrupt data transfers are more efficient than programmed I/O transfers. In the program interrupt transfer mode, the program is interrupted only when an option demands attention by asserting the OMNIBUS INT RQST L signal. The interrupt system monitors this INT RQST L signal. If the system is turned on when this signal is asserted, the processor executes a hardware-generated JMS to location 0. Simultaneously, it turns off the interrupt system; thus, further interrupts can occur only when the present one has been serviced. A program subroutine is entered to determine the identity of the requesting option. When this identity has been established, a servicing subroutine allows the option to take part in a programmed I/O dialogue with the processor.

The Interrupt On/Off logic is shown in Figure 3-107. The system can be turned on by the ION instruction. Note that the D input of the INT ENA flip-flop is high when the ION instruction (6001) is on the MD lines. Thus, the flip-flop is set at TP3 time of the instruction. Conversely, it is cleared at TP3 time of the IOF instruction (6002). When the 1 output goes high, the low is removed from the clear line of the INT DELAY flip-flop. At TP2 time of the next Fetch (F L) cycle, this flip-flop is set and its 1 output, now high, allows the next INT STROBE signal to clock the NO INT flip-flop. If the instruction being performed at the time that the flip-flop is clocked is in its concluding cycle, i.e., the F SET L signal is low; if the processor is not in the DMA state, i.e., the MS, IR DISABLE L signal is high; and, if an option has asserted the INT RQST L signal, NAND gate E7 is enabled. The two provisions ensure that an instruction that has been broken into by a data break device is completed when the device relinquishes control of the processor.

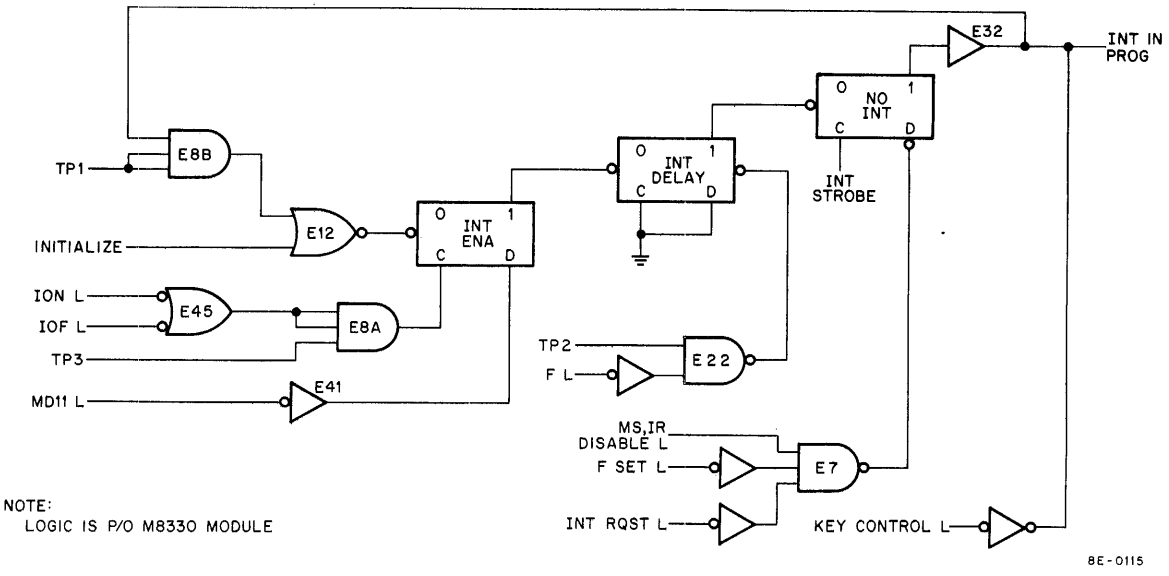


Figure 3-107 Interrupt On/Off Logic

If NAND gate E7 is enabled, the INT STROBE signal sets the NO INT flip-flop, causing the INT IN PROG signal to be asserted. At TP4 time, this signal forces the IR to JMS and forces the EXECUTE state flip-flop in the Major State Register to be set. At TP1 time of this EXECUTE cycle the INT ENA flip-flop is cleared via NAND gate E8B (note that this flip-flop is also cleared by INITIALIZE). The INT DELAY and the NO INT flip-flops are cleared in turn. The processor executes the appropriate JMS operations and then proceeds to the interrupt servicing routine. When the option has been serviced, an IOT instruction again turns the interrupt system on. Note that there is a delay of at least one complete cycle between the setting of the INT ENA flip-flop and the clocking of the NO INT flip-flop (there can be many more than one cycle if data break devices break into the normal timing). This delay allows the processor to obtain the return address from location 0, where it was stored, before a new interrupt can occur.

3.42.2 Interrupt Skip Logic

The SKON instruction (6000) grounds the OMNIBUS Skip line if the interrupt system is turned on (INT ENA flip-flop is set). At TP3 time of this instruction, the system is turned off, as shown in Figure 3-108 (the MD11 L signal is high). If the SKIP L signal is asserted by SKON, TP3 also sets the SKIP flip-flop (Figure 3-105). Then, during TS4, the Carry In line is asserted, the PC Register is incremented, and the instruction following SKON is skipped.

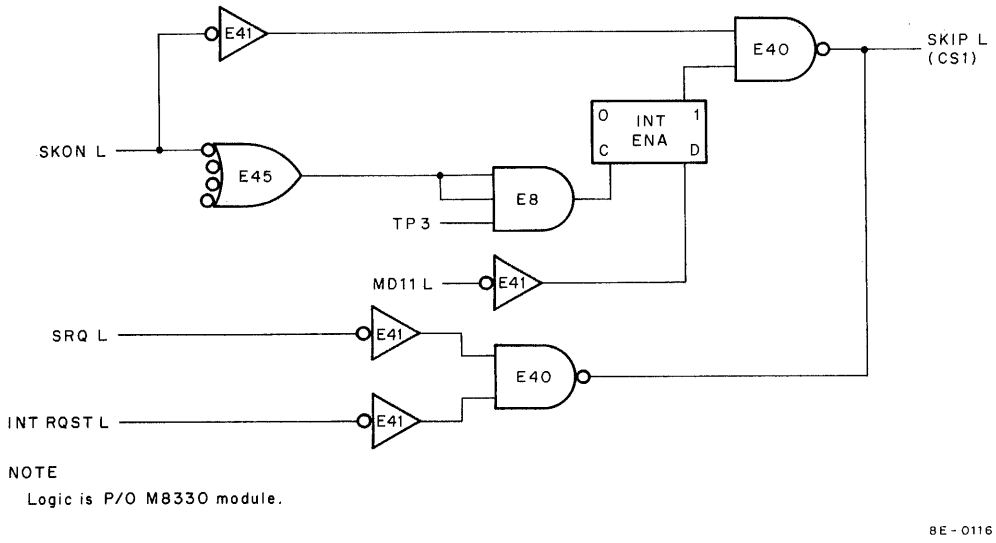


Figure 3-108 Interrupt Skip Logic

The SRQ instruction can also ground the Skip line, but only if the INT RQST L signal has been asserted by an option. Then the Skip logic and the Carry In logic cause the next instruction to be skipped.

3.42.3 Get/Return Interrupt Flags Logic

The GTF and RTF instructions have been discussed in relation to their use with the Link (Paragraph 3.39). The logic covered in Paragraph 3.39 is also presented in Figure 3-109. However, it is repeated only for continuity and is not discussed in detail.

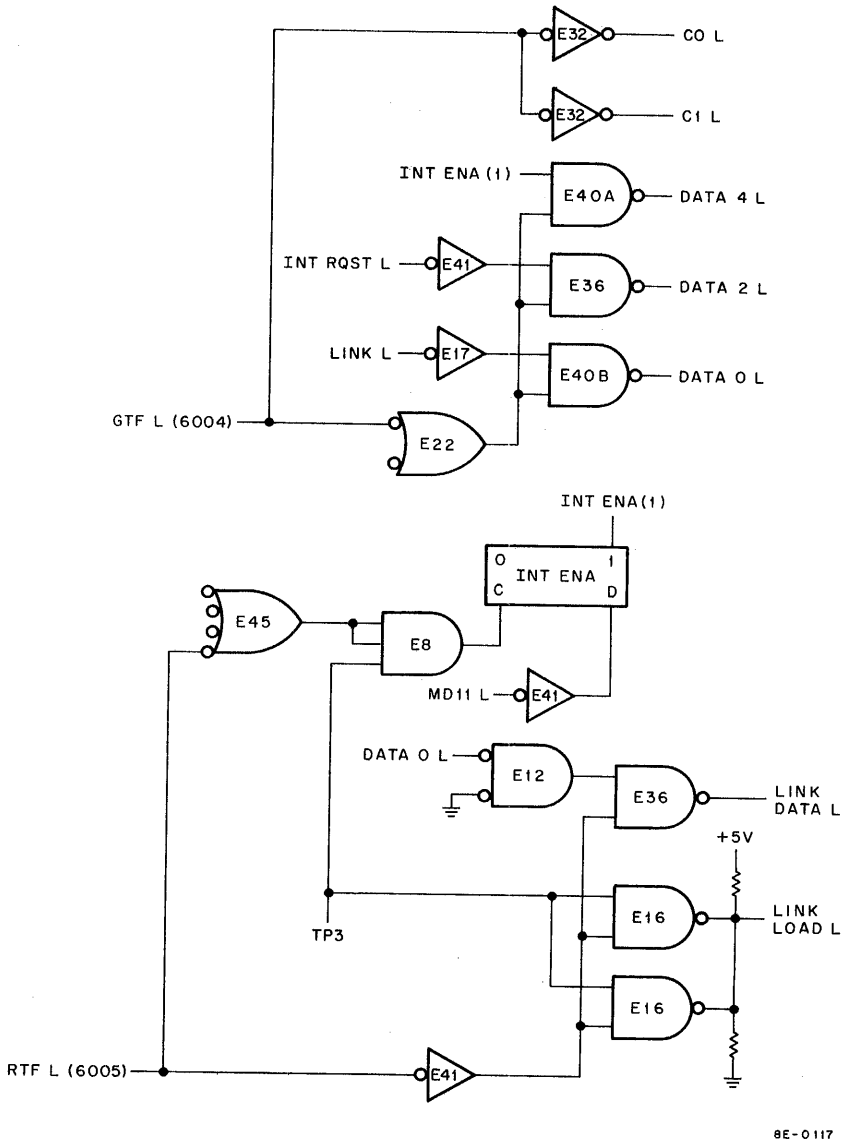


Figure 3-109 Get/Return Interrupt Flags Logic

When GTF L is generated, the states of the OMNIBUS LINK and INT RQST lines are gated to the DATA 0 and DATA 2 lines, respectively. The state of the INT ENA flip-flop is gated onto the DATA 4 line. Simultaneously, the C0 L and C1 L signals are asserted by gates E32, while the C2 L signal is left negated. The result of this gating is a jam input of data to the AC (Table 3-9 and Figure 3-103). The nine remaining AC bits — 1, 3, and 5 through 11 — are provided by the KM8-E and/or KE8-E options.

The RTF instruction, in addition to restoring a previous state of the Link line, also sets the INT ENA flip-flop at TP3 time. Both this instruction and GTF have minor significance within the processor itself, performing only housekeeping functions with the interrupt system. Their full potential is realized only when the KM8-E (Memory Extension) and/or KE8-E (EAE) options are used.

3.43 DATA BREAK TRANSFER CONTROL LOGIC

Data transfers that occur between memory and a data break peripheral are carried out in the Direct Memory Access (DMA) state of the processor (Paragraph 3.34.1). This state provides direct communication between the peripheral and memory by allowing the peripheral to assume control of major register gating. The peripheral accomplishes this by asserting a number of OMNIBUS signals when it is ready to make a data transfer.

The major OMNIBUS signal is the MS, IR DISABLE L signal. Paragraphs 3.34.1 and 3.34.2 describe how this signal is asserted by the peripheral at TP4 of a processor FETCH, DEFER, or EXECUTE state; the asserted signal forces the processor to enter the DMA state and disables the IR Register. At the same time (TP4), the output of the CPMA Register is removed from the OMNIBUS MA lines, because the peripheral asserted CPMA DIS L at INT STROBE H time. The peripheral, which monitors the MA lines through its control module, then specifies the memory location that is to receive or send a data word. Now the peripheral indicates the direction of transfer and provides the necessary gating signals.

The major register gating for bit 0, reduced to essential details, and the logic that controls the gating during the data break operation are shown in Figure 3-110. Note that MS, IR DISABLE L is also used in the control logic to assert the source control signals. Table 3-10 shows the state of the OMNIBUS signals and the source control signals for each of the three basic data break transfers. The following paragraph discusses the first entry in this table and presents some points that may not be apparent from Figure 3-110 or Table 3-10.

Table 3-10
OMNIBUS and Source Control Signal States,
Data Break Transfer Gating

Type of Transfer	MS IR DISABLE L	CPMA DISABLE L	MD DIR L	BREAK DATA CONT L	MA, MS LOAD CONT L	DATA T/F	EN0/1/2
ADM INPUT	LO	LO	HI	LO	LO	LO/HI	LO/LO/HI
INPUT	LO	LO	HI	HI	LO	LO/HI	HI/HI/HI
OUTPUT	LO	LO	LO	HI	LO	LO/HI	HI/HI/HI

The first entry is an input data transfer called Add To Memory (ADM). The peripheral asserts CPMA DIS L at TP3 and MS, IR DISABLE L at TP4 of the state that precedes entry to the DMA state. The MS, IR DISABLE L signal ensures that the next cycle is carried out in the DMA state, while CPMA DISABLE L allows TP4 to reset flip-flop E17. This flip-flop causes NAND gate E1 to be disabled, thereby removing CPMA0 from the MA0 line. At this time, the peripheral places the memory address of the transfer on the MA0 line; the DMA state is then entered at TS1. At TP1, MA, MS LOAD CONTROL L is asserted, preventing CPMA0 from being clocked during the data break operation (refer to Paragraph 3.34.1 for details concerning MA, MS LOAD CONTROL L). During TS2 time, the MS, IR DISABLE L signal asserts the DATAT/F signals and, with BREAK DATA CONT L, the EN signals. BREAK DATA CONT L, which must be asserted by the peripheral before TS2, causes the MD0 line to be gated to adder 0. DATA T/F causes the DATA 0 line to be gated to the adder. At the beginning of TS2,

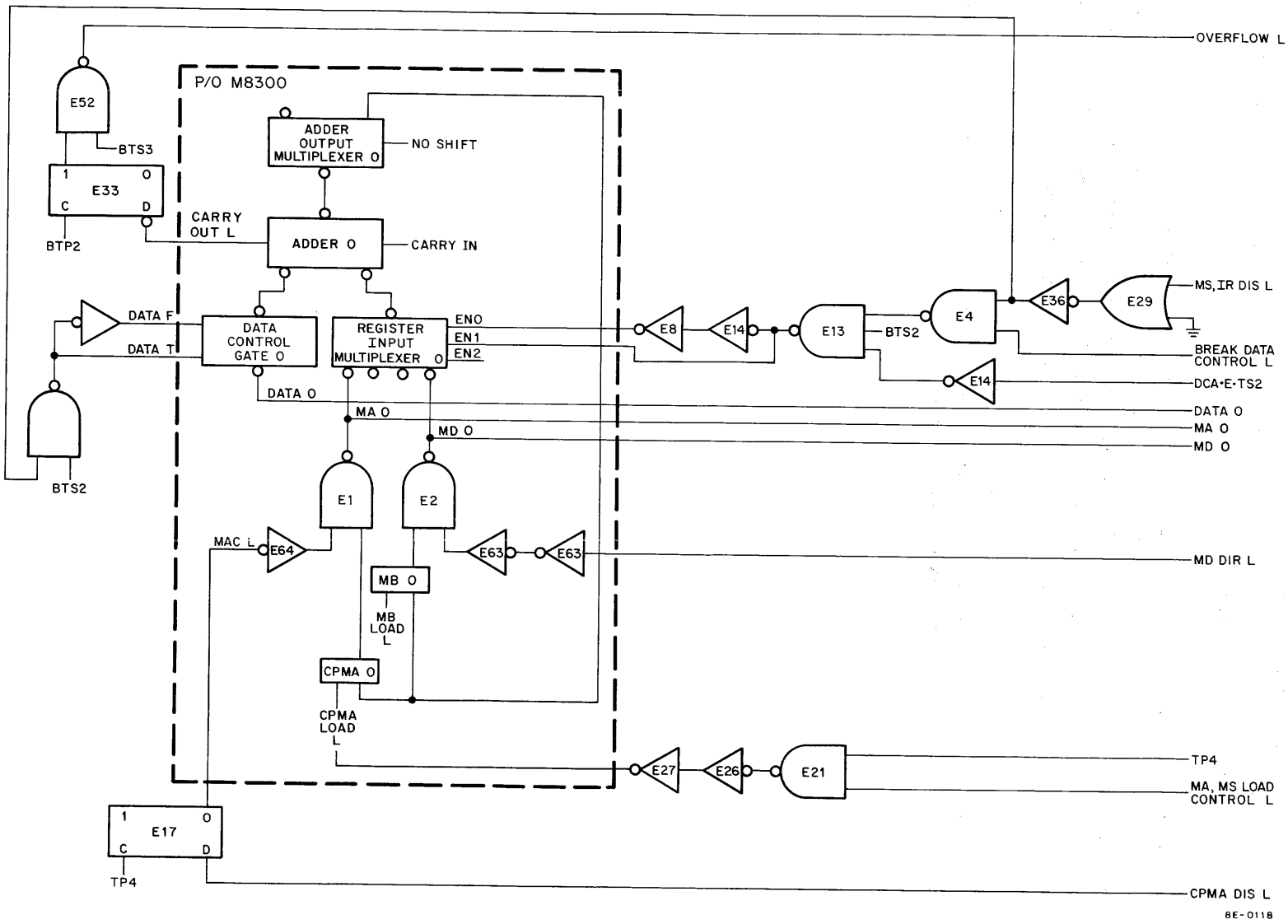


Figure 3-110 Processor, Data Break Transfer Control

the peripheral places the data to be transferred on the DATA lines. Thus, DATA0 + MD0 is placed on the MAJOR REGISTERS BUS during TS2 (disregard the Carry In line at this point). At TP2 time, MB0 is loaded with DATA0 + MD0, while, at the same time, the Timing Generator negates MD DIR L. Thus, the data is transferred to the addressed memory location.

Now consider the Carry In/Out lines of adder 0. Carries may be produced as a result of the ADM operation. The previously discussed method of sensing a Carry Out from adder 0 (LINK, Paragraph 3.39) is not available during the data break operation. Therefore, the Overflow flip-flop, E33, is provided to notify the peripheral when such a carry out occurs. E33 is set at TP2, if CAR OUT L is asserted. During TS3, the OMNIBUS OVERFLOW L signal is asserted; the peripheral uses this signal as determined by the peripheral programming.

The OVERFLOW L signal is commonly used with a 3-cycle data break device. In this application, the OVERFLOW L signal is gated with the word count major state within the data break control to indicate that the last word of a block is about to be transferred by the following Break (B) cycle.

SECTION 7 – CONSOLE TELETYPE CONTROL, KL8-E

3.44 TELETYPE CONTROL, GENERAL DESCRIPTION

The Teletype Control contains logic to transfer data between the Central Processor and the Teletype keyboard, reader, printer, and punch. The transmitter converts parallel information provided by the computer to serial information for the Teletype at the Teletype rate of speed. The 33 ASR Teletype requires one character every 9.09 ms; therefore, the purpose of the transmitter is to transmit (to the Teletype) one bit every 9.09 ms and to transfer a START bit, 8 DATA bits and 2 STOP bits (the format of the character) in 99.99 ms or 100 ms.

The transmitter services the teleprinter and punch. There are two operating modes for the transmit portion of the Teletype Control: punch and print. The punch mode can be disabled by the punch ON/OFF switch at the Teletype. When the punch is OFF, the data path is from the AC Register to the TTO Buffer to the printer. When the punch is ON, the data path includes both the punch and the printer.

A third combination includes the keyboard. The data path starts from the keyboard, continues to the TTI Buffer and to the AC Register. From the AC Register the data path continues to the punch buffer, to the printer, or to the printer and punch.

The receiver services the reader or keyboard. The receiver takes the serial information from the Teletype and converts it to parallel data for the computer. The operation is reversed for the transmitter. The receiver receives a bit every 9.09 ms and, when the character is fully assembled in the receiver (100 ms), the data is applied in parallel to the computer.

Two functions are provided by the receiver portion of the Teletype Control: the reader and the keyboard. The keyboard is always enabled. When a key on the keyboard is depressed, it automatically sends data from the Teletype to the receiver. This data is then transferred to the AC Register when the processor samples the Teletype receiver (TTI) buffer with an IOT instruction. The reader portion of the Teletype applies to the paper-tape reader, which can be disabled. If the processor instructs the reader to read, the reader buffer then receives information; or, the reader portion of the Teletype can be disabled at the Teletype unit, but the keyboard portion cannot be disabled. The assertion of the keyboard key automatically sends the corresponding character to the reader buffer.

3.45 TELETYPE CONTROL, FUNCTIONAL DESCRIPTION

A block diagram of the Console Teletype Control is illustrated in Figure 3-111. The primary logic/functions are illustrated by blocks. The address decoder provides selection logic to ensure that the processor is communicating with the Teletype rather than some other device. It receives bits MD3 L to MD8 L, decodes them, and signals the Operations Decoder that this IOT is addressed to Teletype. The I/O PAUSE L signal is used as a gating input to ensure that the instruction is an IOT instruction. If MD3 L to MD8 L equal 03_8, the receiver function is addressed and 04_8 addresses the transmit function.

The Operations Decoder begins to function when the address decoder signals that Teletype has been addressed. The Operations Decoder then looks at bits MD9 L to MD11 L and decodes the type of instruction to be performed. The Operations Decoder is divided into two sections: receiver functions and transmitter functions. Only one of these can be turned on during any one IOT. The Operations Decoder then enables all of the other functional blocks. If the Teletype Control is to read some information, the Operations Decoder enables the TTI Control. The TTI Control ensures that the correct information is read from the Teletype. Striking a key on the

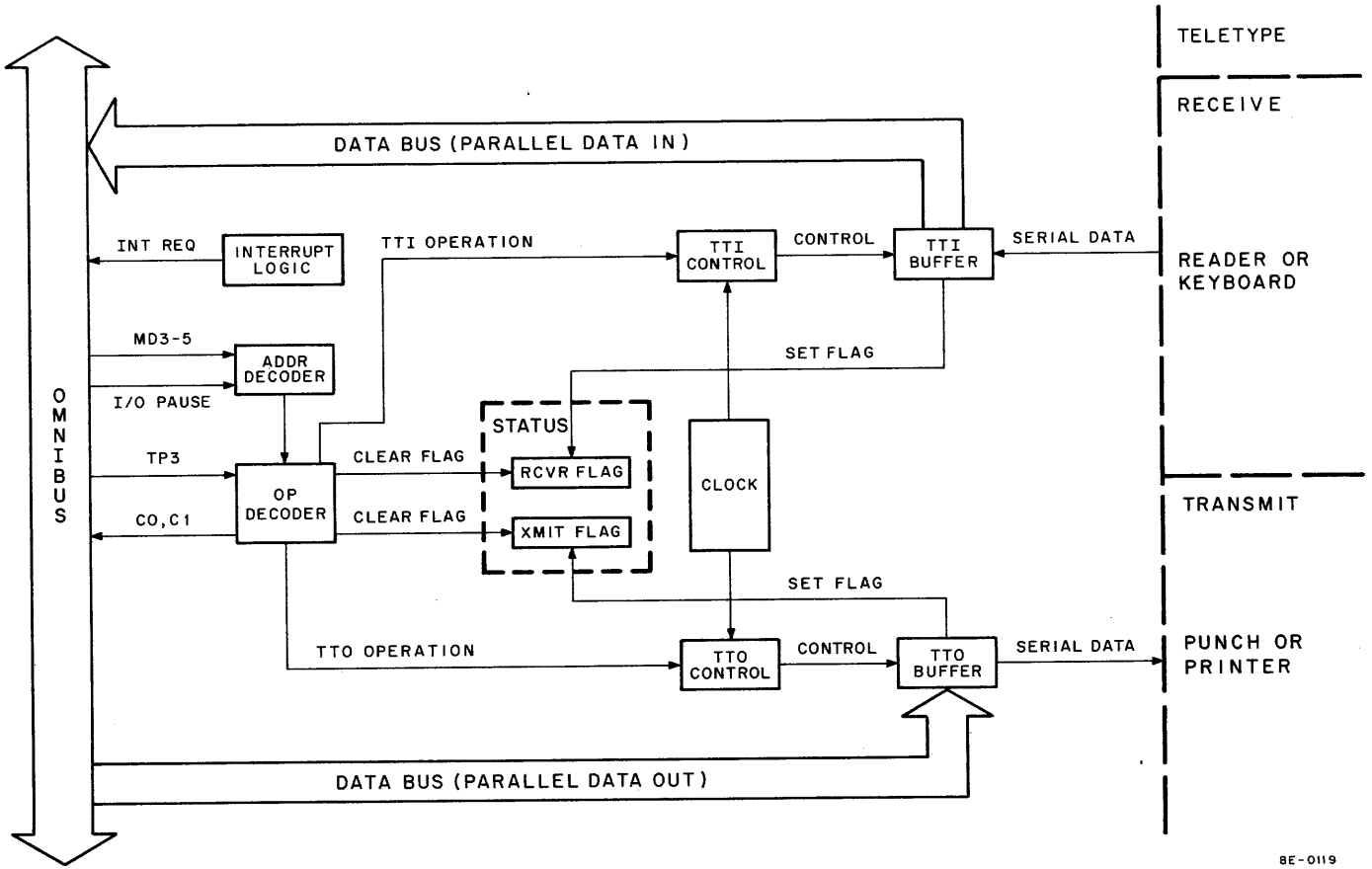


Figure 3-111 Teletype Control, Functional Block Diagram

keyboard brings data into the receiver portion of the Teletype Control. This automatically sends serial information into the receiver buffer. Of the 11 bits received from the Teletype, the first bit is the START bit. The TTI Control looks at the leading edge of the START bit. If the START bit is still present after 4.55 ms, the TTI Control is assured that it is the true START bit and allows the TTI buffer to serially shift in ten more bits from the Teletype. Otherwise, the buffer is inhibited.

After the TTI Control has determined that all of the information is in the TTI buffer, the TTI buffer sets the Reader flag to indicate that the buffer is full. The flag immediately activates the interrupt logic, if the interrupt control logic is enabled. If the Operations Decoder receives a KSF command, SKIP L is generated when the Reader flag is set.

The processor then sends a new IOT to the Teletype Control. The Operations Decoder receives this new instruction, which instructs it to read the buffer. A gating signal is developed in the Operations Decoder and applied to the buffer output gates. The eight data bits are then gated onto the DATA BUS (DATA 4–11) and loaded into the AC.

When the punch or printer is to be activated, the TTO Control logic is used. Another portion of the Operations Decoder directs the operations applying to the punch. Control signals developed in the Operations Decoder logic are applied to the TTO Control.

The TTO Control then clocks the TTO buffer input gates so that parallel data can be loaded from the OMNIBUS into the TTO buffer. The data transfer path is between the AC Register in the Central Processor to the TTO Buffer via the DATA BUS. The TTO Control then begins to clock the TTO Shift Register to enable a serial shift (one bit at a time) of the data to the Teletype at Teletype speed (9.09 ms per bit). In addition, the TTO buffer sends out a START bit, 2 STOP bits, and the 8 data bits to comprise an 11-bit word (one character). When the TTO buffer is empty, the TTO Control sets the Transmitter Flag. The set condition enables the interrupt logic. When the processor checks the flag, SKIP L is generated.

The clock is used to give a standard rate of 9.09 ms as a reference. This controls all events between the Teletype Control and the Teletype to ensure that the Teletype speed is always maintained. The events between the Teletype Control and the Central Processor are controlled by TP3 generated in the Timing Generator.

3.46 TELETYPE CONTROL, DETAILED LOGIC

3.46.1 Address Selection Logic

The Address Selection logic (Figure 3-112) decodes MD3 L through MD11 L. The device address is contained in bits 3 through 8, and the operation code is contained in bits 9 through 11. If the middle six bits are decoded as 03 (octal), the Operations Decoder is directed to the receiver functions. If the middle six bits are decoded as 04 (octal), the Operations Decoder is directed to the transmitter functions. The I/O PAUSE L signal is developed in the Timing Generator whenever bits MD0 through MD2 are decoded as a 6 (octal). I/O PAUSE L gates the address bits through the decoder. The output of the Address Selection logic provides an enabling signal to the receiver portion of the Operations Decoder or an enabling signal to the transmitter portion of the Operations Decoder. It also generates the INTERNAL I/O L signal, which is used in the positive I/O Bus Interface to prevent the generation of IOPs.

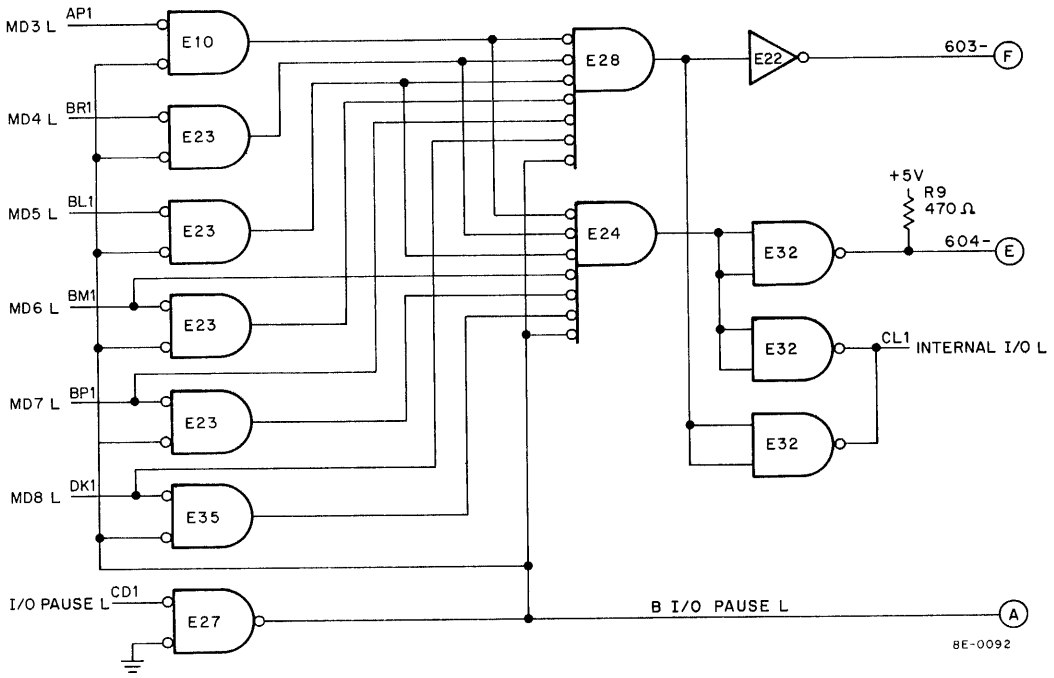


Figure 3-112 Address Selection, Logic Diagram

3.46.2 Interrupt Control Logic

The Interrupt Control logic functions to either enable or disable interrupts from the Teletype (Figure 1-113). Every time a flag is set (either receiver or transmitter), the INT RQST L signal is asserted, if the INTER ENABLE flip-flop is set (the 1 side is high). By modifying the state of the INTER ENABLE flip-flop, the INT RQST L signal can be either asserted or inhibited. To inhibit INT RQST L, a 0 is first placed into AC11L and applied to the DATA BUS. DATA 11 L is gated into the data input of the INTER ENABLE flip-flop by the I/O PAUSE L signal. The data input is clocked in by IOT instruction 6035, which is decoded by the Operations Decoder and applied to the INTER ENABLE flip-flop. This causes the 1 output to go low and negate gate E33 to inhibit the INT RQST L signal. The other qualifying input to E33 is the state of the receiver or transmitter flag. If AC11 L is a 1, the INT RQST L signal is then applied to the Interrupt Control logic via the OMNIBUS as the interface signal that starts the interrupt system sequence of events. The INTER ENABLE flip-flop is also set by CAF and by operation of the CLEAR key.

3.46.3 Operations Decoder Logic

The Operations Decoder logic (Figure 3-113) receives either 03 or 04 (octal) from the address selection logic to enable the receive or transmit logic. The operation to be performed is determined by the last three MD bits, MD9 L through MD11 L, to provide instructions such as SKIP, CLEAR FLAG, SET BUFFER, etc. These functions are given in the timing diagram in Figure 3-114, with respect to signals I/O PAUSE L, TS2 L, TP3, and TS4 L. The Teletype is in control as soon as the I/O PAUSE L signal is asserted low, which occurs 100 ns after the beginning of TS2. Signal SKIP L is generated when the MD9 L through MD11 L bits are decoded as 1 or 5 (octal). The clear operations are accomplished when MD9 L to MD11 L results in a 2 (octal). Table 3-11 illustrates the decoding functions in terms of the receive or transmit function and the last three MD bits.

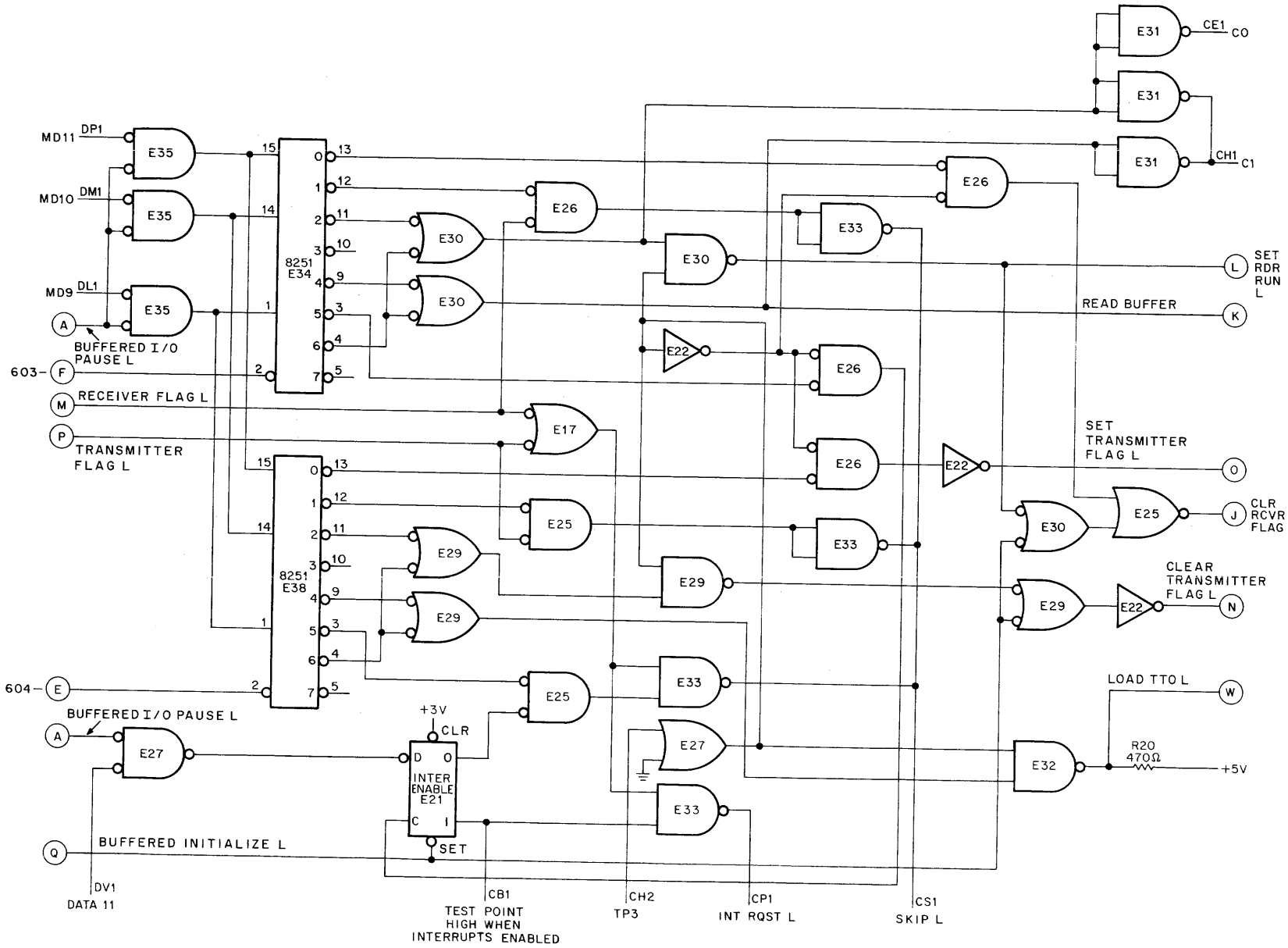


Figure 3-113 Operations Decoder, Logic Diagram

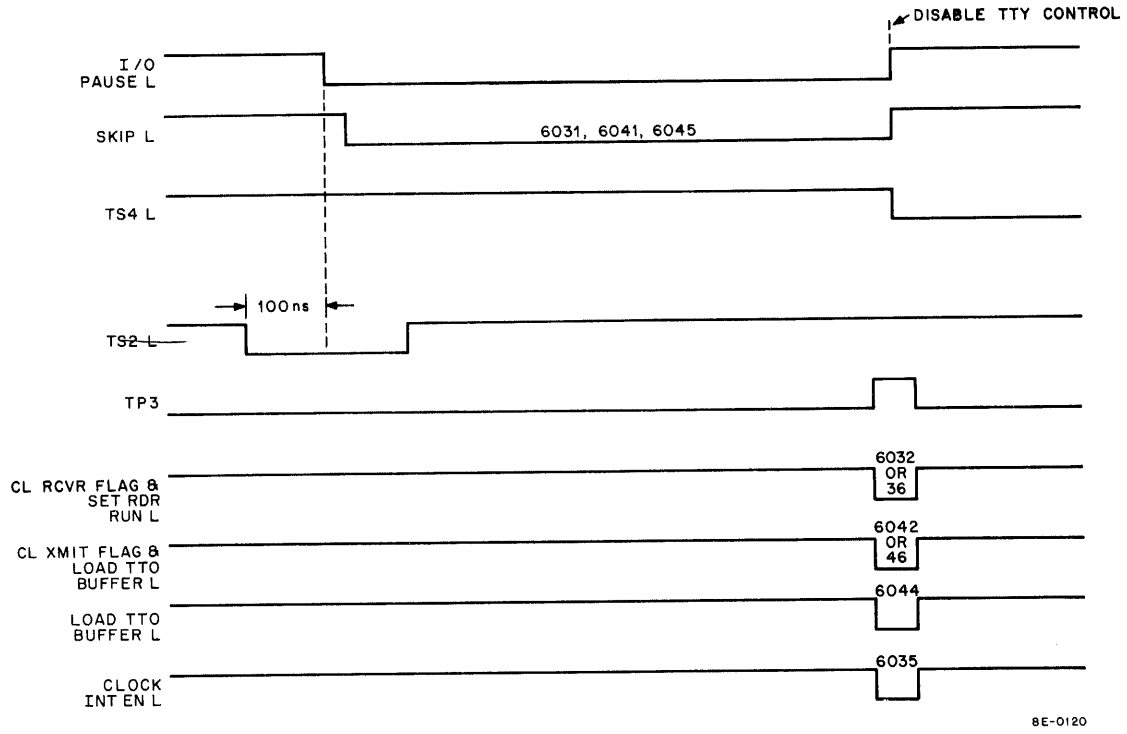


Figure 3-114 Operations Decoder, Timing Diagram

Some of the resulting control signals developed in the Operations Decoder are illustrated in the timing diagram. All are enabled by TP3 except the SKIP instructions; these occur when I/O PAUSE L is asserted. Other important control signals developed in the Operations Decoder include C0 L and C1 L, which are used to determine the type of data transfer between the processor and the Teletype Control. When the data in the TTI buffer is transferred to the DATA BUS, the 6036 instruction asserts C0 L and C1 L and takes the contents of the buffer and places it in the AC Register.

3.46.4 RCVR Flag

The RCVR flag (Figure 3-115) is connected to the end of the TTI buffer (Figure 3-117). The flag is set when the START bit is shifted out of the last stage of the TTI Shift Register. The START bit, therefore, sets the flag after all eight bits have been loaded into the TTI buffer. The 0 side of the RCVR flag flip-flop goes from a high to a low. At reference point (M), this low level signal is applied to the Operations Decoder (which looks at both the RCVR and Transmitter flags). The signal is then applied to the Interrupt Control logic (Figure 3-113), where this signal and the 1 side of the INTER ENABLE flip-flop is used to qualify the INT RQST gate and, thus, assert INT RQST L. The programmer clears the flag with the 6032 instruction. The flag indicates that the buffer is full, and that there is information that can be transferred to the AC Register.

Table 3-11
Operations Decoder Functions

REC 03	XMIT 04	MD9 L – MD11 L (octal)	Basic Operation	Off Page Reference	Controlled Logic
x		0	Clear Receiver Flag – Do not start Reader	J	RCVR Flag – Figure 3-115
x		1	Generate SKIP if Receiver Flag is set	M	Operations Decoder – Figure 3-105 RCVR Flag – Figure 3-115
x		2 (C0 L & C1 L = L)	Clear Receiver Flag, Clear AC, Set Reader Run	J	RCVR Flag – Figure 3-115
x		4 (C1 L = L)	Read TTI Buffer (parallel transfer of TTI Buffer to DATA BUS)		TTI Buffer – Figure 3-117
x		5	Sets or clears the INTER ENABLE flip-flop depending on AC11 being a 0 or 1	D	Interrupt Control Logic – Figure 3-113
x		6 (C0 L & C1 L = L)	Clear AC and Flag. Transfer TTI Buffer to DATA BUS	J K	RCVR Flag – Figure 3-115 TTI Buffer – Figure 3-117
	x	0	Sets the Transmitter Flag to ready the logic for another character	O	XMIT Flag – Figure 3-116
	x	1	Generate signal SKIP L if Transmitter Flag is set	P	Operations Decoder – Figure 3-113
	x	2	Clear the Transmitter Flag	N	XMIT Flag – Figure 3-116
	x	4	Enable transfer of TTO Buffer data to teleprinter or punch	W	TTO Buffer – Figure 3-120
	x	5	Generate signal SKIP L if the Transmitter Flag is set and the INTER ENABLE flip-flop is set	B	Operations Decoder – Figure 3-113 Interrupt Control – Figure 3-113
	x	6	Clear the Transmitter Flag and enable transfer of TTO Buffer to printer or punch	N W	XMIT Flag – Figure 3-116 TTO Buffer – Figure 3-120

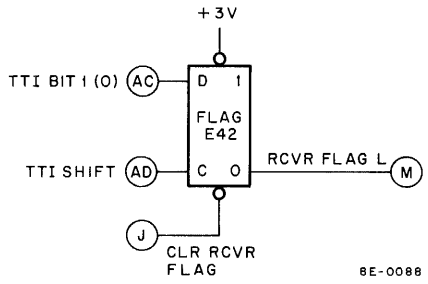


Figure 3-115 RCVR Flag

3.46.5 Transmitter Flag

The Transmitter flag (Figure 3-116) works in an opposite manner to the RCVR flag. The TTO buffer (Figure 3-120) shifts in 0s from the ENABLE flip-flop all the way up to the LINE flip-flop. When all 0s are placed in the TTO buffer, the TTO = 0 (S) signal is brought high and applied to the data input of the Transmitter flag flip-flop, which will again be brought low and applied (reference point P) to the Operations Decoder. At this point, it is applied to the Interrupt Control logic where the INT RQST L signal is generated. The processor is now informed that the Teletype transmitter is ready for another character. If the programmer checks the flag with a 6041 instruction, the SKIP L signal will be generated, which instructs the processor to skip the next instruction. A 6042 instruction will clear the flag. The programmer always clears the flag prior to a new punch operation.

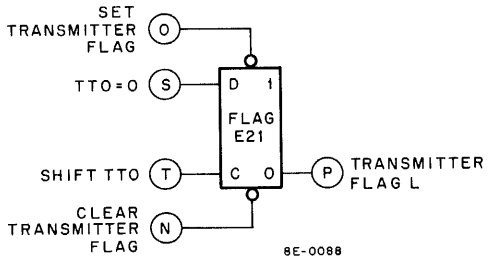


Figure 3-116 Transmitter Flag

3.46.6 TTI Buffer and Control

The TTI Buffer and Control circuits are illustrated in Figure 3-117. The TTI buffer receives an 11-bit code from the Teletype. The first bit turns the reader control circuitry on and presets the TTI buffer to all 1s. The control circuitry makes certain that a true START bit exists. To be a true START bit, the duration must be at least 4.55 ms. If a true START bit exists, the TTI Buffer Control circuit takes the incoming START bit and places it (as a 0) into the least significant bit in the TTI buffer. The output of the Clock (Figure 3-119) clocks the buffer at a 9.09 ms rate or 110 Hz. The original START bit, which was applied to bit 8 of the buffer, shifts one position to the right on each clock input. Following this, the START bit will be 8 bits of ASCII code. Two STOP bits are included at the end; thus, a total of nine clock pulses are applied to the buffer. The first clock pulse shifts in the START bit. The ninth clock pulse shifts the START bit from bit 1 to the RCVR flag and the flag is then set. The

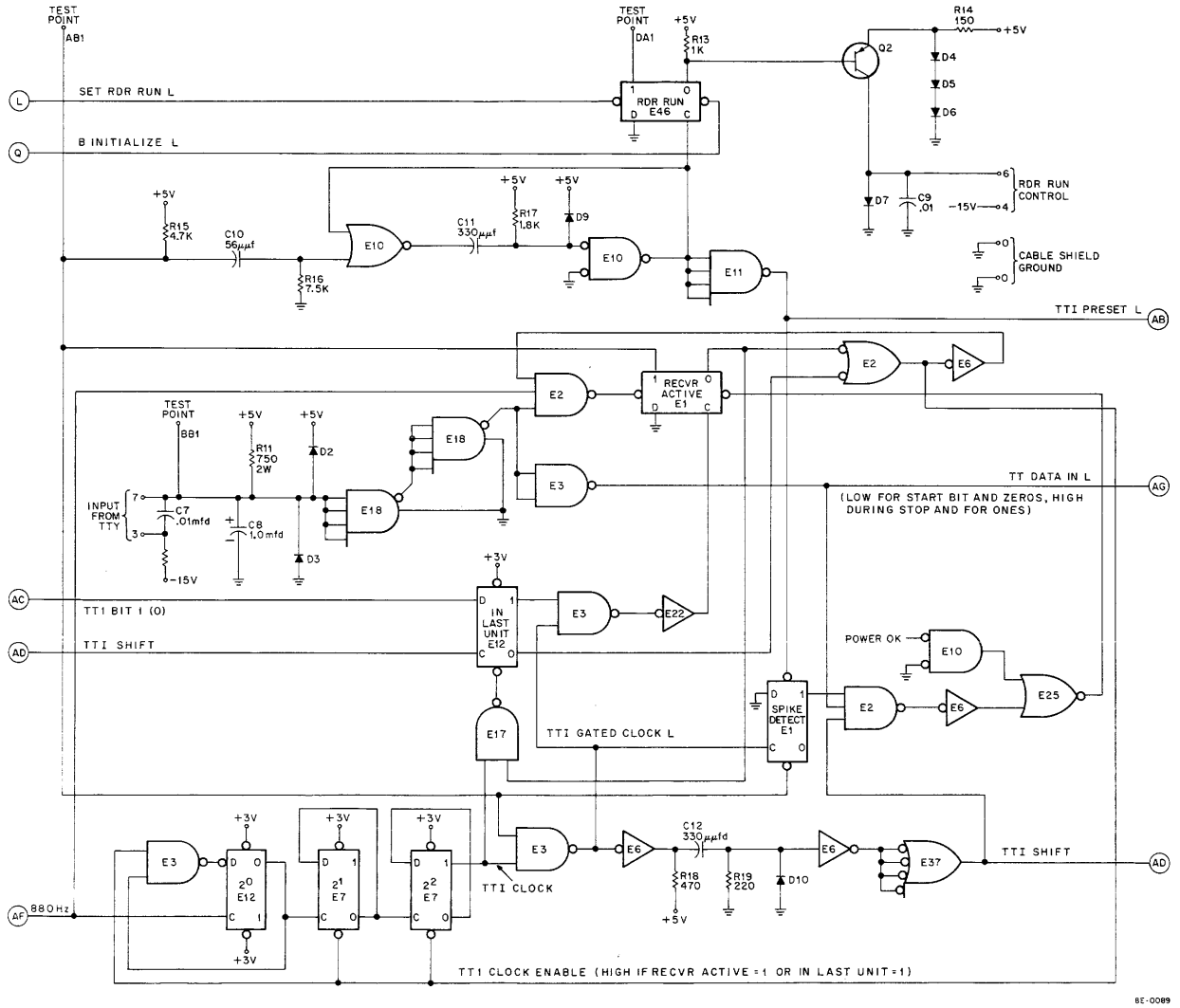


Figure 3-117 TTI Buffer and Control, Logic Diagram (Sheet 1 of 2)

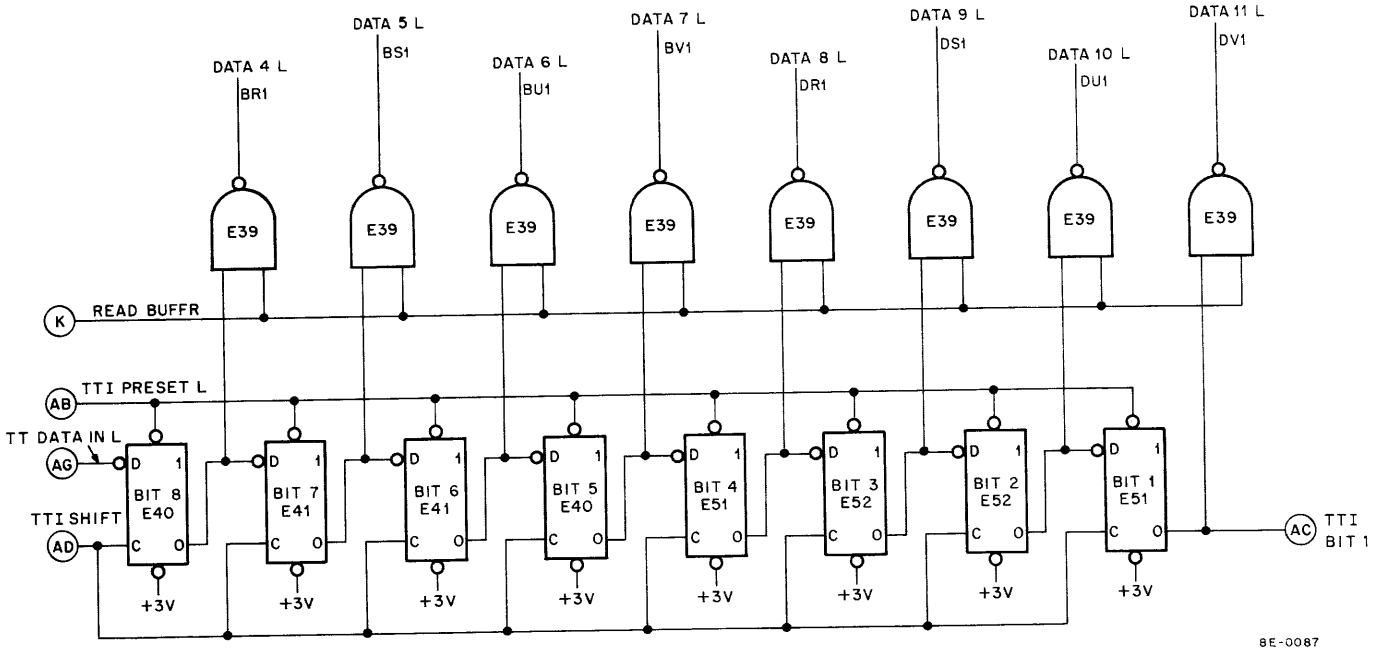


Figure 3-117 TTI Buffer and Control, Logic Diagram (Sheet 2 of 2)

START bit is also shifted into the IN LAST UNIT flip-flop in the control circuitry. The 1 side of this flip-flop is brought high and used to enable TTI GATED CLOCK, which clocks the RCVR ACTIVE flip-flop. The 0 side of the RCVR ACTIVE flip-flop is brought high when TTI GATED CLOCK goes high again (approximately the end of the last data element). At that time, the IN LAST UNIT flip-flop is cleared and the TTI CLOCK ENABLE L signal goes low. The TTI receiver is now ready to receive a new character. The RCVR ACTIVE flip-flop is the key to the entire operation; it prevents the clocking of the buffer when the buffer contains eight bits of information. The STOP bits are ignored for the receiver functions.

The SPIKE DETECTOR monitors the START pulse and ensures that it is at least 4.55 ms. If it is not, the SPIKE DETECT flip-flop causes the TTI SHIFT PULSE to clear the RCVR ACTIVE flip-flop.

The TTI timing is illustrated in Figure 3-118. Each bit lasts a duration of 9.09 ms, with a total of approximately 100 ms for all 11 bits. The serial line input is compared to the state of the flag and illustrates that the flag is set on the ninth clock pulse.

There are two methods of transferring data from the TTI Buffer to the AC Register: by a 6034 instruction or a 6036 instruction. A 6034 instruction causes the content of the buffer to be ORed with the AC and places the results in the AC. A 6036 instruction causes the content of the buffer to be placed on the DATA BUS, the AC is cleared, and the DATA BUS is loaded into the AC Register. Normally, a 6036 instruction is used. C0 L and C1 L will be asserted low by the Operations Decoder. This is used to transfer the buffer into the AC. The READ BUFFER L signal places the data in the TTI Buffer onto the DATA BUS. This qualifies the buffer output gates; whatever is in the TTI Buffer is gated out to the DATA BUS.

3.46.7 Teletype Control Clock

The clock is controlled by a 14.418 MHz crystal (Figure 3-119). The output is sent to a divide by 8 network (E9) and four divide by 16 networks (E5, E4, E8, and E13). Two outputs are available on E13. One is a 220 Hz output that is applied (reference AE) to the TTO Buffer Control where it is divided by 2 to provide 110 Hz for the TTO Buffer Control. The second output, 880 Hz, is applied (reference AF) to the TTI Buffer Control, where a 3-stage dividing network provides synchronized 110 Hz to the TTI Buffer Control Logic. The INITIALIZE signal is used to clear the dividing network when power is turned on.

3.46.8 TTO Buffer and Control

The TTO Buffer and Control logic is illustrated in Figure 3-120. The TTO Buffer functions to receive information from the AC via the DATA BUS, in parallel form, and send the information out to the Teletype in serial form. When the TTO is not transmitting a character, the LINE flip-flop is set. A START bit must first be sent by the LINE flip-flop. The XMITR ACTIVE flip-flop is originally cleared with the STOP 1 and STOP 2 flip-flops, due to the initialize state of the TTO control circuitry. Thus, when the ENABLE flip-flop (E42) clears, the XMITR ACTIVE flip-flop will be unconditionally direct set. Setting the XMITR ACTIVE flip-flop clears the LINE flip-flop (E36), which, in turn, generates the START bit for the Teletype. Because the contents of the DATA BUS (bits 4 through 11) are gated into the TTO buffer with instruction 6044 or 6046, the ENABLE flip-flop (E42) is unconditionally set and the FREQ DIV flip-flop (E20) is allowed to toggle. Each time the FREQ DIV flip-flop clears, the contents of the TTO buffer are shifted toward the LINE flip-flop. Because the ENABLE flip-flop is unconditionally set, its 1 side is transferred to bit 8 on the first 110 Hz clock input from the FREQ DIV flip-flop. This clock input also moves all other bits in the buffer up one position. Bit 1 shifts into the LINE flip-flop, and the first data bit is applied to the Teletype. This process continues at a 110 Hz clock rate until the bit that was in the ENABLE flip-flop is in the Bit 1 position of the buffer. Because all 0s are clocked in

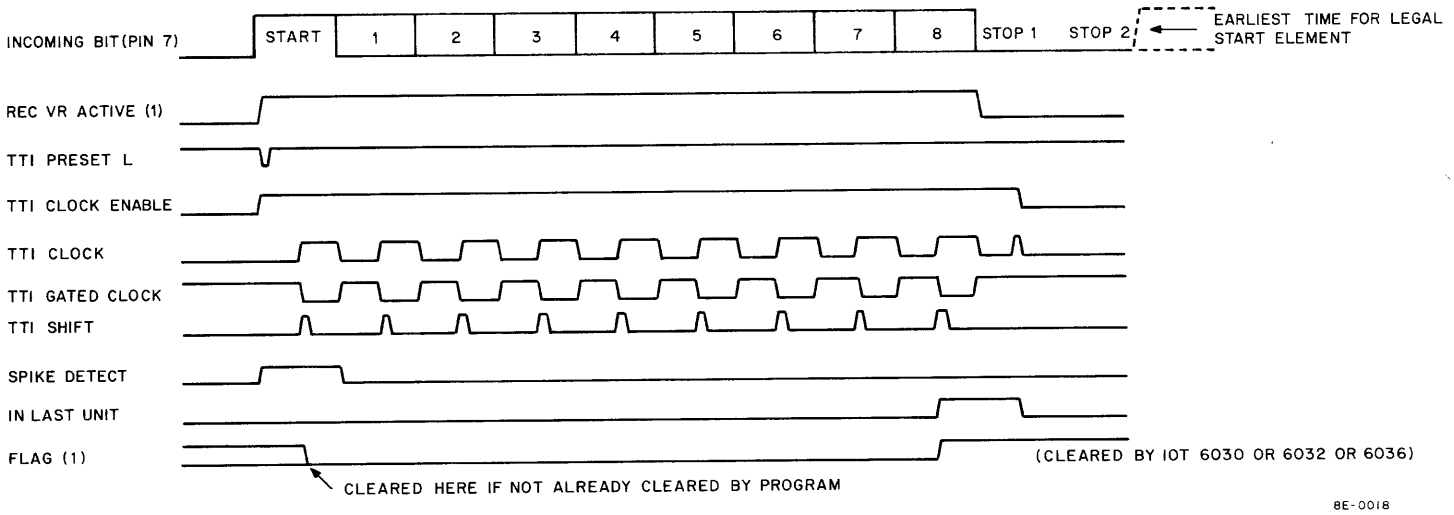


Figure 3-118 TTI Timing

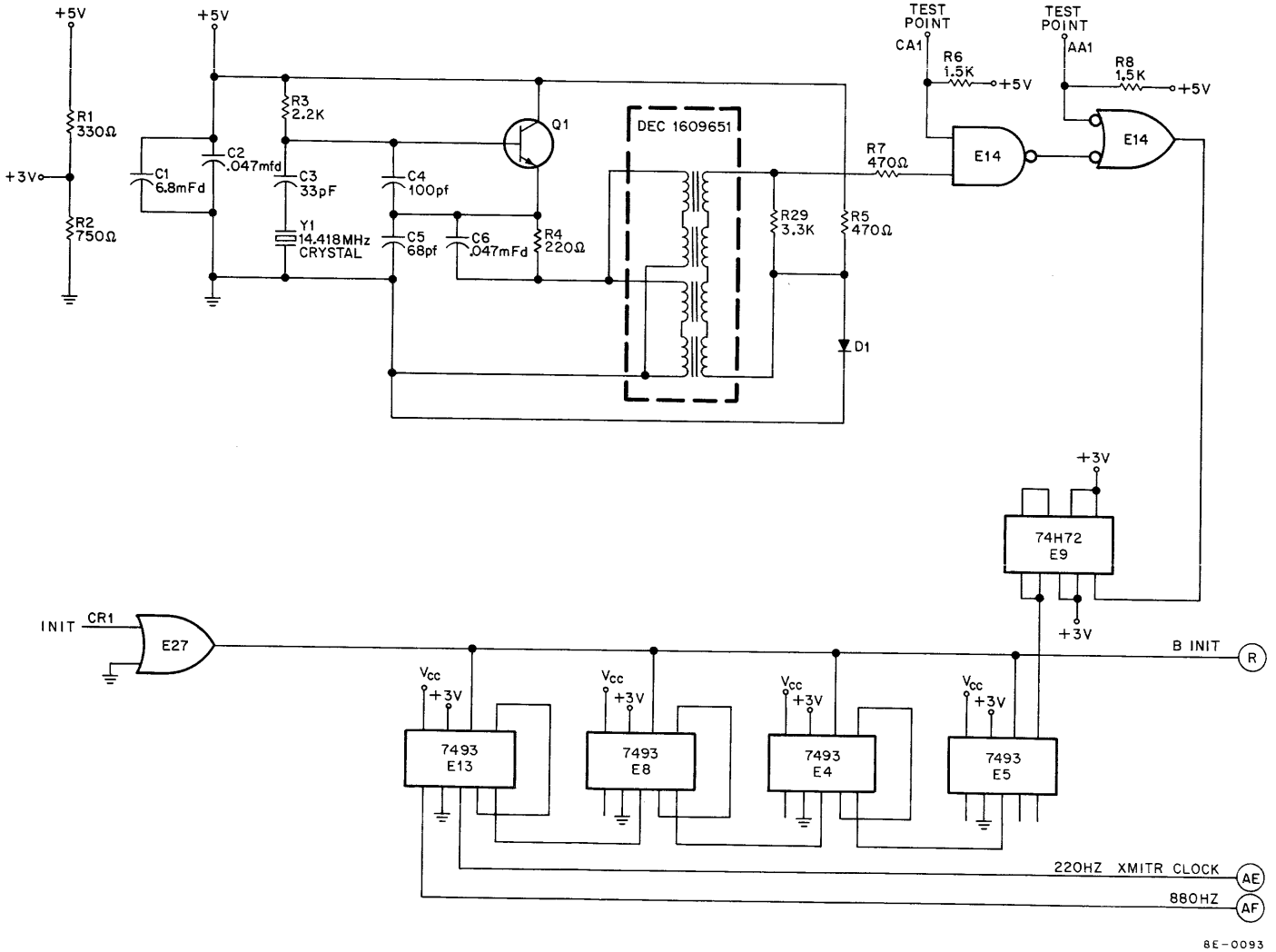


Figure 3-119 Teletype Control Clock, Logic Diagram

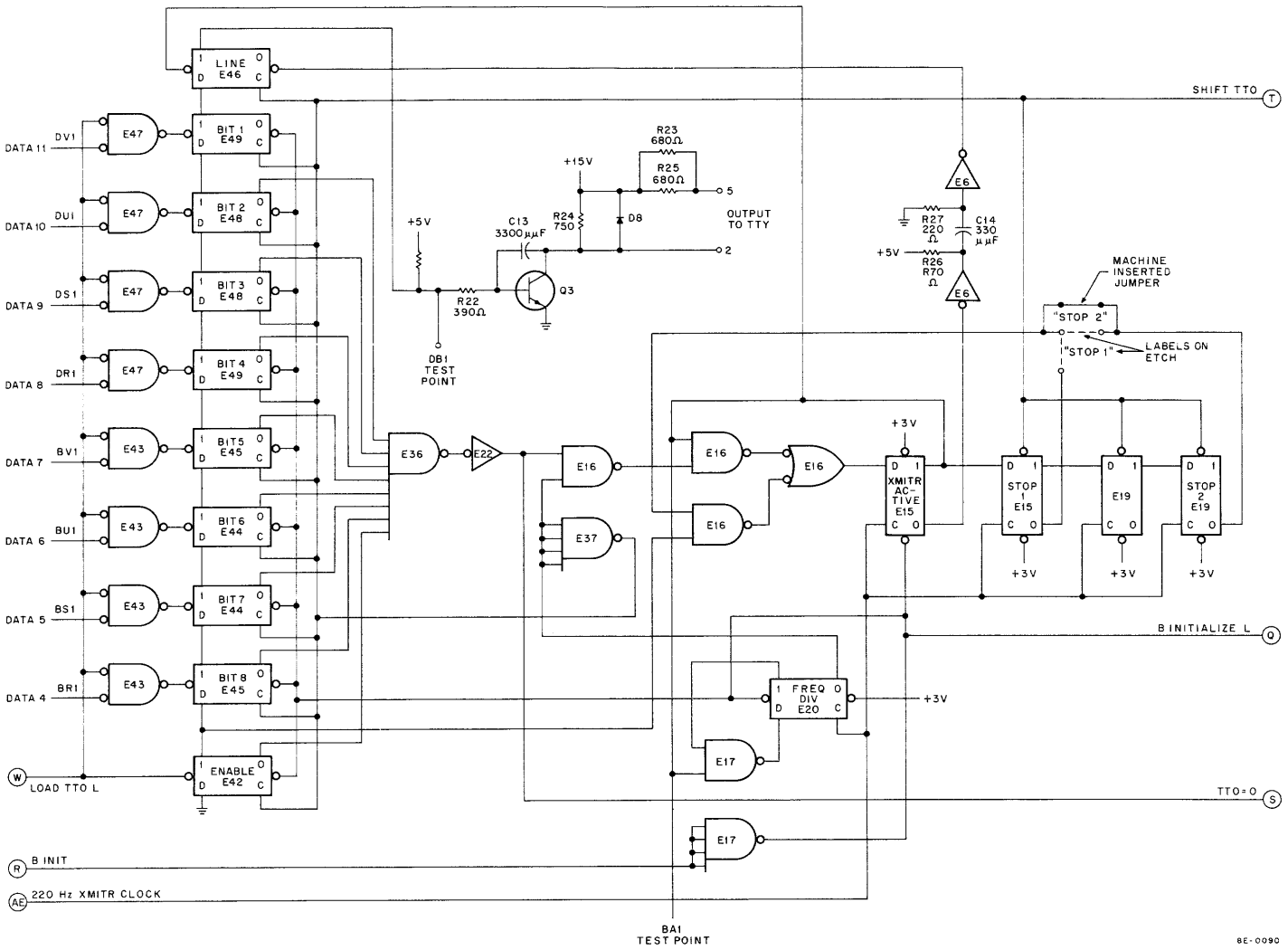


Figure 3-120 TTO Buffer and Control

behind the data bits, the 0 side of each flip-flop is high. When NAND gate E36 receives all eight qualifying inputs, the resulting output is applied to clear the XMITR ACTIVE flip-flop and set the Transmitter flag. The 1 side of XMITR ACTIVE is applied to the Stop flip-flops which, in turn, provide a delay equivalent to 2 bits (18.18 ms) before XMITR ACTIVE can be set again. (The STOP bits are set while the START and first data element were being transmitted to the Teletype.) On the 220 Hz pulse after XMITR ACTIVE clears, STOP 1 clears. On the next clock pulse, the middle flip-flop clears, its 0 side goes high again. This enabling level is then applied to the data input of the XMITR ACTIVE flip-flop.

Before a new character can be transmitted from the TTO to the Teletype, STOP 2 must clear. STOP 2 is cleared 18.18 ms after the last bit is shifted out to the Teletype. The machine inserted jumper provides 2 STOP bits. Without the jumper only one STOP bit is provided, and only STOP 1 need be cleared.

The TTO Buffer and Control Timing is illustrated in Figure 3-121. The data example (DATA = 125 (octal)) is used for illustrative purposes only. It illustrates that while the TTO buffer is shifting data out to the Teletype, the flag is cleared. When the last bit has been sent out, the flag is set. Notice that the TTO buffer can then be immediately loaded, but that transmission of the second character will be delayed until the two STOP bits have been sent.

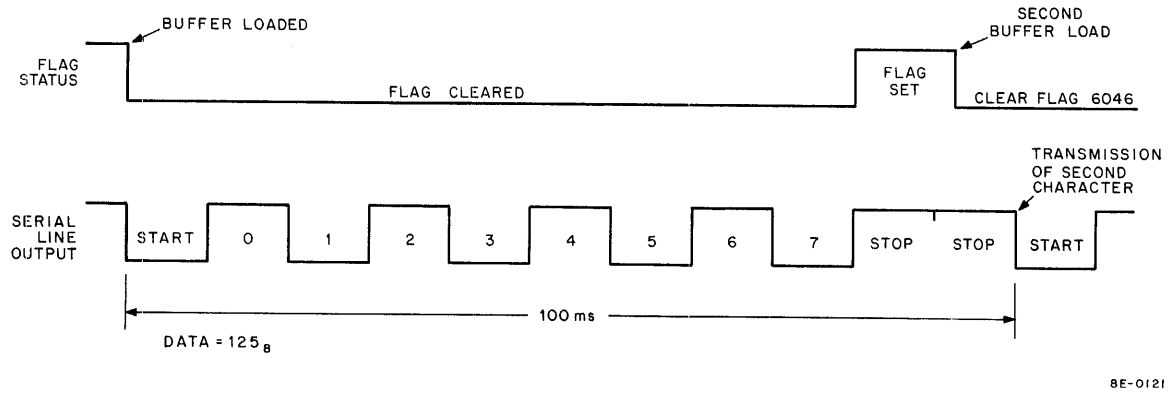


Figure 3-121 TTO Buffer and Control Timing

SECTION 8 – POWER SUPPLIES

The PDP-8/E computer uses a DEC H724 or H724A (the latter for 230 Vac lines) Power Supply that provides three regulated dc voltages, one non-regulated dc voltage, and one center-tapped ac winding that delivers 28 Vac. The PDP-8/F and the PDP-8/M use a DEC H740 Power Supply that provides three regulated dc voltages and 28 Vac, center-tapped.

Each type of power supply features dc-voltage monitoring, protection against overvoltage and thermal overload, and fusing of all dc power supplies. The PDP-8/E power supply is detailed in Paragraph 3.47; the PDP-8/F and PDP-8/M supply is described in Paragraph 3.48.

3.47 PDP-8/E POWER SUPPLY

3.47.1 Primary Network

The primary network of power transformer T1 is shown in Figure 3-122. The input ac voltage is controlled by relay K1. When the key switch on the front panel is turned to the POWER position, and the interlocks are connected, the relay closes, applying the input ac to the power transformer.

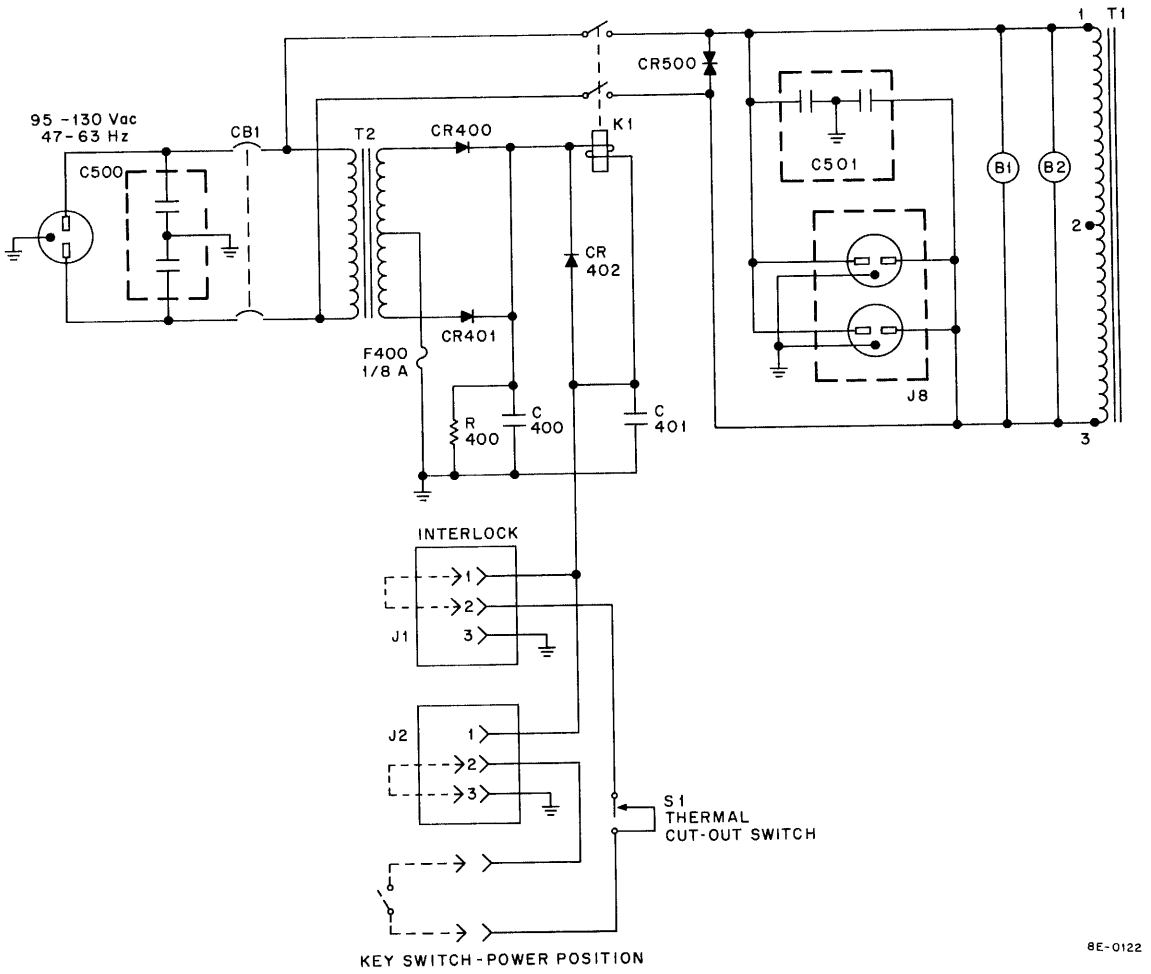


Figure 3-122 H729 Power Supply Primary Network

Switch S1 monitors the ambient temperature and opens when the temperature reaches 90°C, ±5°C. Relay K1 is, in turn, opened and removes the input ac. S1 must be reset by hand if it has been tripped.

3.47.2 +8 Vdc Power Supply

Figure 3-123 shows the +8 Vdc power supply. The +8V is obtained from a full-wave, center-tapped rectifier providing 2A, rated load. Because the +8 Vdc is used only as the supply for front panel indicators, filtering and regulation are unnecessary.

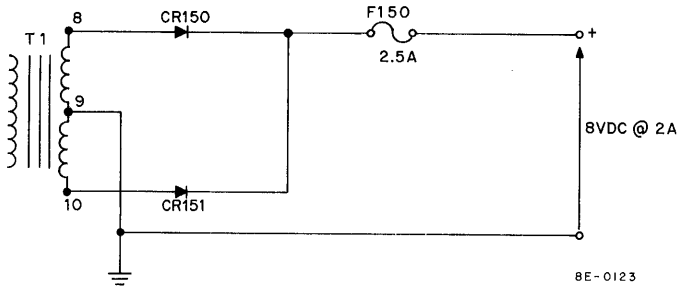


Figure 3-123 +8 Vdc Power Supply

3.47.3 +15 Vdc Power Supply

The +15 Vdc power supply is shown in Figure 3-124. The rectified dc voltage is filtered and applied to the series pass transistor, Q100, which provides +15V at its emitter. Load changes at the emitter are transferred by the R6/R7 voltage divider to the regulating difference amplifier, Q2/Q3. This amplifier, which becomes unbalanced when the base of Q3 changes from 0V, provides an error signal for emitter-follower Q1. The error signal is passed on to Q100, which then acts to correct the condition that produced the error. For example, an increase in the load on the output terminals requires that more current be supplied by Q100; therefore, the +15V output tends to decrease. The voltage divider produces a more negative level at the base of Q3. Q3 provides a positive error signal that is passed on to the base of Q100. The increase in forward-bias causes Q100 to oppose the tendency of the emitter voltage to decrease. The operating point of Q100 has been shifted; thus, the demand for more current is met, even though the collector-emitter voltage remains constant.

The +15 Vdc supply is also regulated against static and dynamic line voltage variation. Changes in the rectified dc voltage cause the collector-emitter voltage of Q100 to change in the same direction. The +15V output also changes, but in such small proportion that it essentially remains constant over the allowable ac input range.

Note that this power supply has no adjustment. The -15 Vdc regulated supply voltage works with the +15V output to develop error voltages at the R6/R7 voltage divider. In addition, the -15 Vdc voltage controls the total emitter current of the difference amplifier. Thus, static changes in the -15 Vdc output can be passed on to the +15 Vdc regulator. An adjustment potentiometer is included in the -15 Vdc supply; consequently, both supplies can be adjusted at the same time, the +15V output tracking the -15V output.

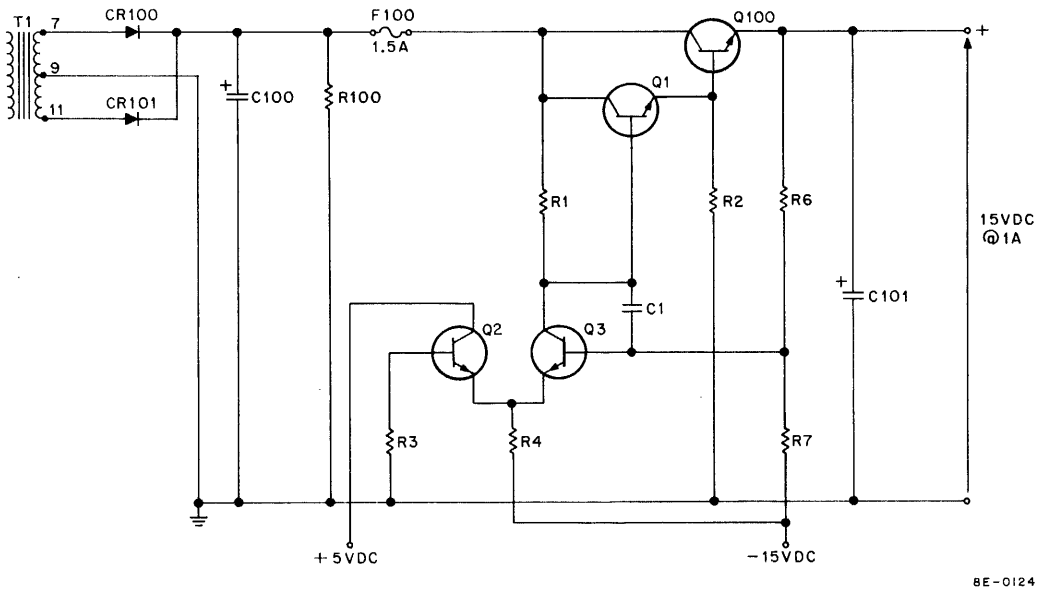


Figure 3-124 +15 Vdc Power Supply

3.47.4 -15 Vdc Power Supply

The -15 Vdc power supply is shown in Figure 3-125. This power supply is regulated in a manner similar to that described in the last paragraph. However, the procedure is carried out more precisely. The regulating amplifier is a precision voltage regulator IC, VR1. This IC contains a temperature-compensated reference amplifier, an error amplifier, and a series power-pass transistor. Pin 4 is the output of the reference amplifier. The reference voltage for the error amplifier is taken from the wiper arm of potentiometer R5, the -15 Vdc adjustment. This reference is compared with a sample of the -15 Vdc output, which is applied to the error amplifier at pin 2. The error signal is amplified and transferred, via pin 6, to Q300, which provides a change in base drive for Q301–304. Thus, static and dynamic load and line changes are regulated as in the +15 Vdc regulator.

Note that the series pass transistor consists of four transistors, Q301 through Q304, in parallel. Each transistor has a 0.25Ω, 3W resistor connected to its emitter lead. The 0.25Ω resistors encourage equal division of the regulated load current through the pass transistors. In the event of an overload that is not sufficiently large to burn out F300, there is less likelihood of damage to a pass transistor. In addition, the parallel arrangement reduces the possibility of a pass transistor burning out before F300 if the output terminals are shorted.

3.47.5 +5 Vdc Power Supply

The +5 Vdc power supply is shown in Figure 3-126. Again, precise regulation is possible through the use of a voltage regulator IC, VR5. The reference voltage is taken from potentiometer R21, the +5V adjustment, and compared to the +5V output. The error signal controls the parallel pass transistors.

3.47.6 dc Voltage Monitor Circuit

The dc voltage monitor circuit is shown in Figure 3-127. This circuit negates the POWER OK H signal whenever a regulated dc voltage is less than an established absolute value. Such a condition occurs when the power is turned on or off, or when a failure occurs within the power supply. These absolute values are 4.3V for +5 Vdc voltage, 12V for +15 Vdc voltage, and 13.5V for the -15 Vdc voltage.

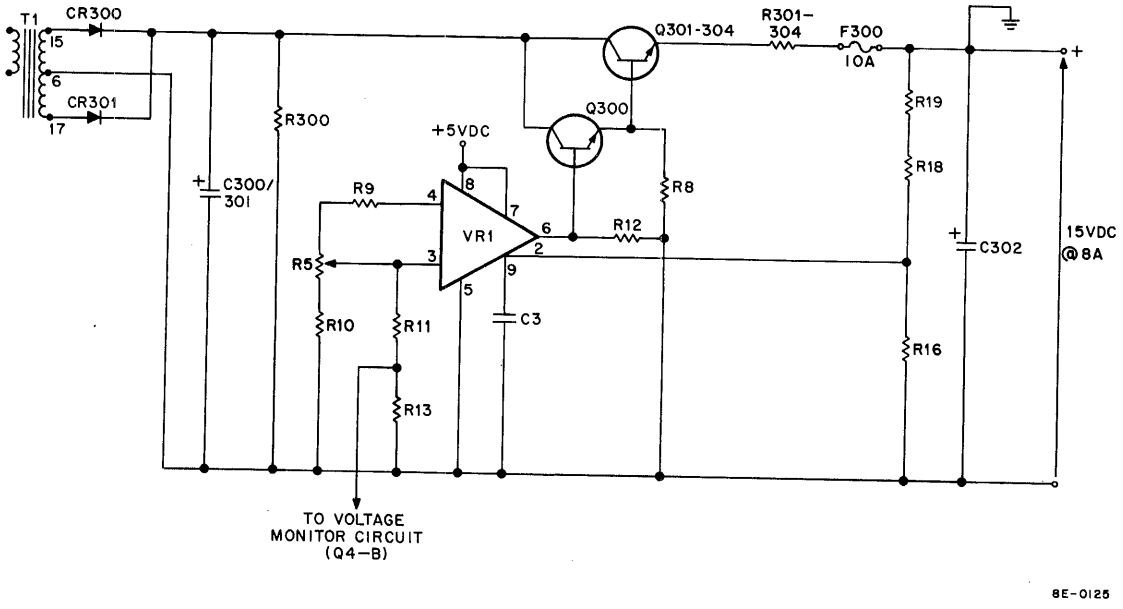


Figure 3-125 -15 Vdc Power Supply

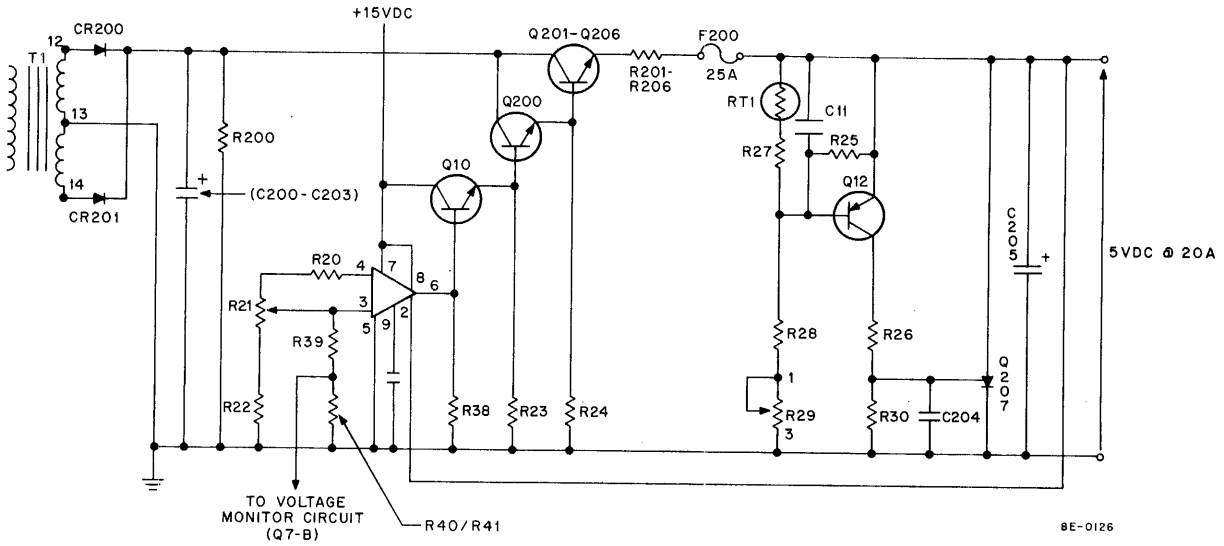


Figure 3-126 +5 Vdc Power Supply

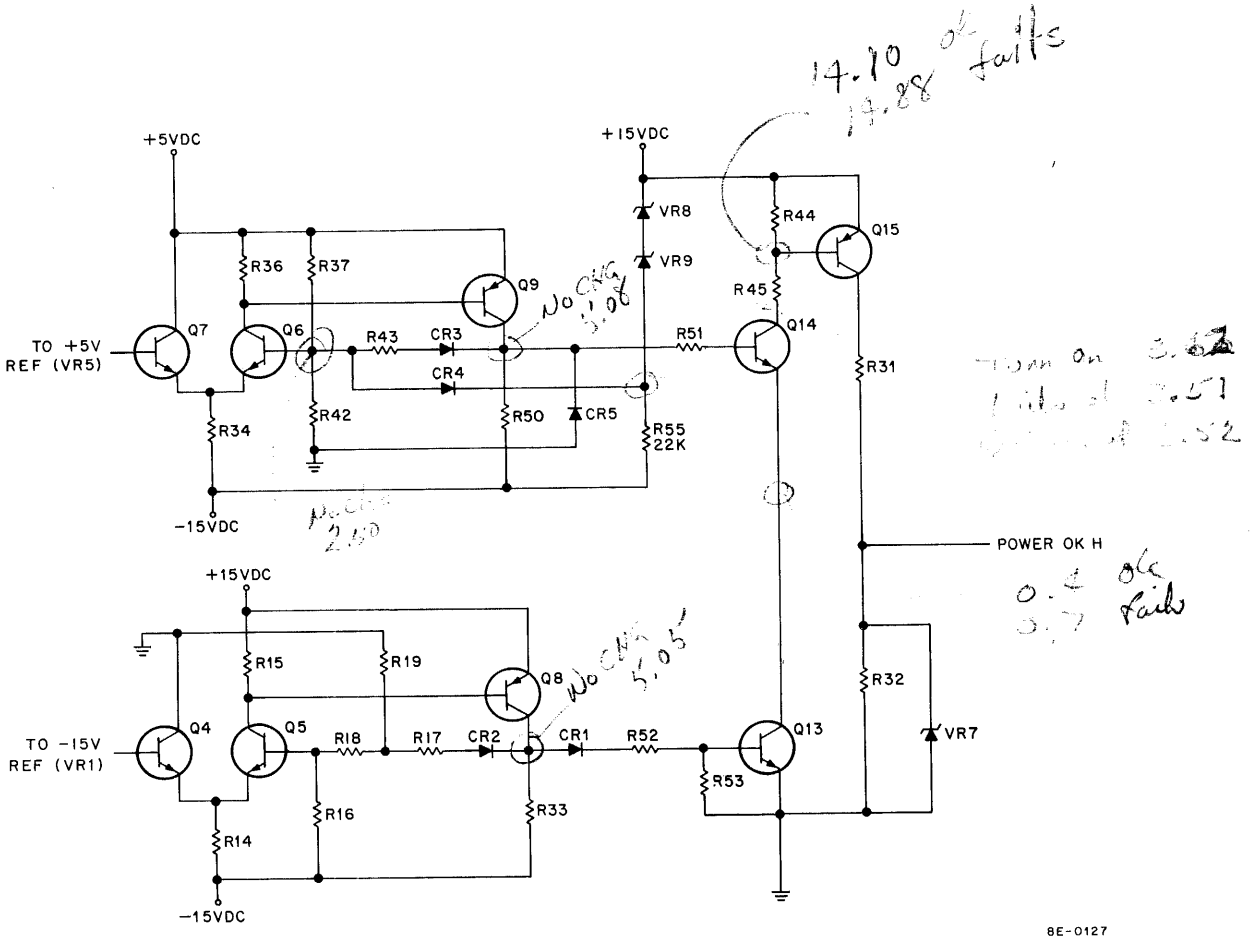


Figure 3-127 dc Voltage Monitor

If all three regulated voltages are above the limit, Q13, Q14, and Q15 are switched on. Zener diode VR7 maintains the POWER OK line at approximately 4.3V. If the -15 Vdc voltage goes more positive than -13.5V, Q13 is switched off, leaving the emitter of Q14 floating. Q15 turns off and the POWER OK line goes to ground. If the +15 Vdc voltage goes more negative than +12V, or if the +5 Vdc voltage goes more negative than +4.3V, Q14 is switched off, accomplishing the same result as before.

The circuits that control the switching of Q13 and Q14 are nearly identical. The circuit that includes Q6, Q7, and Q9 monitors both +5 Vdc and +15 Vdc. The Q6/Q7 difference amplifier is balanced when +5 Vdc is satisfactory. If +5 Vdc goes negative, Q6 is turned off, removing the emitter-base voltage of Q9, which turns off. The cathode of CR3 goes to ground, causing Q14 to turn off. If, instead of +5 Vdc, +15 Vdc goes more negative than its limit, CR4 is allowed to conduct. This action causes Q6 to turn off and, in turn, Q9 and Q14.

The circuit that includes Q4, Q5, and Q8 monitors the -15 Vdc voltage and works almost identically to the upper circuit. In this case, Q5 is turned off when -15 Vdc goes more positive. This action removes the base current from Q8. This removes base current from Q13, which then turns off.

3.47.7 Overvoltage Protection

The +5V power supply is provided with overvoltage protection, in the form of an SCR trigger circuit (Figure 3-126). If the +5V output rises to 6.5V, Q12 provides a triggering voltage for the gate of the SCR, Q207. The SCR conducts, and the resulting short circuit on the output terminals causes fuse F200 to burn out.

3.48 PDP-8/F and PDP-8/M POWER SUPPLY

3.48.1 Input Circuit

The H740 Power Supply input circuit is shown in Figure 3-128. The ac input is shown for a 130 Vac line only. When the turn-key switch is placed in the POWER position, line voltage is applied to the transformer and the fans. The thermostat on the regulator board opens if the ambient temperature reaches 100°C; the switch closes automatically when the temperature returns to approximately 64°C.

The line voltage is transformed to 28 Vac, center-tapped, and applied to the regulator board assembly via the secondary harness. All dc voltages are derived from this 28 Vac output. Connector J1 of the secondary harness is to be used for connecting either a KP8-E option (Power Fail Detect and Auto-Restart) or a DK8-EA option (Real-Time Clock Line Frequency).

3.48.2 +15 Vdc Power Supply

The +15 Vdc power supply (Figure 3-129) is series-regulated. The pass transistor, Q1, is a high-gain power Darlington and is mounted on the heat sink. Base drive current is supplied to Q1 via R38. Q3 limits the value of this current by shunting it away from the base of Q1. Q4, the voltage detector amplifier, biases Q3 and, thus, limits current in Q1. The +15 Vdc output is sampled by the voltage divider of R34, R35, and R36 and compared to the voltage across reference diode D8. If the output tends to change from the regulated value, Q4 generates an error signal. The error signal is returned to Q1, via Q3, and causes Q1 to correct the condition that produced the error.

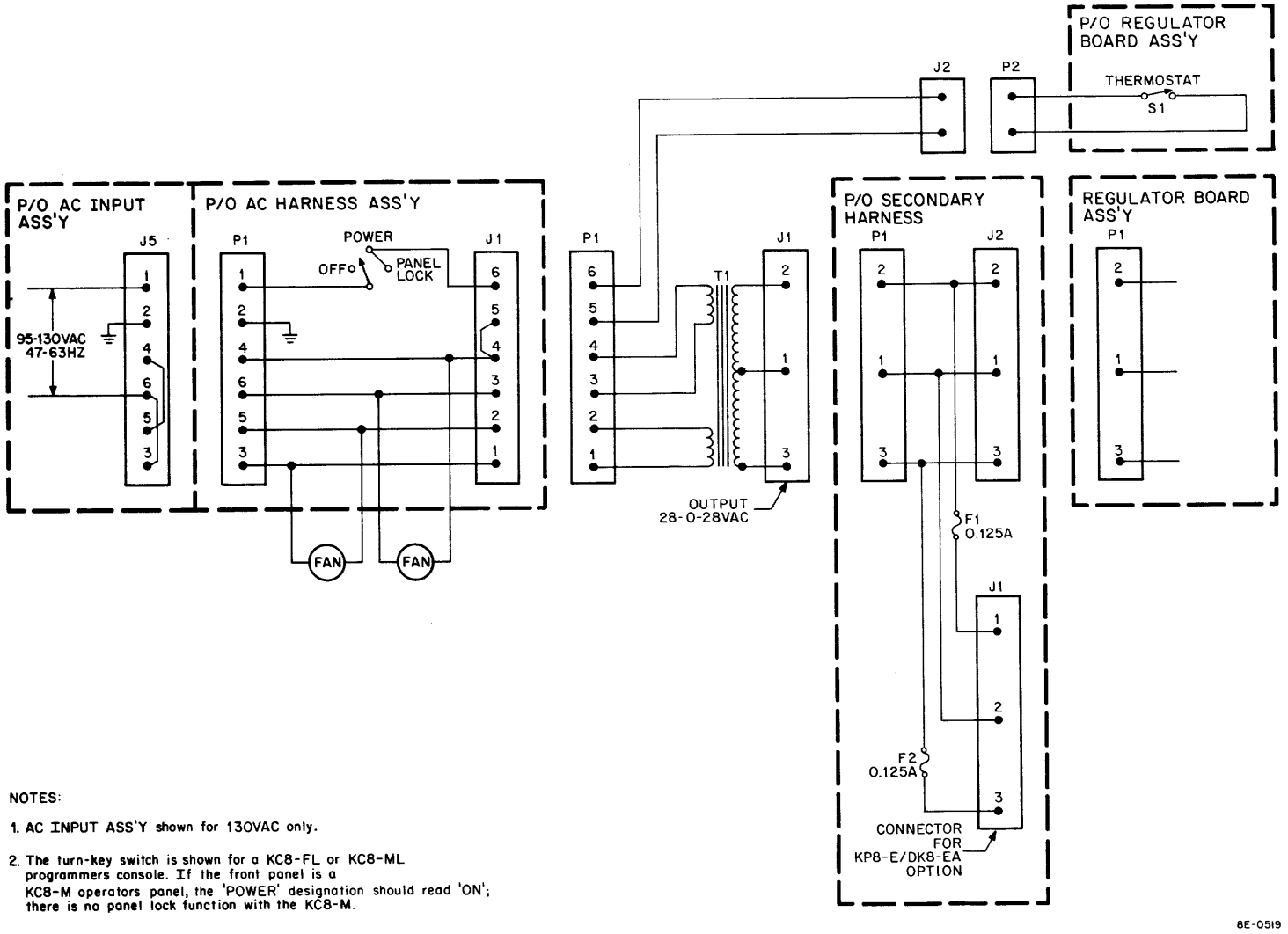
Static and dynamic line voltage variations are also controlled by the power supply. Changes in the rectified dc voltage cause the output voltage to change, but in such small proportion that the output remains essentially constant over the allowable ac input range.

Transistor Q2 is an overload detector. When the output current reaches 1.5A the voltage across R33 is large enough to cause Q2 to conduct; thus, the base drive is removed from Q1, thereby limiting the output current.

3.48.3 +5 Vdc Power Supply

The +5 Vdc power supply is shown in Figure 3-130. This supply is similar to the +15 Vdc supply; i.e., the output voltage is sampled and compared to the voltage across a reference diode, and an error signal is developed that causes the pass transistor to rectify the error.

However, regulation of the output voltage is more efficient than in the +15 Vdc supply. The +5 Vdc regulator operates in a switching mode; the entire circuit is a power Schmitt trigger that is either on or off depending on the output voltage level. When Q6 is on, it supplies current through the filter choke, L1, to the output smoothing capacitor, C7, and the load. When Q6 is off, the L1 current decays through commutating diode D10, which becomes forward biased by the back EMF of L1. The waveform across D10 is a 30V rectangular pulse train. The filtered output across C7 is +5 Vdc with a 200 mV, peak-to-peak, 10 kHz sawtooth ripple. At the crest of the ripple Q6 turns off; at the valley of the ripple Q6 turns on. This switching mode of operation limits the dissipation in the circuit to the saturated forward losses of Q6 and D10, and the switching losses of Q6. Therefore, the heat sink can be smaller than in the +15 Vdc supply, and the number of power semiconductors can be fewer.



NOTES:

1. AC INPUT ASS'Y shown for 130VAC only.
2. The turn-key switch is shown for a KC8-FL or KC8-ML programmers console. If the front panel is a KC8-M operators panel, the 'POWER' designation should read 'ON'; there is no panel lock function with the KC8-M.

Figure 3-128 H740 Power Supply Input Circuit

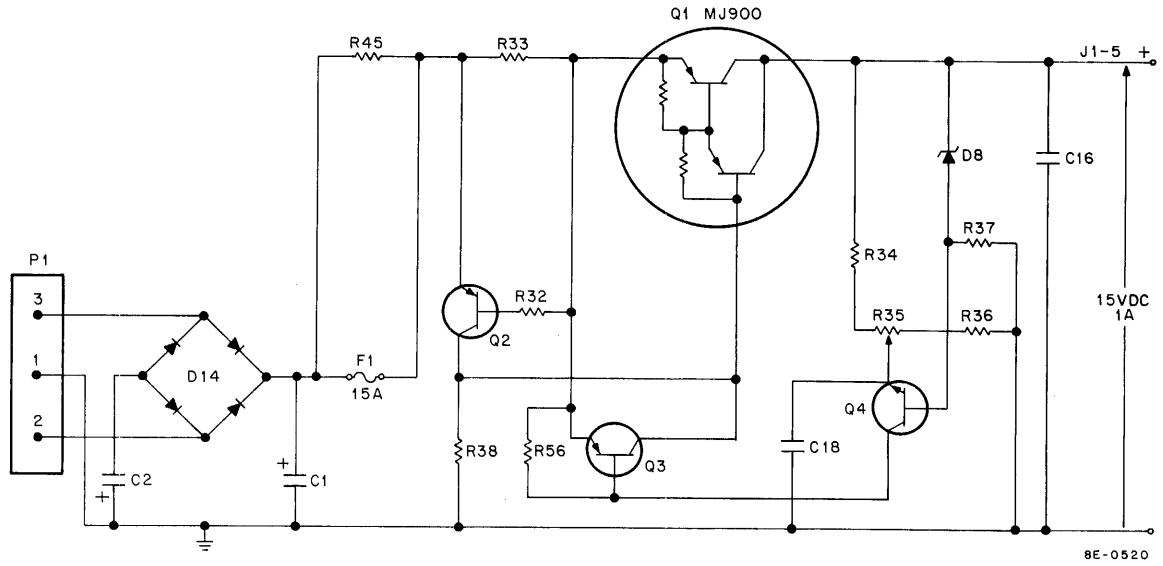


Figure 3-129 +15 Vdc Power Supply

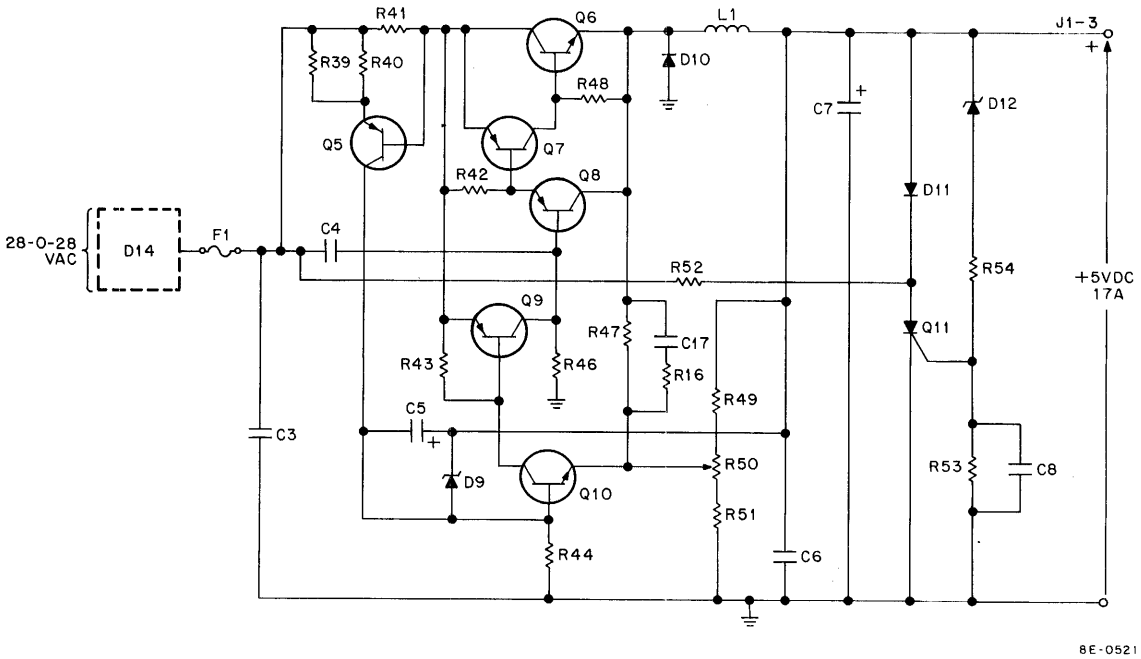


Figure 3-130 +5 Vdc Power Supply

Transistor Q5 detects an over-current condition when the voltage across R41 is sufficiently high. Output current is limited to a safe value since conduction of Q5 makes the reference voltage across D9 decrease to zero. Thus, Q10 conducts, shutting down the regulator.

If a fault causes the output voltage to increase beyond 6.3V, diode D12 conducts. The increased voltage on the gate of the SCR, Q11, fires the SCR, forcing the output voltage to a low value through D11 and causing F1 to burn out.

3.48.4 -15 Vdc Power Supply

The -15 Vdc power supply is shown in Figure 3-131. The circuit is the complement of that of the +5 Vdc supply. Minor differences in component types and values are necessary, but the switching mode of regulation is identical to that described in the preceding paragraph.

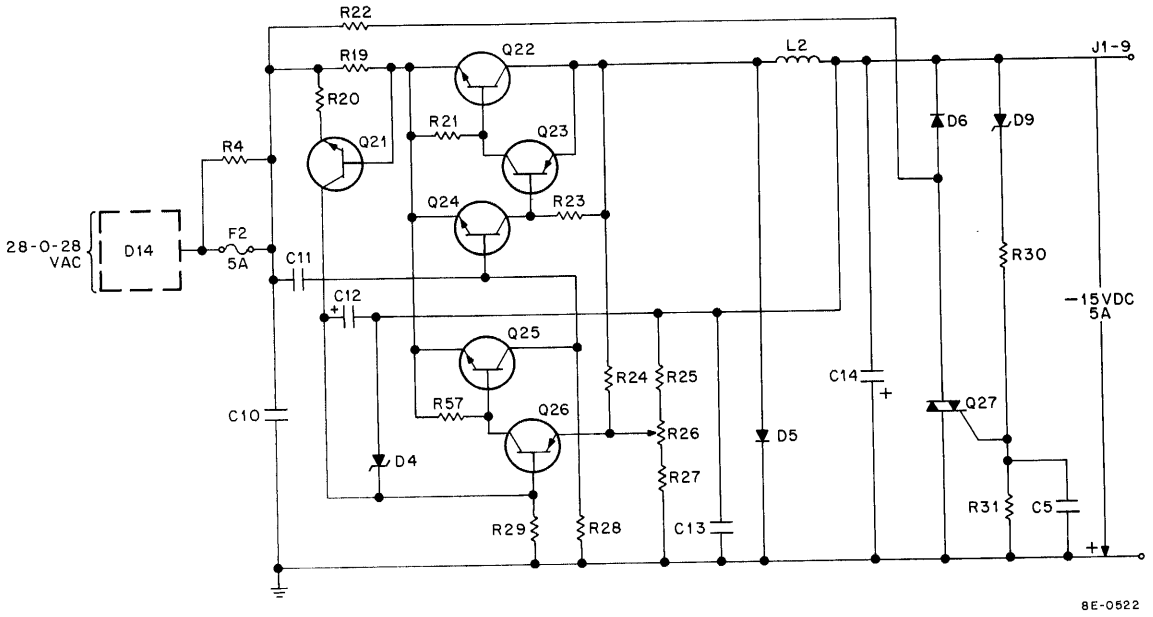


Figure 3-131 -15 Vdc Power Supply

3.48.5 Voltage Monitor Circuit

The voltage monitor circuit is shown in Figure 3-132. The circuit monitors the 28 Vac output of transformer T1 and the output of the +5 Vdc and +15 Vdc regulators.

The 28 Vac is rectified and filtered by diodes D1 and D2 and by capacitor C9, respectively. As C9 charges after power-on, transistor Q16, which is off initially, begins to conduct, while Q15 starts to turn off. A few milliseconds after power-on, the feedback provided by Zener diode D3 turns Q16 on heavily. The collector voltage of Q16 is positive enough to turn off both Q14 and Q13. The base of Q12 goes toward +5 Vdc and the POWER OK signal goes high.

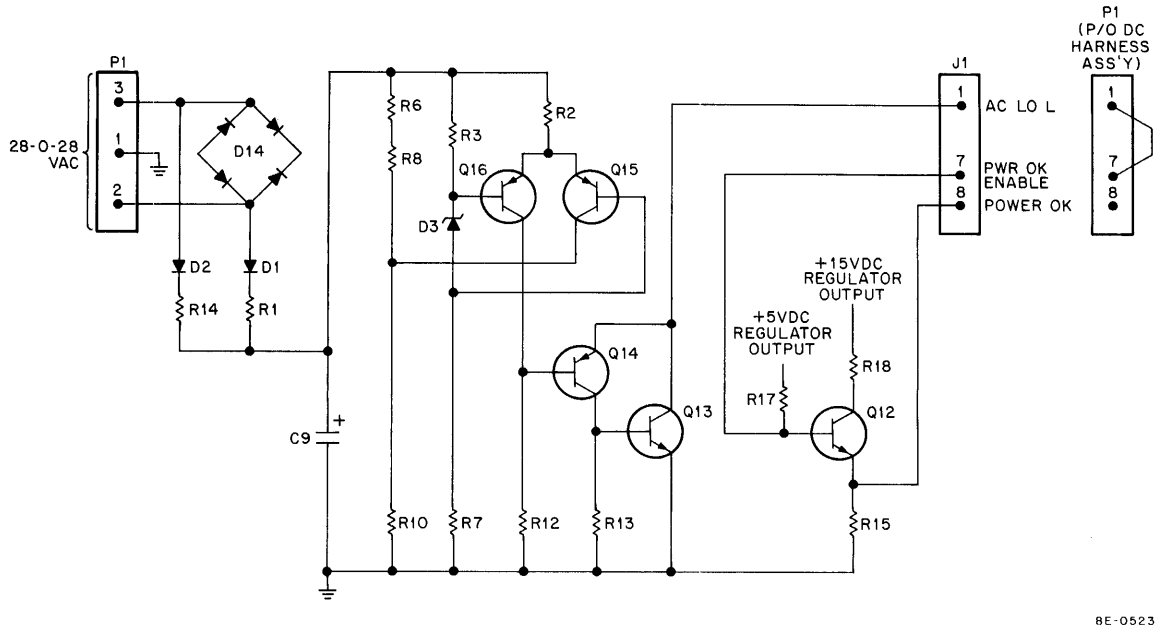


Figure 3-132 Voltage Monitor Circuit

Circuit parameters are chosen so that the regulated dc voltages are stable before Q14 and Q13 are turned off. If either the +15 Vdc output or the +5 Vdc output is missing or drops during normal operation, POWER OK is negated and the timing generator is halted.

CHAPTER 4
MAINTENANCE

This chapter contains information pertinent to preventive maintenance, corrective maintenance, and troubleshooting techniques of the PDP-8/E.

SECTION 1 - PREPARATION FOR MAINTENANCE

4.1 EQUIPMENT

Table 4-1 lists the equipment and relevant specifications needed for maintenance of the basic PDP-8/E. Also included in the list is the equivalent equipment used by DEC Field Service personnel.

4.2 PROGRAMS

Table 2-4 in Chapter 2 lists the maintenance programs supplied by DEC for ascertaining proper PDP-8/E operation. To supplement these programs, there are eight short test routines detailed in the following paragraphs. These routines can be used, as needed, to perform the required maintenance.

NOTE
All diagnostics require a Programmer's Console, a working Teletype and at least 4K memory with the basic system.

4.2.1 TTY Receiver Test

Perform the following test to display a character (any character depressed on keyboard or read from paper tape) in the ac. Load address 0000 and deposit the following test routine in sequence:

Location	Contents
0000	6032
0001	6031
0002	5001
0003	6036
0004	5001

Load address 0000 and press CONT.

Table 4-1
Maintenance Equipment

Equipment	Specifications	Equivalent
Multimeter	10kΩ/V minimum	Triplett Model 310
Oscilloscope	dc to 50 Hz with calibrated deflection factors from 5 mV to 10V/div. Maximum horizontal sweep rate of 0.1 μs/div. Delaying sweep is desirable and dual trace is a necessity.	Tektronix Type 453
Probes	X10 with response characteristics matched to oscilloscope.	Tektronix Type P6010
Recessed Probe Tip (2)		Tektronix
Ground Leads (for each probe)		Tektronix
Integrated Circuit Pin Extender	AP Inc	DEC 29-10246
Double-Height Extender (2)		W984
Edge Connector Extender Cables (2)		BC08M-OM
Light Bulb Extractor		DEC 12-9151
Tool Kit		DEC Type 142
Black Spray Paint		DEC 120-68
White Spray Paint		DEC 120-94
Jumper Wire		30-Gauge with TERMI POINT Connections
Silicone Grease		Dow Corning Compound
1/16 in. Allen Wrench		Hunter 4Z 035
Single-Height Extender Module (1)		W980

4.2.2 TTY Transmitter Test

Perform the following test to print the character in the Switch Register (bits 04–11). Load address 0000 and deposit the following test routine in sequence:

Location	Contents
0000	7604
0001	6046
0002	6041
0003	5002
0004	5000

Load address 0000 and press CONT. To print a different character, change the contents of the Switch Register.

4.2.3 Echo Test

Perform the following test to type a character on the keyboard. Load address 0000 and deposit the following test routine in sequence:

Location	Contents
0000	6032
0001	6031
0002	5001
0003	6036
0004	6046
0005	6041
0006	5005
0007	5001

Load address 0000 and press CONT. Type any character on the keyboard and observe a corresponding echo return on the printer.

4.2.4 Print Test

Perform the following test to print all characters. Load address 0000 and deposit the following test routine in sequence:

Location	Contents	
0000	7001	/Increment ac
0001	6046	/Load buffer and print
0002	6041	/Skip if flag is set
0003	5002	/JMP .-1
0004	5000	/JMP 0

Load address 0000 and press CONT.

4.2.5 Deposit SR into Corresponding Address

Perform the following test to deposit the contents of the Switch Register into the corresponding address. Load address 0000 and deposit the following test routine in sequence:

Location	Contents
0000	7604
0001	3005
0002	1005
0003	3405
0004	5000

Load address 0000, change SR to any number equal to or greater than 5, and press CONT.

4.2.6 4K Core Transfer (8K or more systems only)

Perform the following test to test the relocation process. Load address 7600 and deposit the following routine in sequence:

Location	Contents	
7600	6201	/Change data field to 0 (specifies source field)
7601	1670	/TAD I 7670
7602	6211	/Change data field to 1 (specifies destination field)
7603	3670	/DCA I 7670
7604	2270	/Increment LOC 7670
7605	-5300	/JMP .-5
7606	7402	/Halt when transfer complete
7670	0000	

Load address 7600 and press CONT. This routine can also be used to relocate diagnostic programs from one field to the other.

4.2.7 Write All Zeros

Perform the following test to write 0s in all address locations except some locations already occupied by the program. Load address 0004 and deposit the following test routine in sequence:

Location	Contents
0004	1007
0005	3410
0006	5004
0007	0000
0010	0011

Load address 0004 and press CONT. Computer will hang-up and all addresses will contain 0s, except locations occupied by the program. Note: addresses 0004 and 0005 will contain 0s after one program pass.

To write any other word, repeat the same procedures but change address 0007 to the desired word.

SECTION 2 - PREVENTIVE MAINTENANCE

4.3 PREVENTIVE MAINTENANCE INSPECTIONS

This section provides information for performing preventive maintenance inspections. This information consists of visual, static, and dynamic tests that provide better equipment reliability. Preventive maintenance consists of procedures that are performed prior to the initial operation of the computer and periodically during its operating life. These procedures include visual inspections, cleaning, mechanical checks, and operational testing. A log should be kept to record specific data that indicates the performance history and rate of deterioration; such a record can be used to determine the need and time for performing corrective maintenance on the system.

Scheduling of computer usage should always include specific time intervals that are set aside for scheduled maintenance purposes. Careful diagnostic testing programs can then reveal problems which may only occur intermittently during on-line operation.

4.4 SCHEDULED MAINTENANCE

The PDP-8/E must receive certain routine maintenance attention to ensure maximum life and reliability. Digital Equipment Corporation suggests the maintenance schedule defined in Table 4-2.

Table 4-2
Processor Preventive Maintenance Schedule
(3 months or 500 hours)

Type	Action
Cleaning	a. Clean the exterior and interior of the computer cabinet, using a vacuum cleaner and/or clean cloths moistened in nonflammable solvent.
	b. Clean the air filter. Use a vacuum cleaner to remove accumulated dirt and dust, or wash with clean hot water and thoroughly dry before using.
Lubricate	a. Lubricate slide mechanisms and casters with a light machine oil or powdered graphite. Wipe off excess oil.
Inspect	a. Visually inspect equipment for general condition. Repaint any scratched areas.
	b. Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strains, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.
	c. Inspect the following for mechanical security: key switches, control knobs, lamps, connectors, transformers, fans, capacitors, etc. Tighten or replace as required.
	d. Inspect all module mounting panels to ensure that each module is securely seated in its connector. Remove and clean any module that may have collected excess dirt or dust.

Table 4-2 (Cont)
Processor Preventive Maintenance Schedule
3 months or 500 hours

Type	Action
	e. Inspect power supply components for leaky capacitors, overheated resistors, etc. Replace any defective components.
	f. Check the output of the H724(A) power supply as specified in Table 4-8. Use a multimeter to make these measurements without disconnecting the load. If any output voltage is not within tolerance, the supply is considered defective, and corrective maintenance should be performed.
Perform	a. Run all MAINDEC programs to verify proper computer operation in Table 2-4. Each program should be allowed to run for at least three minutes or two passes, whichever is longer.
	b. Perform all preventive maintenance operations for each peripheral device included in the PDP-8/E System as directed in the individual maintenance instructions supplied with each peripheral device.
	c. Enter preventive maintenance results in log book.

4.4.1 Weekly Preventive Maintenance Schedule

Under weekly maintenance, time should be scheduled each week to operate the MAINDEC programs as listed in Table 2-4. Run each program for a minimum of three minutes. Take any corrective action necessary at this time and log the results. External cleanliness of the system should also be maintained on a weekly basis.

4.4.2 The Importance of a Preventive Maintenance Schedule

Computer downtime can be minimized by rigid adherence to a preventive maintenance schedule. A dirty air filter can cause machine failure through overheating. All filters should be cleaned periodically. The procedure for filter cleaning is described in Table 4-2.

SECTION 3 - CORRECTIVE MAINTENANCE

4.5 MAINTENANCE PROCEDURES

The PDP-8/E is constructed of highly reliable MSI IC logic modules. Use of these circuits and a minimum amount of preventive maintenance ensures relatively little equipment downtime due to failure. If a malfunction occurs, maintenance personnel should analyze the condition and correct it as indicated in the following procedures. Neither special test equipment nor special tools are required for corrective maintenance other than a broad-bandwidth oscilloscope and a multimeter. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance should become thoroughly familiar with the system concept, logic drawings, operation of specific IC circuits, and location of mechanical and electrical components.

It is virtually impossible to outline any specific procedures for locating faults within complex digital systems such as the PDP-8/E. However, diagnosis and remedial action for a fault condition can be undertaken logically and systematically in the following phases:

a. Preliminary Investigation
b. System Troubleshooting
c. Logic Troubleshooting
d. Circuit Troubleshooting
e. Repairs and Replacement
f. Validation Tests
g. Log Entry

4.5.1 Preliminary Investigation

Before beginning troubleshooting procedures, explore every possible source of information. Gather all available information from those users who have encountered the problem and check the system log book for any previous references to the problem. The troubleshooting flowchart (Figure 4-1) should be used to localize the problem. This flowchart is not a complete guide to determining system fault; it is intended to give the user some thoughts on where a problem could be, a possible solution, and how to describe it to the DEC representative before he arrives on site.

Do not attempt to troubleshoot by use of complex system programs alone. Run the MAINDEC programs and select the shortest, simplest program available that exhibits the error conditions. MAINDEC programs are carefully written to include program loops for assistance in system and logic troubleshooting.

4.5.2 System Troubleshooting

When the problem is understood and the proper program is selected, the logical section of the system at fault should be determined. Obviously, the program that has been selected gives a reasonable idea of what section of the system is failing. However, faults in equipment that transmit or receive information, or improper connection of the system, frequently give indications similar to those caused by computer malfunctions.

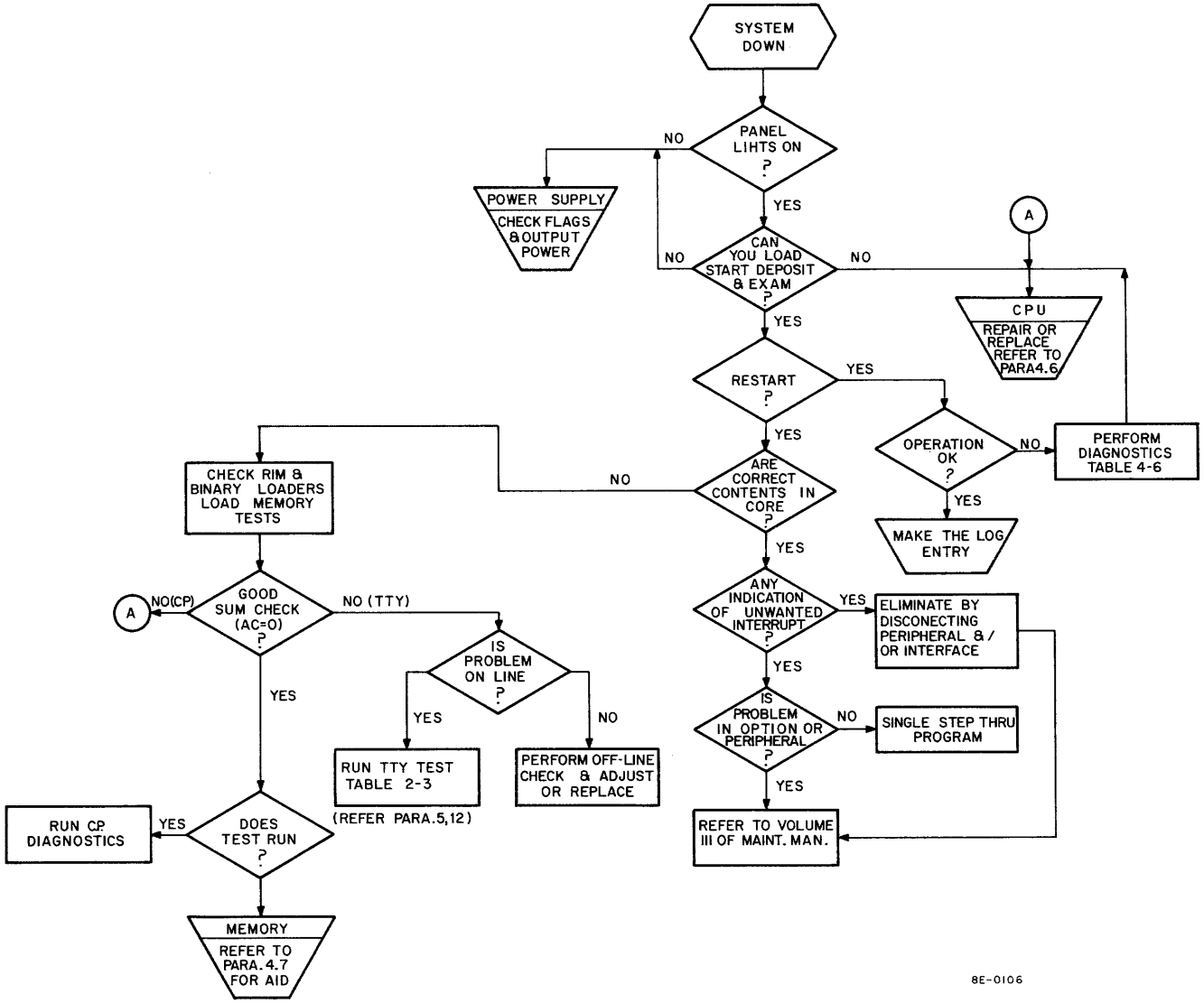


Figure 4-1 System Troubleshooting Flow Chart

Disconnect any peripheral devices that are not necessary to operate the failing program. At this time, reduce the program to its simplest scope loop and duplicate this loop in a dissimilar portion of memory to verify, for instance, that an operation failure is not dependent on memory location. This process can aid in distinguishing memory failures from processor failures. Use of the techniques described above often pinpoints the problem to a module or several ICs.

4.5.3 Logic Troubleshooting

Before attempting to troubleshoot the logic, make certain that proper and calibrated test equipment is available. Always calibrate the vertical preamp and probes of an oscilloscope before using. Make sure the oscilloscope has a good ground via the ac line cord, and keep the ground to the probe as short as possible with the aid of probe ground leads.

To extend the suspected module in the OMNIBUS perform the following procedure:

1 Turn off power.

2 Remove the H851 Edge Connector, if applicable, from the module.

3 Remove the module.

4 Insert two double-extender boards into the same slot.

5 Insert the suspected module into the extender board.

6 If applicable, connect the two edge-connector extender cables (BC08M-OM). This method should be used only with short program loops.

7 Turn power on.

8 Use IC pin extender for signal tracing and for grounding of scope.

NOTE

Test points on individual modules can be observed by connecting the oscilloscope to available pins on the extender.

Use the oscilloscope and IC pin extender to trace signal flow through the suspected logic elements. Oscilloscope sweep can be synchronized by control pulses or by level transitions that are available on individual IC pins at the component side of the module. Exercise care when probing the logic, to prevent shorting between pins. Shorting of signal pins to power supply pins can result in damaged components. Within modules, unused gate inputs are held at +3V.

NOTE

If vibration of the PDP-8/E is desired during troubleshooting, ensure that the vibration is of low enough amplitude that intermodule shorts will not occur.

4.5.4 Circuit Troubleshooting

Engineering schematic diagrams of each module are supplied with each PDP-8/E System and should be referred to for detailed circuit information.

Visually inspect the module on both the component side and the printed wiring side to check for overheated or broken components or etch. If this inspection fails to reveal the cause of trouble or confirm an observed fault condition, use the multimeter to measure resistance of suspected components.

CAUTION

Do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the forward and reverse resistances of diodes. Diodes should measure approximately 20Ω forward and more than 1000Ω reverse. If readings in each direction are the same and no parallel paths exist, replace the diode.

Measure the emitter-collector, collector-base, and emitter-base resistances of transistors in both directions. Short circuits between collector and emitter or an open circuit in the base-emitter path cause most failures. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50Ω to 100Ω exist between the emitter and the base, or between the collector and the base in the forward direction, and an open circuit condition exists in the reverse direction. To determine forward and reverse directions, consider a transistor as two diodes connected back to back. In this analogy, PNP transistors would have both cathodes connected together to form the base, and both the emitter and collector would assume the function of an anode. In NPN transistors, the base would be a common-anode connection; and both the emitter and collector, the cathode.

Multimeter polarity must be checked before measuring resistance, because many meters apply a positive voltage to the common lead when in the resistance mode.

ICs contain complex integrated circuits with only the input, output, and power terminals available; thus, static multimeter testing is limited to continuity checks for shorts between terminals. IC checking is best done under dynamic conditions using a module extender to make terminals readily accessible. Using PDP-8/E logic diagrams and M-series module schematics, locate an IC on a circuit board as follows:

1 Hold the module with the handle in your left hand; component side facing you.

2 ICs are numbered starting at the contact side of the board; upper right-hand corner.

3 The numbers increase toward the handle.

4 When a row is complete, the next IC is located in the next row at the contact end of the board (Figure 4-2).

5 The pins on each IC are located as Figure 4-3 illustrates.

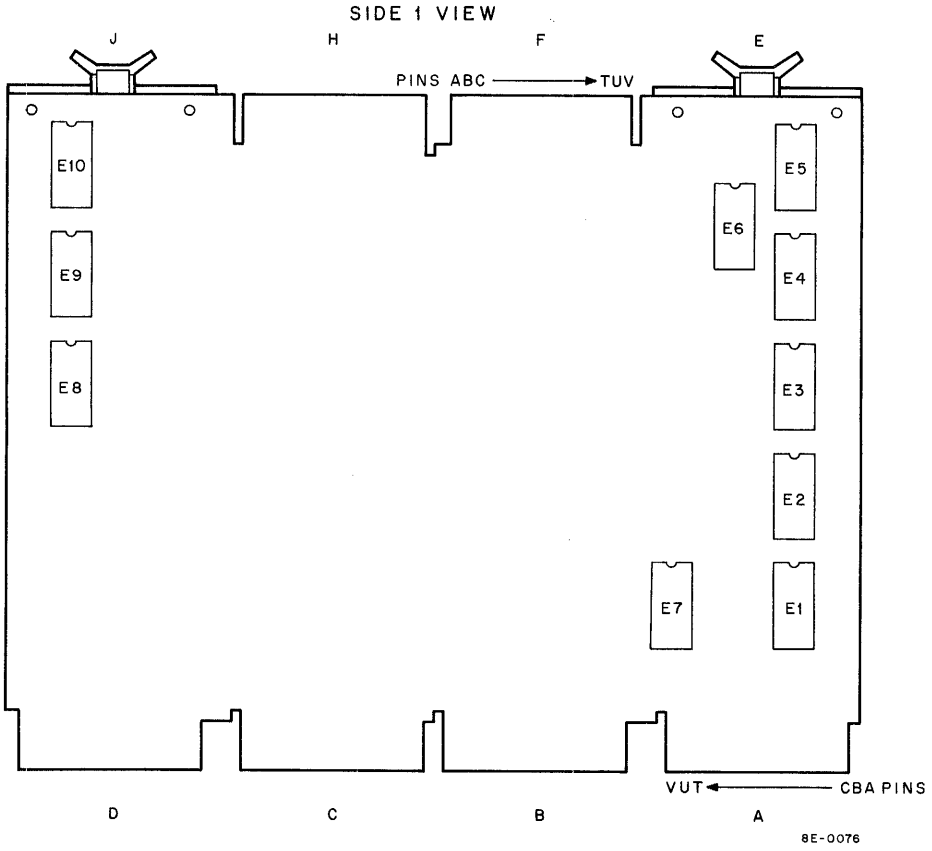


Figure 4-2 IC Location

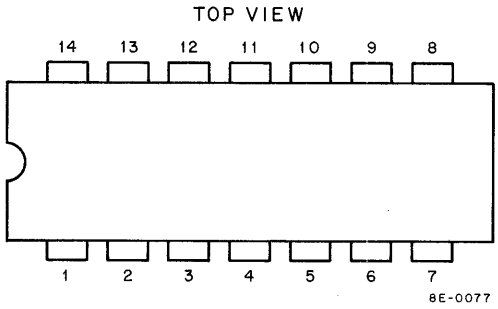


Figure 4-3 IC Pin Location

4.5.5 Repairs and Replacements

When soldering semiconductor devices (transistor, diodes, rectifiers, or integrated circuits) that can be damaged by heat, physical shock, or excessive electrical current, take the following special precautions:

1 Use a heat sink, such as a pair of pliers, to grip the lead between the joint and device being soldered.

2 Use a 6V iron with an isolation transformer. Use the smallest iron adequate for the work. Use of an iron without an isolation transformer can result in excessive voltages presented at the iron tip. Use only pencil-pointed tip soldering irons on PC boards.

3 Perform the soldering operation in the shortest possible time to prevent damage to the component and delamination of the module etched wiring.

4 ICs can be removed by using a solder puller to remove all excessive solder from contacts. Then, by straightening the leads, lift the IC from its terminal points. If it is not desired to save the defective IC for test purposes, perform Steps 5 through 12. If the IC is to be saved, perform Steps 8 through 12 (remove IC following Step 8).

5 Clip IC leads at top of lead at the connection to chip.

6 Remove chip portion of IC.

7 Apply heat to individual leads from siside #1 and remove leads slowly from side #1, using a pair of needle nose pliers. Do not hold lead with pliers while applying heat; the pliers will act as a heat sink.

8 Turn board over to side #2 and heat each hole individually, removing excess solder with desoldering tool.

9 Insert new component, bending appropriate leads. (Only leads with tear drop lands should be bent. They should be bent in the direction of the point.)

10 Clip protruding component leads from side #2. Do not cut flush with the board. (Leads and solder joints cannot exceed 1/16 in. from bottom of board.)

11 Solder all leads on side #2.

12 Clean flux from both sides of board with TRICHLORETHYLENE, FREON, or equivalent. *Be careful — both substances will damage the plastic handle.*

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or service lines. When repair has been completed, remove all excess flux by washing junctions with a solvent such as trichlorethylene. Be very careful not to expose paint or plastic surfaces to this solvent.

CAUTION

Never attempt to remove solder from terminal points by heating and rapping module against another surface. This practive can result in module or component damage. Remove solder with a solder-sucking tool or solderwick.

When removing any part of the equipment for repair and replacement, make certain that all leads or wires that are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals. Replace defective component only with parts of equal or better quality and equal tolerance.

To remove a switch on the Programmer's Console, follow the procedure below:

1 Turn power off.

2 Loosen Allen screw and remove knob from rotary switch.

3 Remove four screws from Bezel.

4 Carefully remove the face plate.

5 Remove two screws retaining aluminum mounting bracket.

6 Remove two wires from tab terminals on the left-hand side of the console.

7 Remove Programmer's Console board.

8 Remove faulty switch.

9 When replacing the panel, the yellow wire goes to the top tab terminal and blue wire to the bottom.

To remove the power supply heat sink assembly (Paragraph 4.8), follow the procedure below:

1 Remove ac power by turning off CB1 and disconnecting the ac plug.

NOTE
If the PDP-8/E is rack-mounted, remove carefully and place on table.

2 Remove the power supply assembly from the chassis as follows:

a. Remove five Phillips-head screws. Two are located on the front side of the chassis, one on the rear side, and two are located on the back side.

NOTE
If the PDP-8/E is rack-mounted, the chassis tracks and the five mounting screws must be removed.

b. Unplug the OMNIBUS power and switch power harness.

c. Lift up the power supply and slide it back just far enough to remove the blue and the yellow power wires from the front panel.

d. Lift out the power supply.

3 Remove the protective screen from the side of the power supply by removing the 12 countersunk screws on the screen.

4 Remove the heat sink assembly as follows:

   a. Remove the nylon plug from the heat sink assembly bracket.
   b. Remove the six screws from the heat sink assembly bracket.
   c. Lift out the heat sink assembly.

5 During replacement, the yellow wire goes to the top tab terminal of the front panel.

4.5.6 Validation Tests

If a defective module is replaced by a new one while repairs are being made, tag the defective module noting the nature of the failure. When repairs are completed, ascertain that the repairs have resolved the problem.

To confirm that repairs have been completed, run all tests that originally exhibited the problem. If modules have been moved during the troubleshooting period, return all modules to their original positions before running the validation tests.

4.5.7 Log Entry

A log book is supplied with each PDP-8/E System. Corrective maintenance is not complete until all activities are recorded in the log book. Record all data indicating the symptoms given by the fault, the method of fault detection, the component at fault, and any comments that would be helpful in maintaining the equipment in the future.

The log book should be maintained on a daily basis, recording all operator usage and preventive maintenance results.

4.6 CPU TROUBLESHOOTING

After it is established that the CPU is causing the problem (Figure 4-1), Table 4-3 can be used as a troubleshooting aid to isolate the problem. The symptoms and causes are examples that may help the computer technician to find the area in which to look, once an abnormal indication is noted on the Programmer's Console.

When troubleshooting the PDP-8/E, remember that the OMNIBUS is designed so that all pins that are lettered the same are connected to each other, and that a signal can be provided from more than one place. An example is MD6, which is on pins BM1 of all slots of the OMNIBUS. The source of MD06 can come from either the Major Register module (M8300) or the Sense/Inhibit module (G104) and is used by five of the nine modules in the basic computer. To find the source and destination of all the signals used in the basic computer, refer to Appendix B.

4.7 MEMORY TROUBLESHOOTING

After it is established that the memory is the source of the problem through symptom analysis using the system troubleshooting flowchart (Figure 4-1), the memory troubleshooting flowchart (Figure 4-4) and associated troubleshooting Tables 4-4 and 4-5 and waveforms in Figure 4-5 may be used to isolate the problem.

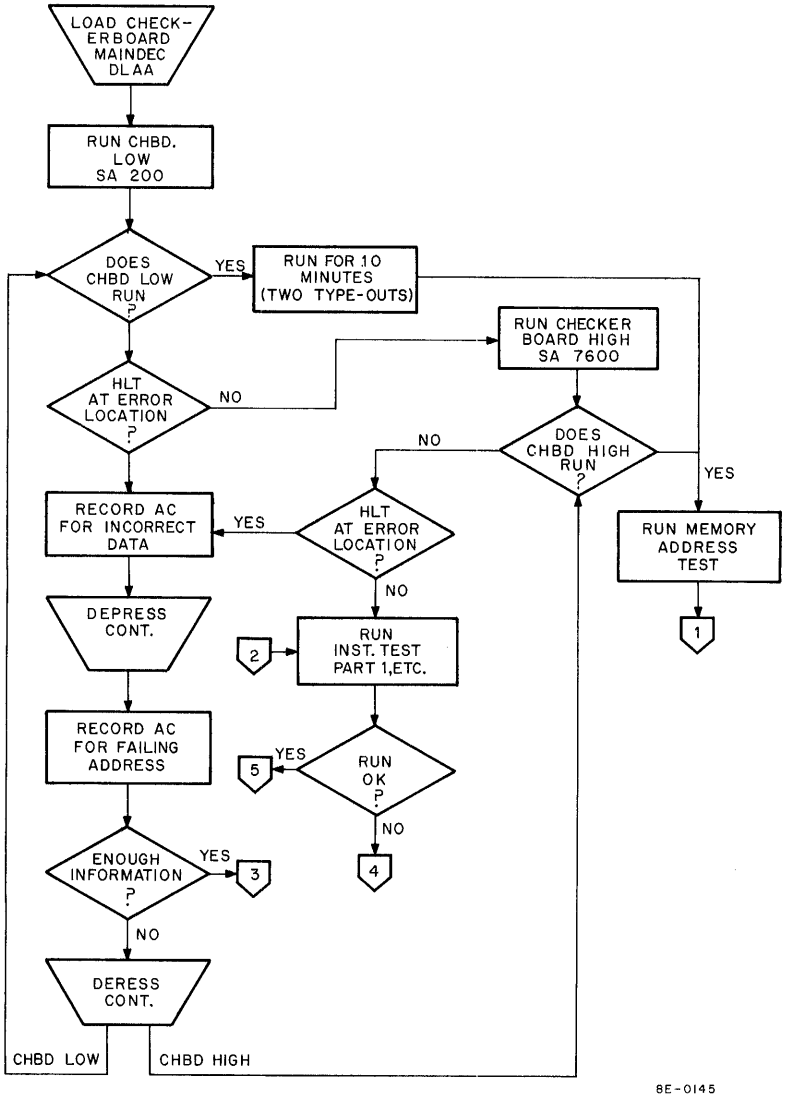


Figure 4-4 Memory Troubleshooting Flowchart (Sheet 1 of 2)

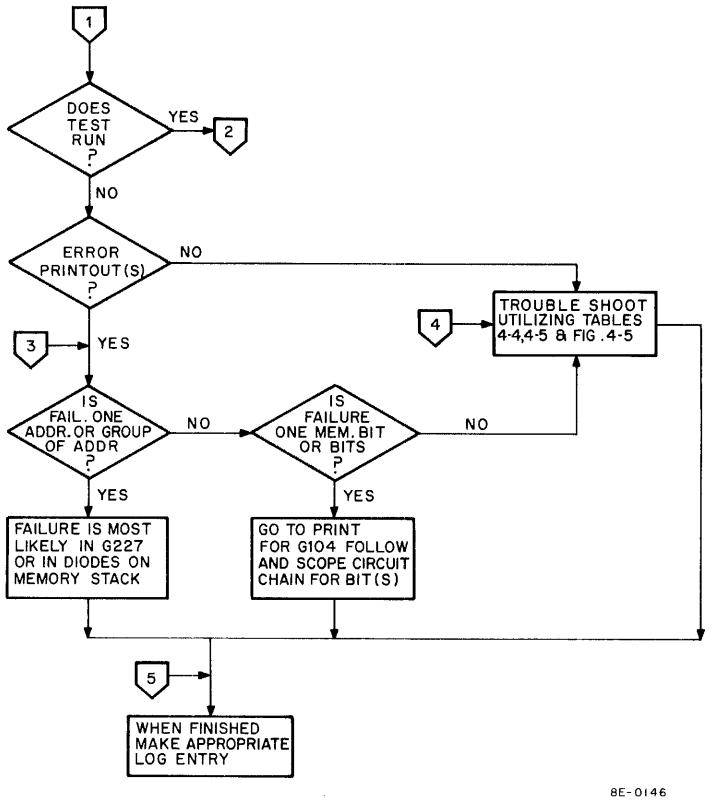


Figure 4-4 Memory Troubleshooting Flowchart (Sheet 2 of 2)

4.7.1 Memory Resistance Checks

There are also some resistance checks that can be performed to aid in isolating a trouble in the memory. These resistance checks are summarized below:

1 Turn power off.

2 Remove memory stack module.

3 Resistance of thermistor network is approximately 150Ω.

4 Resistance of individual thermistor when out of the circuit is approximately 56Ω.

5 Resistance of winding for one bit is approximately 3Ω (for example, between pins FA and FB for bit 6).

6 Resistance of diodes FSA2501 is as follows: Forward – approximately 24Ω; Reverse – approximately greater than 1MΩ.

CAUTION

Metal can transistors have their casing connected to the collector. Care should be exercised to prevent a ground lead or the back of another module from touching the metal can during troubleshooting.

Table 4-3
Processor Troubleshooting

Item	Symptom	Likely Cause	Module
1	A signal on the OMNIBUS is always low.	Bus loads, diode from GND to the OMNIBUS is shorted.	M8320
2	Unable to start automatic operations (run light always off).	a. Missing MEM START L, which is a 300 to 500 ns pulse for everytime CONT, DEP, or EXAM key is depressed. b. Power OK "delayed" or Power OK is true.	M8330 and KC8-E
3	Unable to change Major States.	Missing CPMA LOAD L. MA, MS LOAD CONT L grounded.	M8310
4	Unable to modify any memory locations.	a. MB LOAD b. Memory direction always low c. INHIBIT always low d. WRITE L stays low e. SOURCE stays low f. FIELD L is high (Refer to Table 4-4, Memory Data Errors.)	M8310 M8330 M8330 M8330 M8330 G104
5	Data from memory is not getting to the MB.	a. Memory direction always high b. No MB LOAD L c. No TIME STROBE d. WRITE L staying high (Refer to Table 4-4, Memory Data Errors.)	M8330 M8310 G104 M8330
6	When loading an address, the word in the MA is not the same as the Switch Register.	LA ENABLE is always high (this causes the switch register to be ORed with AC, MQ, or STATUS if the rotary switch is in one of these positions).	KC8-E
7	When using LOAD ADDR, DEPOSIT, or EXAM, the MA changes to an incorrect value (EX:0020 → 0634).	EN0, EN1, EN2 or LEFT L, RIGHT L, TWICE L are an incorrect level. Refer to truth table on M8310 logic print, sheet 3 of 3.	M8310
8	Depressing ADDR LOAD key will enter all 1s in the MA. By examining and observing the MD, it will be noted that the register will change when the key is released.	DATA T always high.	M8310

Table 4-3 (Cont)
Processor Troubleshooting

Item	Symptom	Likely Cause	Module
9	The MA decrements when doing an EXAM or DEPOSIT.	DATA F is always low. Refer to truth table on M8310 logic print, sheet 3 of 3.	M8310
10	When doing an EXAM, DEPOSIT, CONTINUE, or a JUMP instruction, the MA bits 0 – 4 are zeroed.	PAGE Z L is high. (If just one of MA 0 → 4 check PAGE Z circuit on M8300.)	M8310 M8300
11	CPMA, MB, PC, or AC do not increment.	CAR IN L is always high to the adder. It should be generated for: a. During TS1 with DEPOSIT, EXAM, or EX TO LOAD depressed. b. TS1 of FETCH state. c. TS2 of DEFER state. d. EXECUTE state and TS2 of an ISZ, or TS3 of a JMS. e. TS3 of a Group 2 OPR instruction. f. If SKIP is set: TS2 of EXECUTE doing a JMS, or TS4 of a MRI.	M8310
12	Unable to SKIP on an ISZ instruction.	a. SKIP F/F will not clear. b. No "carryout". c. No "overflow".	M8310
13	Information being read from Teletype is loading into MA and PC.	C2 L is always low, which causes PC LOAD at BUS STROBE (TP3) time instead of AC loading.	M8320 M8310 M8330

Table 4-4
Memory Data Errors — Possible Causes

Symptom	Cause	Module	Check
One Bit = 1 OR 0	Inhibit Driver	G104	Collector of 2007 transistors
One Bit = 1 OR 0	Sense Amplifier	G104	E31-42 Pin 8
Random = 1 OR 0	Time Strobe	G104	E9-3
Random/All = 0	XY current/voltage is low	G227	≈5.3V across +5V and Pin JU2
Random/All = 1	XY current/voltage is high	G227	Same as above
Random/All = 1	Slice voltage low	G104	≈5.3V across GND and test point DA1
Random/All = 0	Slice voltage high	G104	≈5.3V across GND and test point DA1
Random/All = 1	Inhibit current/voltage low	G227	-15 Vdc power
Random = 0	Inhibit current/voltage high	G227	-15 Vdc power

Table 4-5
Memory Module Test Point Voltage Levels

Signal	Pin	Module	Approximate Readings
Current Control	HA1	G104	1.2V
	HV2	G104	2.3V
Current Source	JU2	G227	1.4V
	FU2	G104	0.25V
Test Point	DA1	G104	-5.3V
Test Point	CB1	G104	6V
Test Point	DB1	G104	-6V
Current Source	HU2	G104	4V
	FA1	G104	2.3V
	FB1	G104	-4V
	Q17 Emitter	G104	-4.8V
Memory Stack	Top of Thermistor		2.5V
Test Points	Q18 Collector	G104	-6V
	Q15, 16 Emitter	G104	+3V
	Q13 Base	G104	+1.3V

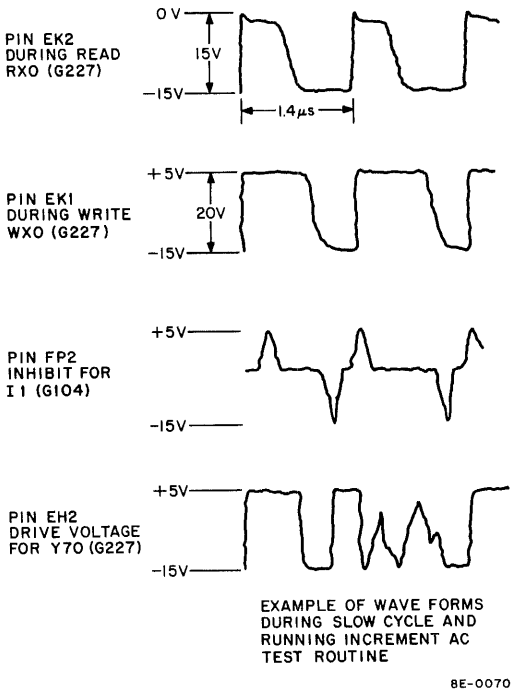


Figure 4-5 Memory Waveforms

4.7.2 Memory Circuit Variables

There are a number of variables in the MM8-E memory system such as current, slice, and field, that have to be set properly. Although some of the settings are permanent for a particular board, interchangeability in the field is assured. These variables are summarized in Table 4-6 and detailed in the following paragraphs.

Table 4-6
Memory Circuit Variables

Variables on MM8-E Memory System	Means for Settings	Location	Who Makes the Settings
Field Select	3 Jumpers EMA0, EMA1, EMA2	G104	Factory or Field Service
Strobe	6-position rotary switch	G104	Factory or Field Service
Slice	2 Jumpers – SLA, SLB	G104	Factory only
X/Y Current Control	2 Jumpers – CCA, CCB	G227	Factory only
Temperature Tracking	Thermistor-Resistor Combination RT, R1, R2, R3	G619	Factory only

4.7.3 Field Select Jumpers

The octal combination of the appropriate *cut* jumpers represents the selected field; therefore, for the basic system (no extended memory), all jumpers must be in place.

4.7.4 Strobe Adjustment

A 6-position rotary switch optimizes the strobe positioning in discrete steps of 10 ns. For detailed setting procedures, refer to Paragraph 4.7.9.

4.7.5 Slice Level

Any variation on the +5V power supply will cause a proportional change of the absolute value of the slice level.

The slice level can be set to four different levels according to the following truth table:

Jumpers		Slice Level (Testpoint DA1 on G104)
SLA	SLB	
In	In	-4.3V
Cut	In	-4.8V
In	Cut	-5.3V
Cut	Cut	-6.0V

NOTE
Do not field-adjust the slice level under any circumstances.

4.7.6 X/Y Current Control (G227)

On the G227 module there are two jumpers in the upper center of the module. These jumpers can be removed and a 24 AWG wire loop soldered in their place if it is necessary to measure currents with a current probe.

The X/Y current control can be set to four discrete levels to calibrate the current source. The nominal voltage varies with temperature and its corresponding X/Y current is 370 mA measured on a loop between the X/Y drive and the stack board. The pertinent truth table follows:

Jumpers		Current Control Voltage (Voltage across +5V and Pin JU2 on G227)
CCA	CCB	
In	In	+3.7%
In	Cut	+2.2%
Cut	In	Nominal (~3.5V at 25°C)
Cut	Cut	-1.7%

NOTE
Do not field-adjust current control voltage under any circumstances.

4.7.7 Temperature Tracking

A thermistor-resistor combination on the memory stack board provides a temperature-sensitive voltage divider, which is connected to the current control circuit.

4.7.8 Inhibit Current

The inhibit current is fixed; however, it varies proportionally to the -15V supply; its corresponding nominal value is 340 mA.

4.7.9 Strobe Setting Procedure

Setting the strobe properly is very important and must be done carefully. The chosen setting scheme makes this procedure relatively simple. Figure 4-6 illustrates the relation between X/Y current sense amplifier output and strobe.

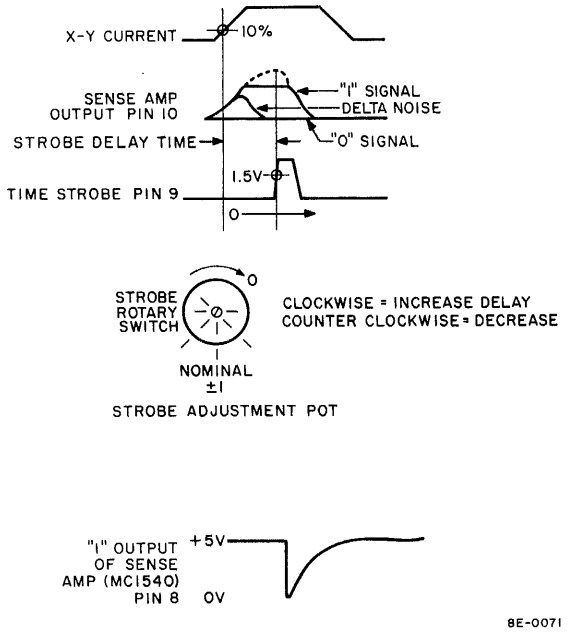


Figure 4-6 Setting of Strobe

It is not advisable to set the strobe timing using an oscilloscope and a current probe. Because of the length of the current probe cables, the bandwidth of the probe and scope may vary in each case.

The resulting correlation error can exceed the tolerance allowed, resulting in a misadjusted memory. To set the strobe accurately, perform the following procedure at room temperature:

1 The switch has to be set to one of the three possible nominal positions (Figure 4-6).

2 Load "Memory Checkerboard" maintenance program and run it.

3 Program should run without error.

4 Halt program and delay strobe 10 ns (1 position clockwise), then restart.

5 If program still runs without error, proceed to the next position. When errors occur, stop and memorize this strobe position.

6 Repeat the same procedure advancing the strobe (counterclockwise) until errors occur, then stop and memorize this position.

7 A reliable system has to have a minimum of three working consecutive positions.

8 Finally set strobe to the middle working position. If there is an even number of working positions, favor the most delayed (clockwise) of the two center positions.

9 In checkout, "Checkerboard" should always run in the middle position and, for at least 15 minutes, in the positions to the left and right of middle with no errors.

10 Acceptance is to be run only in the final strobe position.

11 Setting strobe for extended memories, load basic memory checkerboard (MAINDEC-8E-D1AA-D) into extended fields and proceed to set strobe position according to Steps 1 through 10.

4.8 H724 POWER SUPPLY TROUBLESHOOTING PROCEDURES

The H724 Power Supply provides power for CPU logic, the memory, bus loads, and the lamps on the Programmer's Console. If the power supply is established to be the source of the problem through symptom analysis with the aid of the system troubleshooting chart (Figure 4-1), voltage checks should be performed. Voltages and tolerances are given in Table 4-7. A component troubleshooting aid, Table 4-8, and parts location, Figure 4-7, are included as aids to isolating and correcting the malfunction.

The following paragraphs describe some of the power supply features and characteristics that can aid in isolating the malfunction.

Table 4-7
H724 Power Supply Parameters

Output Voltage	Wire Color	Minimum Voltage	Maximum Voltage	Tolerance	Current Rating	Maximum Ripple
+5V	Red	4.85V	5.15V	± 3%	20A	50 mV p-p
-15V	Blue	-14.25V	-15.75V	± 5%	8A	50 mV p-p
+15V	Orange	13.5V	16.5V	± 10%	1A	75 mV p-p
+8V	Yellow	6V	10V	± 26%	2A	
dc Volts OK	Grey	3.75V	5V			
Overvoltage Protection			6.5V			
14 Vac				± 26%	0.2A	
AC INTLK					0.12A	

Table 4-8
Component Troubleshooting Aid for H724 Power Supply

Output Volts	Wire Color	Jack & Pin	Fuse (amps)	Module	Transistors	Adjustment	Use
+5 Vdc	Red	J3-3 J4-3	25	A2	Q200 Q201-6	R21	CPU Logic
-15 Vdc	Blue	J3-4 J4-4 J6-3	10	A1	Q300 Q301 Q304	R5	Memory
+15 Vdc	Orange	J3-5 J4-5	1	A1	Q100	R5	Bus Loads
+8 Vdc	Yellow	J6-4	25				Lights
14 Vac	-	J5-1 J5-3	.5				Options
Overvoltage Protect	-			A2			Power Surge
dc Volts OK (3.75)	Grey	J3-6 J4-6		A2		R29 (Factory Adjustable Only)	Power Loss

Static ohmeter reading of thermistor is approximately 23Ω.

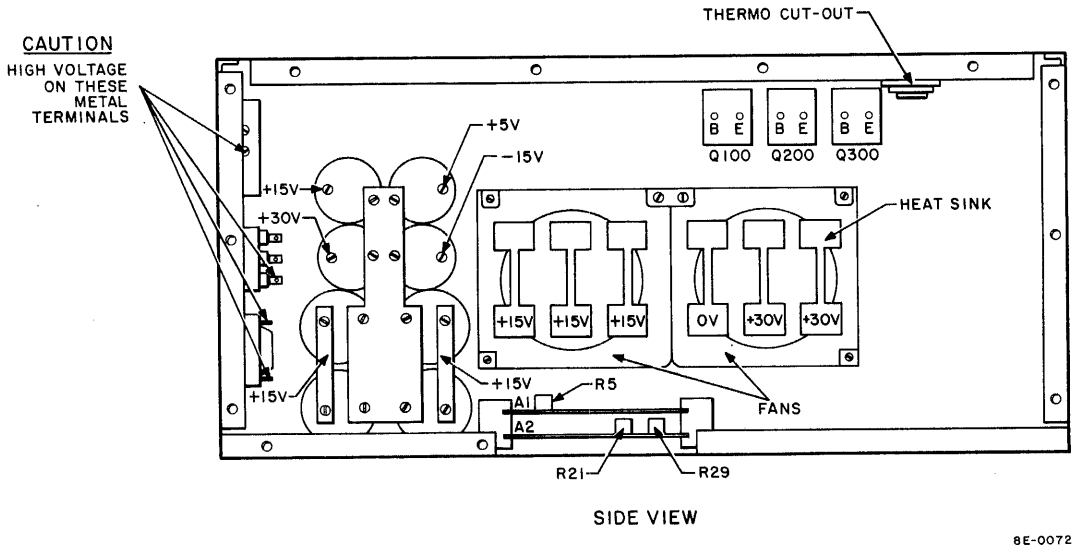


Figure 4-7 H724 Power Supply

4.8.1 Overcurrent Protection

The power supply should not be loaded by more than 175 percent of the rated output current (Table 4-7).

4.8.2 Hold-Up Time

The regulated output voltages under maximum load conditions should remain stable for a minimum of 2 ms after loss of line voltage.

4.8.3 Thermal Protection

A thermal switch is in series with the interlock circuit. This switch is located in the forward top section of the power supply (Figure 4-6). It will disconnect primary power at 90°C ±5°. The thermal switch must be reset manually if it is tripped.

4.8.4 Contact Protection

Contact protection is provided to limit the primary power at the input to the convenience outlet to twice the nominal peak voltage. In addition, protection is provided against a rate of change in the voltage exceeding 10V/second as the solenoid or circuit breaker is opened.

4.8.5 Input Switching

The primary power is switched by a 24 Vdc relay, controlled by an interlock circuit. Grounding pin A on the interlock panel will operate the solenoid and apply power to the computer. The solenoid will break both sides of the line.

4.8.6 Power ON-OFF Switch Adjustment

The Power ON-OFF switch is cam-adjusted according to Table 4-9.

Table 4-9
Power ON-OFF Switch Adjustment

Power Switch Position	Three Cam-Operated Switches Switch Position	
	Back 2 Switches	Front Switch
OFF	ON	OFF
ON	ON	ON
Panel Lock	OFF	ON

4.8.7 Parallel Operation

Two or more power supplies must not be wired in parallel to extend the current driving capability.

4.8.8 Large Configuration

When more than one box is in the sytem, the interlock panel is wired so that the front panel power switch of the first box and the thermal cut-out switch of each additional box are in series and will control power to all boxes, though they may be connected to independent primary power sources.

4.9 H740 POWER SUPPLY TROUBLESHOOTING PROCEDURES

4.9.1 Troubleshooting Rules and Precautions

Observe the following rules and precautions when maintaining the power supply.

1 Do not adjust voltages beyond their 105 percent rating; adjust slowly to avoid overvoltage crowbar that blows dc output fuses.

2 Use a calibrated voltmeter, preferably a digital voltmeter. Voltages should be adjusted to their center values: +15.0, +5.0, and - 15.0, all under load at the dc cable termination.

3 Ensure that power is turned off and unplugged before servicing the power supply.

4 Ensure that input capacitors C1 and C2 are discharged before servicing the power supply. A 10Ω to 100Ω, 10W resistor can be used to hasten the discharge of the capacitors. (Ensure power is off.)

5 The dc regulator module is not internally grounded to the chassis. Therefore, shorts to ground can be located after disconnecting the dc output cable.

6 The dc output fuses, F1 and F2, can be replaced without removing the dc regulator module. Before unsoldering fuses, observe cautions described in 3 and 4.

7 For proper operation, all hardware must be secured tightly to about 12 inch pounds (i.e., capacitors, chokes, semiconductors). All hardware should be replaced with identical hardware replacement parts.

8 The dc regulator module can be removed from the top of the power chassis assembly while the latter is still bolted to the computer chassis. The dc regulator module is held in place by six screws.

9 When replacing power semiconductor components that are secured to the heat sink, apply a thin coat of Wakefield #128 compound or Dow silicone grease to heat sink contact side (bottom) of the semiconductor. Insulating wafers are not required.

4.9.2 Troubleshooting Chart

The most likely source of a power supply malfunction is the dc regulator. A quick remedy for a malfunction is to replace this entire module. The problem, however, could be a short in the system unit or possibly a defective component or other problem in the ac input circuit. Table 4-10 applies to the regulator module and helps to isolate problems in this area.

Table 4-10
Regulator Module Troubleshooting Chart

Problem	Cause
No +5V and +15V output	F1 opened D14 or transformer opened +5V adjusted too high (1)
+5V output too low	Q5, D9, Q10, Q9, Q11, D12, or D10 shorted C5 or C7 shorted R49, R50, R46, or R44 opened
	Q6, Q7, Q8, or D11 shorted A9, Q10, or D9 opened (1)
	R51 or R50 opened
+15V output too high	Q1 shorted D8 opened R35 or R36 opened
+15V output too low	Q3, Q4, Q5, or D8 shorted R56, R35, or R34 opened C19 shorted
-15V output too low	F2 opened D14 or transformer opened Q25, D4, Q26, Q21, Q27, D7 or D5 shorted C14 or C12 shorted R22, R26, R25, or R29 opened
	Q22, Q23, Q24, or D6 shorted Q25, Q26, or D4 opened R26 or R27 opened (1) -15V adjusted too high (1)
AC LO L will not go high	Q13, Q14, or Q15 shorted Q16 or D3 opened R7, R3, R6, or R8 opened C9 shorted
AC LO L will not go low and/or acts erratically on power-on/power-off	Q13, Q14, or Q16 opened Q15 or D3 shorted R12, R13, R7, or R10 opened

SECTION 4 - TELETYPE MAINTENANCE

This section contains information pertinent to the maintenance of the TTY and associated control logic. Perform the test routines described in Paragraph 4.2 to localize trouble in the Teletype.

4.10 SPECIAL TOOLS

Table 4-11 lists the special tools needed to maintain the 33 ASR Teletype. All of these items can be obtained from Digital Equipment Corporation or from Teletype Corporation.

4.11 PROGRAMS

The Teletype control test referenced in Table 2-4 serves as an aid in maintaining the 33 ASR Teletype and associated control logic.

Table 4-11
Teletype Maintenance Tools

Item	Part No.
Set of gauges	117781
Offset screwdriver	94644
Offset screwdriver	94645
Handwheel	161430
Handwheel adapter	181465
Contact adjustment tool	172060
Gauge	180587
Gauge	180588
Gauge	183103
Bending Tool	180993
Extractor	182697
Tweezer	151392
Spring hook (push)	142555
Spring hook (pull)	142554
Screw holder	151384

SECTION 5 - PREVENTIVE MAINTENANCE PROCEDURES

4.12 PREVENTIVE MAINTENANCE

Teletype preventive maintenance should be scheduled every 3 months.

CAUTION

Do not use alcohol, mineral spirits, or other solvents to clean plastic parts with protective decorative finishes. Normally, a soft, dry cloth should be used to remove dust, oil, grease, or otherwise clean parts or subassemblies.

To clean plastic surfaces, we recommend using any of several household cleaner-waxer liquids. To clean the printer platen, we recommend a lacquer thinner.

During an overhaul, subassemblies and metal parts can be cleaned in a bath of trichlorethylene. Proper lubrication should be performed often.

4.12.1 Weekly Tasks

The following procedures should be followed on a weekly basis.

1 Inspect platen and paper guides. Wipe clean, using a soft, dry cloth.

2 Clean external areas of paper-tape punch and reader, using a soft brush or cloth.

3 Remove and empty the paper-tape punch chad box.

4 Run the Teletype control test for approximately 15 minutes.

4.12.2 Preventive Maintenance Tasks

Follow the procedure outlined below.

1 Inspect platen and paper guides. Clean platen, using a lacquer thinner to remove shiny surface.

2 Clean ribbon guides and replace ribbon, if necessary.

3 Remove cover and check for vibration effects, loose nuts, screws, retaining clips, etc.

4 Clear distributor rotor and clean disk surface, using cotton swab moistened in freon or trichlorethylene.

5 Clean between selector magnet-pole piece and armature with bond paper to remove any lubricant or dirt.

6 Clean and lubricate the Teletype, per Teletype Bulletin 273B. Follow instructions literally; do **not** over lubricate.

7 The following adjustments should be checked. Pages indicated are in Bulletin 273B, Volume 2.

Trip Shaft	574-122-700 Page 13
Trip Lever	574-122-700 Page 14
Brush Holder (Distributor)	574-122-700 Page 15
Clutches	574-122-700 Pages 16-24
Code Bar Reset	574-122-700 Pages 30-34
Print Suppression	574-122-700 Page 35
Blocking Levers	574-122-700 Page 37
Print Suppression	574-122-700 Page 43
Carriage Drive Bail	574-122-700 Page 44
Print Trip Lever	574-122-700 Pages 61-62
Dashpot	574-122-700 Page 78
Final Printing Alignment	574-122-700 Page 85
Line Feed	574-122-700 Pages 89-95
Keyboard Trip Lever	574-122-700 Page 141
Reader Trip Lever	574-124-700 Pages 6-9
Detent Lever	574-124-700 Page 10
Sensing Pin	574-124-700 Page 15
Tape Lid Latch Handle	574-124-700 Page 18
Feed Pawl	574-125-700 Page 11
Registration	574-125-700 Page 12

8 Run each of the Teletype MAINDEC Programs; at least two passes each.

9 Check that tape holes are being punched cleanly.

4.13 CORRECTIVE MAINTENANCE PROCEDURES

Details of the cable connector fusing and test points are included in Tables 4-12 and 4-13. During off-line operation, the keyboard distributor effectively drives the printer selector magnet; thus, any character received from the keyboard or paper-tape reader is automatically reproduced on the printer and paper-tape punch. During on-line operation, this continuity is broken and a Teletype receiver (M8650) is used to accept the input from the reader or keyboard while a Teletype transmitter (M8650) is used to drive the printer and paper-tape punch.

Table 4-12
Connections of TTY Cable

33 ASR Connections	W076D Split Lug	Mate-N-Lok Pin No.	M8650 Split Lug	Keyboard	Printer	Reader Advance
		1 (N/C)	0 (N/C)			
T.B. Pin #6	6	2	2		X	
T.B. Pin #3	3	3	3	X		
*-15	-Relay	4	4			X
T.B. Pin #7	7	5	5		X	
*To CP (F)	+Relay	6	6			X
T.B. Pin #4	4	7	7	X		
	-30V (N/C)	8 (N/C)	0 (N/C)			

*Wheelock Relay Card

Table 4-13
TTY Cabling, Fusing and Test Points

Check	Reader	Receiver	Transmitter
Fuses	1/2A		3, 3/8, 2.5, 3A
Terminal No.	6 and 4	7 and 3	5 and 2
Test Points	DA1 Reader Run	AB1 Receiver Active '1'	

A crystal clock is used to shift the bits through the transmitter and receiver buffers; therefore, no clock adjustments are required. Most Teletype problems can be traced to one of three areas:

a. 33 ASR keyboard or reader
b. 33 ASR printer or punch
c. M8650 receiver/transmitter

Isolation of bit-related problems is relatively simple. Off-line duplication can usually determine whether the problem is in the teleprinter or the control logic. Steps may be taken to isolate the problem to subassemblies within the teleprinter. Picking up bits during a read operation can be caused by a defect in any of three sets of contacts that are tied in parallel. Reader, keyboard, and answer-back contacts provide parallel inputs to the distributor contact disk. Bit pick-up problems can be isolated to one of these three areas by disengaging the related contact from the suspected contact set.

Printer/punch problems can sometimes be isolated by comparing the printed character with the output of the paper-tape punch. If the printed character agrees with the punch output, and both are incorrect, then the problem lies in the selector mechanism or in the TTY receiver/transmitter module (M8650). If the printed character and the paper-tape punch output disagree, and the paper-tape punch output is correct, then the problem lies within the printer assembly. Figure 4-8 shows the Teletype signal relationship between the computer and the Teletype.

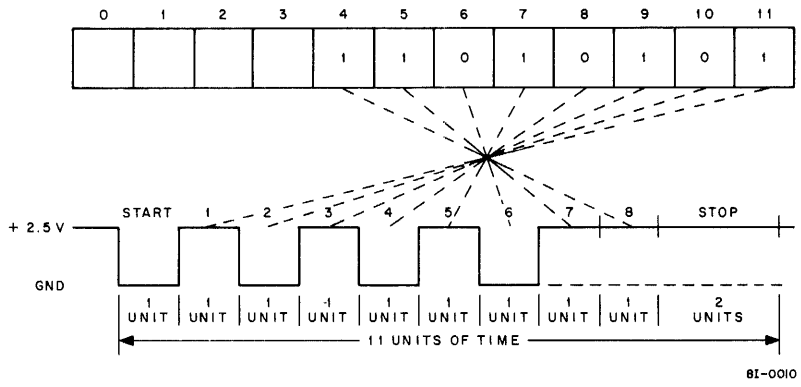


Figure 4-8 Teletype Signal Waveform
and Bit Relationship for the Character "U"

SECTION 7 - I/O CABLE TROUBLESHOOTING

4.14 I/O AND BREAK CABLES

Pin assignments for the positive I/O adapter module and break are provided in Figure 9-20 of the *PDP-8/E & PDP-8/M Small Computer Handbook*. The figure provides a source and destination in the event that cable troubleshooting is necessary.

4.15 TEST CLOCK (M499)

The test clock module serves as a troubleshooting tool for the PDP-8/E when problems with memory prevent the use of troubleshooting programs. The M499 module provides a MEM START signal of 100–500 ns width every 15 μs with the DEP or EXAM key depressed. This procedure makes signals available for associated troubleshooting at a continuous rate. Troubleshooting procedures using the M499 Test Clock are as follows:

1 Insert M499 into any slot in row A of PDP-8/E OMNIBUS.

2 Depress the SING STEP key on the Programmer's Console.

3 The Switch Register may now be used in conjunction with the EXAM or DEP key to scope manual functions.

4 The EXAM or DEP key may be taped into the depressed position (thus leaving the operator free).

SECTION 9 - PREPARATION FOR RESHIPMENT

4.16 RESHIPMENT

If the computer must be moved to a location far removed from the original installation, good packaging procedures should be followed. If the original packing materials have been retained, the instructions given below will ensure that the computer is transported safely.

1 Disconnect the computer and remove it from its enclosure.

2 If the computer is a PDP-8/F or PDP-8/M, remove the chassis tracks and ship them separately; remove the filter from the side of the computer. If the computer is a PDP-8/E table-top model, remove the air filter from both sides of the super cover and ship them with cables, software, manuals, etc.

3 Roll the power cord and tape it to the rear of the computer.

4 Place the computer in a polyethylene bag and seal the bag with tape.

5 Use the original packing materials to pack computer and accessories snugly in an inner carton.

6 Seal the inner carton, place the inner carton in an outer carton, and seal the outer carton.

CHAPTER 5
SPARE PARTS

5.1 INTRODUCTION

This chapter lists the recommended spares for the PDP-8/E, PDP-8/F, and PDP-8/M basic computers and for the 33 ASR Teletype. Two levels of spares are recommended, viz., "Remove and Replace at the Module Level" and "Remove and Replace at the Component Level".

5.2 PDP-8/E SPARES

5.2.1 PDP-8/E First-Level Spares

First-level spares for the PDP-8/E basic computer, which are included in spare parts option kit SP8-EA, are listed in Table 5-1. Table 5-2 lists those parts that are not recommended as spares. Additional spares may be purchased separately.

Table 5-1
PDP-8/E Recommended First-Level Spares

Part No.	Description	Quantity
M8300	Major Registers Module	1
M8310	Major Register Control Module	1
M8330	Timing Generator Module	1
G104	Sense Inhibit Module	1
G227	X/Y Drive Module	1
1205941	Slide Switch	2
1205375	Slide Switch, Momentary	2
125849-13	Switch Handle, Terra Cotta	2
125849-12	Switch Handle, Amber	2
1209219	Indicator Bulb	6
7006994	Key Switch Assembly	1
5409264	Power Supply Control Module A1	1
5409262	Power Supply Control Module A2	1

Table 5-2
Not Recommended as Spare Parts for PDP-8/E

Part No.	Description
M8320	Timing Loads
H220	Memory Stack
M8650	Teletype Control
54-9057	Programmer's Console (includes printed circuit board, switches, indicators, etc.)
H724	Power Supply
BE8-E	OMNIBUS Expander

5.2.2 PDP-8/E Second-Level Spares

Second-level spares for the PDP-8/E basic computer, which are included in spare parts option kit SP8-EB, are listed in Table 5-3.

Table 5-3
PDP-8/E Recommended Second-Level Spares

DEC Part No.	Description	Quantity
12-05317	Switch	2
12-09219	Lamp	6
12-05375	Switch	1
12-05941	Switch	2
12-10043	Switch Rotary	1
12-05849-12	Switch Handle	2
12-05849-13	Handle	2
13-02871	Resistor 1.21K 1/8W	2
13-04833	Resistor 1.96K 1/8W	2
13-04868	Resistor 2.74K 1/8W	2
13-05128	Resistor 5.62K 1/8W	2
13-05252	Resistor 68.1K 1/8W	2
13-10032	Resistor 16.9Ω 6W 1%	2
13-02941	Resistor 14.7K 1/8W	2
13-03156	Resistor 34.8K 1/8W	2
13-01420	Resistor 27Ω 1/4W	2
13-00317	Resistor 470Ω 1/4W	2
13-00439	Resistor 3.3K 1/4W	2
13-00229	Resistor 100Ω 1/4W	2
15-09649	Transistor 2N3762	3
15-100150	Transistor DEC 4008	4
15-05321	Transistor DEC 2007	3
15-09632	Transistor DEC 2007	4
15-09854	Transistor 8251	2
10-03053	Capacitor 0.47 MFD	2

Table 5-3 (Cont)
PDP-8/E Recommended Second-Level Spares

DEC Part No.	Description	Quantity
10-00004	Capacitor 0.02 MFD	2
10-00016	Capacitor 100 pF	2
10-09678	Capacitor 0.047 MFD	2
10-05306	Capacitor 6.8 MFD	2
19-09004	IC DEC 7402	2
19-09686	IC DEC 7404	2
19-09930	IC DEC 7405	1
19-09955	IC DEC 7412	1
19-09928	IC DEC 7416	2
19-09929	IC DEC 7417	1
19-09056	IC DEC 74H00	1
19-09931	IC DEC 74H04	1
19-09057	IC DEC 74H10	1
19-09267	IC DEC 74H11	1
19-05586	IC DEC 74H40	2
19-05547	IC DEC 7474	3
19-09667	IC DEC 74H74	1
19-09594	IC DEC 8251	2
19-09932	IC DEC 7483	1
19-09927	IC DEC 74H87	1
19-010011	IC DEC 7486	1
19-09055	IC DEC 7495	2
19-09971	IC DEC 6380A	3
19-09972	IC DEC 6314A	1
19-09973	IC DEC 97401	5
19-09936	IC DEC 74151	2
19-09937	IC DEC 74153	1
19-09935	IC DEC 8235	1
19-09934	IC DEC 8266	2
19-09373	DEC ML-9601	1
19-09867	DEC ML-4007	1
19-05521	DEC ML-1540	2
16-09996	Transformer 6501	1
16-09651	Transformer 8010	2
16-09478	Transformer 17Z5	2
18-09880-01	Crystal 14.418 MHz	1
18-09880	Crystal 19.661 MHz	1
12-10089	Berg Socket	2
12-10090	Berg Housing	2
13-02955	Resistor 750Ω 1/8W	2
13-02956	Resistor 196Ω 1/8W	2
13-04855	Resistor 9.09K 1/8W	2

Table 5-3 (Cont)
PDP-8/E Recommended Second-Level Spares

DEC Part No.	Description	Quantity
91-07722		2
12-10073	Terminal	2
12-10072	Connector Socket	2
FSA 2501	Diode Pack	4
13-10071	Thermistor	2
BC08J	BC08J	1
12-09340	AMP Pin Housing (Mate-N-Lok)	1
12-09379-01	Pin Connector Terminal	1
12-09340-01	AMP Socket Housing	1
12-09378-01	Socket Connector Terminal	1
12-9350-6	AMP Socket Housing	1
12-9351-6	AMP Pin Housing	1
12-9378-1	Pin Connector Terminal	1
12-9379-1	Socket Connector Terminal	1

5.2.3 H724 Power Supply Recommended Spare Components

Recommended spares for the H724 Power Supply are listed in Table 5-4.

Table 5-4
H724 Power Supply Recommended Spare Parts

DEC Part No.	Description	Quantity
11-10181-0	CR500 Thyractor 6RS05P5B5	1
11-05314	CR400 IN645	1
11-09979	CR200 IN1185A	1
11-10006	CR300 IN1201A	1
11-09977	VR7 IN749A	1
11-00114	CR1,2,3 IN914 or 644	4
12-09403	Fan (Super)	1
13-10170	Thermistor	1
13-09143-8	R29 Pot. 2K, 3/4W, 10%	1
13-09143-6	R5, 21 Pot. 500, 3/4W, 10%	1
15-09338	Q2-7, 13, 14 MPS6531 or 2N1613	1
15-10151	Q1, 10 RCA 40372	2
15-03409	Q8, 9, 12, 15 MPS6534 or 2N3133	2
15-5819	Q100, 200, -206, 300 2N3055 (to-41 Case)	2
12-10198-0	Relay K1	1

Table 5-4 (Cont)
H724 Power Supply Recommended Spare Parts

DEC Part No.	Description			Quantity
11-10182-0	CR100 IN4721			2
11-10183-0	Q207 SCR			1
54-09262	A1 Control Module			1
54-09264	A2 Control Module			1
12-10199-0	Thermal Relay			1
19-09981	VR1, 5 VA 723C			1
90-07208	0.5A	250V	AGC 1/2	2
90-083890-0	0.125	250V	AGC 1/8	2
90-08390-0	10A	250V	ABC 10	2
90-08388-0	1.5A	250V	AGC 1-1/2	2
90-08387-0	2.5A	250V	AGC 2-1/2	2
90-08386-0	25A	125V	ABC 25	2

5.3 PDP-8/F AND PDP-8/M SPARES

5.3.1 PDP-8/F First-Level Spares

First-level spares for the PDP-8/F basic computer, which are included in spare parts option kit SP8-FA, are listed in Table 5-5.

Table 5-5
PDP-8/F Recommended First-Level Spares

DEC Part No.	Description	Quantity
M8300	Major Registers Module	1
M8310	Registers Control Module	1
M8330	Timing Module	1
G104	Sense/Inhibit Module	1
G227	X/Y Drive Module	1
11-10625	Light Emitting Diode	2
12-10626	Slide Switch	2
12-05375	Slide Switch, Momentary	2
12-5849-12	Handle, Amber	2
12-5849-13	Handle, Terra Cotta	2
54-09728	Regulator Board Assembly	1

5.3.2 PDP-8/M First-Level Spares

First-level spares for the PDP-8/M basic computer, which are included in spare parts option kit SP8-MA, are listed in Table 5-6.

Table 5-6
PDP-8/M Recommended First-Level Spares

DEC Part No.	Description	Quantity
M8300	Major Registers Module	1
M8310	Registers Control Module	1
M8330	Timing Module	1
G104	Sense/Inhibit Module	1
G227	X/Y Drive Module	1
11-10625	Light Emitting Diode	2
12-10626	Slide Switch	2
12-05375	Slide Switch, Momentary	2
12-05849-06	Handle, Russett Orange	2
12-05849-13	Handle, Terra Cotta	2
54-09728	Regulator Board Assembly	1

5.3.3 PDP-8/F and PDP-8/M Second-Level Spares

Second-level spares for the PDP-8/F and PDP-8/M basic computers, which are included in spare parts option kits SP8-FB and SP8-MB, respectively, are listed in Table 5-7.

Table 5-7
PDP-8/F and PDP-8/M Recommended Second-Level Spares

DEC Part No.	Description	Quantity
10-00004	Capacitor, 0.02 MFD	2
10-00016	Capacitor, 100 pF	2
10-03053	Capacitor, 0.47 MFD	2
10-05306	Capacitor, 06.8 MFD	2
10-09678	Capacitor, 0.047 MFD	2
11-10324	Solid State Lamp	1
11-10714	12A Diode Bridge NSS3514	1
12-09355	Switch, Micro	1
12-05033	Fan, Boxer	1
12-10043	Switch, Miniature Rotary	1
12-10073	Connector, 40 Terminal	2
12-10627	Rotary Switch	1
12-10790	Switch, DPSTN.O.	1
12-10824	Thermostat	1
12-10830-5	Circuit breaker, 5 AMP	1
12-10830-7	Circuit Breaker, 7 AMP	1
13-00229	Resistor 100Ω 1/4W	2
13-00317	Resistor 470Ω 1/4W	2
13-00439	Resistor 3.3K 1/4W	2
13-01420	Resistor 27Ω 1/4W	2

Table 5-7 (Cont)
PDP-8/F and PDP-8/M Recommended Second-Level Spares

DEC Part No.	Description	Quantity
13-02871	Resistor 1.21K 1/8W	2
13-02941	Resistor 14.7K 1/8W	2
13-02955	Resistor 750Ω 1/8W	2
13-02956	Resistor 196Ω 1/8W	2
13-03156	Resistor 34.8K 1/8W	2
13-04833	Resistor 1.96K 1/8W	2
13-04855	Resistor 9.09K 1/8W	2
13-04868	Resistor 2.74K 1/8W	2
13-05128	Resistor 5.62K 1/8W	2
13-05252	Resistor 68.1K 1/8W	2
13-05872	Resistor	2
13-10032	Resistor 16.9Ω 6W	2
13-10071	Resistor	2
13-10709	Resistor	2
15-03409-01	MPS6534B or 2N3133	2
15-05321	2N4258	3
15-09338	MPS6531 or 2N1613	1
15-09632	DEC 2007	4
15-09649	2N3762	3
19-09594	DEC 8251	2
15-10015	DEC 4008	4
15-10151	RCA 40372 (2N3054)	2
15-10196	2N5302	2
15-10706	GPS–A55 or MPS–A55	2
15-10765	TRIACMAC 11-3	2
16-09478	Transformer 1725	2
16-09651	Transformer 8010	2
16-09996	Transformer 6501	1
18-09880	Crystal, 19.661 MHz	1
18-09880-01	Crystal 14.418 MHz	1
19-05521	IC DEC 1540	2
19-05547	IC DEC 7474	3
19-05586	IC DEC 74H40	2
19-09004	IC DEC 7402	2
19-09055	IC DEC 7495	2
19-09056	IC DEC 74H00	1
19-09057	IC DEC 74H10	1
19-09267	IC DEC 74H11	1
19-09373	IC DEC ML-9601	1
19-09594	IC DEC 82513-930	2
19-09667	IC DEC 74H74	1
19-09686	IC DEC 7404	2
19-09705	IC DEC 8881	1
19-09867	IC DEC 4007	1
19-09927	IC DEC 74H87	1
19-09928	IC DEC 7416	2
19-09929	IC DEC 7417	1

Table 5-7 (Cont)
PDP-8/F and PDP-8/M Recommended Second-Level Spares

DEC Part No.	Description	Quantity
19-09930	IC DEC 7405	1
19-09931	IC DEC 74H04	1
19-09932	IC DEC 7483	1
19-09934	IC DEC 8266	2
19-09935	IC DEC 8235	1
19-09936	IC DEC 74151	2
19-09937	IC DEC 74153	1
19-09955	IC DEC 7412	1
19-09971	IC DEC 6380A	3
19-09972	IC DEC 6314A	1
19-09973	IC DEC 97401	5
19-10010	IC DEC FSA2501	4
19-10011	IC DEC 7486	1
90-7221	Fuse	5
90-07226	Fuse	5
90-08389	Fuse	5

5.3.4 H740 Power Supply Recommended Spares

Recommended spares for the H740 power supply are listed in Table 5-8.

Table 5-8
H740 Power Supply Recommended Spare Parts

DEC Part No.	Description	Quantity
1510712	Transistor, MJ900	1
1510706	Transistor, GPS855	2
1510705	Transistor, GPS A05	2
1510928	Transistor, C32A X 135	1
1510708-2	Transistor, D45 H8/B	1
1510196	Transistor, 2N5302	1
1501311	Transistor, 2N1309	1
1500583	Transistor, 2N1308	1
1510765	Transistor, MAC 11-3	1
1110766	Zener Diode, IN5248B	1
1110715	Diode, 20A Fast Recovery Rectifier	1
1110714	Diode, Bridge Rectifier	1
1110925	Zener Diode, 5.1V	1
1110420	Diode, A15B	1
1105796	Diode, IN4004	1
1102421	Zener Diode, IN753A	1
1101938	Zener Diode, AZ5, 2.4V	1
1100122	Zener Diode, IN748A	1

Table 5-8 (Cont)
H740 Power Supply Recommended Spare Parts

DEC Part No.	Description	Quantity
1102802	Zener Diode, IN752A	1
1309150-05	Resistor, Variable, 100Ω, 1/2W, 20%	1
1310927	Thermistor, 100Ω, 3%	1
1610717	Choke, 100 μH, 20A, MMC 4289	1
1610849	Choke, 200 μH, 7A, MMC 4340	1
1210824	Thermostat, SPST	1
1205747	Fuse, 5A Pico	1
1210929	Fuse, 15A Pico	1

5.4 33 ASR TELETYPE SPARES

The recommended Teletype spare parts are listed in Table 5-9.

Table 5-9
Spare Parts for Keyboard-Model 33 ASR Teletype

DEC Part No.	Description	Quantity
181821	Circuit Board	1
183071	Tape Feed Sprocket	2
182240	Lever, Universal	2
90-07208	Fuse, 1/2A	1
90-07207	Fuse, 3/8A	1
90-08387-0	Fuse, 2.5A	1
120167	Fuse, 3.2A	1
180979	Distributor Brush	2
181420	Belt Driven Gear	1
181411	Drive Gear	1
181409	Belt	2
181007	Shaft	1
181002	Bearing	2

Users who do not have maintenance personnel trained in the maintenance and repair of Teletype units should keep a complete Model 33 Automatic Send Receive Teletype near the computer. If the on-line unit becomes defective, substitute the spare to avoid computer down time. Many users have facilities for the maintenance of Teletype units, in which case it is suggested that spare parts be stocked as listed in Table 5-9 and that one of each Teletype maintenance tool listed in Table 4-10 be stocked. All of these items can be obtained from Digital Equipment Corporation or from Teletype Corporation.

APPENDIX A
IC DESCRIPTIONS

A.1 DEC 7474 and 74H74 ICs

The 7474 and 74H74 ICs are dual D-type, edge-triggered flip-flops. The 74H74 has a smaller propagation delay and a higher maximum clock frequency, but can be represented by the same illustrations as the 7474. These are shown in Figure A-1.

The dc-set and dc-reset inputs are independent of the clock. A low input on either one of these lines holds the flip-flop in the specified state for as long as the low level is maintained. Data on the D-input line is transferred to the outputs on the positive-going edge of the clock pulse. If the clock is at either a high or a low level, the D-input signal has no effect.

The functional logic symbol shows the flip-flop as it normally appears in the manual. Thus, a high level at the D-input causes the flip-flop to be set (the 1 side goes high) by the positive-going edge of the clock pulse. However, many control signals in the PDP-8/E are asserted at ground, rather than at a high level; consequently, if the D input is asserted (is active) at ground, the flip-flop is reset by the clock pulse, and an active signal causes the flip-flop to go to its inactive state. To rectify this inconsistency, DEC redefines flip-flops with D inputs that are asserted at ground. The redefined 7474 flip-flop appears as shown in Figure A-2. If the D input is active (at ground), the clock pulse sets the flip-flop. Note that redefinition involves only the defining of pin numbers in a different manner. Pin 5 is redefined as the 0 side of the flip-flop, pin 6 is redefined as the 1 side, pin 4 becomes dc-reset, and pin 1 becomes dc-set.

A.2 DEC 74H87 IC

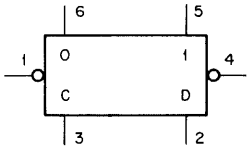
The 74H87 IC is a 4-bit true-false/0-1 element. The logic diagram, the truth table, and the pin locator are shown in Figure A-3.

If control input B is low, control input C determines if an output bit represents the true or the false state of the respective input. However, if B is high, C forces the output to be either high or low, regardless of the respective input. The 74H87 is used in major register gating, where it is designated Data Control Gate.

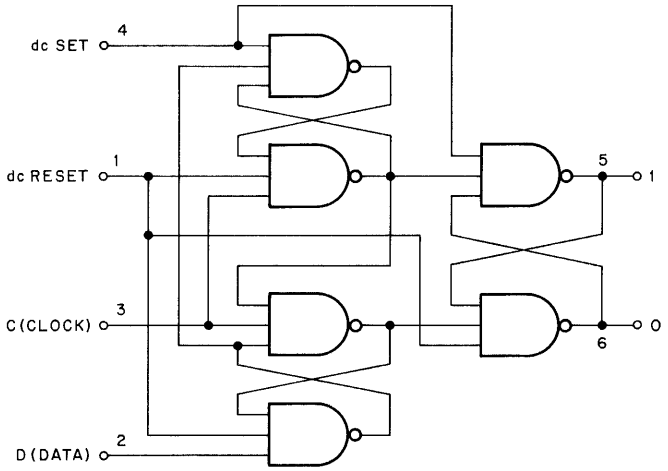
A.3 DEC 7483 IC

The 7483 IC is a 4-bit binary full-adder. The logic diagram and the pin locator are shown in Figure A-4.

The 7483 is used for parallel-add/serial-carry applications. It adds two 4-bit binary numbers (A and B) and provides a sum (S) output for each bit. The resultant carry (CARRY OUT) is taken from the last bit of each adder. This IC is used in the adder network of major register gating.



FUNCTIONAL LOGIC
SYMBOL (EACH F/F)



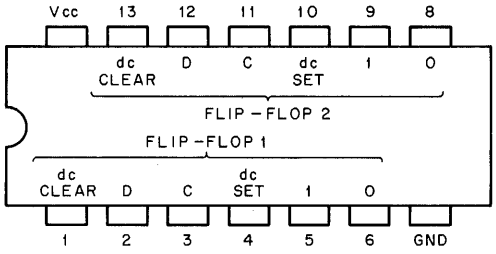
LOGIC DIAGRAM (EACH F/F)

t_n	t_{n+1}	
D - INPUT	1-OUTPUT	0-OUTPUT
LOW	LOW	HIGH
HIGH	HIGH	LOW

t_n = BIT TIME BEFORE CLOCK PULSE

t_{n+1} = BIT TIME AFTER CLOCK PULSE

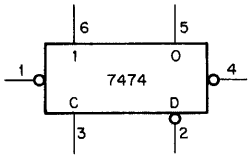
TRUTH TABLE (EACH F/F)



PIN LOCATOR
(TOP VIEW OF IC)

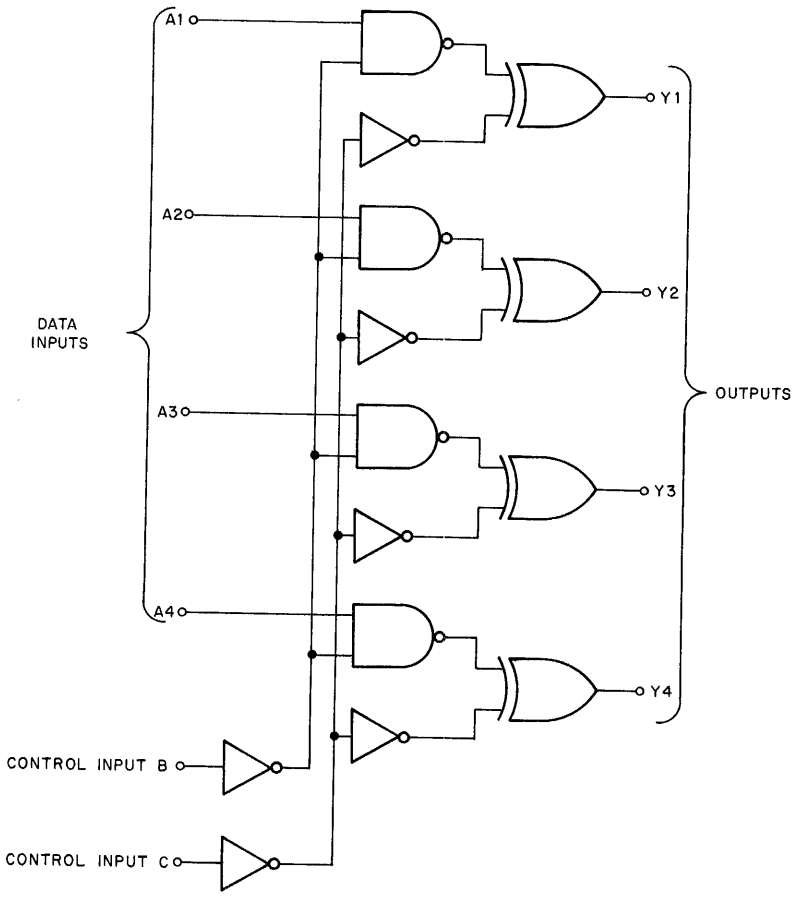
8E-0135

Figure A-1 DEC 7474 and 74H74 IC Illustrations



8E-0132

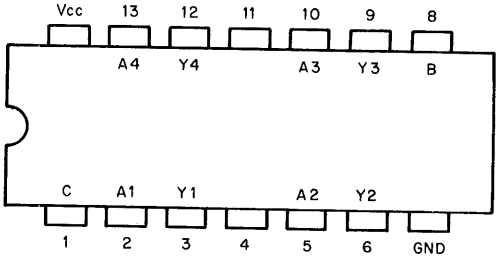
Figure A-2 DEC 7474 IC; Redefined Functional Logic Symbol



LOGIC DIAGRAM

CONTROL INPUTS		OUTPUTS			
B	C	Y1	Y2	Y3	Y4
LOW	LOW	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$
LOW	HIGH	A1	A2	A3	A4
HIGH	LOW	HIGH	HIGH	HIGH	HIGH
HIGH	HIGH	LOW	LOW	LOW	LOW

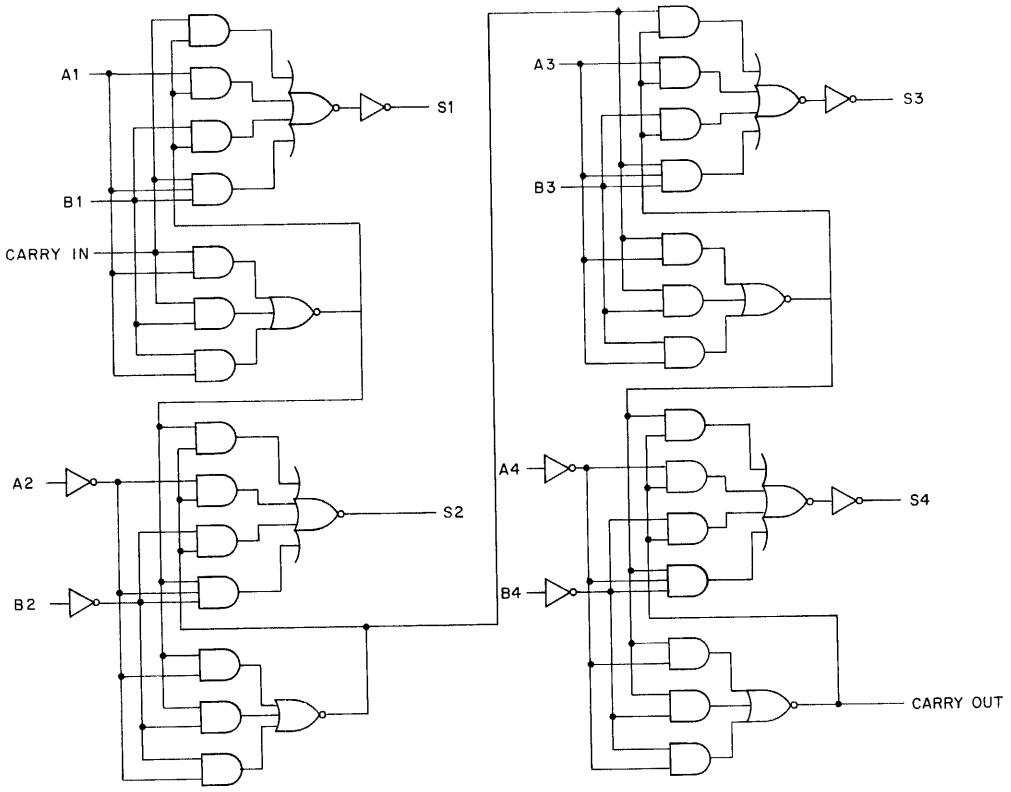
TRUTH TABLE



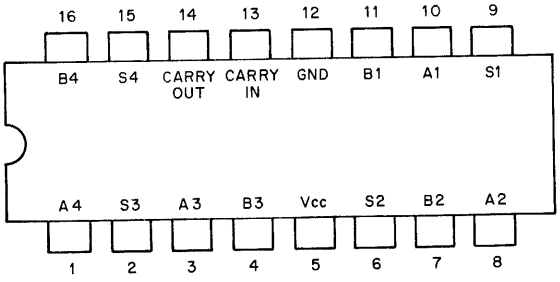
PIN LOCATOR
(TOP VIEW OF IC)

8E-0131

Figure A-3 DEC 74H87 IC Illustrations



LOGIC DIAGRAM



PIN LOCATOR
(TOP VIEW OF IC)

8E-0130

Figure A-4 DEC 7483 IC Illustrations

A.4 DEC 7495 IC

The 7495 IC is a 4-bit shift register. The logic diagram and the pin locator are shown in Figure A-5.

This IC can be used for both parallel-loading operations and shifting operations, depending on the state of the mode control (M) input. If the M-input is high, data can be placed on the parallel input lines, A1 through D1, and loaded into the R/S master-slave flip-flops by a clock pulse at the Clock 2 input. If the M-input is low, the output of each flip-flop is coupled to the R/S input of the succeeding flip-flop. Data is placed on the Serial Input line, and a clock pulse at the Clock 1 input shifts the data into the first R/S flip-flop. Each succeeding pulse does likewise, at the same time right-shifting the register. The outputs of the flip-flops, A2 through D2, are available during both shifting and parallel-loading operations. The 7495 is used in the Timing Generator, where a number of them are connected in series to form the Timing Shift Register.

A.5 DEC 8235 IC

The 8235 is a 4-bit, dual data input logic element. The logic diagram, the truth table, and the pin locator are shown in Figure A-6.

If both control inputs are low, a bit output can be either high or low, depending on the state of both A_n and B_n. If both control inputs are high, a bit output is high, regardless of the state of A_n and B_n. The two remaining possible combinations of C and D produce the output state shown by the truth table. The 8235 is used as a multiplexer in major register gating, where it is designated Data Line Multiplexer.

The output circuits of the 8235 are open-collector, enabling the 8235 to direct drive many signal lines on the OMNIBUS.

A.6 DEC 8251 IC

The 8251 IC is a BCD-to-Decimal decoder. The logic diagram, the truth table, and the pin locator are shown in Figure A-7.

As an example of the logic operation, consider the BCD representation for three: 0011. This combination of voltage levels (A and B high, C and D low) results in all output gates, with the exception of gate 3, being disqualified. The voltage at the output of gate 3 goes low, indicating a decimal 3 to the succeeding circuit.

In the truth table, 0s and 1s are used because binary numbers are generally recognized in these terms. However, it is important to remember that these 0s and 1s represent only voltage levels. A signal in the PDP-8/E can be logically true when the signal is at ground; this is usually the case. Furthermore, care should be exercised when attempting to relate the 8251 decimal outputs to the PDP-8/E basic instruction octal codes. For example, the octal code for an OPR instruction is 7XXX (we are concerned only with the three most significant bits). The 8251 IC in major register control decodes the OPR instruction and asserts decimal output 0, rather than 7. The concept detailed in this paragraph will help avoid confusion when considering this particular use of the 8251.

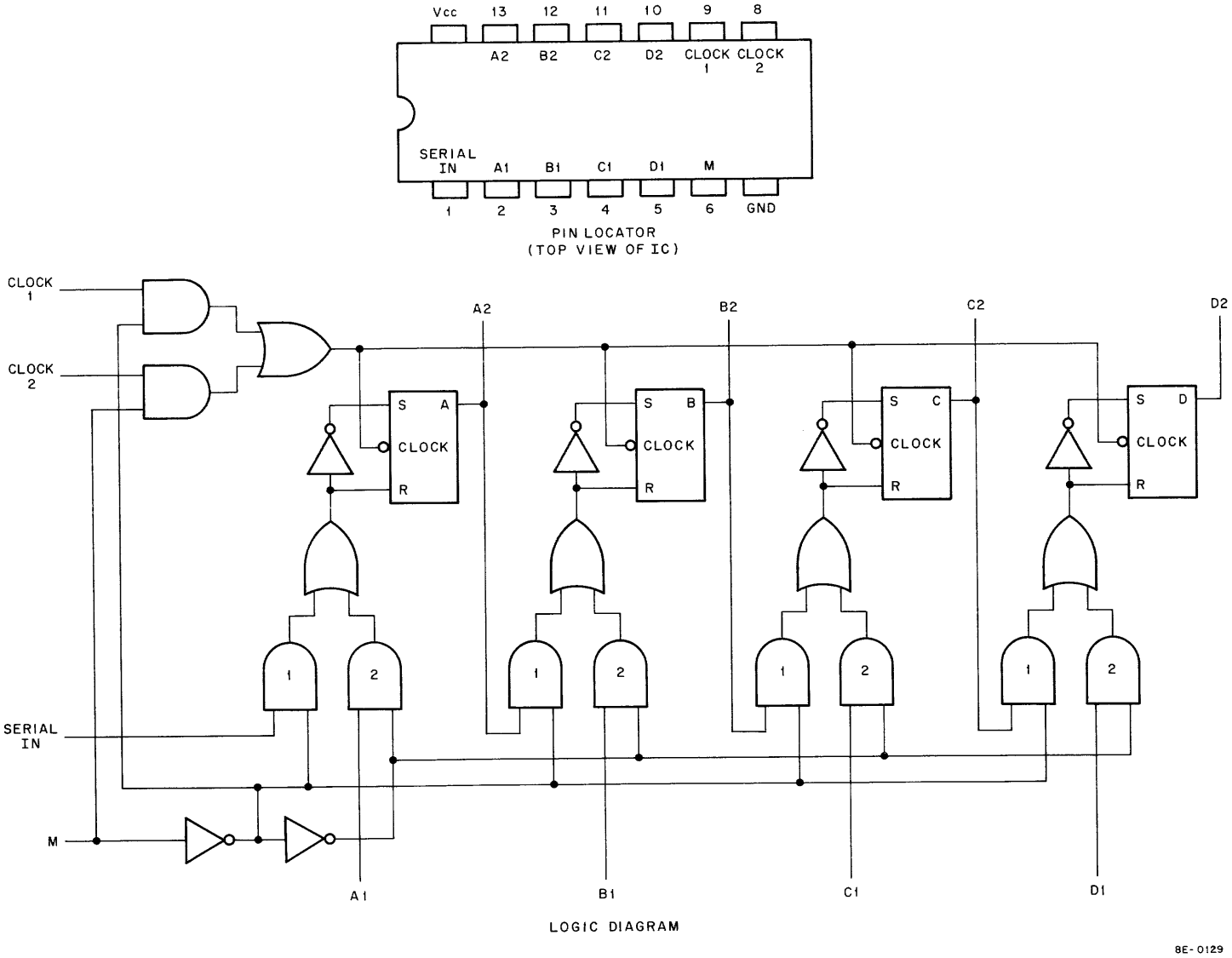
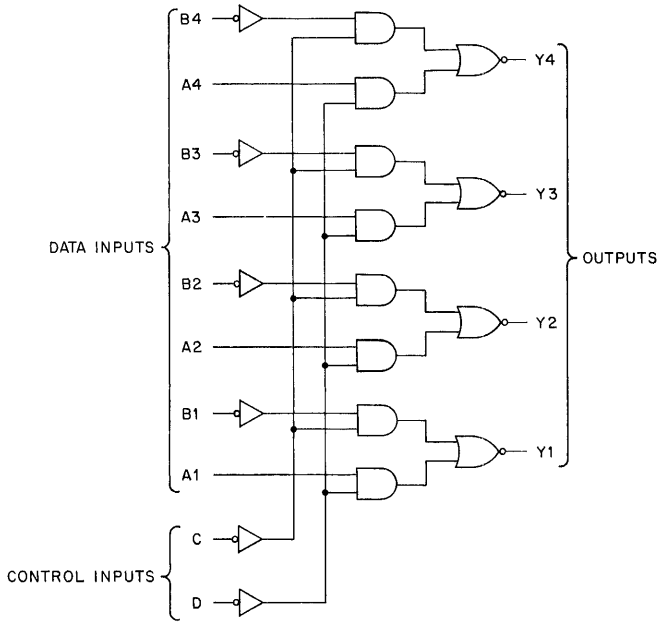


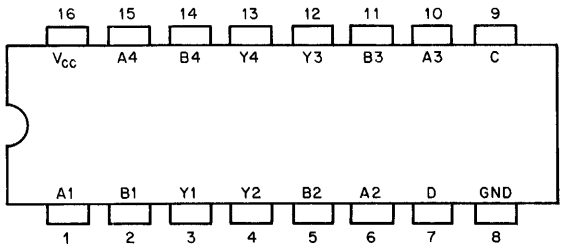
Figure A-5 DEC 7495 IC Illustrations



LOGIC DIAGRAM

CONTROL INPUT		DATA INPUT		OUTPUT
C	D	An	Bn	Yn
LOW	LOW	LOW	LOW	LOW
		LOW	HIGH	HIGH
		HIGH	LOW	LOW
		HIGH	HIGH	LOW
LOW	HIGH	–	–	Bn
HIGH	LOW	–	–	$\overline{An}$
HIGH	HIGH	–	–	HIGH

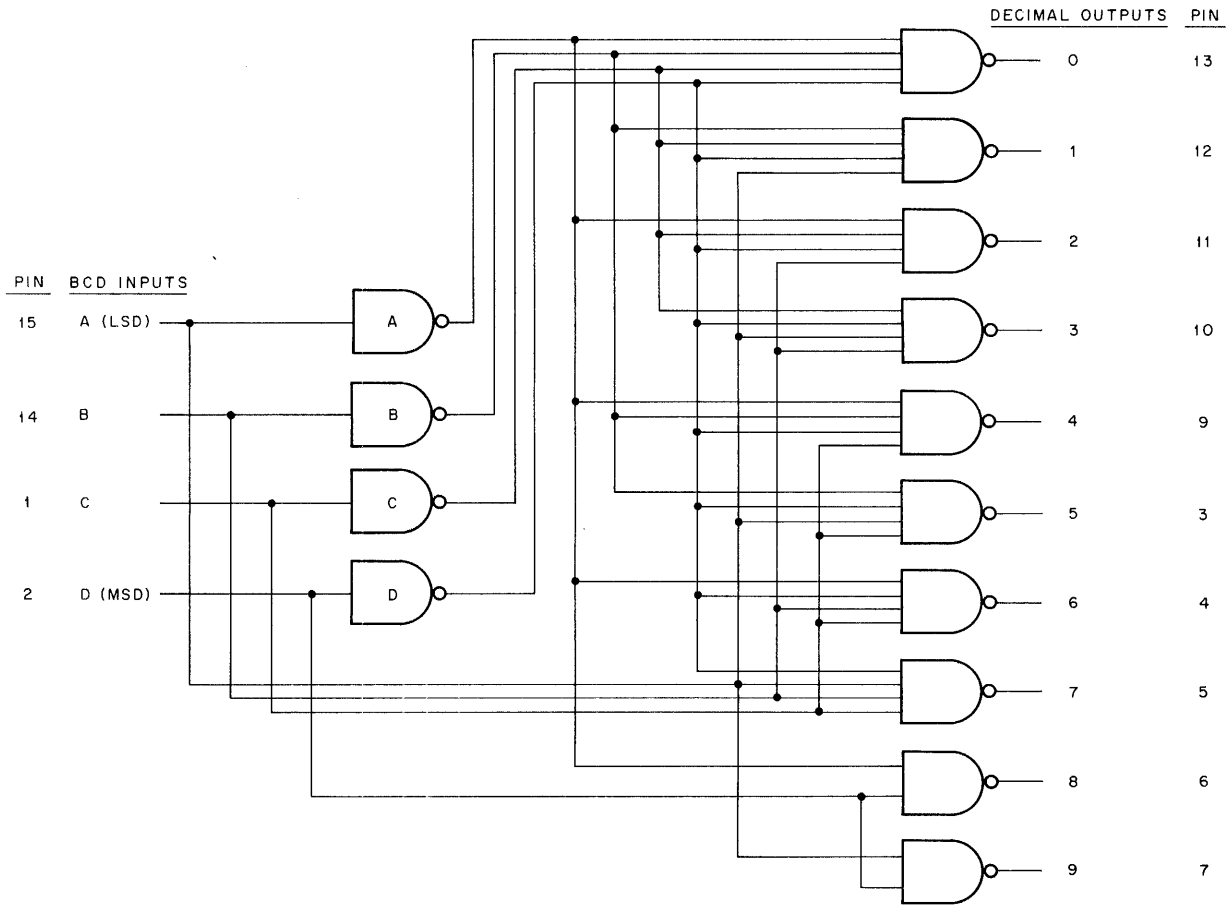
TRUTH TABLE



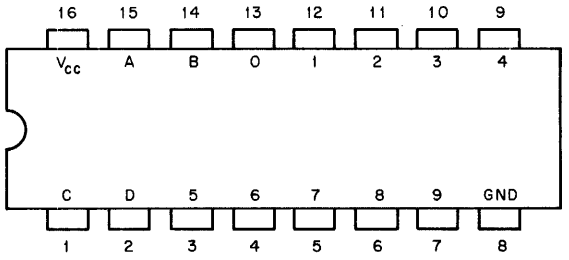
PIN LOCATOR
(TOP VIEW OF IC)

8E-0128

Figure A-6 DEC 8235 IC Illustrations



LOGIC DIAGRAM



PIN LOCATOR
(TOP VIEW OF IC)

8E-0134

Figure A-7 DEC 8251 IC Illustration

Input States					Output States									
D	C	B	A		0	1	2	3	4	5	6	7	8	9
0	0	0	0		0	1	1	1	1	1	1	1	1	1
0	0	0	1		1	0	1	1	1	1	1	1	1	1
0	0	1	0		1	1	0	1	1	1	1	1	1	1
0	0	1	1		1	1	1	0	1	1	1	1	1	1
0	1	0	0		1	1	1	1	0	1	1	1	1	1
0	1	0	1		1	1	1	1	1	0	1	1	1	1
0	1	1	0		1	1	1	1	1	1	0	1	1	1
0	1	1	1		1	1	1	1	1	1	1	0	1	1
1	Repeat above sequence	Repeat above sequence	Repeat above sequence		1	1	1	1	1	1	1	1	0	1
1					1	1	1	1	1	1	1	1	1	0
1					1	1	1	1	1	1	1	1	0	1
1					1	1	1	1	1	1	1	1	1	0
1					1	1	1	1	1	1	1	1	0	1
1					1	1	1	1	1	1	1	1	1	0
1					1	1	1	1	1	1	1	1	0	1
1					1	1	1	1	1	1	1	1	1	0
Note: 0 represents a low voltage level; 1 represents a high voltage level.														

A.7 DEC 8266 IC

The 8266 IC is a 4-bit, dual data input logic element. The logic diagram, the truth table, and the pin locator are shown in Figure A-8.

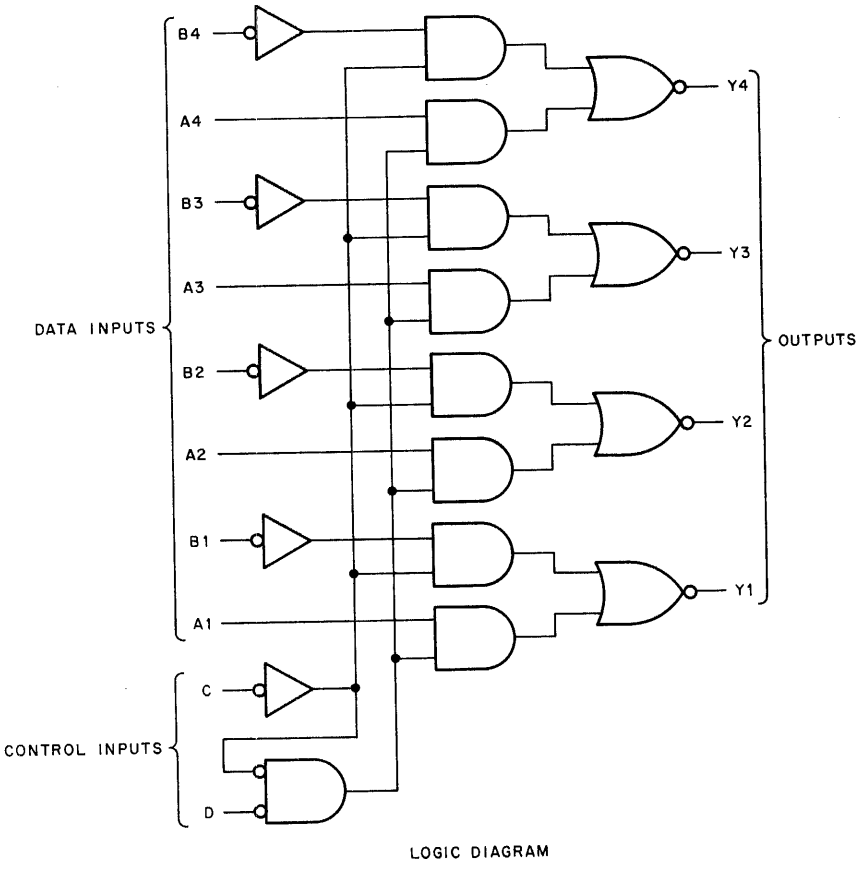
The 8266 is similar to the 8235 IC, already introduced. The major difference between the two is in the Y_n output state, when both control inputs are low. The 8266 provides an output of the same state as the B_n data input. This IC is used as a multiplexer in major register gating, where it is part of the Register Input Multiplexer.

The output circuits of the 8266 are TTC, making them unsuitable for directly driving the OMNIBUS.

A.8 DEC 8271 IC

The 8271 IC is a 4-bit shift register. The logic diagram, a function table, and the pin locator are shown in Figure A-9.

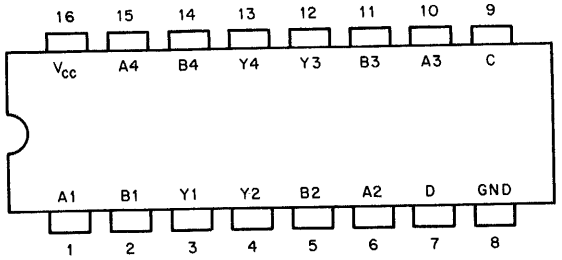
This IC can be used for either serial or parallel data entry. As the function table indicates, the SHIFT signal is high for right-shift operation. The 1 output of each flip-flop is coupled to the R_c/S_c input of the next flip-flop. Data is placed on the D_s line, and a pulse at the CLOCK input shifts the data into the first flip-flop. Each succeeding pulse does likewise, at the same time right-shifting the register. If the SHIFT line is low, the register may be either parallel loaded, or placed in the "hold" condition, depending on the state of the LOAD signal. Data to be parallel-loaded is placed on the D_n inputs and clocked into the respective flip-flop by the negative-going edge of the clock pulse. The outputs of the flip-flops are available during both shifting and parallel loading.



LOGIC DIAGRAM

CONTROL INPUT		OUTPUT
C	D	Yn
LOW	LOW	Bn
LOW	HIGH	Bn
HIGH	LOW	$\overline{An}$
HIGH	HIGH	HIGH

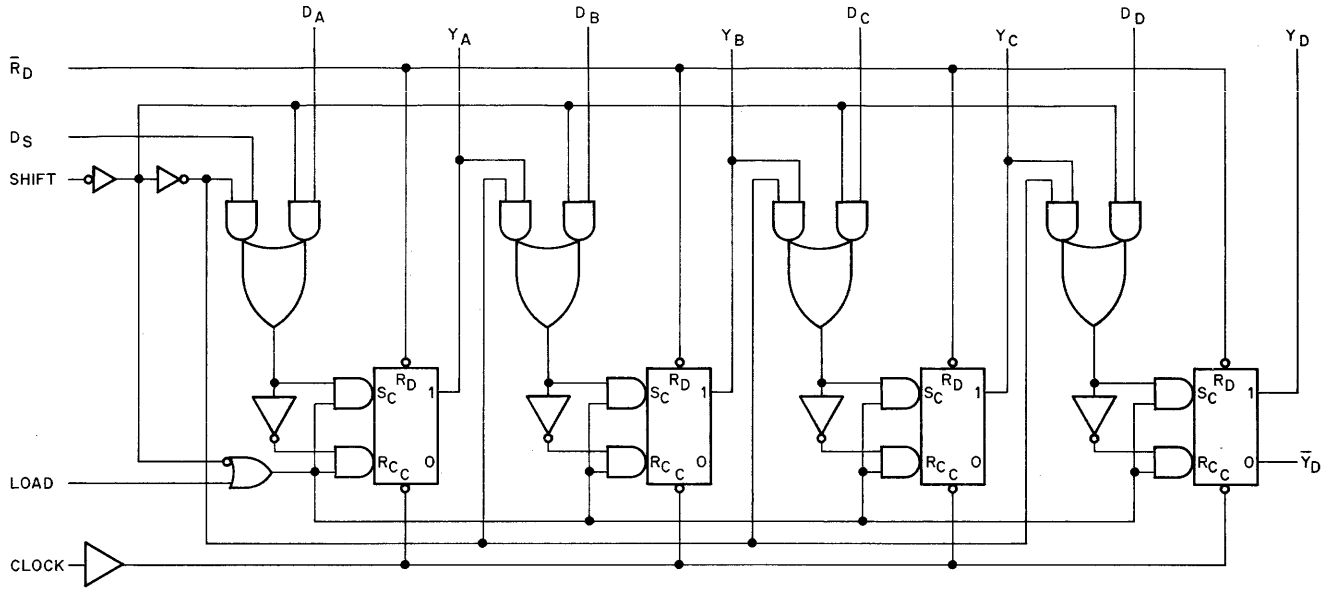
TRUTH TABLE



PIN LOCATOR
(TOP VIEW OF IC)

8E-0141

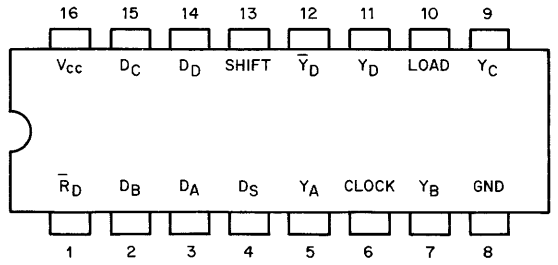
Figure A-8 DEC 8266 IC Illustrations



LOGIC DIAGRAM

CONTROL SIGNAL		REGISTER FUNCTION
LOAD	SHIFT	
LOW	LOW	HOLD
HIGH	LOW	PARALLEL LOAD
LOW	HIGH	SHIFT RIGHT
HIGH	HIGH	

FUNCTION TABLE



PIN LOCATOR

(TOP VIEW OF IC)

8E-0140

Figure A-9 DEC 8271 IC Illustrations

The PDP-8/E uses the 8271 as the component flip-flop of the major registers. In this application, only the parallel entry mode is used. Thus, the SHIFT input is grounded, and the LOAD input is connected to a positive voltage.

A.9 DEC 74151 and 74153 ICs

The 74151 and 74153 ICs are data selectors/multiplexers. The 74151 is an 8-bit element, which provides an output signal and its complement. The 74153 is a dual 4-bit element that provides a single output for each section.

The 74151 illustrations are shown in Figure A-10; the 74153 illustrations are presented in Figure A-11. These ICs are used in the PDP-8/E CPU, exclusively.

A.10 DEC 723C IC

The 723C IC is a monolithic voltage regulator, used in the PDP-8/E power supply. The device equivalent circuit and a pin locator are shown in Figure A-12.

The voltage regulator IC consists of a temperature compensated reference amplifier (this supplies a V_{ref} of 7.15V, typical), an error amplifier, a power series pass transistor, and current limit circuitry. Because of the high current requirements of the power supplies, additional pass transistors are used with this voltage regulator. The current limit and current sense capabilities of the IC are not used in the PDP-8/E application; these connections are left open.

A.11 DEC 1540G IC

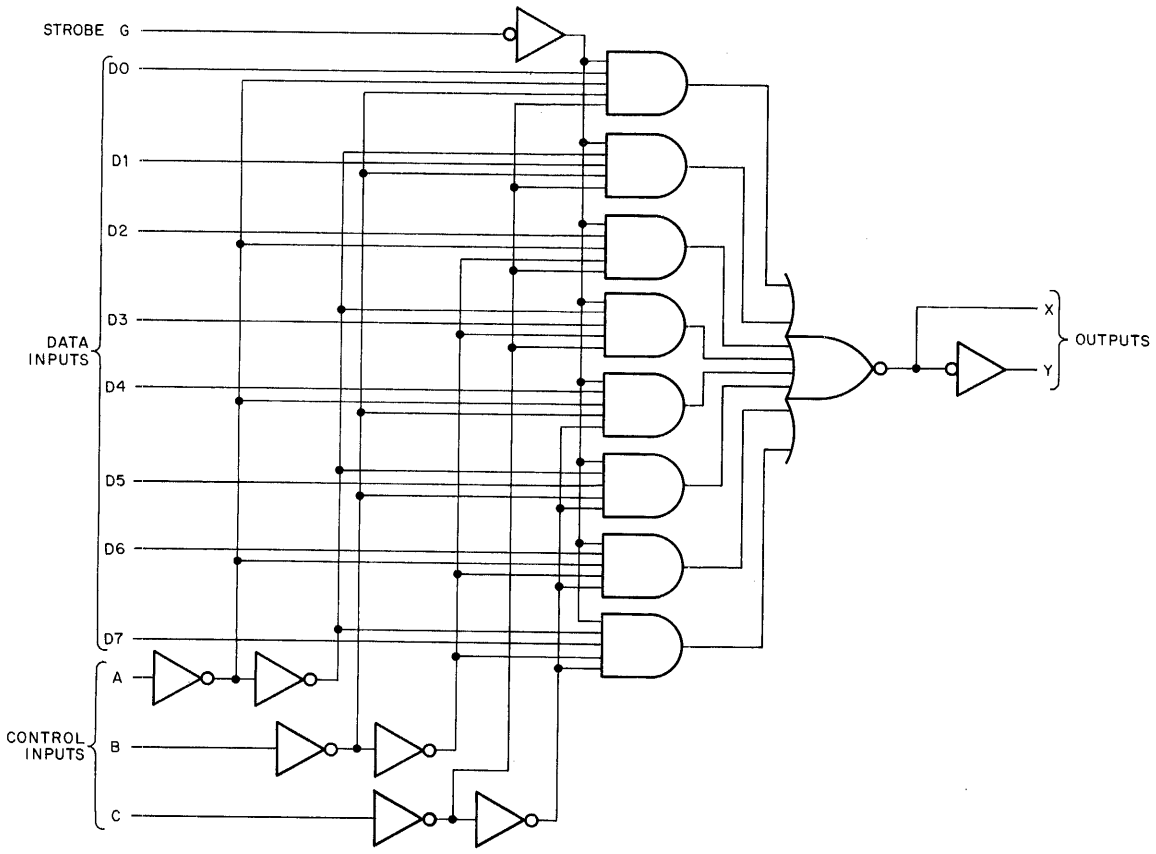
The DEC 1540G IC is a sense amplifier, slicer, and strobe gate used in the PDP-8/E memory, type MM8-E. The device block diagram and a pin locator are shown in Figure A-13.

The input differential amplifier has a typical gain of 85. The resulting output waveform (points A and A^1) is compared with the slice level, and the normally low signal at point B goes positive when the signal at point A or at A^1 is more positive than the internal slice voltage controlled by the voltage on the SLICE LEVEL pin. The slice level is strobed by a pulse applied to the TIME STROBE, and the resulting OUTPUT is used to set a flip-flop external to the IC.

A.12 DEC 7493 IC

The 7493 IC is a binary counter that can be externally wired to operate in either a 4-bit or a 3-bit mode. The logic diagram, the truth table, and the pin locator are shown in Figure A-14.

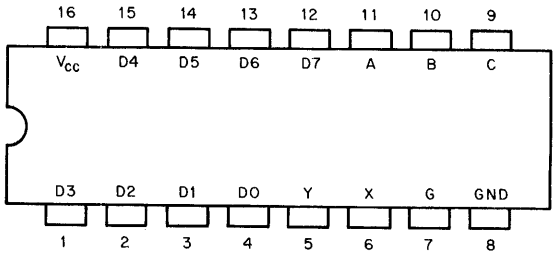
The 7493 counter consists of four J-K master-slave flip-flops. The counter can operate in the 3-bit, ripple-through mode if the operator applies clock pulses at the A2 input. The counter can operate in the 4-bit ripple-through mode if the operator connects Y1 to A2, and applies clock pulses at A1. A gated reset input is provided to inhibit the count inputs and, simultaneously, return each flip-flop to logical 0.



LOGIC DIAGRAM

CONTROL INPUTS			STROBE	OUTPUT
A	B	C	G	X
LOW	LOW	LOW	LOW	$\overline{D0}$
HIGH	LOW	LOW	LOW	$\overline{D1}$
LOW	HIGH	LOW	LOW	$\overline{D2}$
HIGH	HIGH	LOW	LOW	$\overline{D3}$
LOW	LOW	HIGH	LOW	$\overline{D4}$
HIGH	LOW	HIGH	LOW	$\overline{D5}$
LOW	HIGH	HIGH	LOW	$\overline{D6}$
HIGH	HIGH	HIGH	LOW	$\overline{D7}$
DON'T CARE			HIGH	HIGH

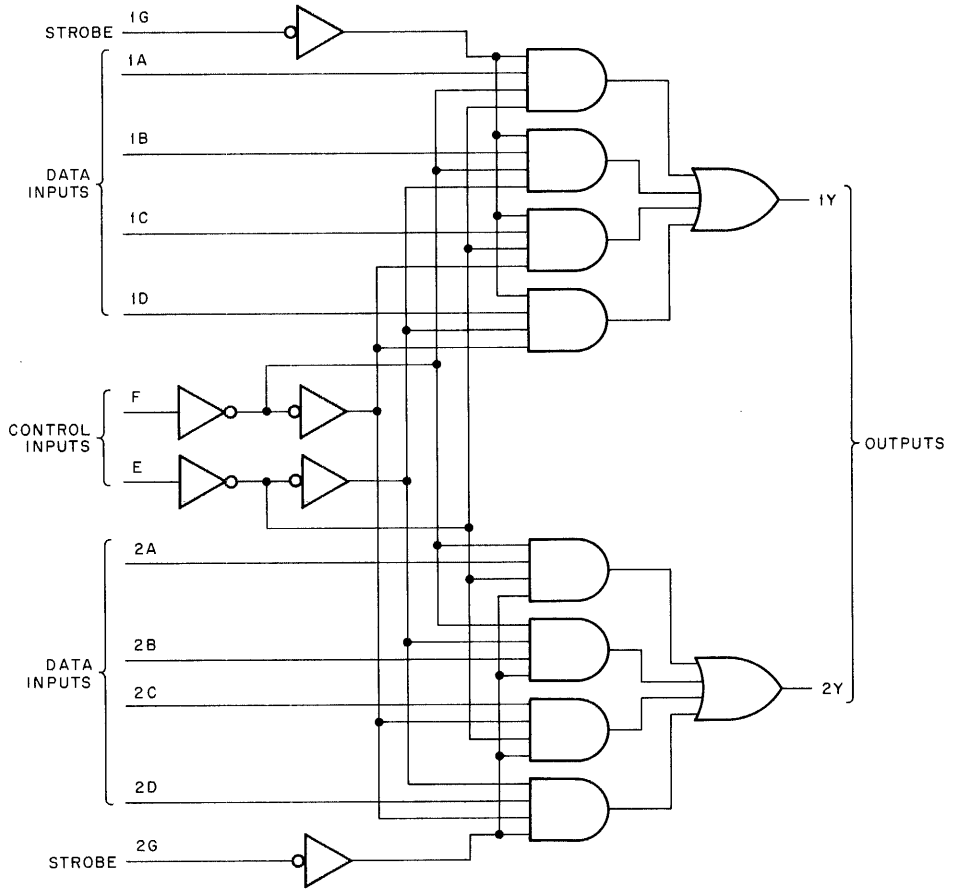
TRUTH TABLE



PIN LOCATOR
(TOP VIEW OF IC)

8E-0139

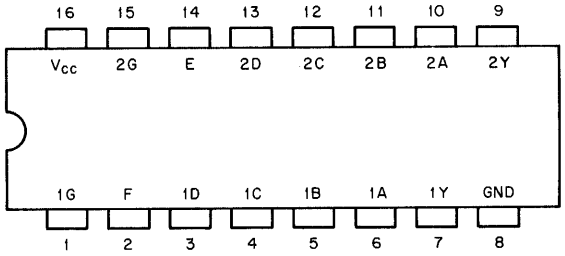
Figure A-10 DEC 74151 IC Illustrations



LOGIC DIAGRAM

CONTROL INPUT		STROBE	OUTPUT
E	F	G	Y
LOW	LOW	LOW	A
HIGH	LOW	LOW	B
LOW	HIGH	LOW	C
HIGH	HIGH	LOW	D
DON'T CARE		HIGH	LOW

TRUTH TABLE (EACH HALF)



PIN LOCATOR
(TOP VIEW OF IC)

8E-0138

Figure A-11 DEC 74153 IC Illustrations

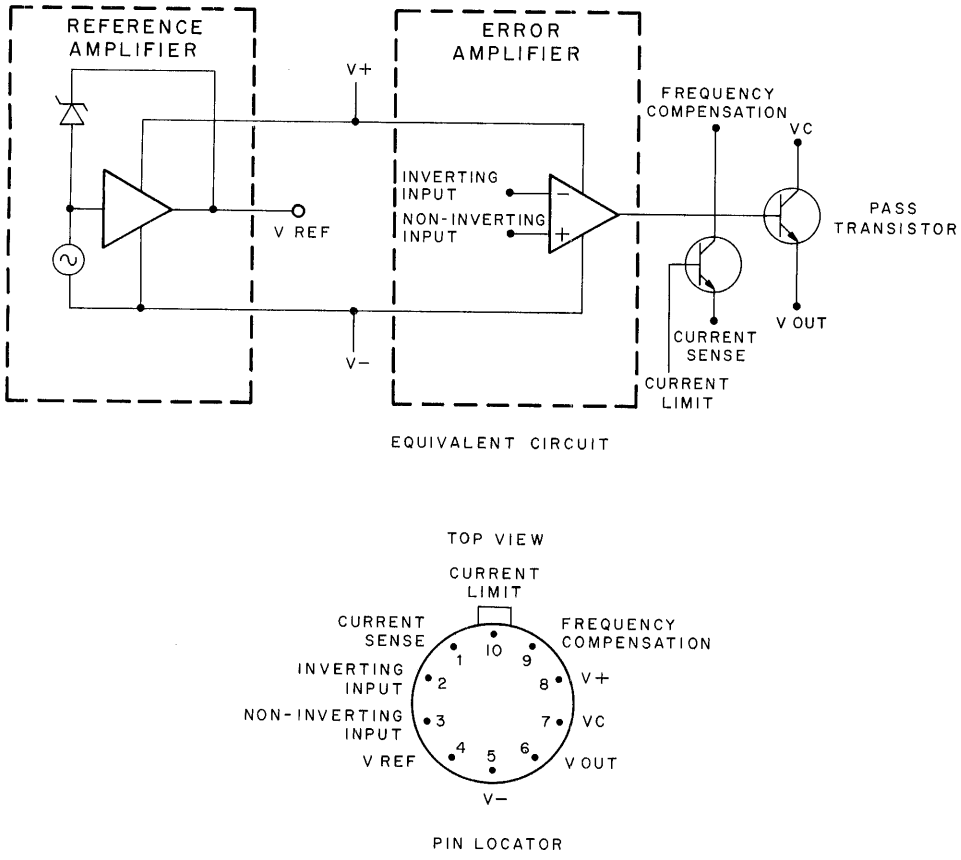


Figure A-12 DEC 723C IC Illustrations

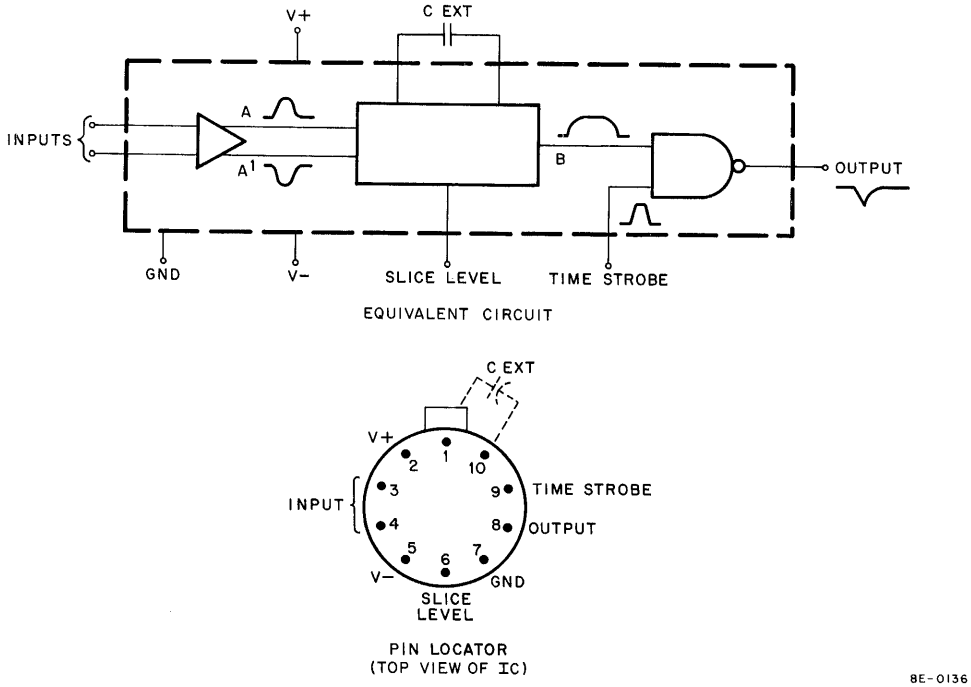


Figure A-13 DEC 1540G IC Illustrations

TOGGLE INPUT PULSE	OUTPUT			
	Y1	Y2	Y3	Y4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

*TRUTH TABLE

*Applies When 7493 Is Used As 4-Bit Ripple-Through Counter.

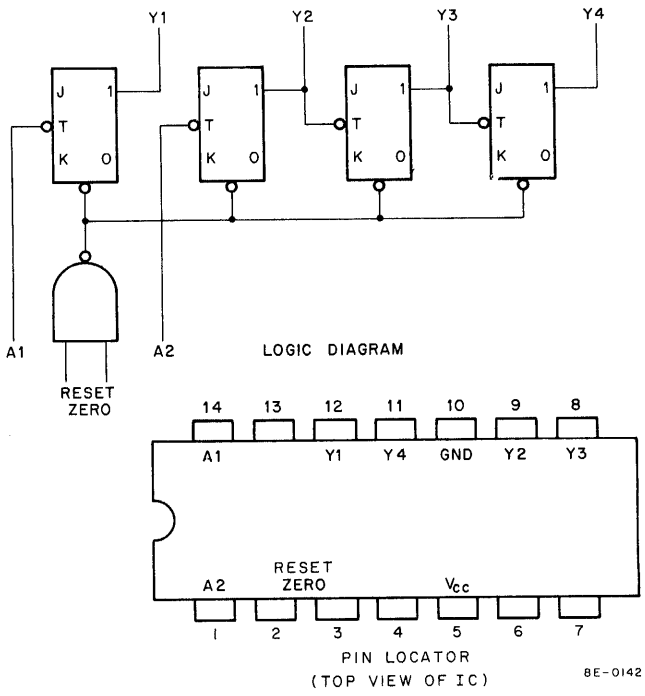


Figure A-14 DEC 7493 IC Illustrations

A.13 DEC 709C IC

The DEC 709C IC is an operational amplifier. The circuit schematic and the pin locator are shown in Figure A-15.

The IC is designed for general-purpose analog amplifier application. In the DK8-EP Programmable Real-Time Clock option, the 709C is used as a comparator and, as such, is the central component in the Schmitt trigger circuits on the M518 module. In this application only half the IC circuitry is used, the output being taken from pin 8 of the IC. As can be seen from the circuit schematic, the output at pin 8 has the same relationship to the summing inputs as does the output at pin 6.

A.14 DEC 7475 IC

The DEC 7475 IC is a 4-bit bistable latch. The logic diagrams, a truth table, and a pin locator are shown in Figure A-16.

Information present at the data input (D) of a latch is transferred to the 1 output when the clock input (C) goes high. If the C input remains high, the 1 output follows the D input. When the C input goes low the 1 output holds the state it was in prior to the transition.

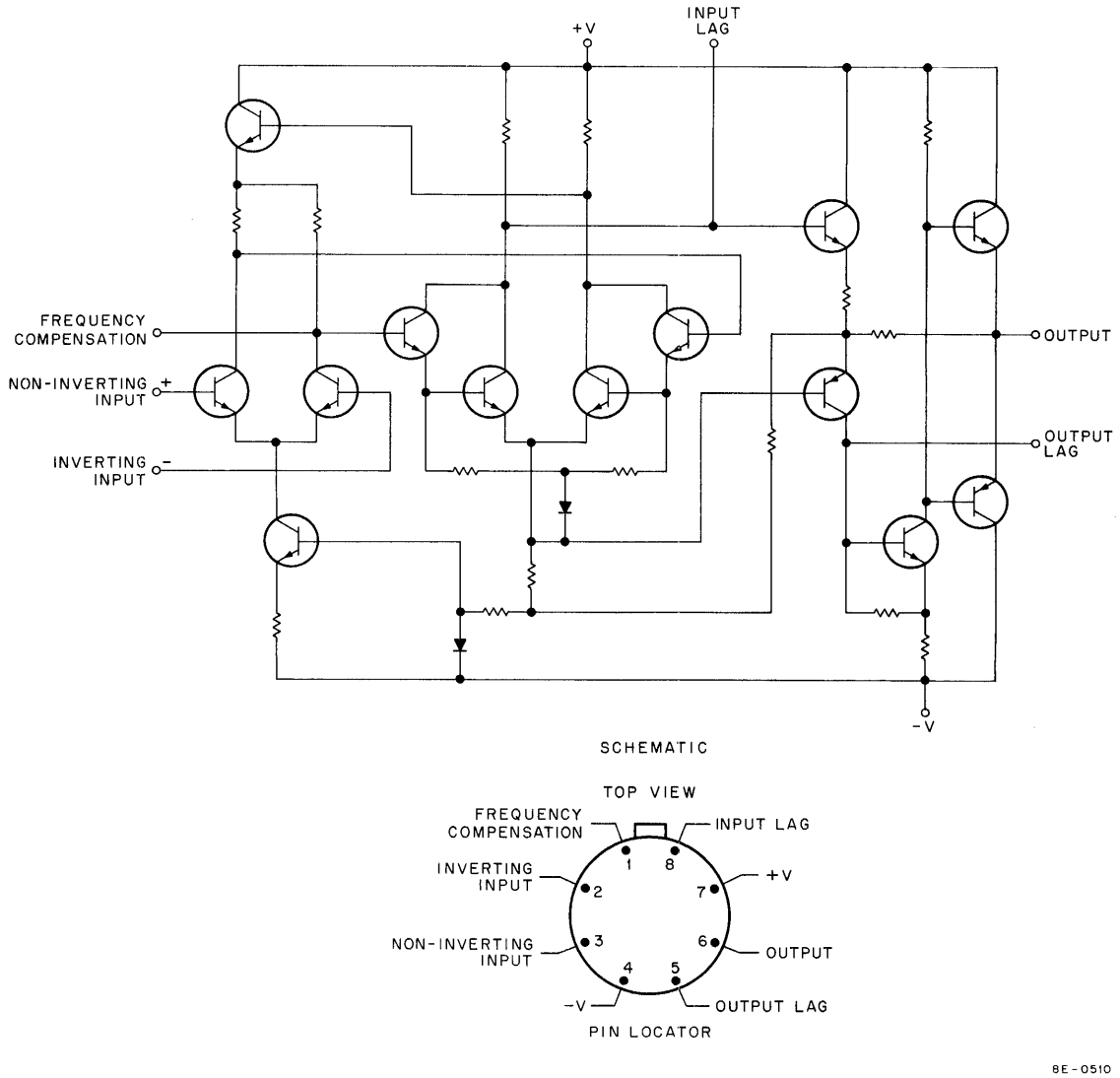


Figure A-15 DEC 709C IC Illustrations

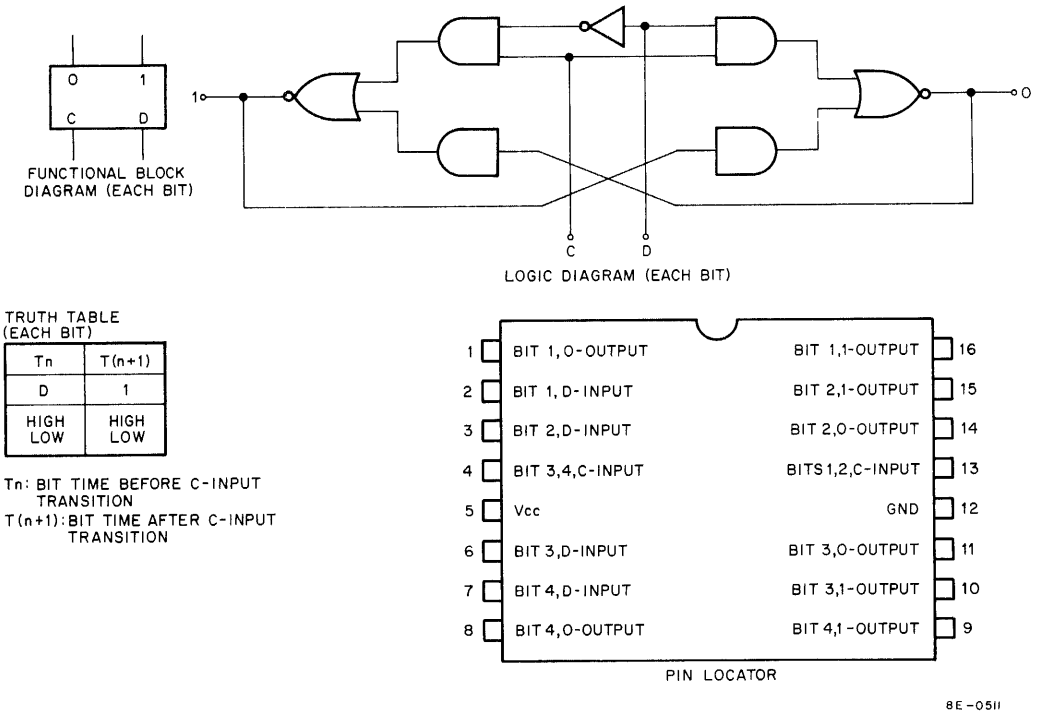


Figure A-16 DEC 7475 IC Illustrations

A.15 DEC 7490 IC

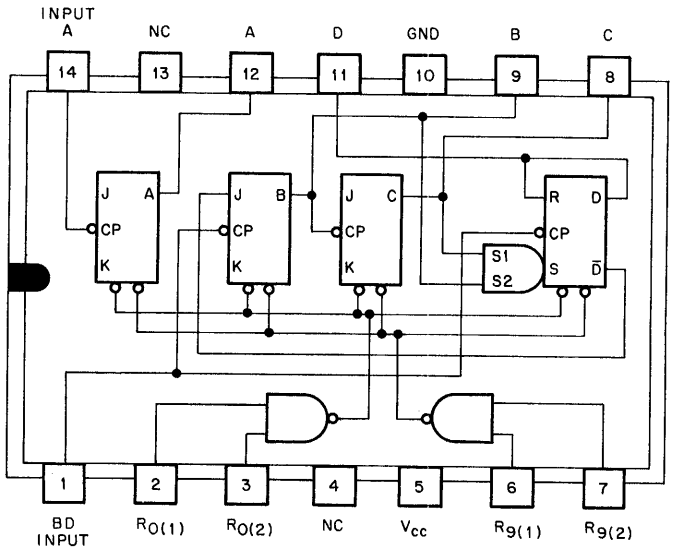
The DEC 7490 IC is a high-speed counter consisting of 4 master-slave flip-flops, connected to provide a divide-by-two counter and a divide-by-five counter. The logic diagram, truth tables, and a pin locator are shown in Figure A-17.

The 7490 can be used in three independent counting modes, namely; a divide-by-two/divide-by-five mode, a divide-by-ten mode, and a BCD count mode. No external interconnections of the IC pins are necessary in the first listed mode. An input at pin 14 is divided by two by flip-flop A and the result is taken from pin 12; an input at pin 1 is divided by five by flip-flops B, C, and D, and the result is taken from pin 11. The output of each flip-flop is made available and all four flip-flops are reset simultaneously, if the gated reset lines are used.

If the divide-by-ten mode is desired, pin 11 must be connected to pin 14. The input at pin 1 is divided by ten and the output is taken from pin 12 (this mode of operation is used in the DK8-EP Programmable Real-Time Clock option). The third listed mode is obtained by connecting pin 1 to pin 12 and applying the input at pin 14; the BCD count sequence is shown in truth table A. The reset inputs are provided to reset a BCD count for 9's complement decimal applications.

A.16 DEC 7470 IC

The DEC 7470 IC is an edge-triggered J-K flip-flop. The logic diagram, pin locator, and truth table are shown in Figure A-18.



LOGIC DIAGRAM/PIN LOCATOR

TRUTH TABLES

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

A– BCD COUNT SEQUENCE

RESET INPUTS				OUTPUT
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

B–RESET/COUNT

NOTES:
1. X in tables indicates either 1 or 0 may be present.
2. NC indicates no internal connections.

8E-0512

Figure A-17 DEC 7490 IC Illustrations

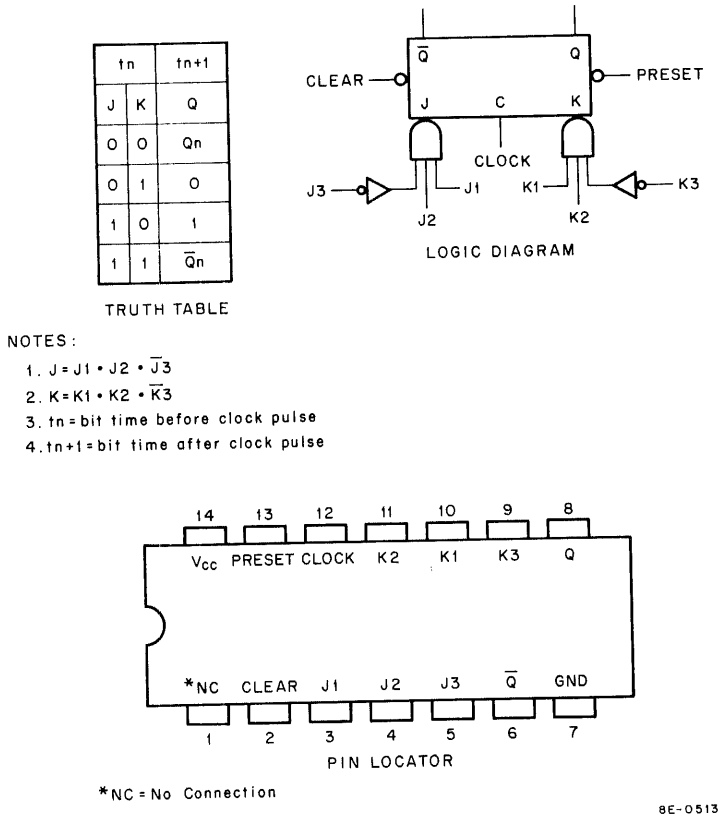


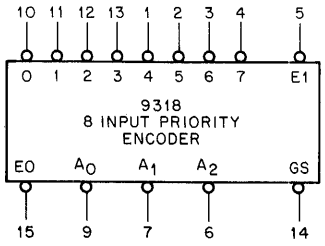
Figure A-18 DEC 7470 Illustrations

The 7470 features gated inputs and direct clear and preset inputs. Input information is transferred to the outputs on the positive edge of the clock pulse. Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; when the input threshold has been exceeded, the gated inputs are locked out. The preset and clear inputs have effect only when the clock input is low.

A.17 DEC 9318 IC

The DEC 9318 IC is an 8-input priority encoder. The functional logic diagram and a truth table are shown in Figure A-19.

The 9318 accepts data from 8 active low inputs and provides a binary representation on the 3 active low outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority. A high on the input enable (EI) will force all outputs to the inactive state and allow new data to settle without producing erroneous information at the outputs. A group signal output (GS) and an enable output (EO) are provided with the three data outputs. The GS is active level low when any input is low; this indicates when any input is active. The EO is active level low when all inputs are high. Using the output enable along with the input enable allows priority encoding of N input signals. Both EO and GS are inactive high when the input enable is high.



FUNCTIONAL LOGIC DIAGRAM

TRUTH TABLE

E1	0	1	2	3	4	5	6	7	GS	A_0	A_1	A_2	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = High Voltage level
L = Low Voltage level
X = Don't Care

8E-0514

Figure A-19 DEC 9318 IC Illustrations

A.18 DEC 74194 IC

The DEC 74194 IC is a 4-bit bidirectional shift register. The logic diagram, mode-control table, and pin locator are shown in Figure A-20.

In the parallel load mode, data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Clocking of the flip-flops is inhibited when both mode-control inputs are low. The mode control should be changed only while the clock input is high.

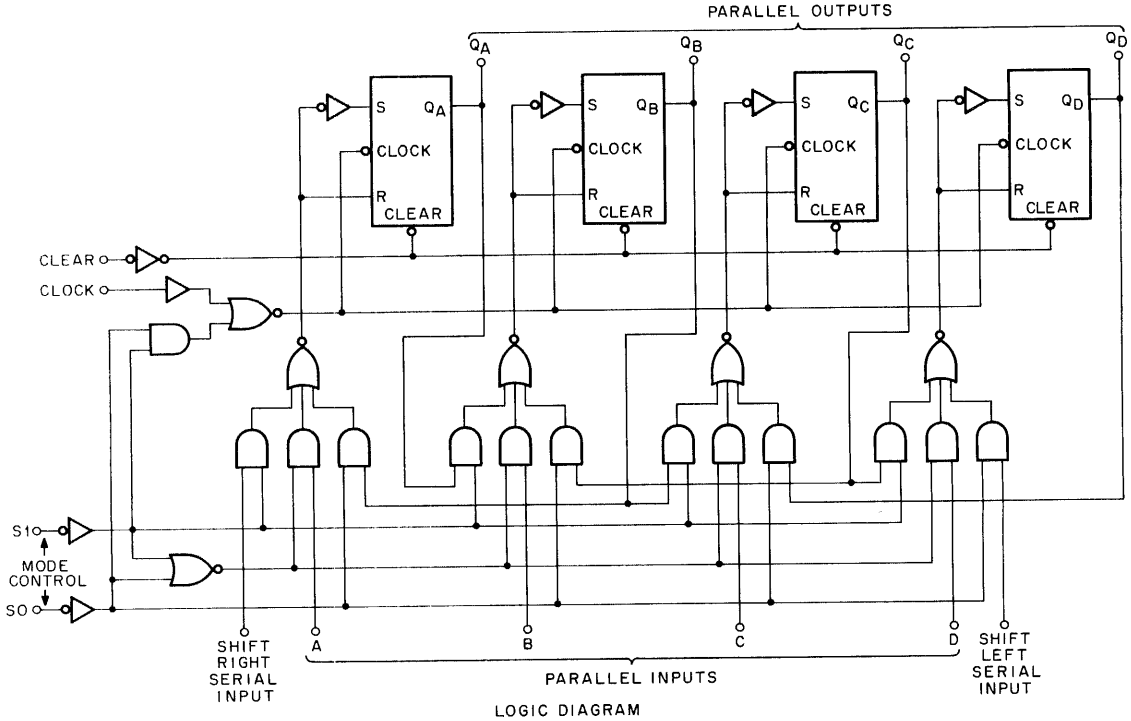
A.19 DEC 74123 IC

The DEC 74123 IC is a retriggerable monostable multivibrator (one-shot). The functional logic diagram/pin locator and a truth table are shown in Figure A-21.

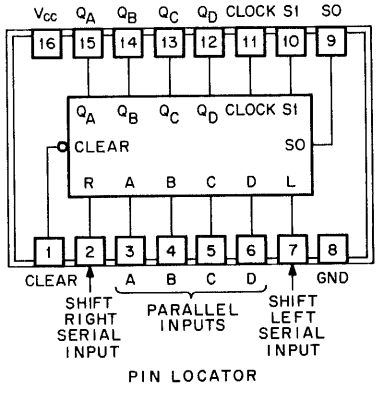
Output pulse width is a function of the external capacitor and resistor. For C_{ext} greater than 1000 pF, the output pulse width (t_w) is:

$$t_w = 0.32\ R_T\ C_{ext}\ (1 + \frac{0.7}{R_T}),$$ where R_T is in kΩ, C_{ext} is in pF, and t_w is in ns.

For pulse widths when C_{ext} is less than or equal to 1000 pF, see the plot in Figure A-22.

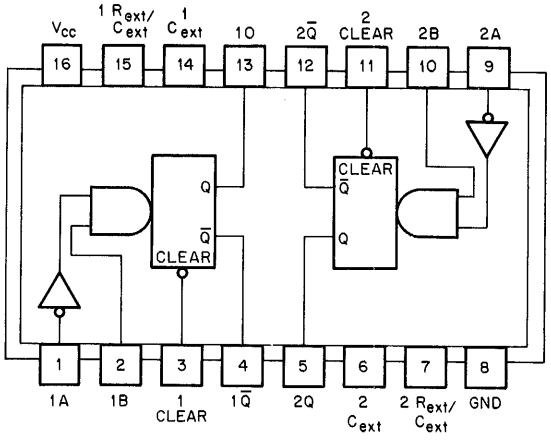


	MODE CONTROL	
	S1	SO
PARALLEL LOAD	H	H
SHIFT RIGHT (IN THE DIRECTION Q_A TOWARD Q_D)	L	H
SHIFT LEFT (IN THE DIRECTION Q_D TOWARD Q_A)	H	L
INHIBIT CLOCK (DO NOTHING)	L	L



8E-0515

Figure A-20 DEC 74194 IC Illustrations



FUNCTIONAL LOGIC / PIN LOCATOR

TRUTH TABLE

INPUTS		OUTPUTS	
A	B	Q	$\bar{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎴
↓	H	⎍	⎴

NOTE: H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎴ = one low-level pulse, X = irrelevant (any input, including transitions).

8E-0516

Figure A-21 DEC 74123 IC Illustrations

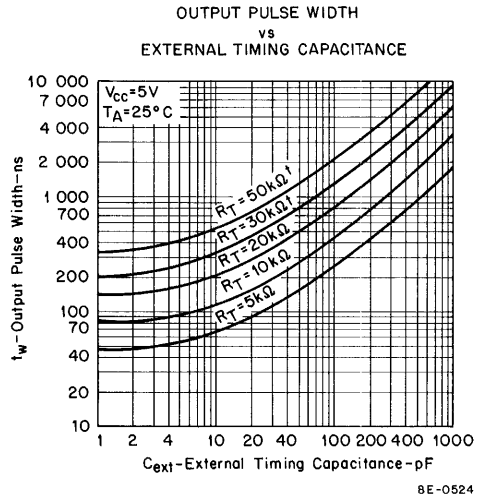


Figure A-22 DEC 74123 IC Output Pulse width vs. External Timing Capacitance

A.20 DEC 74197 IC

The DEC 74197 IC is a pre-settable binary counter that can also be used as a latch. The IC consists of four dc-coupled master-slave flip-flops connected to provide a divide-by-two counter and a divide-by-eight counter. The logic diagram is shown in Figure A-23. A truth table and a pin locator are shown in Figure A-24.

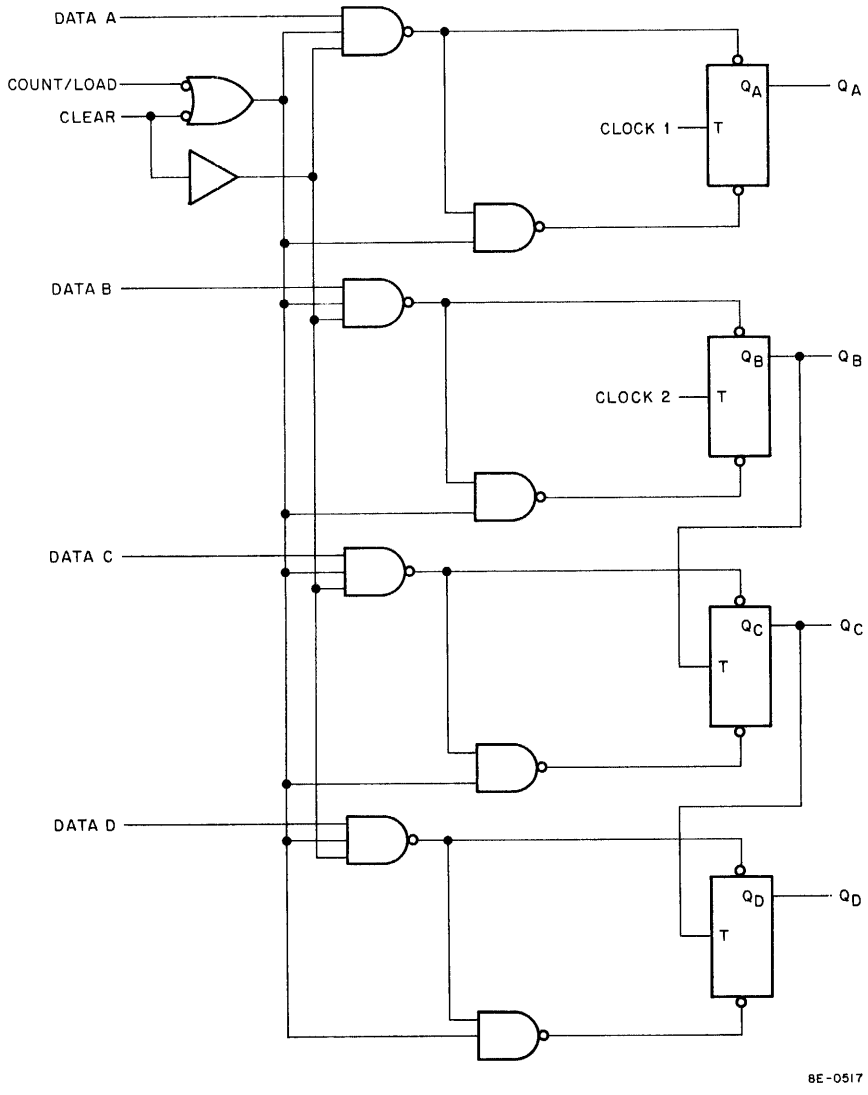


Figure A-23 DEC 74197 Logic Diagram

TRUTH TABLE

COUNT	OUTPUT			
CLOCK 1 INPUT	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Q_A connected to CLOCK 2 input.

PIN LOCATOR

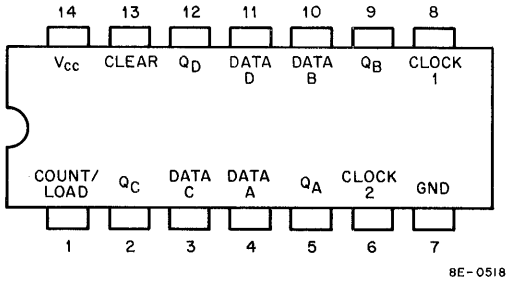


Figure A-24 DEC 74197 Truth Table and Pin Locator

The 74197 can be used in any one of three modes, viz; the divide-by-two/divide-by-eight mode, requiring no external interconnection of IC pins, the latch mode, and the binary counter mode. If the first listed mode is used, an input at pin 8 is divided by 2 by flip-flop A and the result is taken from pin 5; an input at pin 6 is divided by 8 by flip-flops B, C, and D and the result is taken from pin 12. Transfer of information to the outputs takes place on the negative-going (trailing) edge of the clock pulse.

If one wishes to use the latch mode, one must enter data at the four data inputs (pins 4, 10, 3, and 11) and enter a strobe pulse at pin 1. The output pins, 5, 9, 2, and 12, respectively, will follow the inputs when pin 1 is low, but will remain unchanged when pin 1 is high and the clock inputs are inactive.

The third mode, binary counting, is used in the DK8-EP Programmable Real-Time Clock option. Pin 5 must be externally connected to pin 6. The clock input is applied at pin 8. The initial count can be preset to any value by placing a low on pin 1 and entering the data on pins 4, 10, 3, and 11. When pin 13 is taken low, all outputs are set low, regardless of the state of the clock inputs.

APPENDIX B
OMNIBUS SIGNAL LOCATOR

Pin	Signal	Source	Destination
A1A	TP		Not bussed
A1B	TP		Not bussed
A1C	SP GND	P.S.	ALL
A1D	MA0 L	M8360 M8300	KC8-EA, M8330, M8300, G227
A1E	MA1 L	M8360 M8300	KC8-EA, M8330, M8300, G227
A1F	GND	P.S.	ALL
A1H	MA2 L	M8360 M8300	KC8-EA, M8330, M8300, G227
A1J	MA3 L	M8360 M8300	KC8-EA, M8330, M8300, G227
A1K	MD0 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8350
A1L	MD1 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8350
A1M	MD2 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8350
A1N	GND	P.S.	ALL
A1P	MD3 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8650, M835

Pin	Signal	Source	Destination
A1R	DATA0 L	KC8-EA M8350 M8300 M8360	KC8-EA, M8330, M8300, M8350, M8360
A1S	DATA1 L	KC8-EA M8350 M8300 M8360	KC8-EA, M8300, M8350, M8360
A1T	GND	P.S.	ALL
A1U	DATA2 L	KC8-EA M8350 M8300 M8360	KC8-EA, M8330, M8300, M8350, M8360
A1V	DATA3 L	KC8-EA M8350 M8300 M8360	KC8-EA, M8300, M8350, M8360
A2A	+5	P.S.	ALL
A2B	-15	P.S.	ALL
A2C	GND	P.S.	ALL
A2D	EMA0 L	M8360	KC8-EA, G104
A2E	EMA1 L	M8360	KC8-EA, G104
A2F	GND	P.S.	ALL
A2H	EMA2 L	M8360	KC8-EA, G104
A2J	MEM START L	KC8-EA	M8330
A2K	MD DIR L	M8330 KC8-EA M8360	KC8-EA, M8300, G104
A2L	SOURCE	M8330	G227
A2M	STROBE	M8330	G104
A2N	GND	P.S.	ALL

Pin	Signal	Source	Destination
A2P	INHIBIT	M8330	G104
A2R	RETURN	M8330	G104, G227
A2S	WRITE L	M8330	G104, G227
A2T	GND	P.S.	ALL
A2U	ROM ADDR L	M880	M8310, G104, M880
A2V	LINK L	M8310	M8330
B1A	TP		Not bussed
B1B	TP		Not bussed
B1C	GND	P.S.	ALL
B1D	MA4 L	M8360 M8300	KC8-EA, M8330, M8300, G227
B1E	MA5 L	M8360 M8300	KC8-EA, M8330, M8300, G227
B1F	GND	P.S.	ALL
B1H	MA6 L	M8360 M8300	KC8-EA, M8330, M8300, G227
B1J	MA7 L	M8360 M8300	KC8-EA, M8330, M8300, G227
B1K	MD4 L	G104 M8300	KC8-EA, M8330, M8310, M830, G104, M8650, M8350
B1L	MD5 L	G104 M8300	KC8-EA, M8330, M8310, M830, G104, M8650, M8350
B1M	MD6 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8650, M8350
B1N	GND	P.S.	ALL
B1P	MD7 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8650, M8350
B1R	DATA4 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350

Pin	Signal	Source	Destination
B1S	DATA5 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350
B1T	GND	P.S.	ALL
B1U	DATA6 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350
B1V	DATA7 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350
B2A	+5	P.S.	ALL
B2B	-15	P.S.	ALL
B2C	GND	P.S.	ALL
B2D	INT STROBE	M8330	M8330, M8360
B2E	BRK IN PROG L	M8360	KC8-EA
B2F	GND	P.S.	ALL
B2H	MA, MS LOAD CONT L	M8360	M8310
B2J	OVERFLOW L	M8310	M8360
B2K	BRK DATA CONT L	M836 KC8-EA	KC8-EA, M8310
B2L	BREAK CYCLE L	M8360	KC8-EA
B2M	LD ADD ENABLE L	KC8-EA	KC8-EA, M8310
B2N	GND	P.S.	ALL
B2P	INT IN PROG H	M8330	M8310, M8330
B2R	RES1		Reserved for DEC use only
B2S	RES2		Reserved for DEC use only

Pin	Signal	Source	Destination
B2T	GND	P.S.	ALL
B2U	RUN L	M8330	KC8-EA, M8330, M8350
B2V	POWER OK	P.S.	M8330, G104
C1A	TP		Not bussed
C1B	TP		Not bussed
C1C	GND	P.S.	ALL
C1D	I/O PAUSE L	M8330	M8330, M8310, M8650, M8350
C1E	C0 L	M8650 M8350 M8330	M8310
C1F	GND	P.S.	ALL
C1H	C1 L	M8650 M8350 M8330	M8310
C1J	C2 L	M8350	M8310
C1K	BUS STROBE	M8330 M8350	M8310, M8330
C1L	INTER. I/O L	M8330	M8650, M8350
C1M	NOT LAST TRANSFER L	M8350	M8330
C1N	GND	P.S.	ALL
C1P	INT RQST L	M8650	M8330, M8350
C1R	INITIALIZE	KC8-EA M8330	KC8-EA, M8330, M8310, M8300, M8650, M8350 M836
C1S	SKIP L	M8650	M8330, M8310
C1T	GND	P.S.	ALL
C1U	CPMA DISABLE L	M836	M8300
C1V	MS,IR DISABLE L	KC8-EA M836	M8330, M8310

Pin	Signal	Source	Destination
C2A	+5	P.S.	ALL
C2B	-15	P.S.	ALL
C2C	GND	P.S.	ALL
C2D	TP1 L	M8330	M8310, M8330, M8350, M8360
C2E	TP2 L	M8330	M8310, M8330, M8350, M8360
C2F	GND	P.S.	ALL
C2H	TP3	M8330	M8310, M8330, M8650, M835
C2J	TP4	M8330	KC8-EA, M8310, M836
C2K	TS1 L	M8330	KC8-EA, M8330, M8310, M8350, M8360
C2L	TS2 L	M8330	M8310, M8360
C2M	TS3 L	M8330	KC8-EA, M8310, M8350
C2N	GND	P.S.	ALL
C2P	TS4 L	M8330	KC8-EA, M8310, M8360
C2R	LINK DATA L	M8330	M8310
C2S	LINK LOAD L	M8330	M8310
C2T	GND	P.S.	ALL
C2U	IND1 L	KC8-EA	M8330, M8310
C2V	IND2 L	KC8-EA	M8330, M8310
D1A	TP		Not bussed
D1B	TP		Not bussed
D1C	GND	P.S.	ALL
D1D	MA8 L	M8360 M8300	KC8-EA, M8330, M8300, G227
D1E	MA9 L	M8360 M8300	KC8-EA, M8300, G227
D1F	GND	P.S.	ALL

Pin	Signal	Source	Destination
D1H	MA10 L	M8360 M8300	KC8-EA, M8300, G227
D1J	MA11 L	M8360 M8300	KC8-EA, M8300, G227
D1K	MD8 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8650, M8350
D1L	MD9 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8650, M8350
D1M	MD10 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8650, M8350
D1N	GND	P.S.	ALL
D1P	MD11 L	G104 M8300	KC8-EA, M8330, M8310, M8300, G104, M8650, M8350
D1R	DATA8 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350
D1S	DATA9 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350
D1T	GND	P.S.	ALL
D1U	DATA10 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350
D1V	DATA11 L	M8360 KC8-EA M8650 M8300 M8350	KC8-EA, M8300, M8650, M8350

Pin	Signal	Source	Destination
D2A	+15	P.S.	ALL
D2B	-15	P.S.	ALL
D2C	GND	P.S.	ALL
D2D	IR0 L	M8310	KC8-EA, M8330, M8310
D2E	IR1 L	M8310	KC8-EA, M8330, M8310
D2F	GND	P.S.	ALL
D2H	IR2 L	M8310	KC8-EA, M8330, M8310
D2J	F L	M8310	KC8-EA, M8330, M8310
D2K	D L	M8310	KC8-EA, M8330, M8310
D2L	E L	M8310	KC8-EA, M8330, M8310
D2M	USER MODE	USER	KC8-EA, M8330
D2N	GND	P.S.	ALL
D2P	F SET L	M8310	KC8-EA, M8330, M8310
D2R	PULSE LA ADDR H	KC8-EA	M8310
D2S	STOP L	M8330 KC8-EA	M8330
D2T	GND	P.S.	ALL
D2U	KEY CONT L	KC8-EA	M8330, M8310
D2V	SWITCH L	KC8-EA	KC8-EA

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VOLUME 1
DEC-8E-HR1C-D

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