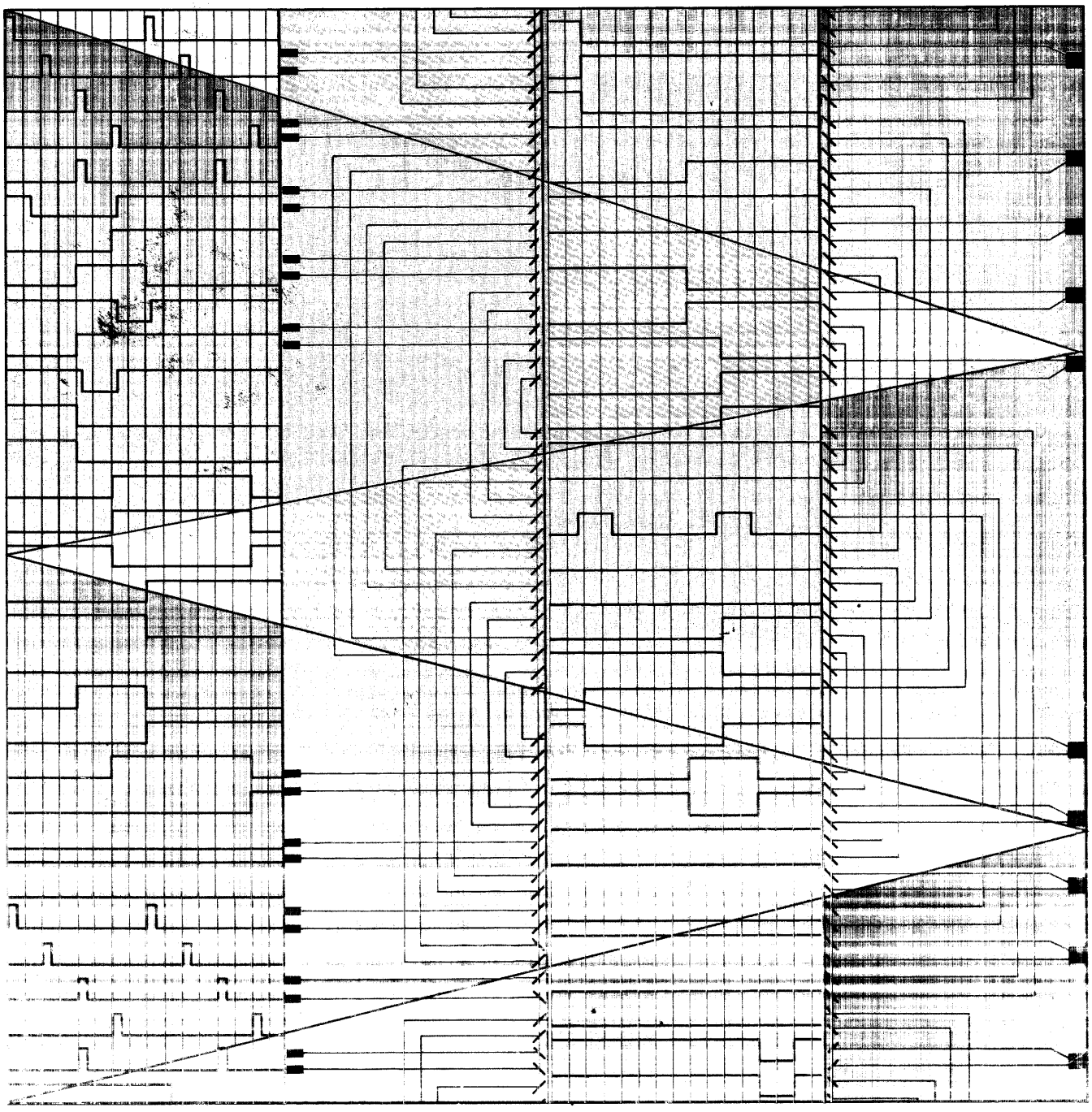
pdp8/e

pdp8/f & pdp8/m

external bus options maintenance manual volume 3



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pdp8/e, pdp8/f & pdp8/m

MAINTENANCE MANUAL
VOLUME 3

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PREFACE

This manual, the third in a series of three, describes peripheral controller options of the PDP-8/E, PDP-8/F, and PDP-8/M.

The content of this manual includes installation procedures, theory of operation, and maintenance procedures for the options described. It is assumed that the reader is thoroughly familiar with Volume 1 of this series, and with the applicable sections of the *1972 PDP-8/E & PDP-8/M Small Computer Handbook.*

PART 1
CONSOLE TELEPRINTER

CHAPTER 1
LC8-E DECWRITER CONTROL

SECTION 1 INTRODUCTION

The LC8-E DECwriter Control interfaces the parallel version of the LA30 DECwriter (LA30P) to the PDP-8/E. The Control consists of a single M8329 quad module that plugs into the OMNIBUS and connects to the DECwriter with a signal cable that is supplied with the module.

The LA30 DECwriter is discussed here only to the extent necessary to both fully describe LC8-E Control operation and present supplementary information concerning installation and checkout. Details concerning the installation, operation, troubleshooting, and maintenance of the LA30, itself, can be found in the *LA30 DECwriter Maintenance Manual,* DEC-00-LA30-DA. Other publications and documents relevant to the LC8-E are:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* – DEC, 1972
b. *PDP-8/E Maintenance Manual, Volume 1*
c. LA30 DECwriter Diagnostic, MAINDEC-8E-D2FA
d. DEC Engineering Drawing, DECwriter Control, E-CS-M8329-0-1.

SECTION 2 INSTALLATION

The LC8-E DECwriter Control is installed on site by DEC Field Service personnel. The customer should *not* attempt to unpack, inspect, install, checkout, or service the equipment.

Insert the LC8-E Control in the PDP-8/E OMNIBUS. See Table 2-3, Volume 1, for information concerning recommended module priorities (the LC8-E is a "non-memory" option).

Connect the LC8-E to the DECwriter with the signal cable provided. J1 of the LC8-E, a 40-pin Berg Connector, connects to module slot A02 of the LA30P logic rack.

See Chapter 2 of the *LA30 DECwriter Maintenance Manual* for additional information concerning system installation and for procedures to be followed to checkout both the Control and the DECwriter.

SECTION 3 DESCRIPTION

Figure 1-1 is a block diagram of the LC8-E Control. Pin assignments for OMNIBUS signals and connector J1 signals can be found on engineering drawing no. E-CS-M8329-0-1. Information concerning pin assignments of the interconnecting cable is given in Section 5.

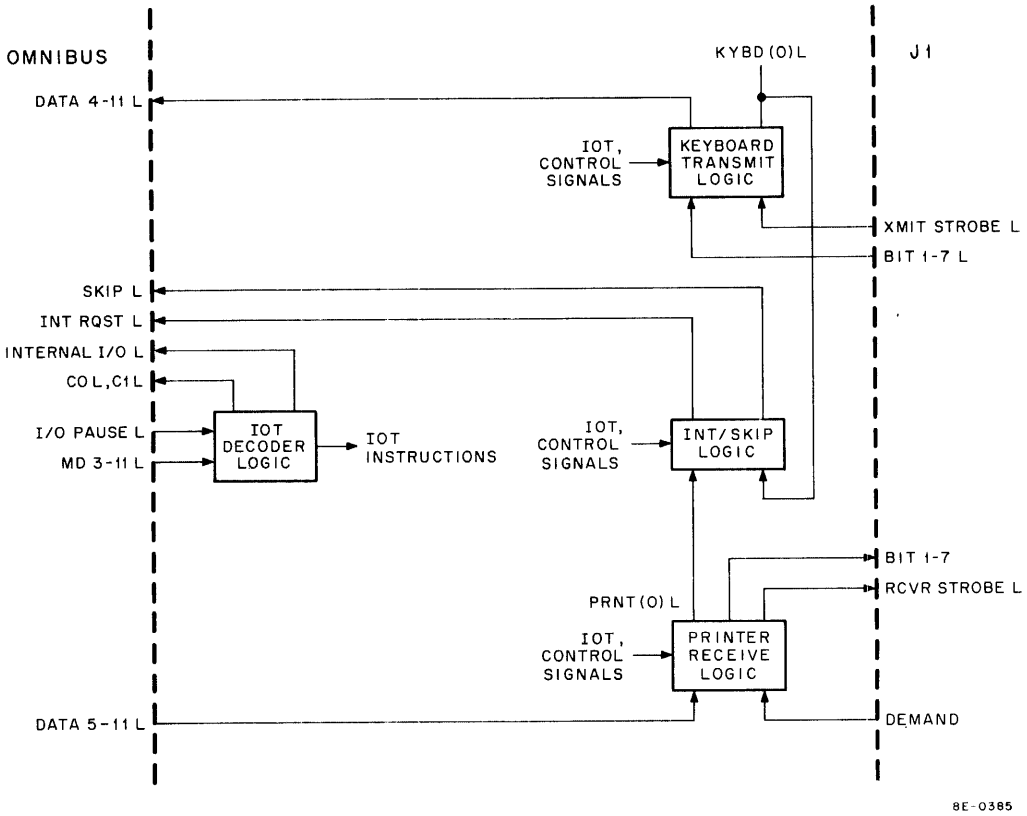

Figure 1-1 LC8-E Block Diagram

The LC8-E has two distinct functions: transfer of data from the CPU AC Register to the LA30 Printer Buffer Register and transfer of data from the LA30 Keyboard Buffer Register to the AC Register. The transfer of data to the LA30 Printer Buffer is carried out by the printer receive logic. When the LA30 is able to receive data, it asserts the DEMAND signal. This signal sets the printer flag in the printer receive logic. The resulting PRNT (0) L signal causes the INT/skip logic to assert OMNIBUS INT RQST L if the LC8-E has been logically connected to the interrupt system. Alternatively, PRNT (0) L can be tested by a program skip instruction in the INT/skip logic. In either case, the computer ultimately proceeds to a program subroutine that begins the data transfer. When this subroutine is executed, the information is transferred from the AC Register to the DATA 5–11 lines and clocked into a 7-bit register in the printer receive logic. The register outputs are available at J1 as the BIT 1–7 signals. The logic then generates a RCVR STROBE L signal that clocks the BIT 1–7 data into the Printer Buffer Register, clears the Printer flag, and causes the LA30 to negate the DEMAND signal.

The transfer of data from the LA30 Keyboard Buffer Register to the AC Register is carried out by the keyboard transmit logic. When an LA30 key is depressed, information is applied, via the BIT 1–7 lines, to a 7-bit register in the keyboard transmit logic. When the LA30 generates an XMIT STROBE L signal, the information is clocked into the 7-bit register and the KYBD (0) signal is asserted. The KYBD (0) L signal can be tested in the INT/skip logic with a skip instruction, or the interrupt system can be used to cause the program to enter an appropriate subroutine. When the subroutine is executed, the information is gated from the register in the keyboard transmit logic to lines DATA 5–11 (the logic asserts the DATA 4 L signal separately so that the input character is compatible with the modified-ASCII Teletype® code), then to the AC Register. The AC is loaded and, simultaneously, KYBD (0) L is negated.

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SECTION 4 DETAILED LOGIC

1.1 IOT DECODER LOGIC

The IOT decoder logic is shown in Figure 1-2. The LC8-E uses 12 IOT instructions, 6 for the keyboard functions and 6 for the printer functions (one of the listed printer IOTs — Skip on Printer or Keyboard Interrupt — applies to both functions). More than one LA30 DECwriter can be interfaced to the PDP-8/E at the same time. The LC8-E Control associated with each LA30 must have a unique device selection code. Therefore, the M8329 Control Module is fabricated with machine-inserted jumpers and solder terminals that allow the user to assign any two of 64 possible device selection codes to a particular LC8-E (care should be taken when assigning device selection codes to preclude multiple assignments of the same code). Figure 1-2 illustrates the octal codes and mnemonics that pertain when the LC8-E Control is manufactured. The octal codes and mnemonics are listed in Table 1-1 and the respective functions, which remain constant regardless of the code or mnemonic, are detailed.

Figure 1-2 identifies the 12 machine-inserted jumpers, W1 through W12, and 6 groups, lettered from A to F, of 4 numbered solder terminals (jumper and terminal designations are etched on the quad module for each identification). To change a control device selection code, first cut a selected "W" jumper (or jumpers); then, solder a new jumper between designated terminals associated with the "W" jumper(s). For example, the device selection code for the keyboard functions can be changed from 03 to 13 by removing W5 and connecting terminals C3 and C4; the printer functions device code can be changed from 04 to 10 by removing W6 and W8 and connecting terminals C2 and C4 and D2 and D3.

As Figure 1-2 shows, the device selection code signals, 603X and 604X, are applied to separate DEC 7442 Decoder ICs. The device operation codes represented by bits MD 9, 10, and 11 are then decoded by E9 and E6 to provide the listed IOT instruction signals. Note that the device selection code signals assert the OMNIBUS INTERNAL I/O L signal; thus, the positive I/O bus interface ignores the IOT instruction.

Three of the keyboard IOT instruction signals cause OMNIBUS "C" lines to be activated. When the KCC L signal is generated, both the C0 L and C1 L signals are asserted; the resulting transfer of 0s clears the AC Register. The KRB L signal also results in a transfer to the AC; however, this transfer involves data from the keyboard, rather than 0s. Finally, the KRS L signal causes only the C1 L signal to be asserted; the result is an inclusive-OR transfer of data to the AC.

1.2 PRINTER RECEIVE LOGIC

The printer receive logic is shown in Figure 1-3. The 7-bit register is shown only in part, the logic associated with bits DATA 10—6 being similar to that illustrated for bits 11 and 5. Significant signals are related by the timing diagram in Figure 1-4. Refer to both figures when reading the logic description.

The LA30 printer routine is initiated by the program instruction TFL, Set the Printer Flag. At TP3 time of this instruction, NAND gate E7 is enabled, causing the PRNT flip-flop to be set. This flip-flop is also set by the DEMAND signal, which is asserted by the printer each time it completes a print cycle (Figure 1-4 illustrates this signal rather than the TFL L signal). If the LC8-E is logically connected to the interrupt system, as Figure 1-4 and this discussion assume, PRNT (0) L causes the INT/skip logic to assert OMNIBUS INT RQST L. The program proceeds to an interrupt servicing routine to determine the identity of the requesting device. The TSK instruction in the routine causes the program to jump to an LC8-E routine that determines if the printer or keyboard requested the interrupt (other options are open to the programmer, this is but one example). Ultimately, the LC8-E printer routine executes the TLS instruction.

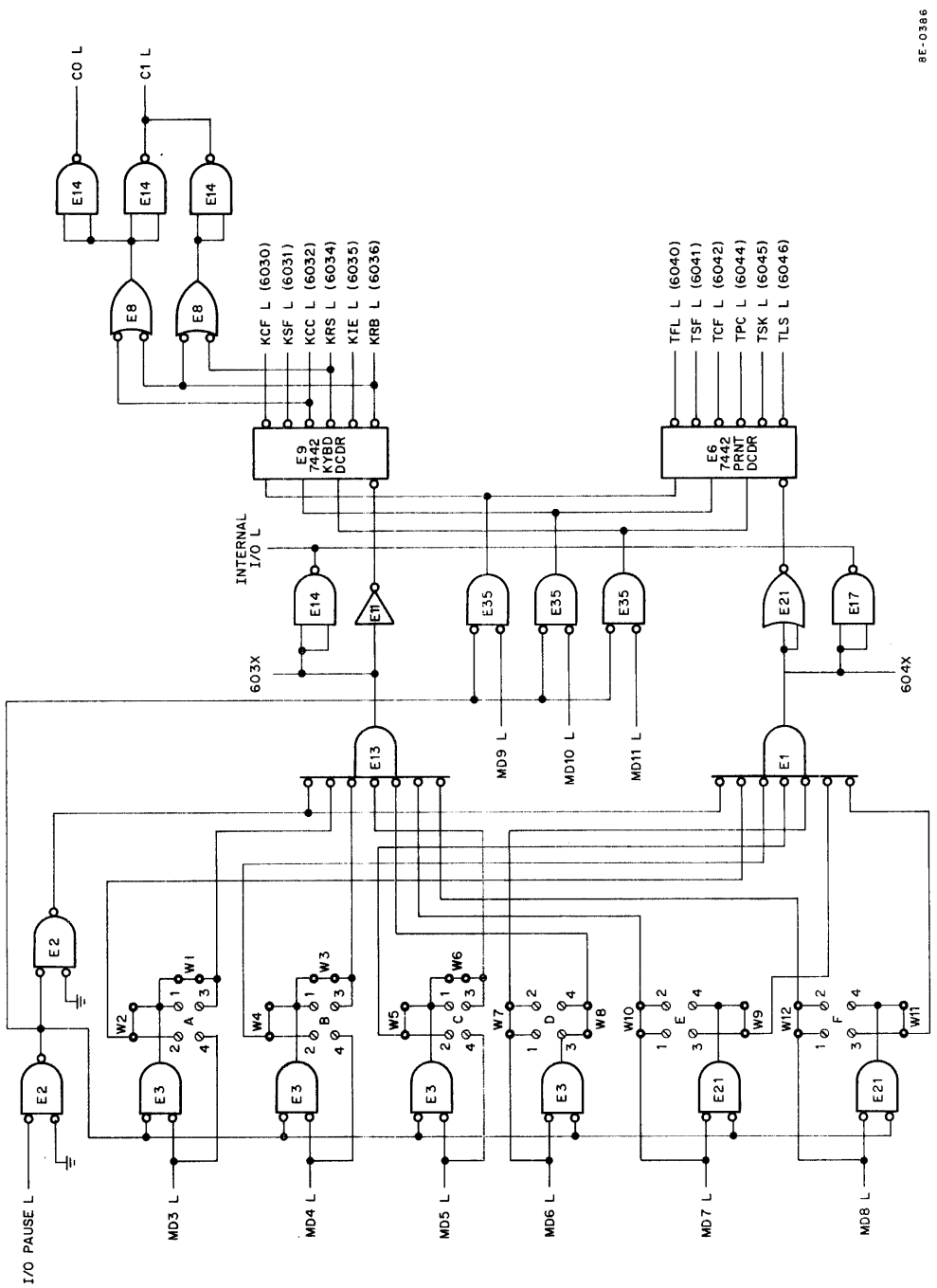


Figure 1-2 LC8-E IOT Decoder

Table 1-1
LC8-E IOT Instruction List

Octal Code	Mnemonic	Function
6030	KCF	Clear the Keyboard flag. Clears the KYBD flip-flop.
6031	KSF	Skip on the Keyboard flag. Senses the state of the KYBD flip-flop. If the flip-flop is set, increments the program counter so that the next sequential instruction is skipped.
6032	KCC	Clear the flag, clear the AC. Clears both the KYBD flip-flop and the AC Register.
6034	KRS	Read the keyboard buffer. Gates character information from the keyboard transmit logic and ORs it into AC Register bits 5 through 11. Sets AC4.
6035	KIE	Set/clear interrupt enable. Sets the INT ENA flip-flop if AC11 is logic 1; clears the flip-flop if AC11 is logic 0.
6036	KRB	Read the keyboard buffer, clear the flag, clear the AC. Gates character information from the keyboard transmit logic and jams it into AC Register bits 5 through 11. Sets AC4. Clears the KYBD flip-flop.
6040	TFL	Set the printer flag. Sets the PRNT flip-flop.
6041	TSF	Skip on the Printer flag. Senses the state of the PRNT flip-flop. If the flip-flop is set, increments the program counter so that the next sequential instruction is skipped.
6042	TCF	Clear the Printer flag. Clears the PRNT flip-flop.
6044	TPC	Load the printer buffer and print. Causes the character information to be gated to the BIT 1—7 lines. Sets the RCVR STROBE flip-flop. At TS2 of the next instruction, the information is loaded into the LA30 input buffer.
6045	TSK	Skip on a keyboard/printer interrupt request. Skips the next sequential instruction if the INT ENA flip-flop is set (the LC8-E is logically connected to the interrupt system) and if either the KYBD flip-flop or the PRNT flip-flop is set.
6046	TLS	Load the printer buffer and print. Clears the flag. The character information is gated to the BIT 1—7 lines. Sets the RCVR STROBE flip-flop. At TS2 of the next instruction, the information is loaded into the LA30 input buffer. Clears the PRNT flip-flop.

During TS2 of the TLS instruction, information is gated from the AC Register to the DATA lines and remains on the DATA lines through TS3. When TLS L is decoded in the IOT Decoder logic, it enables NOR gates E5B and E5D (Figure 1-3). The enabled output of E5D causes the information on lines DATA 5—11 to be gated to the D-inputs of the register flip-flops, while at the same time providing a high level on the D-input of E27B, the RCVR STROBE L flip-flop. At TP3 time of the instruction the register flip-flops are clocked, flip-flop E27B is set, and the PRNT flip-flop is cleared. The register data is applied, via the BIT 1—7 lines, to the printer buffer

register. During TS2 of the instruction following TLS, NAND gate E29 asserts the RCVR STROBE L signal (flip-flop E27B is cleared at TP3 time of this instruction). This signal loads the printer buffer register and negates the DEMAND signal. When the print cycle ends approximately 30 ms later, the DEMAND signal is again asserted and a new transfer is begun.

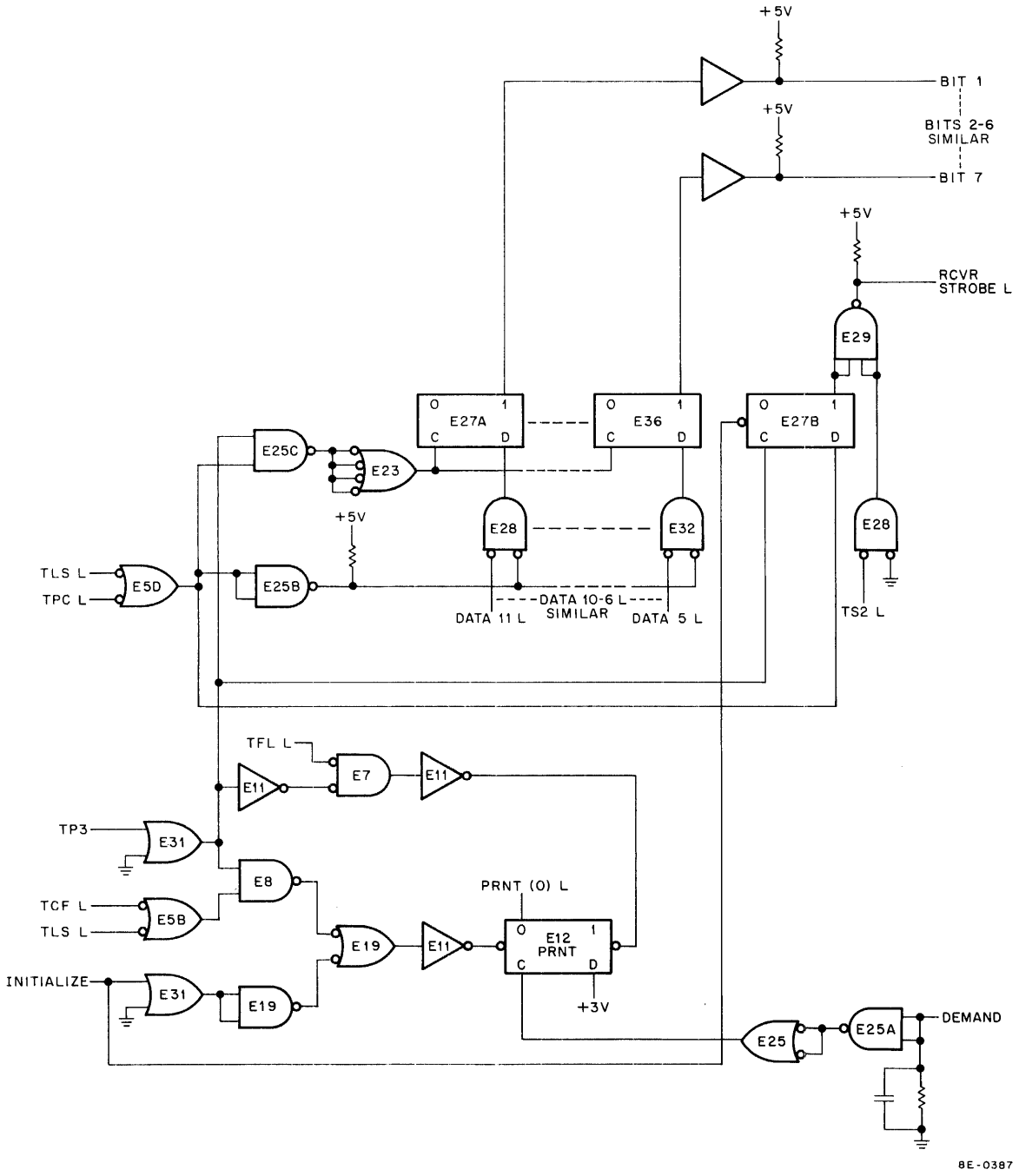


Figure 1-3 Printer Receive Logic

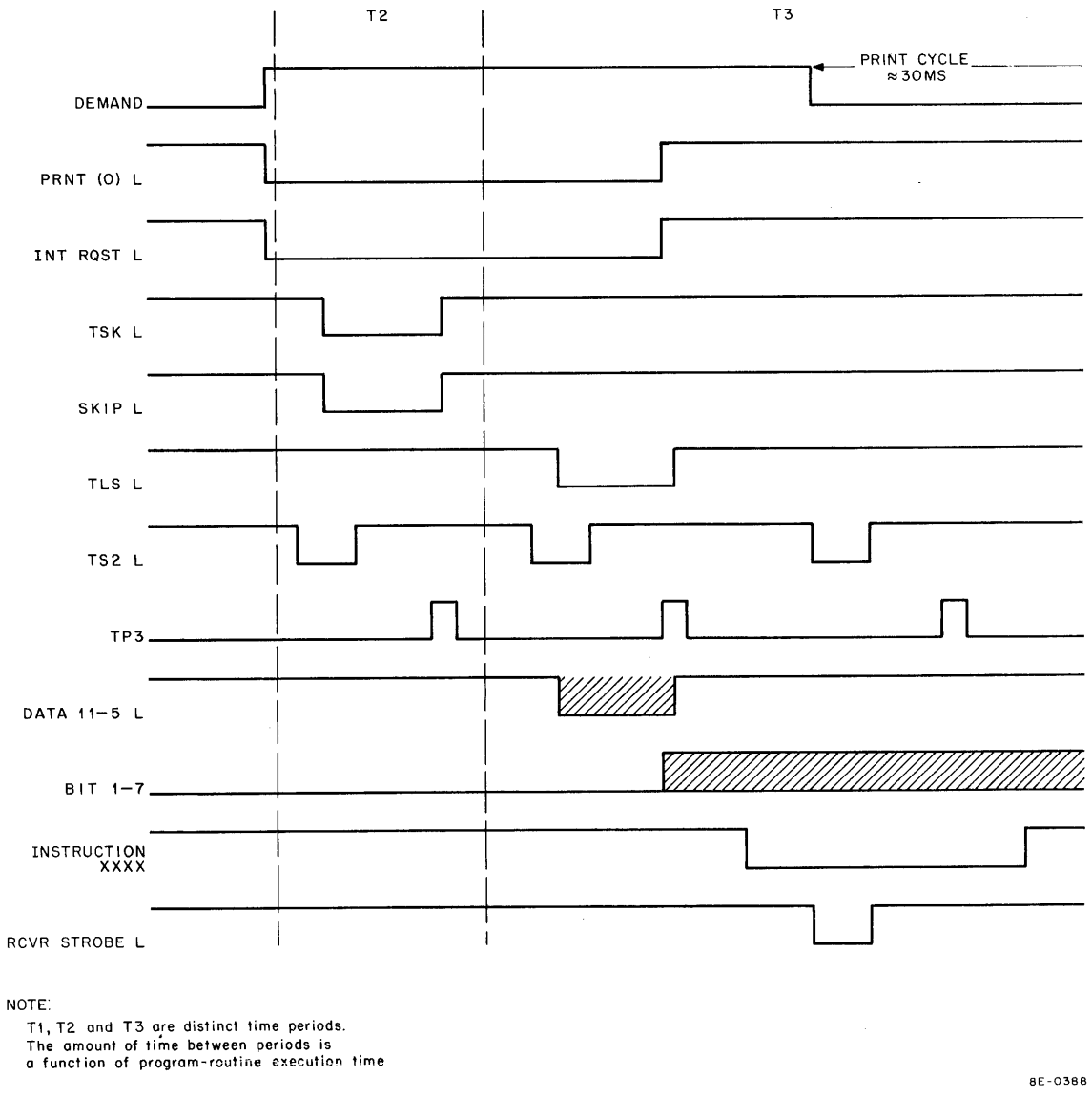


Figure 1-4 Timing, Printer Receive Logic

1.3 KEYBOARD TRANSMIT LOGIC

The keyboard transmit logic is shown in Figure 1-5. The 7-bit register is shown only in part. Significant signals are related by the timing diagram in Figure 1-6. Refer to both figures when reading the logic description.

The user initiates the keyboard sequence by depressing a key on the LA30. The character information is placed on the BIT 1–7 lines. After a period of time that allows the BIT lines to settle, the keyboard generates the XMIT STROBE L signal. This signal clocks the information into the 7-bit register and sets the KYBD flip-flop. If the LC8-E is logically connected to the interrupt system, as assumed, KYBD (0) L causes the INT/skip logic to assert the OMNIBUS INT RQST L signal. The program proceeds to an interrupt servicing routine to determine the identity of the requesting device. The TSK instruction in the routine causes the program to jump to an LC8-E routine that determines if the printer or keyboard requested the interrupt. Ultimately, the LC8-E keyboard routine executes the KRB instruction.

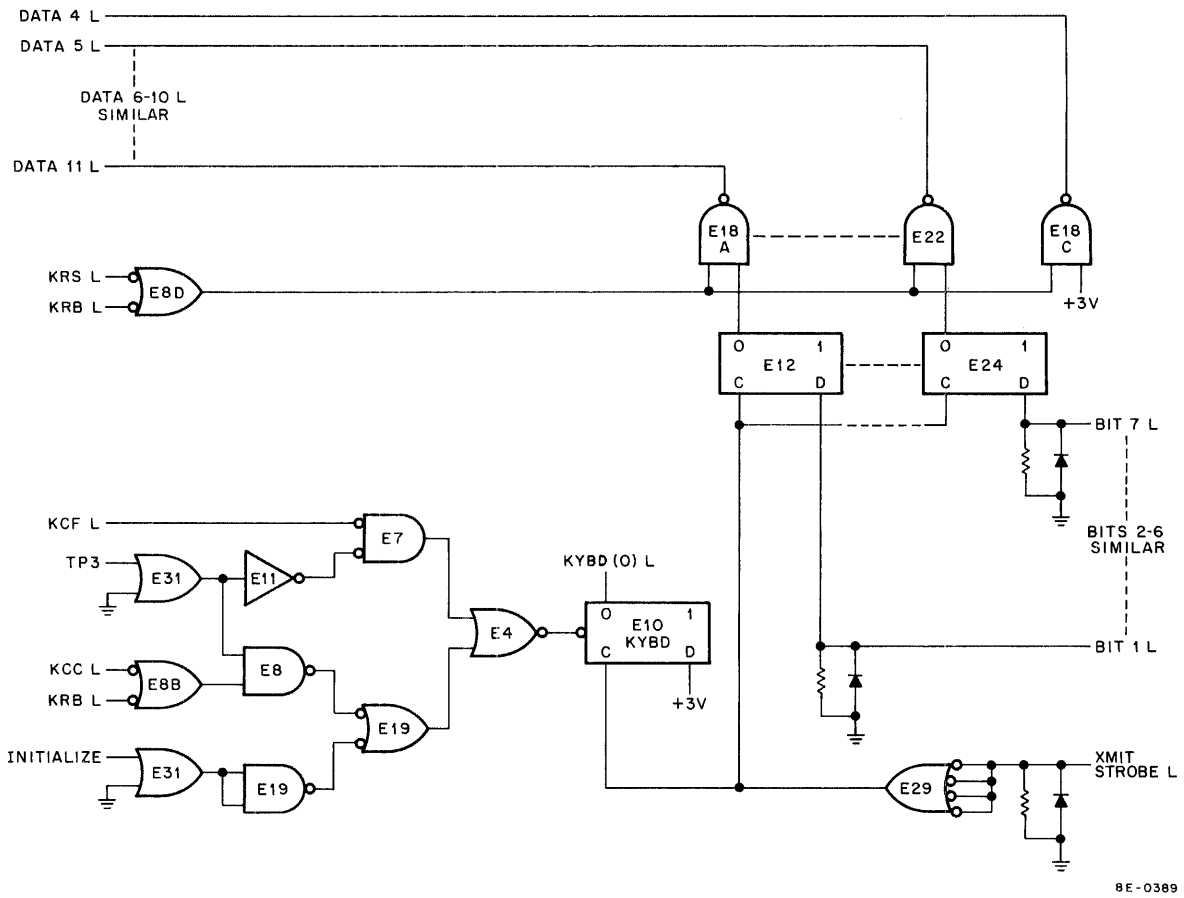


Figure 1-5 Keyboard Transmit Logic

When the KRB instruction is decoded, the IOT decoder logic generates the KRB L signal and activates the C0 and C1 lines. The KRB L signal enables NOR gate E8D; the output signal from E8D gates the information from the register outputs to DATA lines 5–11, and also causes NAND gate E18C to assert DATA 4 L. The DATA lines are gated to the AC Register and the information is clocked into the register at TP3 time. Also at TP3, the KYBD flip-flop is cleared, readying the logic for a new data transfer.

1.4 INT/SKIP LOGIC

The INT/skip logic is shown in Figure 1-7. The PRNT (0) L signal and the KYBD (0) L signal can cause program skips when tested by instructions TSF and KSF, respectively. The signals can also be tested by the TSK instruction, provided the INT ENA flip-flop, E10, has been set, logically connecting the LC8-E to the interrupt system. When E10 is set, the TSK L signal enables NAND gate E4D, which, in turn, enables AND-NOR gate E15 if either the PRNT (0) L signal or the KYBD (0) L signal is asserted. Simultaneously, NAND gate E17 asserts the INT RQST L signal.

The INT ENA flip-flop is set by the OMNIBUS INITIALIZE signal for the PDP-8 Family program compatibility. To clear the flip-flop, removing the LC8-E from the interrupt system, load AC11 with logic 0 and then program the KIE instruction. The logic 0 in AC11 keeps the DATA 11 L signal negated. Thus, the D-input of E10 remains high. At TP3 time, NAND gate E7 provides a clock pulse for E10, clearing the flip-flop. E10 can be set at any time with the same instruction merely by loading AC11 with logic 1.

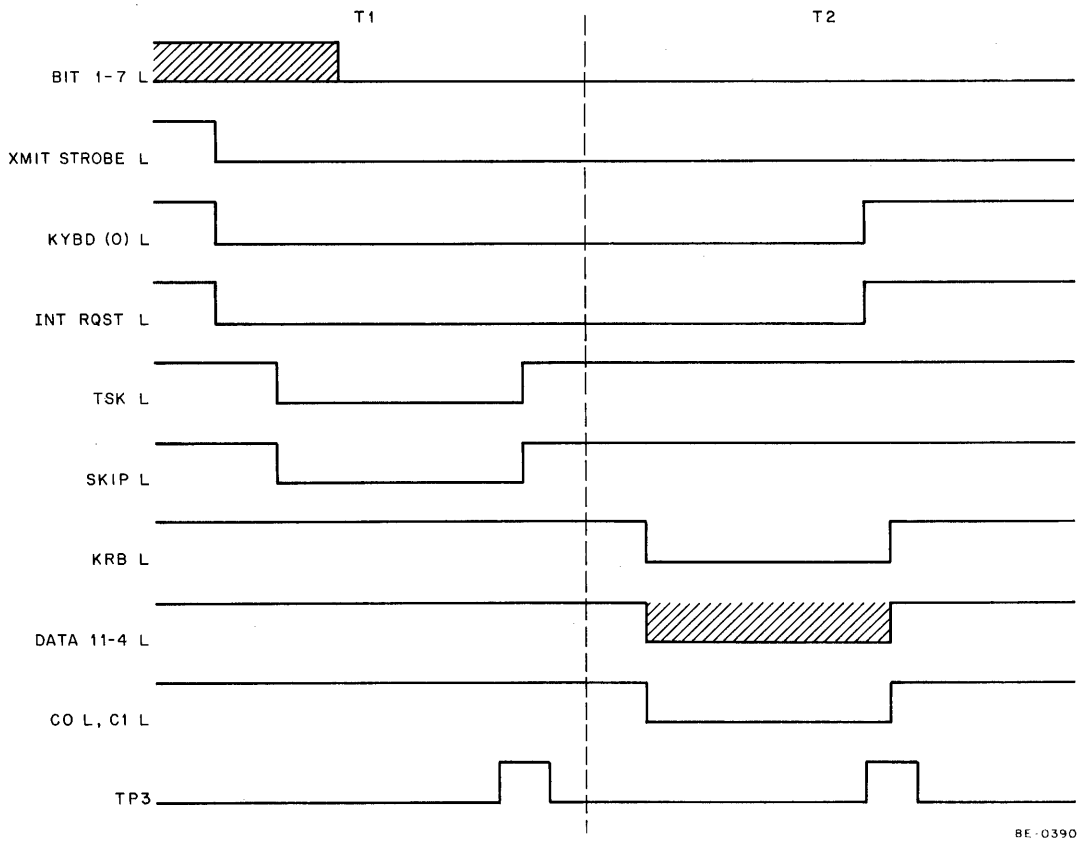


Figure 1-6 Timing, Keyboard Transmit Logic

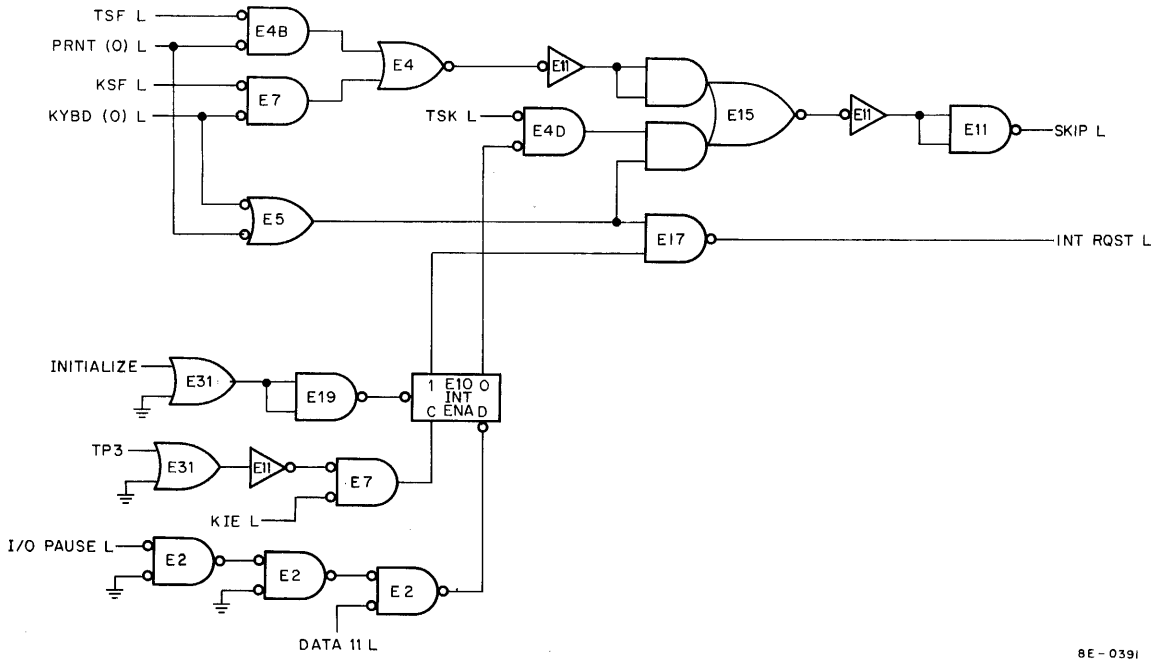


Figure 1-7 INT/Skip Logic

SECTION 5 MAINTENANCE

Refer to Volume 1 and to the *LA30 DECwriter Maintenance Manual* for maintenance information that pertains to both the LC8-E Control and the LA30 DECwriter. The LA30 DECwriter Diagnostic, MAINDEC-8E-D2FA, should be run when an error is suspected.

SECTION 6 SPARE PARTS

Table 1-2 lists recommended spare parts for the LC8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 1-2
LC8-E Recommended Spare Parts

DEC Part No.	Description	Quantity
19-10394	IC DEC 5384	1
19-10392	IC DEC 5380	1
19-10391	IC DEC 5314	1
19-10046	IC DEC 7442	1
19-9929	IC DEC 7417	1
19-9973	IC DEC 97401	1
19-9686	IC DEC 7404	1
19-9056	IC DEC 74H00	1
19-9004	IC DEC 7402	1
19-5580	IC DEC 7450	1
19-5579	IC DEC 7440	1
19-5575	IC DEC 7400	1
19-5547	IC DEC 7474	1
10-1610	Capacitor, 0.01 μF, 100V, 20% Disk	1
10-0067	Capacitor, 6.8 μF, 35V, 20% Tant	1
10-0024	Capacitor, 47 pF, 100V, 5% DM	1
70-8417	Signal Cable	1

PART 2
PAPER-TAPE READER/PUNCH

CHAPTER 2
PC8-E HIGH-SPEED PAPER-TAPE READER/PUNCH

SECTION 1 INTRODUCTION

The PC8-E (or the desk-top model, PC8-EB) Reader/Punch option consists of a control module and a high-speed paper-tape reader/punch manufactured by DEC [Model PC04BL (60 Hz) or PC04BM (50 Hz)]. The control (DEC M840) plugs into the PDP-8/E OMNIBUS and connects to the external reader/punch via two signal cables that are supplied with the system.

The PC04 Reader/Punch is discussed here only to the extent necessary to fully describe control operation and present supplementary information concerning installation and checkout. Details concerning the installation, operation, troubleshooting, and maintenance of the reader/punch, itself, can be found in the *PC04/PC05 Paper-Tape Reader/Punch Maintenance Manual* [DEC-00-PC0A-D (1)]. Other publications and documents relevant to the PC8-E are:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* — DEC, 1972
b. *PDP-8/E Maintenance Manual, Volume 1*
c. *Roytron Model 500 Maintenance Manual*
d. PC8-E Diagnostic, MAINDEC-8E-D2CA
e. DEC Engineering Drawing, Reader/Punch Control, E-CS-M840-0-1.

SECTION 2 INSTALLATION

The PC8-E Reader/Punch and Control is installed on site by DEC Field Service personnel. The customer should *not* attempt to unpack, inspect, install, checkout, or service the equipment.

Insert the PC8-E Control Module in the PDP-8/E OMNIBUS. Refer to Table 2-3, Volume 1, for information concerning recommended module priorities (the PC8-E is a "non-memory" option).

Connect the control to the reader/punch with the two signal cables provided. J1 of the control, a 40-pin Berg Connector, connects to reader/punch module slot B1, a DEC M955 Connector. J2 of the control connects to module slot A1 (refer to Section 5 for cable and connector pin assignments).

Refer to Chapter 2 of the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* (DEC-00-HGPA-D) for additional information concerning system installation and for procedures to be followed to checkout both the control and the reader/punch.

SECTION 3 DESCRIPTION

Figure 2-1 is a block diagram of the PC8-E Control. The functions of the control can be grouped conveniently according to reader functions and punch functions, as illustrated by the block diagram. Consider the reader functions, represented by the logic blocks above the broken line.

The control logic generates signals that control the PC04 tape-feed operation. As the paper tape passes over the PC04 photoarray, signals representing the punched characters are strobed into the Control Buffer Register. The buffered information is then transferred to the PDP-8/E AC Register and operated on by subsequent program instructions.

The tape-feed operation can be initiated under program control or by activation of the Reader FEED switch on the PC04 front panel. If the switch is used, the tape feeds through the read station but data is not transferred from the Control Buffer Register. If data is to be transferred, the tape-feed operation must be program-initiated.

Two IOT instructions, 6014 (Fetch Reader Character) and 6016 (Read Buffer, Fetch Reader Character), read the information currently over the photoarray and then initiate tape feed. When either of these instructions is decoded by the IOT decoder logic, the read tape logic generates an ENABLE signal that triggers the clock logic. The first CLOCK PULSE produced enables the read tape logic to generate an RDR DATA STROBE pulse. This pulse clocks the RDR Buffer Register, loading the register with the information present on the READ HOLE 1–8 lines.

In addition to clocking the RDR Buffer Register, the RDR DATA STROBE signal sets the RDR FLAG flip-flop in the INT/skip logic and clears the RDR RUN flip-flops in the tape read logic. If the control has been logically connected to the computer interrupt system by a previous 6010 instruction, or by the INITIALIZE signal, the OMNIBUS INT RQST L signal is asserted. The computer enters the interrupt servicing routine to determine the identity of the requesting device. The 6011 instruction in the routine causes the computer to proceed to the PC8-E subroutine to service the interrupt request (refer to Table 2-1 for IOT instruction descriptions).

After producing the first CLOCK PULSE, the clock logic generates a SHIFT PULSE. This causes the motor control logic to provide stepping signals for the PC04 Reader Motor. The motor shaft turns, feeding the tape through the read station. After two steps, the next character on the tape appears over the photoarray; the current read operation is completed. If a new 6014 or 6016 instruction has been issued, another RDR DATA STROBE is generated and this character is loaded into the RDR Buffer Register. Each RDR DATA STROBE loads a character into the register. The register data is transferred to the CPU AC Register by the 6012 or 6016 instruction. If a 6014 or 6016 instruction is decoded between each RDR DATA STROBE and the next CLOCK PULSE, reader operation is continuous, at a rate of 300 characters/second. Otherwise, the character rate is limited to 25 characters/second.

The tape status logic monitors the FEED HOLE signal from the PC04. When the tape-read mechanism is out of tape, the tape status logic provides a signal that inhibits program generation of the motor stepping signals and clears the tape read logic.

Now consider the punch functions, represented by the logic blocks below the broken line in Figure 2-1. The punch motor operates continuously when power is applied to the PC04. The punch mechanism (Roytron Model 500) provides a PUNCH SYNC signal at the beginning of each punch mechanical cycle. This signal synchronizes the control timing and the rotating motor shaft. If a 6024 or 6026 instruction is decoded, the ENABLE PUNCH BUFFER L signal is generated by the IOT decoder logic. Whatever information is on the DATA 4–11 lines can now be clocked into the Punch Buffer Register. At TP3 time of the instruction the PUNCH STROBE signal clocks the register, transferring the character signals from the DATA 4–11 lines to the HOLE 1–8 lines.

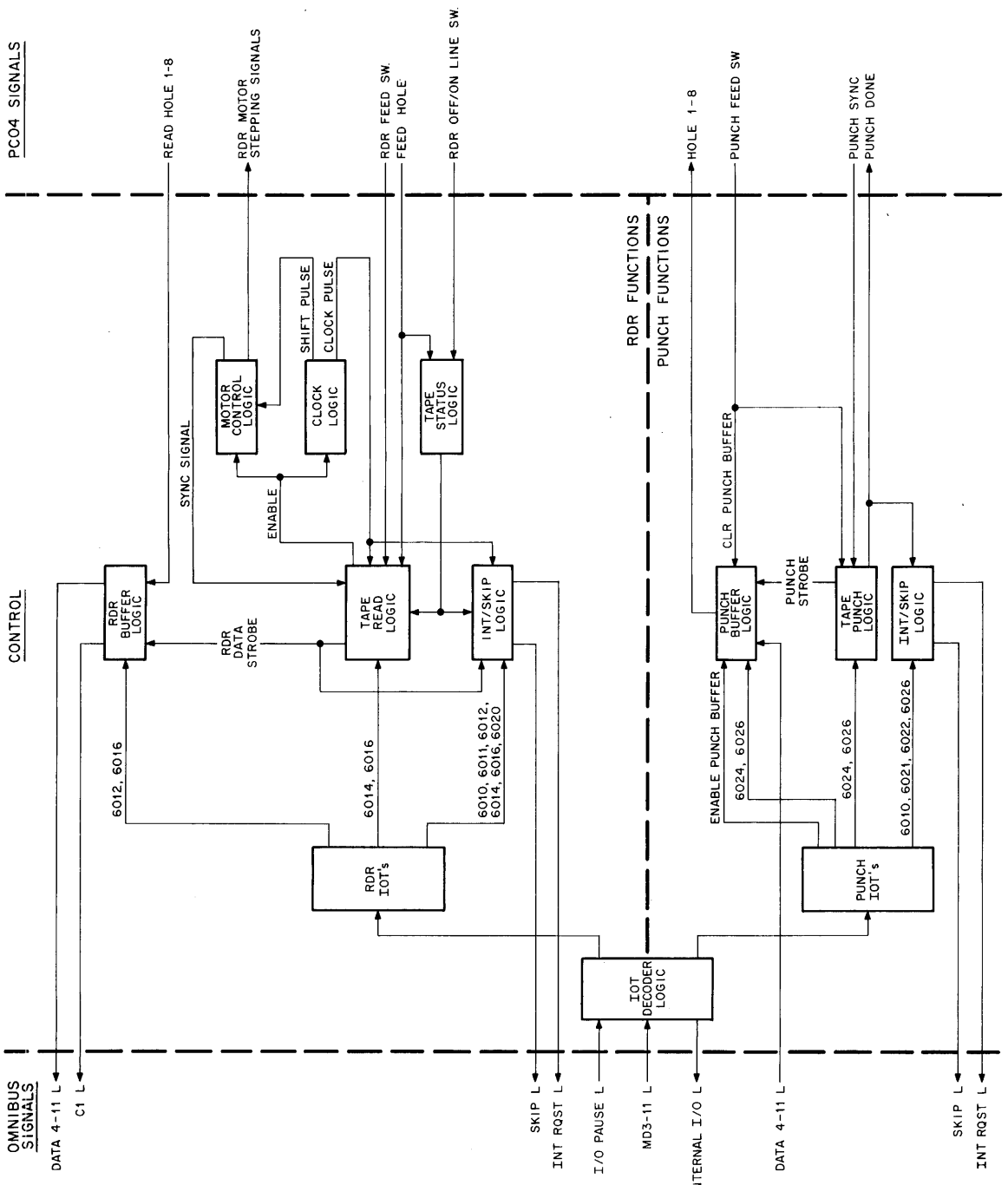


Figure 2-1 PC8-E Control, Block Diagram

Table 2-1
PC8-E IOT Instructions

Octal Code	Mnemonic	Function
6010	RPE	Set the INT ENA flip-flop. The PC8-E is logically connected to the computer interrupt system.
6011	RSF	Skip on Reader flag. Senses the state of the RDR FLAG flip-flop. If the flip-flop is set, the program counter is incremented so that the next sequential instruction is skipped.
6012	RRB	Read the RDR Buffer Register. Causes the RDR Buffer Register to be ORed into the AC Register, clears the RDR FLAG flip-flop.
6014	RFC	Fetch a character from the tape. Clears the RDR FLAG flip-flop, loads a character into the RDR Buffer Register from the tape, sets the RDR FLAG flip-flop when the RDR Buffer Register is loaded.
6016	RRB, RFC	Microprogram of 6012 and 6014. RDR Buffer Register contents are ORed into AC Register, RDR FLAG flip-flop is cleared, character is loaded into Register, and RDR FLAG flip-flop is set.
6020	PCE	Clear the INT ENA flip-flop. The PC8-E is disconnected from the computer interrupt system.
6021	PSF	Skip on Punch flag. Senses the state of the PUNCH FLAG flip-flop. If the flip-flop is set, the program counter is incremented so that the next sequential instruction is skipped.
6022	PCF	Clear the Flag. Clears the PUNCH FLAG flip-flop.
6024	PPC	Load Punch Buffer Register, punch character. Transfers the AC4—11 contents to the Punch Buffer Register, punches the character, sets the PUNCH FLAG flip-flop when done.
6026	PLS	Microprogram of 6022 and 6024. Clears the PUNCH FLAG flip-flop, transfers AC4—11 contents to the Punch Buffer Register, punches the character, sets the PUNCH FLAG flip-flop when done.

At the same TP3 time, the tape punch logic is prepared for the punch cycle. When the PUNCH SYNC signal is generated at the start of the punch cycle, the tape punch logic asserts the PUNCH DONE signal. This signal lasts for 10 ms, during which time the punch solenoid drivers are activated and the character is punched onto the tape. At the end of the PUNCH DONE signal, the PUNCH FLAG flip-flop is set. If the punch logic has previously been logically connected to the computer interrupt system, the PUNCH FLAG flip-flop asserts the OMNIBUS INT RQST L signal. The computer enters the interrupt servicing routine to determine the identity of the device. The 6021 instruction in the routine causes the computer to proceed to the PC8-E subroutine to service the interrupt request.

SECTION 4 DETAILED LOGIC

2.1 IOT DECODER LOGIC

Figure 2-2 shows the IOT decoder logic. Table 2-1 lists the PC8-E IOT instructions and a description of each. Bits MD3–8 and I/O PAUSE L are gated to produce signals 601X and 602X representing reader and punch IOTs, respectively. Both signals cause the OMNIBUS INTERNAL I/O signal to be asserted, thereby ensuring that the positive I/O bus interface ignores the IOT instruction.

The 601X signal and bits MD9–11 are applied to the BCD-to-Decimal Decoder, E31 (refer to Appendix A, Volume 1, for details); the decoder provides the reader IOT signals, as illustrated. The 602X signal and bits MD9–11 are applied to decoder E27, which provides punch IOT signals; in addition, the 602X signal causes the ENABLE PUNCH BUFFER L signal to be asserted each time a punch IOT is generated.

2.2 TAPE READ LOGIC

The tape read logic is shown in Figure 2-3. This logic generates control basic timing signals in response to an IOT instruction or a signal from the PC04 FEED switch. Assume that the PC04 Reader motor is stopped (either the reader is between blocks of characters or has just been put on-line).

When the tape is stopped, a character is always directly over the PC04 photoarray. (Refer to Paragraph 4.1 of the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* for a detailed description of the tape-feed operation.) When an IOT instruction (6014, for example) is decoded, the control logic first causes the character to be loaded into the RDR Buffer Register by the RDR DATA STROBE signal. It then generates stepping signals that cause the PC04 Reader Motor to turn.

Refer to Figure 2-3. The 6014 L signal sets the RDR RUN flip-flop. Both the CLOCK PULSE L signal and the RDR MOTOR STOPPING L signal are negated at this time; thus, the RDR ENA flip-flop is set via NAND gate E5 (the clock logic is disabled until the ENABLE signal turns it on; the RDR MOTOR STOPPING L signal applies only when the stepping signals are removed). The ENABLE signal generated by the 0-output of the RDR ENA flip-flop initiates both the clock logic and the reader motor control logic. The clock logic first produces a single CLOCK PULSE that is applied to NAND gate E32 and to the C-input of the RDR ENA flip-flop. Because the flip-flop D-input is high at this time, the flip-flop remains set. The NAND gate must be enabled if an RDR DATA STROBE signal is to be generated. The second high input to this NAND gate is produced by either the (A·B) L signal or the ($\overline{A}\cdot\overline{B}$) L signal (one of these two sync signals, generated by the reader motor control logic, is high when the paper-tape holes are directly over the PC04; assume, for this discussion, that (A·B) L is asserted). The negative pulse from E32 sets the R/S flip-flop. The FEED HOLE signal, produced by the PC04 photoarray, enables the 1-output of the R/S flip-flop to activate E23. The negative-going edge of E23's output resets the R/S flip-flop after a small delay determined by the RC network. Consequently, the RDR DATA STROBE signal generated by NOR gate E35 is a narrow pulse (approximately 100-ns wide) and occurs only when the tape-feed hole is over the photoarray. The RDR DATA STROBE signal resets the RDR RUN flip-flop.

After the RDR DATA STROBE signal is generated, the clock logic produces a SHIFT PULSE that causes the reader motor control logic to generate a stepping signal. The tape holes move from over the photoarray; the FEED HOLE signal and the (A·B) L signal are negated. The D-input of the RDR ENA flip-flop is now low. If a 6014 L is not provided before the clock logic generates another CLOCK PULSE, the RDR ENA flip-flop is cleared, initiating a controlled motor-stopping operation. The clock logic is disabled and the reader motor control logic generates a final stepping signal. The reader motor stops and the tape halts with the holes directly over the photoarray. The FEED HOLE signal is again asserted and now the ($\overline{A}\cdot\overline{B}$) L signal is high. The RDR RUN flip-flop can be set by an IOT instruction any time after the RDR ENA flip-flop is cleared. However, the RDR ENA flip-flop can be set again only after a 40-ms delay (the reader motor control logic asserts RDR MOTOR STOPPING L for 40 ms after the RDR ENA flip-flop is cleared).

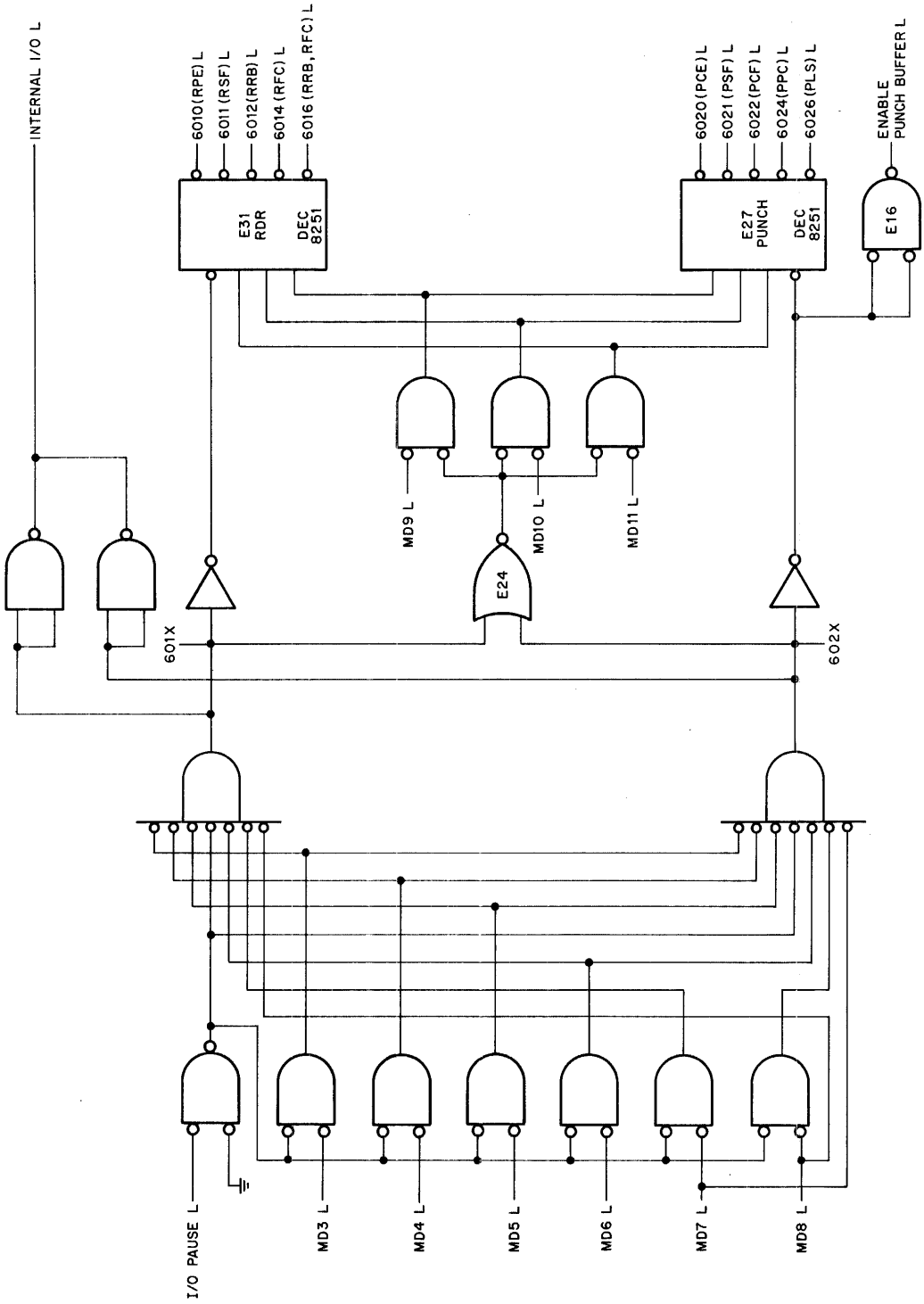


Figure 2-2 IOT Decoder Logic

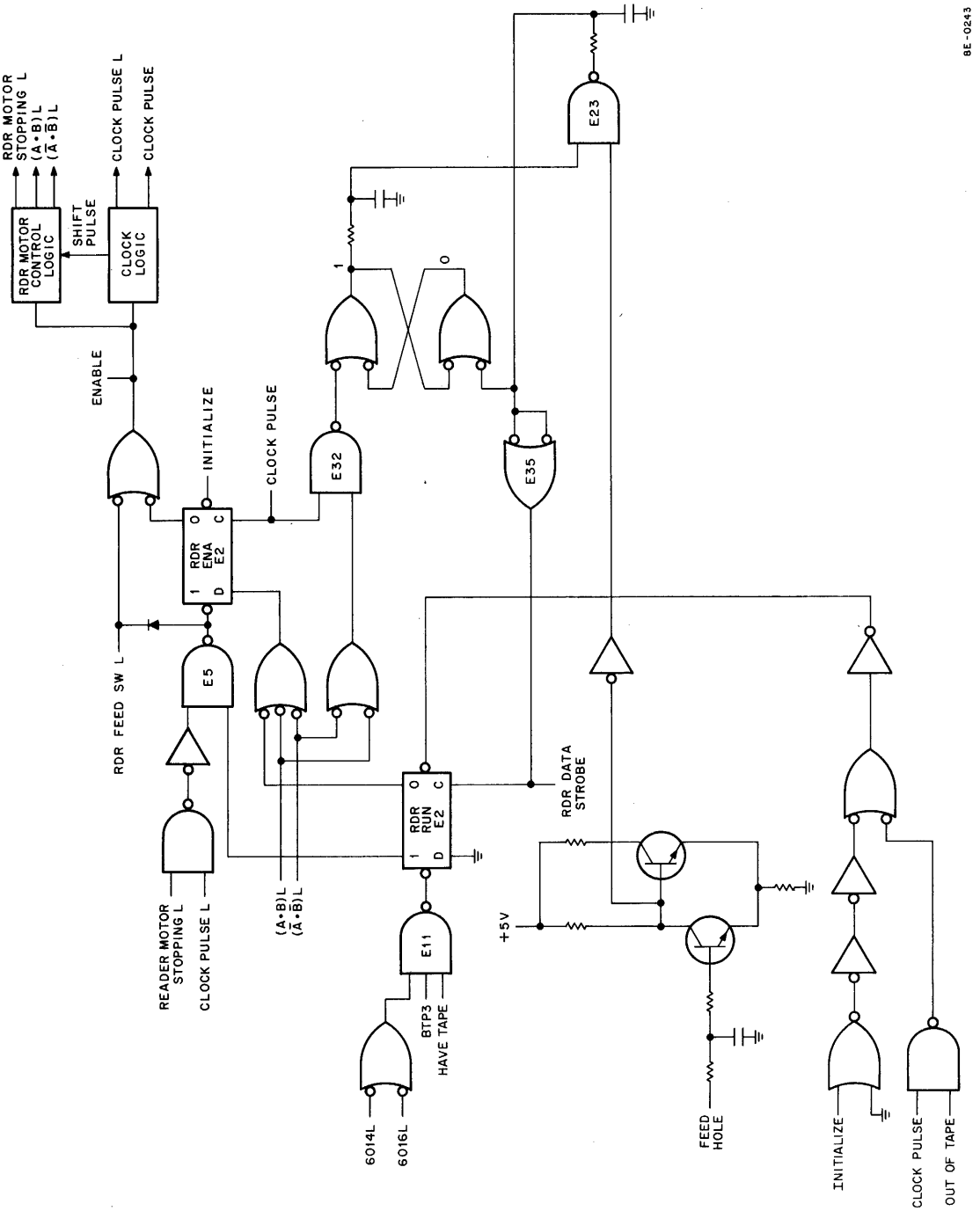


Figure 2-3 Tape Read Logic

If the RDR RUN flip-flop had been set by an IOT instruction before the second CLOCK PULSE occurred, the RDR ENA flip-flop would remain set. The second CLOCK PULSE would then be followed by the second SHIFT PULSE. At this SHIFT PULSE time the $(\overline{A} \cdot \overline{B})$ L and the FEED HOLE signals are asserted. The third CLOCK PULSE causes RDR DATA STROBE to be generated and the RDR RUN flip-flop is again cleared. Thus, a 6014 or 6016 instruction must be decoded at least once for every other clock pulse in order to maintain a 300 character/second rate of operation.

Figure 2-4 is a timing diagram that illustrates the tape read logic signals, as well as those of the reader motor control logic and the clock logic. The first clock period illustrated shows the RDR RUN flip-flop being cleared by an RDR DATA STROBE. A 6014 IOT is decoded before the next CLOCK PULSE. However, between the third and fourth CLOCK PULSES, no IOT is decoded and, therefore, the controlled motor-stopping operation is begun (this is covered fully in Paragraph 2.4).

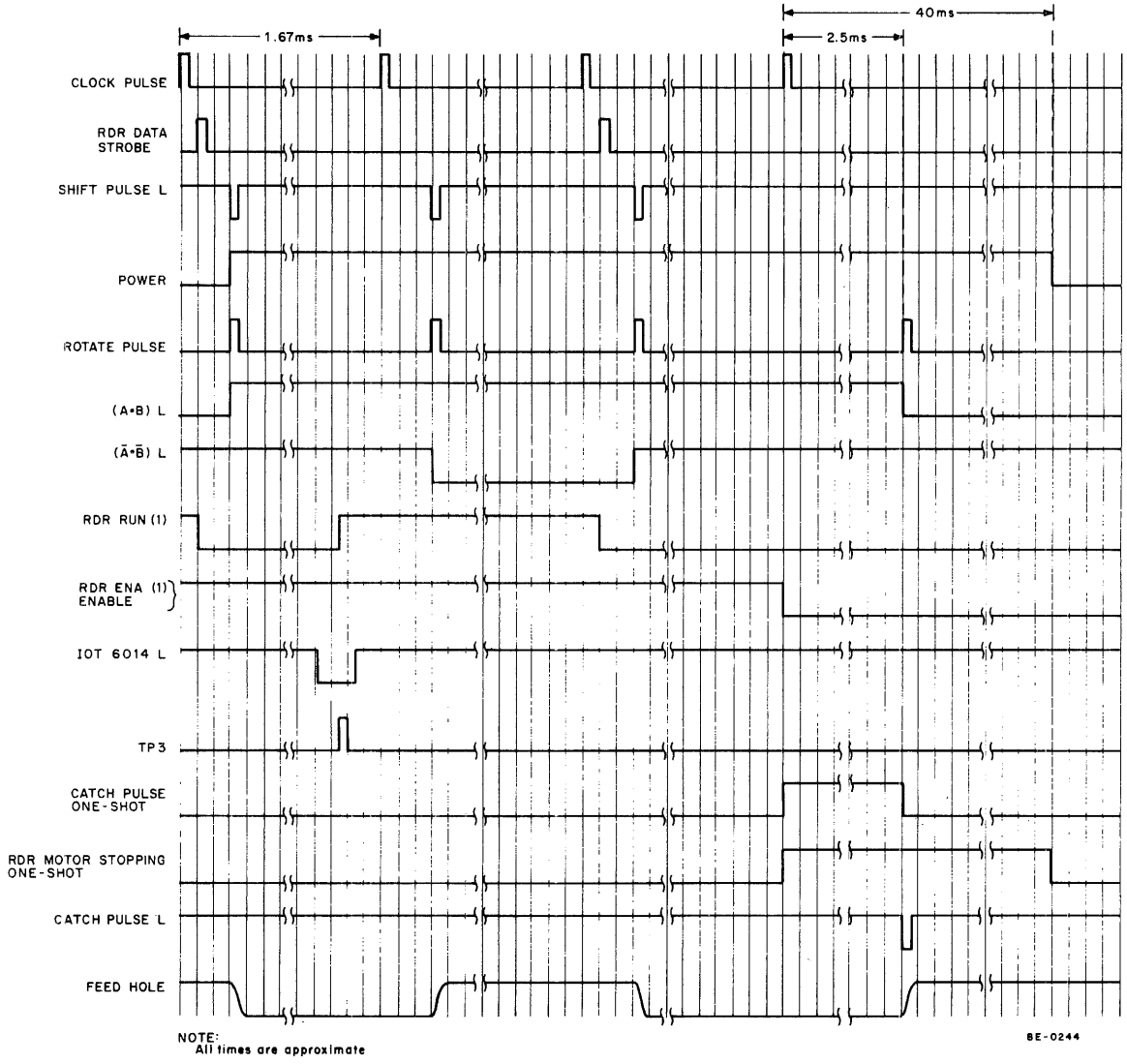


Figure 2-4 Reader Timing

2.3 CLOCK LOGIC

The clock logic is shown in Figure 2-5. The logic consists of a ramp generator, a triggered free-running multivibrator, and two pulse-forming delay networks.

During continuous operation, the reader motor is stepped once every 1.67 ms. However, when the motor must be started from a dead stop, the inertia of the motor and the tape drive wheel must be overcome. Initially, the shaft turns more slowly, and, consequently, the tape moves over the photoarray more slowly than at continuous operating speed. With each step of the motor the speed of the tape approaches continuous operating speed. In order to maintain a nearly constant ratio of tape speed to CLOCK PULSE frequency, the ramp generator, which includes transistors Q1 and Q2, is used.

When the ENABLE signal is asserted by the tape read logic, the free-running multivibrator, Q4/Q5, is triggered on via Q3. At the same time, the ramp generator is triggered. The emitter of Q2 provides the charging potential for the multivibrator. This potential is initially such that the first CLOCK PULSE period is 5 ms. The emitter potential of Q2 rises at a rate determined by the RC time constant, which can be varied by R27 (refer to Paragraph 5.3.8 of the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* for adjustment procedures). As the potential rises, the capacitors in the base circuits of Q4 and Q5 take less time to charge. Thus, the on/off cycle of Q4 and Q5 decreases. Ultimately, when the ramp has ended, the CLOCK PULSE period is 1.67 ms.

The method used to generate the SHIFT PULSE L signal and the CLOCK PULSE signal is illustrated in Figure 2-6. The RC delay circuits are used extensively in the control logic. Because the circuit in Figure 2-5 is more detailed than others, it has been selected as an example of the technique. The timing diagram is mainly self-explanatory. The RC delays indicated can be roughly calculated by using the formula Delay = 0.7 RC.

2.4 READER MOTOR CONTROL LOGIC

The reader motor control logic is shown in Figure 2-7. (Refer to Paragraph 4.1.1 of the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* for a detailed description of how the reader motor control logic stepping signals control the reader motor.) When the ENABLE signal is asserted by the tape read logic, the two one-shot multivibrators, E4 and E7, are readied for triggering. During continuous operation, the clock logic generates SHIFT PULSEs, the first of which sets the PWR flip-flop, thereby asserting the POWER signal. Each SHIFT PULSE L signal generates a ROTATE PULSE that clocks the A/B end-around shift register. At every other ROTATE PULSE either the $(A \cdot B)$ L signal or the $(\overline{A} \cdot \overline{B})$ L signal is asserted, indicating to the tape read logic that a character is over the photoarray.

If, as explained in Paragraph 2.2, the RDR ENA flip-flop is cleared, the ENABLE signal is negated (provided the reader FEED switch is not activated). The down-going edge of the ENABLE signal triggers E4 and E7 (Figure 2-4). After 2.6 ms, E4 times out and a CATCH PULSE L signal is generated. This pulse produces the ROTATE PULSE that steps the motor a final time. The motor stops with either $(A \cdot B)$ L or $(\overline{A} \cdot \overline{B})$ L asserted and the FEED HOLE signal high.

The E7 one-shot remains set for 40 ms before timing out. During this 40-ms period, the RDR MOTOR STOPPING L signal is asserted and prevents the RDR ENA flip-flop from being set. At the end of the period, the 0-output of E7 clears the PWR flip-flop, negating the POWER signal. Reader operation can be restarted by again setting the RDR ENA flip-flop.

The 40-ms delay provided by E7 ensures that the motor, if not pulsed for continuous operation, has sufficient time to come to a complete stop before it is activated again. If the complete stop were not allowed, undesirable oscillations in the drive motor would result, causing possible false data outputs.

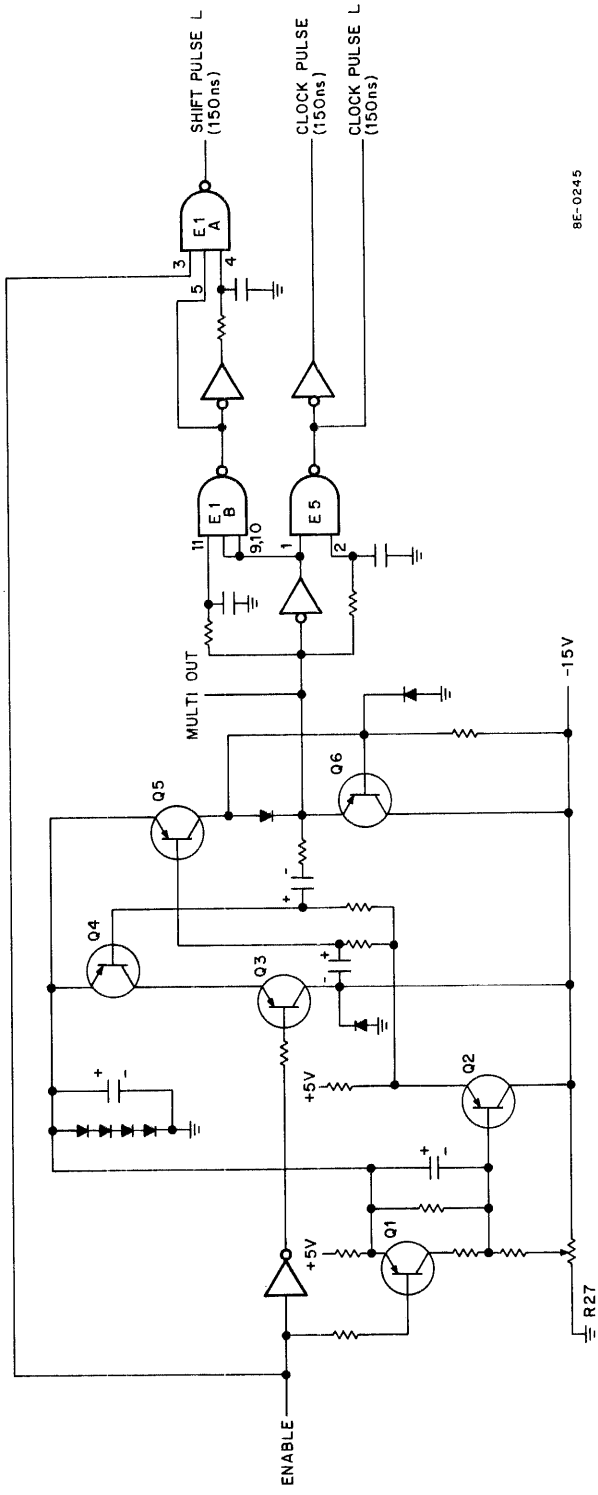


Figure 2-5 Clock Logic

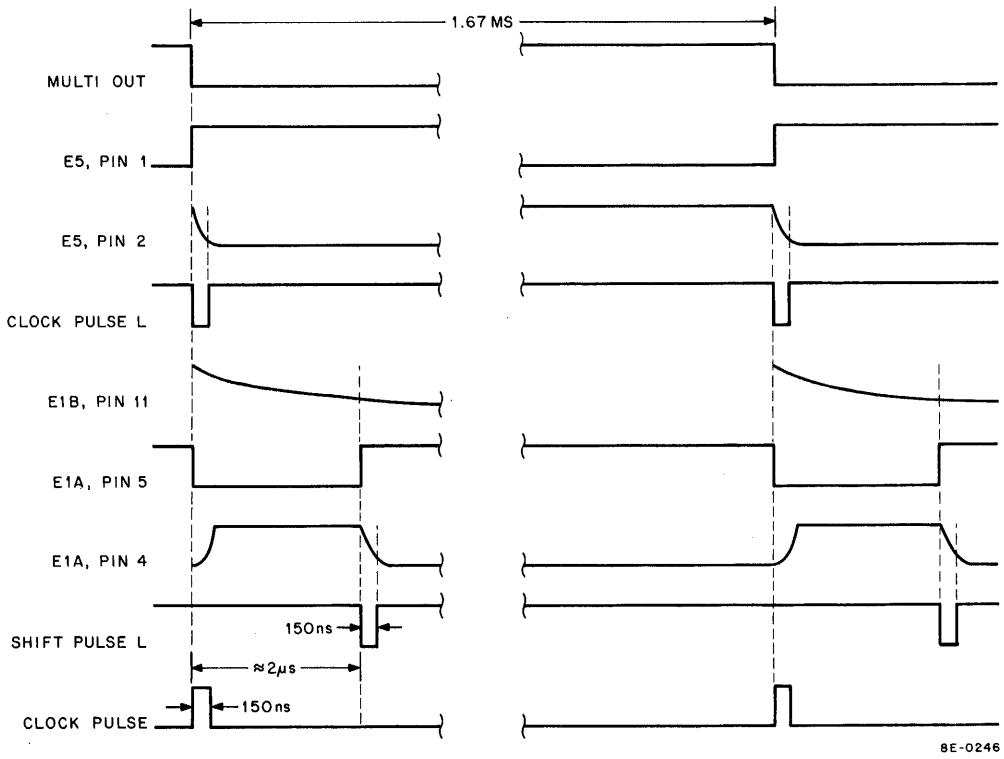


Figure 2-6 Clock/Shift Pulse Timing

2.5 RDR INT/SKIP LOGIC

The RDR INT/skip logic is shown in Figure 2-8. When an RDR DATA STROBE signal is generated it sets the RDR FLAG flip-flop (the RDR RUN flip-flop provides the necessary high at E12's D-input before being cleared, itself, by RDR DATA STROBE). Because RDR DATA STROBE also loads the RDR Buffer Register, the RDR FLAG flip-flop being set indicates that the control is ready to transfer data. If the INT ENA flip-flop has been set previously, either under program control or by INITIALIZE, the OMNIBUS INT RQST L signal is asserted. When the computer enters the PC8-E servicing subroutine, an appropriate IOT instruction reads the Buffer Register and clears the RDR FLAG flip-flop via NOR gate E1.

2.6 RDR BUFFER LOGIC

The reader buffer logic is shown in Figure 2-9. Data supplied on the READ HOLE 1–8 lines is clocked into the register by the RDR DATA STROBE signal. Either 6012 L or 6016 L gates the character onto the OMNIBUS DATA 4–11 lines. At the same time, the IOT instruction asserts the OMNIBUS C1 L signal, resulting in an ORing of the DATA 4–11 bits and the CPU AC Register contents.

2.7 TAPE STATUS LOGIC

The tape status logic is shown in Figure 2-10. The logic monitors both the FEED HOLE signal and the RDR ENA flip-flop, generating an OUT OF TAPE signal when tape is not loaded in the PC04 Tape Feeder. This signal ensures that the tape read logic cannot be triggered by a program instruction read command. The complementary signal, HAVE TAPE, is generated when tape is in the feeder, enabling the tape-feed operation to begin when program-directed.

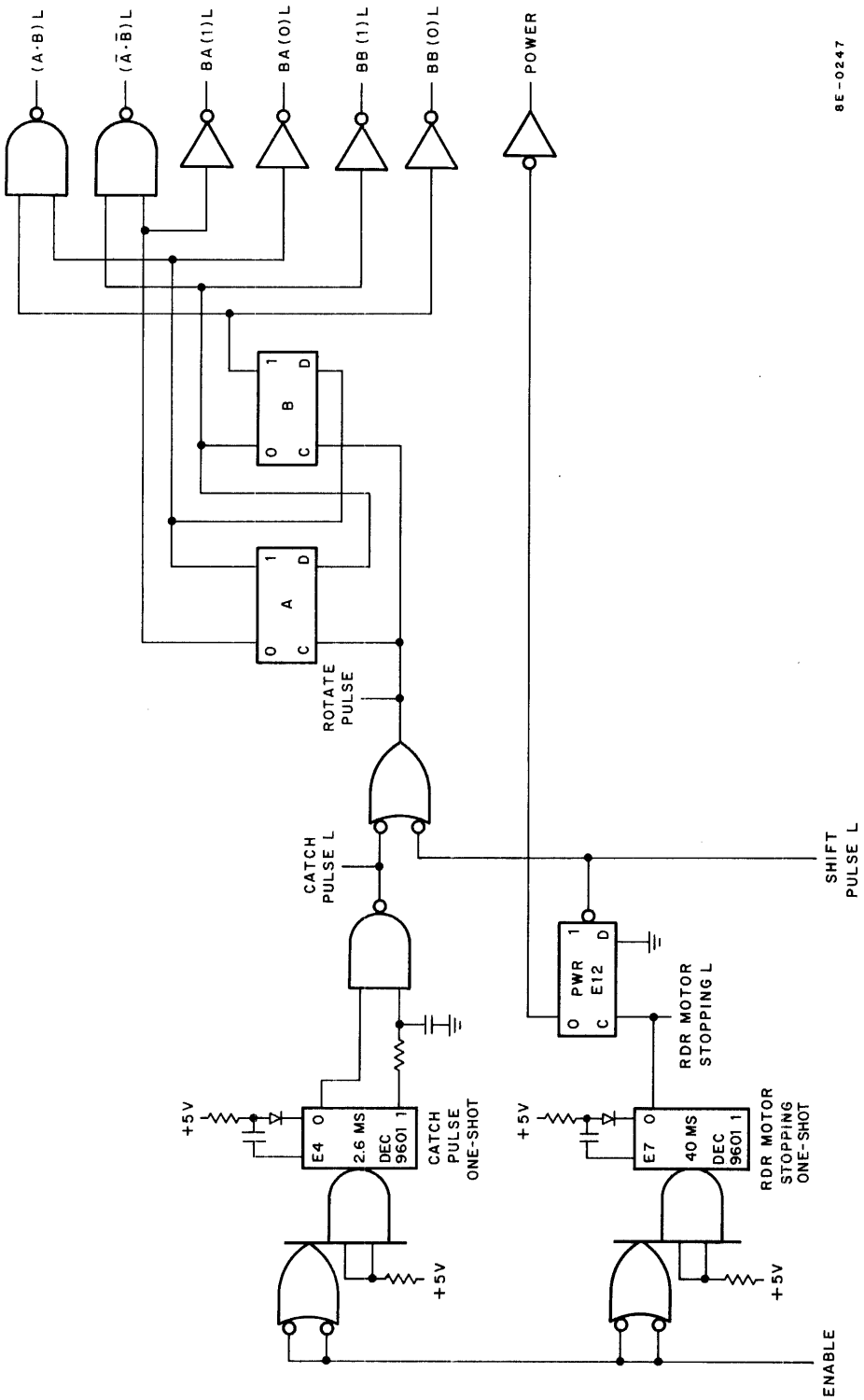


Figure 2-7 Reader Motor Control Logic

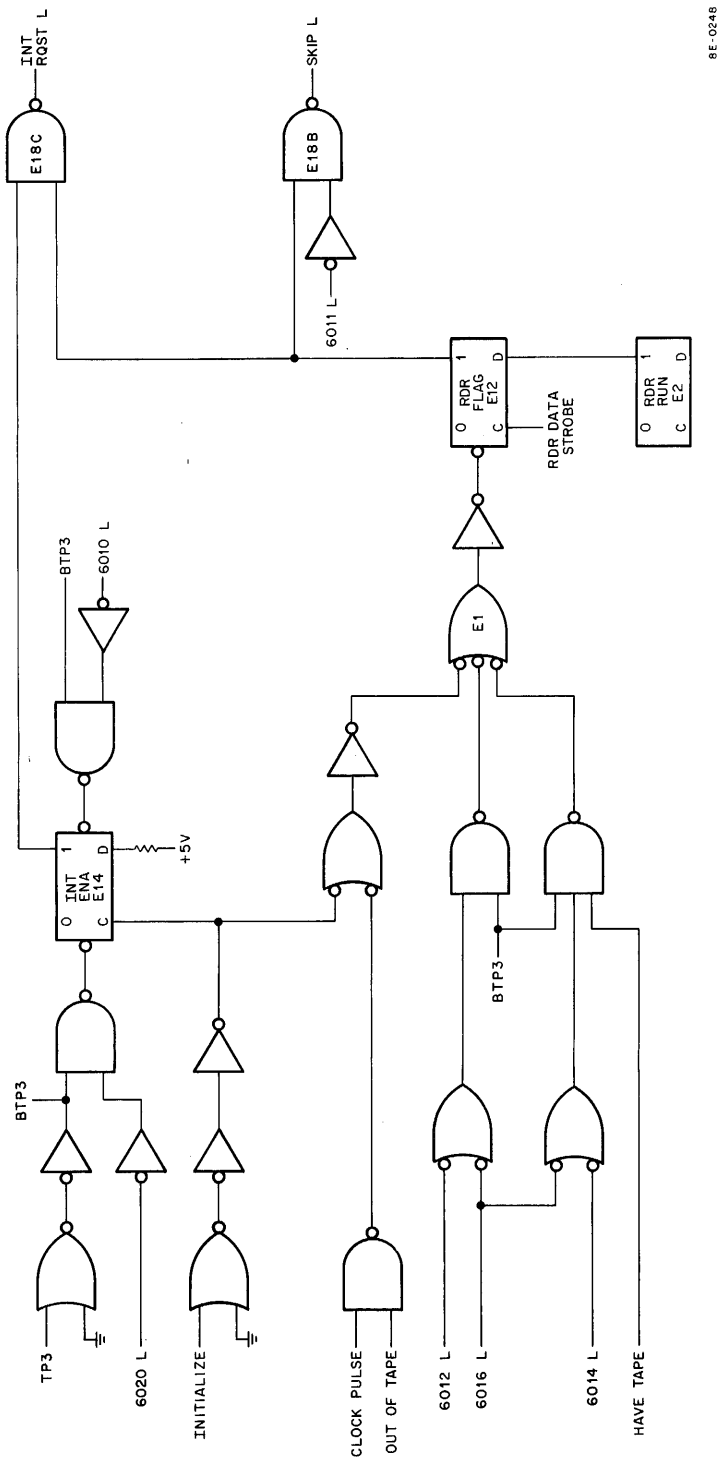


Figure 2-8 RDR INT/Skip Logic

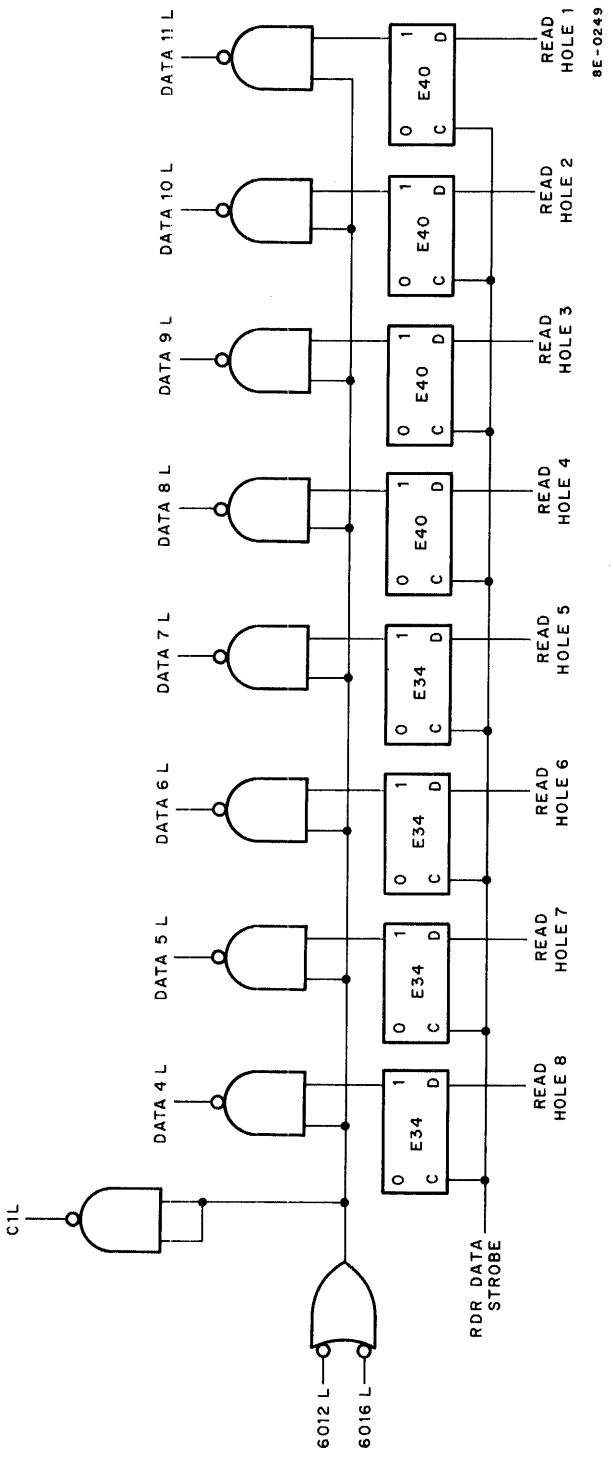


Figure 2-9 Reader Buffer Logic

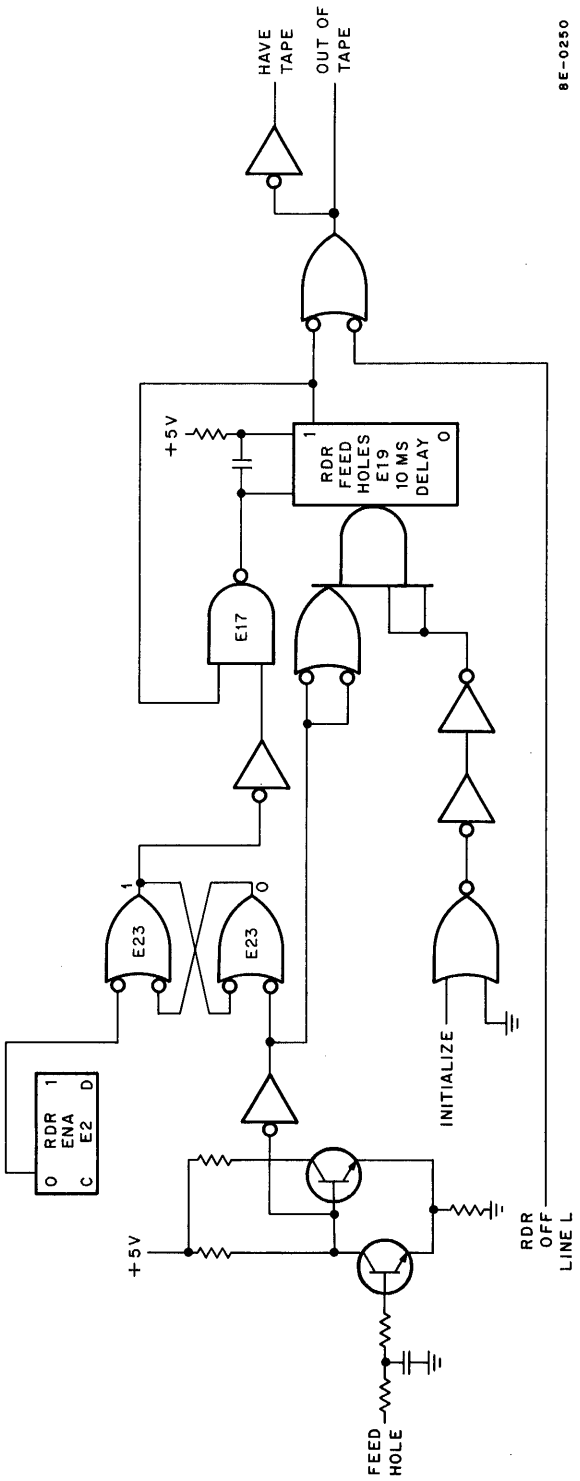


Figure 2-10 Tape Status Logic

If no tape has been inserted in the feeder, the FEED HOLE signal is high, just as it is when an actual feed hole is detected by the photoarray. The RDR FEED HOLES one-shot, E19, is in its stable state; thus, the OUT OF TAPE signal is asserted. If a read command is issued by the program, the RDR RUN flip-flop (Figure 2-3) is prevented from being set by the HAVE TAPE signal that is low at this time. Therefore, the RDR ENA flip-flop is not set and the clock logic is not triggered.

When a tape is inserted in the feeder, the photoarray light source rays are interrupted briefly by the tape web. The FEED HOLE signal goes low, and the negative-going edge causes one-shot E19 to be triggered; thus, the HAVE TAPE signal is asserted. At the same time that E19 is triggered, the flip-flop consisting of the cross-coupled NOR gates is cleared. Because the RDR ENA flip-flop is also clear, flip-flop E23 is latched in the clear state. NAND gate E17 is enabled; the resulting low at pin 11 of E19 holds the one-shot in the triggered state, i.e., the 1-output stays high. The HAVE TAPE signal remains high indefinitely, if the program does not issue a read command.

When a read command is issued, the RDR RUN flip-flop is set, causing the RDR ENA flip-flop to be set, also. The 0-output of the RDR ENA flip-flop triggers the clock logic, which generates a CLOCK PULSE, and sets flip-flop E23, which disables NAND gate E17. The one-shot enters the timeout state, during which it can be re-triggered by each trailing edge of the FEED HOLE signal. A ROTATE PULSE, generated by the clock logic approximately 2 μs after the CLOCK PULSE (Figure 2-4), causes the tape to begin feeding through the read station. The resulting negative transition of the FEED HOLE signal re-triggers the one-shot (note that flip-flop E23 is held in the set state by the 0-output of the RDR ENA flip-flop). If another trailing edge occurs within 10 ms, the one-shot is again re-triggered (a 10-ms period is necessary because the reader motor is being started from a dead stop and, consequently, the tape moves more slowly than at continuous operating speed; in continuous operation, a trailing edge occurs at 3.34-ms intervals). If the program issues read commands at such a rate that continuous operation results (at least one command between each RDR DATA STROBE and the next CLOCK PULSE), one-shot E19 is re-triggered continuously, and the HAVE TAPE signal remains asserted.

Suppose that at some point during this continuous operation a read command is not issued within approximately 3.34 ms of the preceding command. In such a situation, the motor-stopping operation is initiated. At the moment this operation begins, the RDR ENA flip-flop is cleared, and the FEED HOLE signal is low. Therefore, flip-flop E23 is again latched in the clear state, and one-shot E19 is held in its triggered state. The HAVE TAPE signal remains high while the motor is stopped.

If read commands are issued at a continuous rate and the tape runs out of the tape feeder, the OUT OF TAPE signal must be asserted. When the last portion of tape web uncovers the light source, the FEED HOLE signal goes high and remains high. One-shot E19 times out approximately 8.5-ms later, and the OUT OF TAPE signal goes high. During this 8.5-ms period, three RDR DATA STROBE pulses occur. Each of these pulses loads the Reader Buffer with 1s. Consequently, at least two transfers, possibly three, of 1s to the AC Register take place before the RDR RUN flip-flop is cleared and the clock logic is disabled.

2.8 TAPE PUNCH LOGIC

When the punch ON/OFF switch is in the ON position, the punch motor runs continuously. A tape that is loaded in the punch feeder mechanism can be punched if the FEED switch is in the FEED position, or if the program issues a punch command IOT instruction, 6024 or 6026. Either method results in the PUNCH DONE signal being generated in the tape punch logic (Figure 2-11).

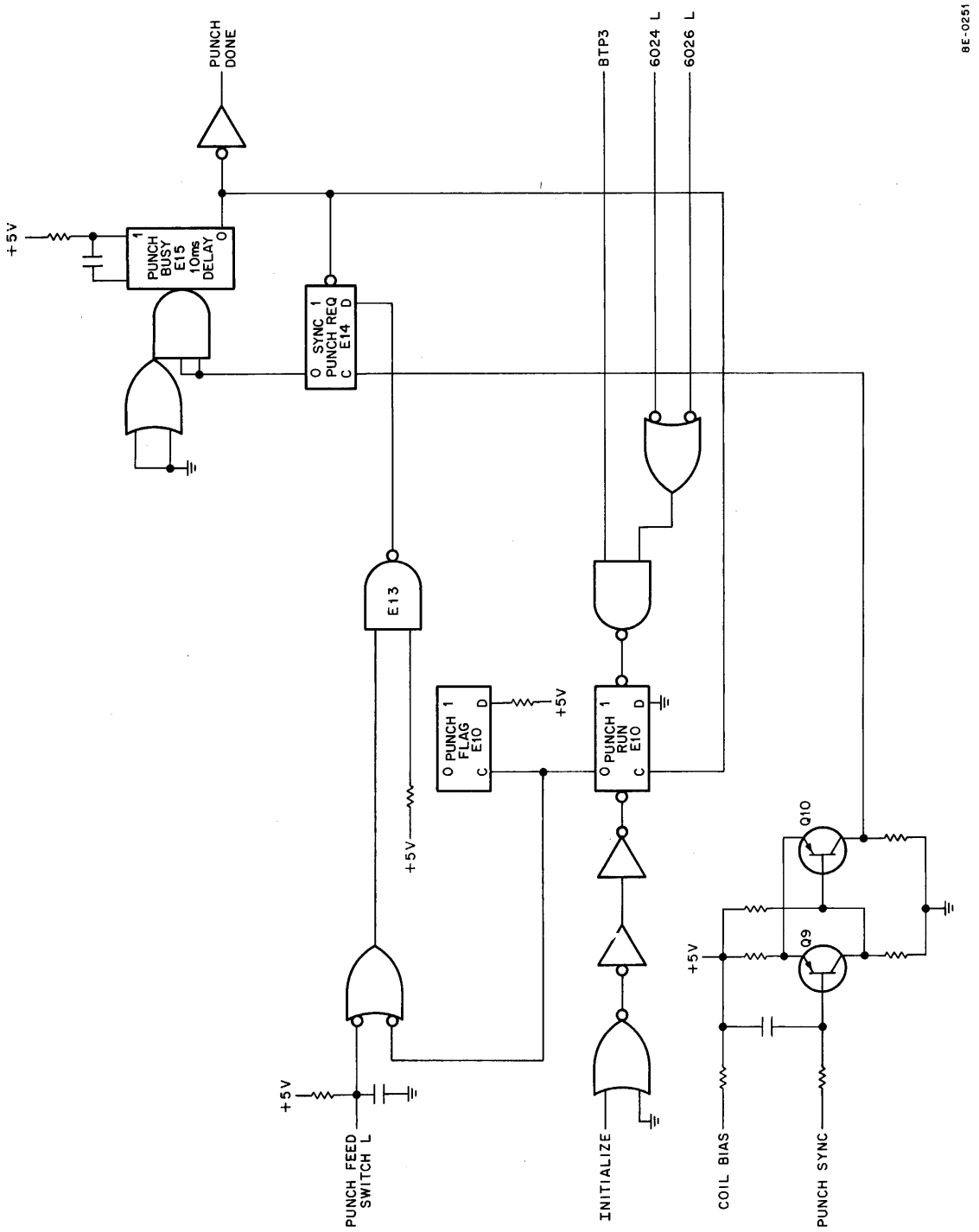


Figure 2-11 Tape Punch Logic

When the 6026 IOT instruction is issued, for example, the PUNCH RUN flip-flop, E10, is set. Setting E10 causes the D-input of the SYNC PUNCH REQ flip-flop, E14, to go low. A PUNCH SYNC signal from the tape punch mechanism can clear E14, thereby triggering the PUNCH BUSY one-shot, E15. This PUNCH SYNC signal occurs once during each punch motor revolution and signals the start of the punch mechanical cycle. The signal is applied to the Schmitt trigger, Q9 and Q10, and the output at the collector of Q10 clears E14. The resulting 10-ms PUNCH DONE signal enables the PC04 solenoid drivers to activate the punch mechanism. The tape is punched with the character that was placed on the HOLE 1–8 lines by the punch buffer logic, shown in Figure 2-12 and discussed briefly in Paragraph 2.9.

2.9 PUNCH BUFFER LOGIC

The punch buffer logic is shown in Figure 2-12. Either the 6024 L signal or the 6026 L signal enables the Buffer Register to be loaded at TP3 time with the information carried on the DATA 4–11 lines. This information is then gated to the HOLE 1–8 lines, respectively. Note that the information loaded at this time remains in the register until another punch instruction is issued or until the FEED switch is activated.

2.10 INT/SKIP LOGIC

After the tape has been punched and the punch mechanical cycle ends, the PUNCH BUSY one-shot times out. The PUNCH RUN flip-flop is cleared and the 0-output of the flip-flop sets the PUNCH FLAG flip-flop (Figure 2-13). If the INT ENA flip-flop, E14, is set at this time, the OMNIBUS INT RQST L signal is asserted. The computer enters the interrupt routine and proceeds from there to the punch subroutine.

SECTION 5 MAINTENANCE

Refer to Volume 1 and the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* for PC8-E maintenance information.

Table 2-2 presents cable and connector pin assignments for the two cables that connect the control and the PC04.

SECTION 6 SPARE PARTS

Table 2-3 lists recommended spare parts for the PC8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

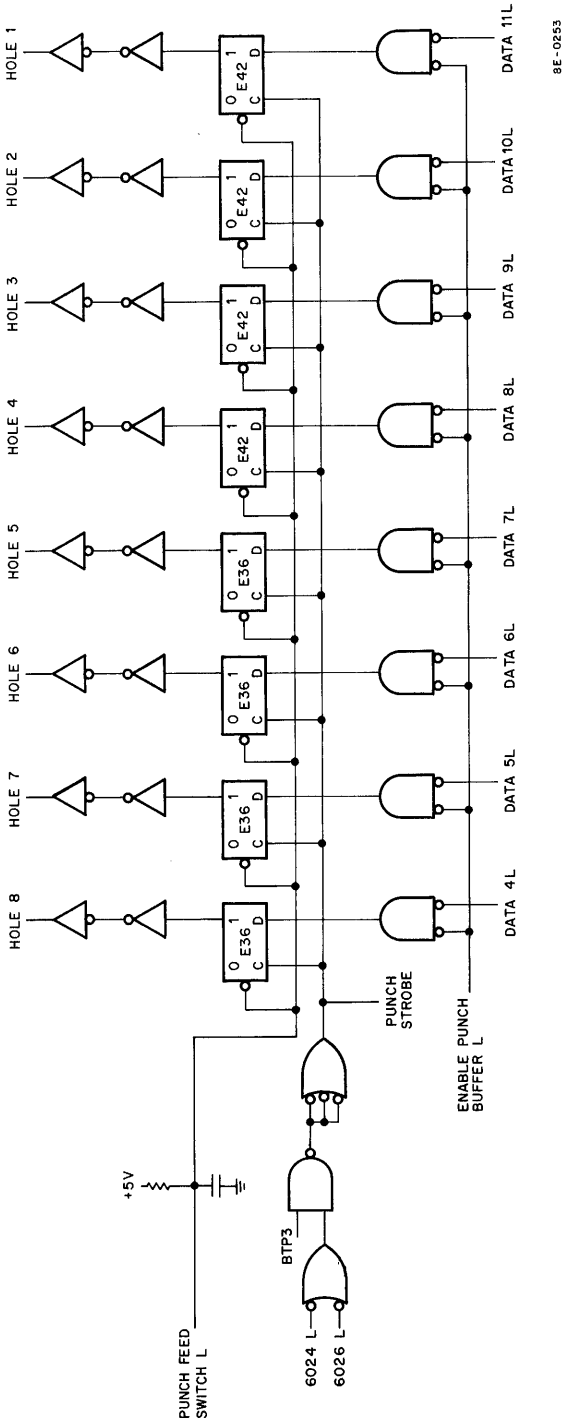


Figure 2-12 Punch Buffer Logic

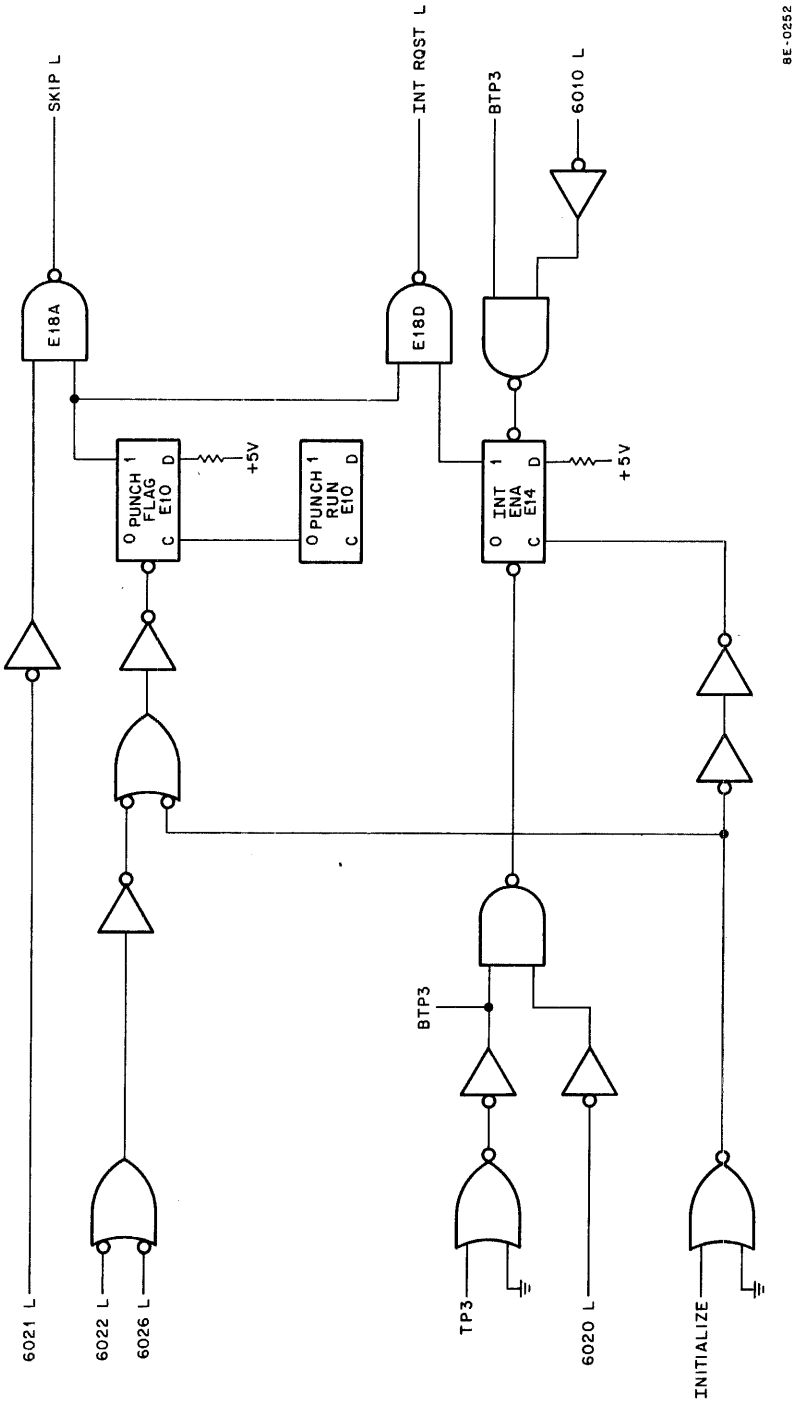


Figure 2-13 Punch INT/Skip Logic

Table 2-2
Cable/Connector Pin Assignments

Control Connector Pin	Signal Name		M955 Connector Pin
	J1 (Connects to B1)	J2 (Connects to A1)	
D	PUNCH FEED SWITCH	N/C	A
F	SCR ACTIVE	RDR ON/OFF LINE	B
J	PUNCH SYNC	GND	C
L	N/C	READ HOLE 1	D
N	PUNCH DONE	READ HOLE 2	E
R	PUNCH NOT UP TO SPEED	READ HOLE 3	F
T	HOLE 8	READ HOLE 4	H
V	HOLE 7	READ HOLE 5	J
X	HOLE 6	READ HOLE 6	K
Z	HOLE 5	READ HOLE 7	L
BB	COIL BIAS	READ HOLE 8	M
DD	HOLE 4	FEED HOLE	M
FF	HOLE 3	BA (0)	P
JJ	HOLE 2	BA (1)	R
LL	HOLE 1	BB (0)	S
NN	N/C	BB (1)	T
RR	N/C	POWER	U
TT	N/C	RDR FEED SWITCH	V
GND PINS A, B, C, E, H, K, M, P, S, U, W, Y, AA, CC, EE, HH, KK, MM, PP, SS, UU, VV			

Table 2-3
PC8-E Recommended Spare Parts

DEC Part Number	Description	Quantity
19-05547	IC DEC 7474	1
19-05575	IC DEC 7400	2
19-05576	IC DEC 7410	1
19-09486	IC DEC 384	1
19-09487	IC DEC 9601	1
19-09686	IC DEC 7404	2
19-09971	IC DEC 6380	1
19-09972	IC DEC 6314	1
19-09973	IC DEC 97401	1
19-09594	IC DEC 8251	1
19-05579	IC DEC 7440	1
19-10087	IC DEC MC4015P	1
15-03409	Transistor, 6543 D	1
15-09338	Transistor, PMS 6531	1
11-00113	Diode, D662	1
11-00114	Diode, D664	2
10-01610	Capacitor, 0.01 μF, 100V, 20%	2

PART 3
X/Y PLOTTER

CHAPTER 3
XY8-E PLOTTER CONTROL

SECTION 1 INTRODUCTION

The XY8-E Plotter Control interfaces a digital incremental plotter with the PDP-8/E. The XY8-E operates with a variety of plotters, both encoded and unencoded types, to display data on paper or film. All XY8-E logic is contained on a single quad module that plugs into the OMNIBUS. The XY8-E connects to the incremental plotter with a signal cable that is supplied.

The XY8-E transmits directions to the plotter that originate in the computer AC Register. Data is transferred in six parallel bits that cause pen or drum movement (the plotter can be either a drum or flatbed type) in the plotter. All plotter operations, except the setting of the coordinates at which plotting begins, are guided by the XY8-E logic and the CPU. A series of functions, specified by IOT instructions, initialize the XY8-E logic, initiate plotter operation, and generate program interrupts to indicate completion of the operation.

The XY8-E will interface readily with any of the following incremental plotters:

a. CalComp Plotters – Series 500, 600, 700, and 800.
b. Houston Instruments Plotters – Types 6400, DP-1, and DP-10.

Four Plotter Control/plotter systems, featuring plotters from those listed, are offered by DEC. Details concerning installation, operation, troubleshooting, and maintenance of these plotters can be found in the respective CalComp or Houston Instruments instruction manual. DEC publications and documents relevant to the XY8-E are:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* – DEC, 1972
b. *PDP-8/E Maintenance Manual, Volume 1*
c. XY8-E Plotter Control and Display Diagnostic, MAINDEC-8E-D6AB
d. DEC Engineering Drawing, Plotter Control, E-CS-M842-0-1.

SECTION 2 INSTALLATION

The XY8-E Plotter Control is installed on site by DEC Field Service personnel. Customers should *not* attempt to unpack, inspect, install, checkout, or service the equipment.

Insert the XY8-E Control Module in the PDP-8/E OMNIBUS. Refer to Table 2-3, Volume 1, for information concerning recommended module priorities (the XY8-E is a "non-memory" option).

Connect the Plotter Control to the plotter with the signal cable provided (if the plotter is one of those listed in Section 1). If the plotter is an unencoded type, J2 of the Plotter Control, a 40-pin Berg Connector, connects to the plotter 19-pin Cannon Plug; if the plotter is an encoded type, J1 of the Plotter Control connects to the plotter Cannon Plug (refer to Section 5 for cable and connector pin assignments).

The XY8-E can be checked for correct operation by running the diagnostic program, MAINDEC-8E-D6AB. Refer to the plotter instruction manual for checkout procedures for the plotter itself.

SECTION 3 BLOCK DIAGRAM

Figure 3-1 is a block diagram of the XY8-E Plotter Control. Programmed IOT instructions are decoded by the IOT decoder logic. Signals representing the IOT instructions are then applied to the timing logic, the interrupt/skip logic, and the direction transfer logic.

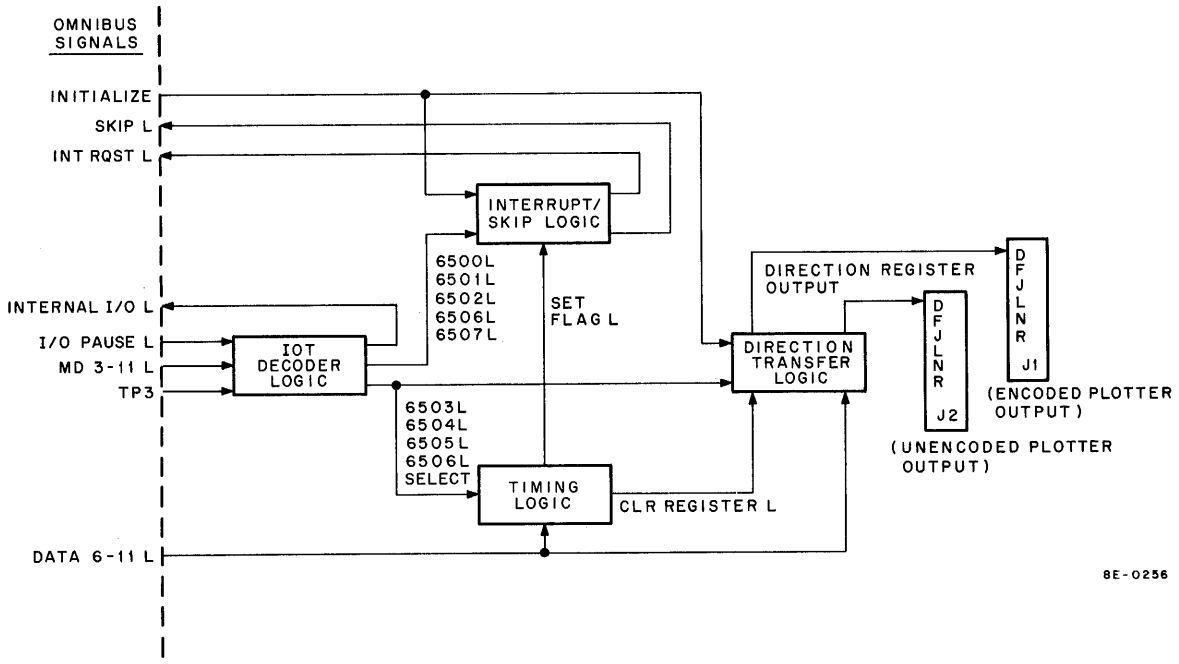


Figure 3-1 XY8-E Block Diagram

Plotter directions are gated from the AC Register via the DATA 6–11 lines to a 6-bit Decision Register in the direction transfer logic. The Direction Register outputs are transferred to the plotter, which begins the directed operation. At the same time, the timing logic is triggered; after a delay period the timing logic generates a signal, CLR REGISTER L, that clears the Direction Register, readying it for the next direction. After a further delay period that ensures completion of the direction by the plotter, the timing logic generates the SET FLAG L signal. This signal is applied to the interrupt/skip logic where it sets the PLOTTER FLAG flip-flop. This action causes the Plotter Control to request a program interrupt, resulting in the transfer of another direction from the AC Register.

SECTION 4 DETAILED LOGIC

3.1 IOT DECODER LOGIC

The IOT decoder logic is shown in Figure 3-2. The I/O PAUSE L signal gates bits MD3—8 to generate the SELECT signal that indicates an XY8-E instruction has been decoded. See Table 3-1 for the XY8-E instruction list and a description of each instruction.

Table 3-1
XY8-E IOT Instruction List

Octal Code	Mnemonic	Function
6500	PLCE	Clear the INT ENA flip-flop.
6501	PLSF	Skip on the Plotter flag. Senses the state of the PLOTTER FLAG flip-flop. If the flip-flop is set, the program counter is incremented so that the next sequential instruction is skipped.
6502	PLCF	Clear the PLOTTER FLAG flip-flop.
6503	PLPU	Pen up. Raises the plotter pen from the surface of the graph paper (unencoded plotters only).
6504	PLLR	Load Direction Register, clear Direction Register, set Plotter flag. Loads the Direction Register from AC06—11 (see Table 3-2 for the list of directions), clears the register after the plotter has had enough time to carry out the direction, sets the PLOTTER FLAG flip-flop.
6505	PLPD	Pen down. Lowers the pen to the surface of the graph paper (unencoded plotters only).
6506	PLCF, PLLR	Microprogram of 6502 and 6504. Clears the PLOTTER FLAG flip-flop, loads the Direction Register, clears the Direction Register, sets the PLOTTER FLAG flip-flop.
6507	PLSE	Set the INT ENA flip-flop.

The SELECT signal asserts the OMNIBUS INTERNAL I/O L signal that directs the positive I/O bus interface to ignore the IOT instruction; also, it gates bits MD9—11 to provide inputs for E21, the BCD-to-decimal decoder (see Appendix A, Volume 1, for details). With one exception, E21 provides the signals that represent the XY8-E IOT commands. The exception is the signal that represents the 6501 instruction, Skip on the Plotter Flag. Note that the IOT signals generated by E21 are produced at TP3 time. However, the OMNIBUS SKIP L signal is sampled at TP3 time by the CPU skip logic. Therefore, the XY8-E Plotter Control must assert the SKIP L signal before TP3 time; this is the reason for generating the 6501 L signal separately.

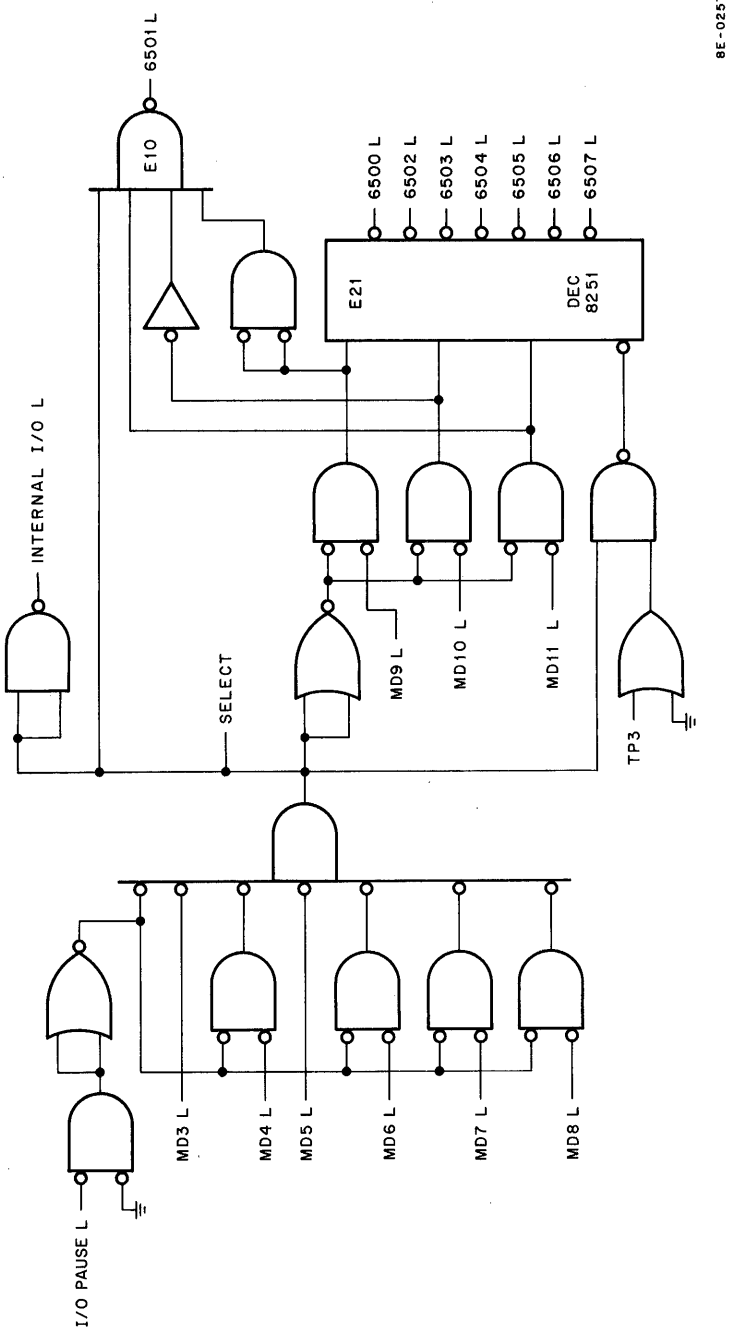


Figure 3-2 IOT Decoder Logic

3.2 TIMING LOGIC

The timing logic is shown in Figure 3-3. This logic generates delay periods that allow the plotter to carry out the direction contained in the Direction Register. The delay periods are initiated simultaneously with the loading of the Direction Register. When the first delay ends, the Direction Register is cleared; when the second delay ends, the PLOTTER FLAG flip-flop is set. Then, if the XY8-E is logically connected to the computer interrupt system, a program interrupt is requested and another direction is transferred from the AC Register to the Direction Register.

Three one-shot multivibrators are shown in Figure 3-3. For directions other than Pen Up/Pen Down, only one-shots E1 and E7 are triggered. Either the 6504 L or the 6506 L signal, in addition to clocking the Direction Register, triggers both E1 and E7. The plotter begins the directed operation and the direction remains in the Direction Register for 3.3 ms (an arbitrary but optimal period of time). At this time, E1 times out and the CLR REGISTER L signal is asserted. This signal is applied to the direction transfer logic and clears the Direction Register. E7 times out after 7.5 ms (more than enough time for the plotter to carry out the mechanical operation), causing the SET FLAG L signal to be asserted. This signal is applied to the interrupt/skip logic, Figure 3-6, where it sets the PLOTTER FLAG flip-flop.

If the direction to be carried out by the plotter is either Pen Up or Pen Down, the third one-shot, E4, is triggered. This situation is illustrated by the timing diagram, Figure 3-4. The timing shown applies to an encoded plotter. However, an unencoded plotter could be represented by replacing the 6504 L/6506 L signal with either 6503 L or 6505 L. If the Pen Up direction is to be carried out by an encoded plotter, for example, AC Register bits 6—11 must be loaded with octal code 31 (Table 3-2). This code is placed on the DATA 6—11 lines and loaded into the Direction Register by the leading edge of the 6504 L/6506 L signal. At the same time, NAND gate E3A, Figure 3-3, is enabled, and both E1 and E7 are triggered. DR11 is set, enabling NOR gate E3B to trigger one-shot E4. As before, the CLR REGISTER L signal is asserted after 3.3 ms. However, the SET FLAG L signal, rather than occurring after 7.5 ms, is delayed for 72.7 ms. This period of time is required to satisfy the plotter's pen stabilizing time. Note that one-shot E7 is superfluous in this operation.

If the Pen Up instruction, 6503, is issued for an unencoded plotter, E4 is triggered in essentially the same way as for the encoded plotter. The 6503 L signal dc-sets DR11. NOR gate E3 is enabled, triggering E4 which, in turn, triggers E1 (E7 is not triggered in this situation). The two delays generated carry out their respective functions as detailed earlier.

3.3 DIRECTION TRANSFER LOGIC

The direction transfer logic is shown in Figure 3-5. Directions are placed on the DATA 6—11 lines from the AC Register by IOT instruction 6504 or 6506. At TP3 time, the 6504 L signal or the 6506 L signal loads the Direction Register. Separate transistor driver outputs are provided for encoded and unencoded plotters; unencoded outputs undergo a transition from -15V to +5V, while encoded outputs go from ground to +15V. The Direction Register is cleared by the INITIALIZE signal that is asserted both at power turn-on and by the CAF (6007) instruction.

3.4 INTERRUPT/SKIP LOGIC

The interrupt/skip logic is shown in Figure 3-6. The Plotter Control is logically connected to the computer interrupt system when the INT ENA flip-flop is set. The flip-flop is set under program control by the 6507 (PLSE) IOT instruction or by the 6007 (CAF) IOT instruction that asserts the INITIALIZE signal; in addition, the INITIALIZE signal sets the flip-flop at power turn-on. The XY8-E is disconnected from the interrupt system by the 6500 (PLCE) IOT instruction that clears the flip-flop under program control.

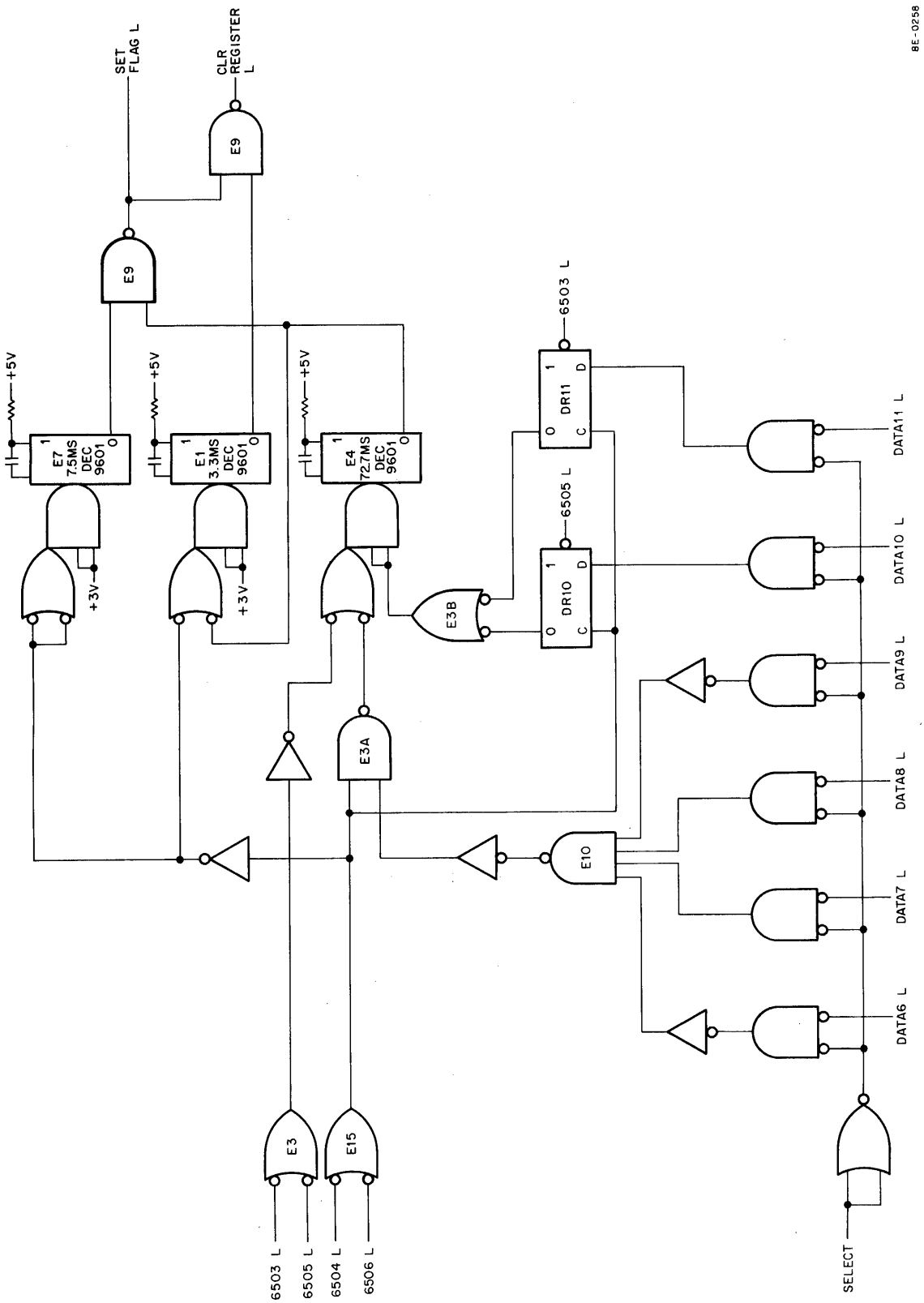


Figure 3-3 Timing Logic

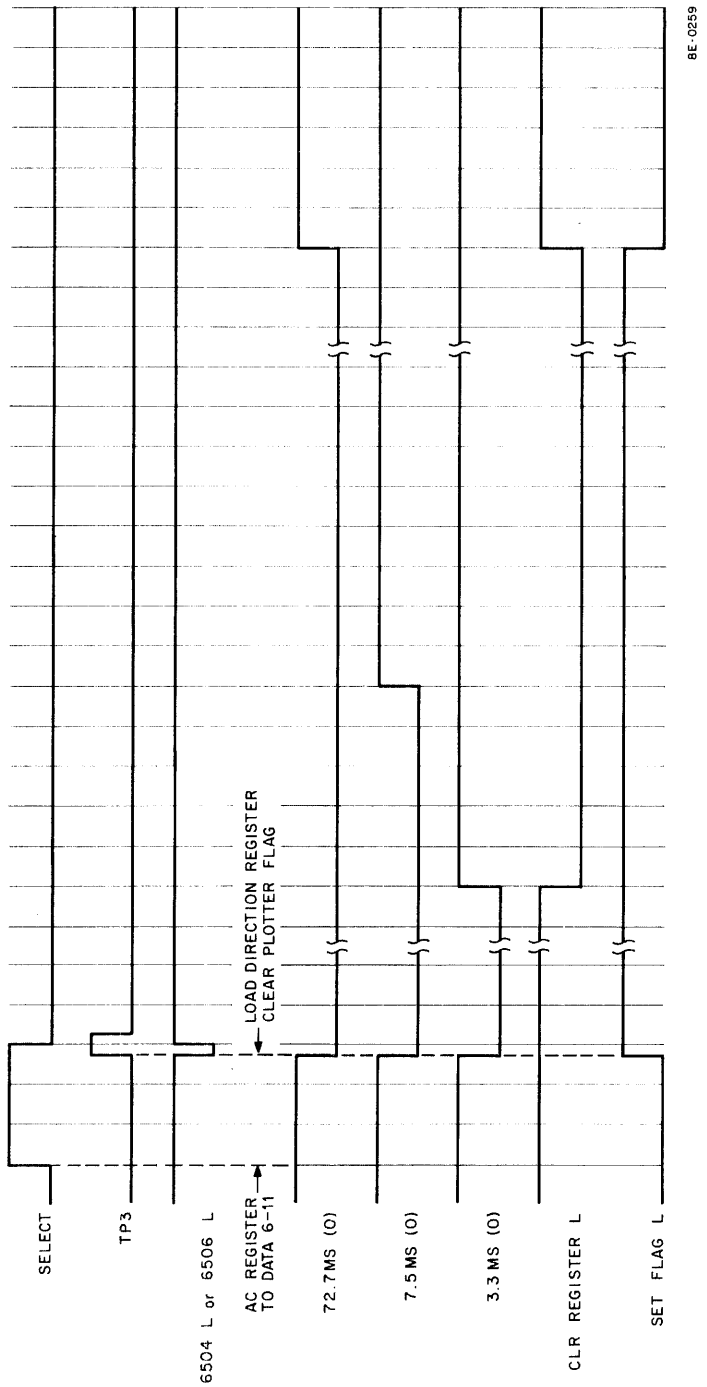


Figure 3-4 Function Timing; Pen Up, Pen Down, Start Zip (Encoded Plotter)

Table 3-2
List of Plotter Directions

AC06–11 Octal Code	Direction		
	Unencoded Plotter	Encoded Plotter	
		Paper	Film
01	Pen up	–	–
02	Pen down	–	–
04	Drum up	–	–
10	Drum down	+y	+y
11	–	+x+y	+x+y
12	–	+x	+x
13	–	+x-y	+x-y
14	–	-y	-y
15	–	-x-y	-x-y
16	–	-x	-x
17	–	-x+y	-x+y
20	Pen left	–	–
21–27	–	–	–
30	–	–	CRT shift
31	–	Pen up	Beam off
32	–	Pen down	Beam on
33	–	Start zip	–
34	–	Block code	-z (+Aux 1)
35	–	Plot code	+z (+Aux 2)
36	–	Start incr	–
37	–	Sync	Sync
40	Pen right	–	–
41–47	–	–	–
50	–	+y/2	–
51	–	+x/2+y/2	–
52	–	+x/2	–
53	–	+x/2-y/2	–
54	–	-y/2	–
55	–	-x/2-y/2	–
56	–	-x/2	–
57	–	-x/2+y/2	–
61–67	–	–	–
70	–	+x+y/2	–
71	–	-x+y/2	–
72	–	+x/2+y	–
73	–	-x/2+y	–
74	–	+x-y/2	–
75	–	-x-y/2	–
76	–	+x/2-y	–
77	–	-x/2-y	–

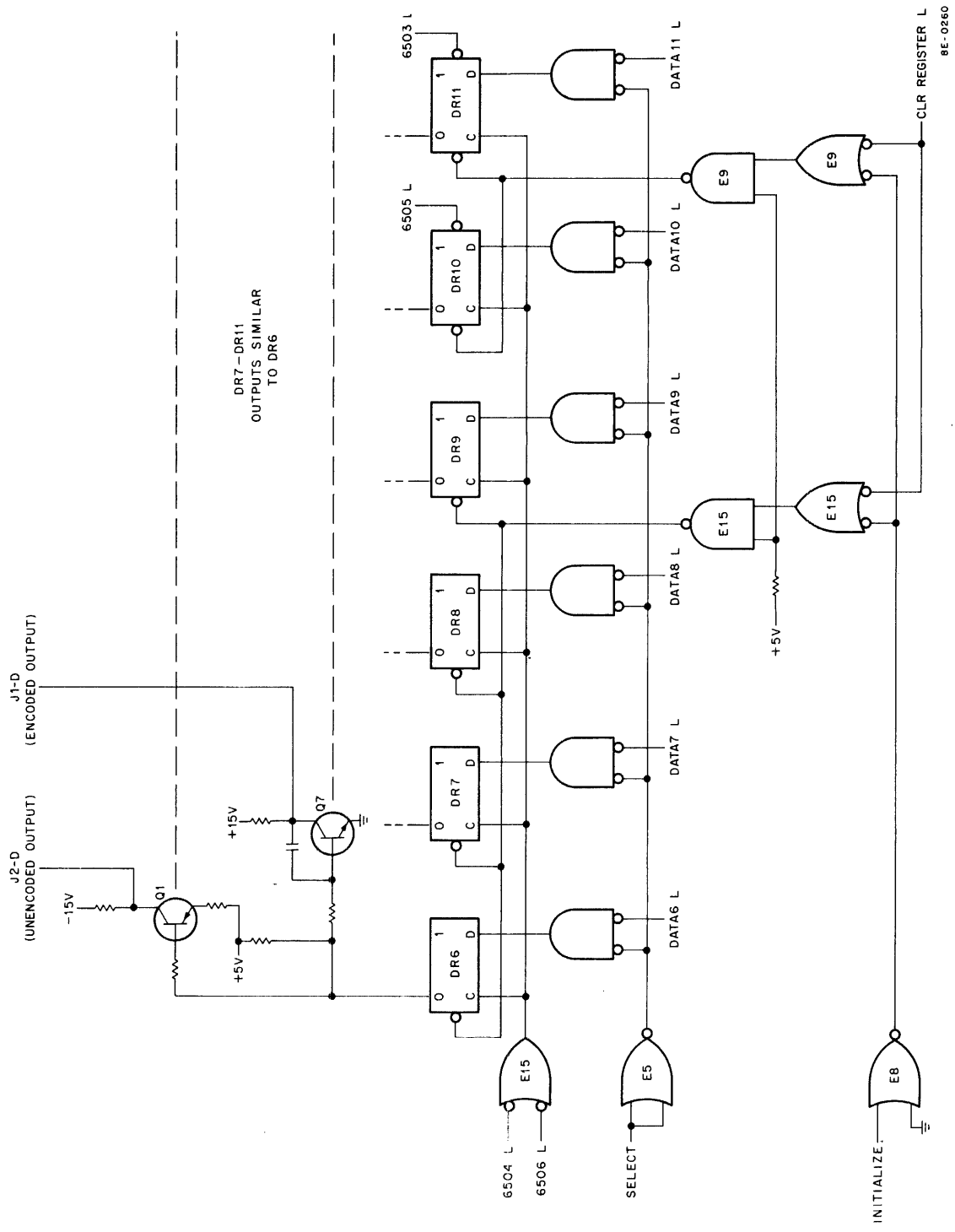


Figure 3-5 Direction Transfer Logic

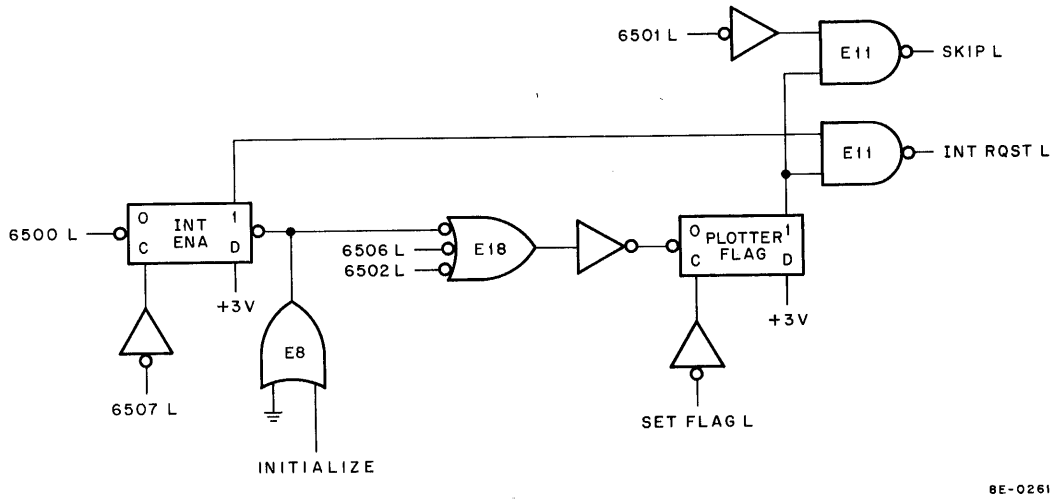


Figure 3-6 INT/Skip Logic

When the INT ENA flip-flop is set, the OMNIBUS INT RQST L signal can be asserted by the PLOTTER FLAG flip-flop. The PLOTTER FLAG flip-flop is set by the SET FLAG L signal when a direction has been carried out by the plotter. The computer identifies the requesting device by entering the interrupt servicing routine. The 6501 (PLSF) IOT instruction in the routine directs the computer to the XY8-E subroutine and another direction is transferred to the Direction Register. The PLOTTER FLAG flip-flop is cleared under program control by the 6502, 6506, and 6007 (via the INITIALIZE signal) IOT instructions, as well as at power turn-on by INITIALIZE.

SECTION 5 MAINTENANCE

The relative simplicity of the XY8-E logic precludes the necessity of a detailed maintenance procedure. Use the diagnostic program to isolate problems that occur in the XY8-E Plotter System. Standard troubleshooting techniques, using the logic drawings and an oscilloscope, will enable the technician to isolate faulty components.

Table 3-3 shows the connector pin assignments for the Plotter Control/plotter interconnecting cable.

SECTION 6 SPARE PARTS

Table 3-4 lists the recommended spare parts for the XY8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 3-3
Pin Assignments, Interconnecting Cable

From Cannon 19-Pin Connector Pin	Signal Name Significant For Unencoded Plotter Only		To Berg 40-Pin Connector Pin
	Houston Inst. Plotter	CalComp Plotter	
1	CHART RIGHT (-X)	DRUM UP (-X)	L
2	CHART LEFT (+X)	DRUM DOWN (+X)	J
3	CARRIAGE UP (+Y)	PEN LEFT (+Y)	F
4	CARRIAGE DOWN (-Y)	PEN RIGHT (-Y)	D
9	PEN UP	PEN UP	R
10	PEN DOWN	PEN DOWN	N
15	GND	GND	S
Pins 5–8, 11–14, 16–19 not used			Pins T, V, X, Z, BB, DD, FF, JJ, LL, NN, RR, TT, not used Pins A, B, C, E, H, K, M, P, S, U, W, Y, AA, CC, EE, HH, KK, MM, PP, SS, UU, VV are gnd.

Table 3-4
XY8-E Recommended Spare Parts

DEC Part Number	Description	Quantity
15-03409-1	Transistor DEC 6534B	1
15-03100	Transistor DEC 3009B	1
19-09705	IC DEC 8881	1
19-09704	IC DEC 314	1
19-09686	IC DEC 7404	1
19-09594	IC DEC 8251	1
19-09373	IC DEC 9601	1
19-09485	IC DEC 380	1
19-05577	IC DEC 7420	1
19-05576	IC DEC 7410	1
19-05575	IC DEC 7400	1
19-05547	IC DEC 7474	1
13-000391	Resistor 1.5K, 1/4W, 5%	1

PART 4
LINE PRINTER

CHAPTER 4
LE8-E LINE PRINTER

SECTION 1 INTRODUCTION

The LE8-E Line Printer Control interfaces an 80- or 132-column line printer to the PDP-8/E. All logic is contained on a single quad module that plugs into the OMNIBUS. The LE8-E connects to the line printer via a signal cable that is supplied with the system.

The LE8-E Line Printer is discussed here only to the extent necessary to both fully describe LE8-E operation and present supplementary information concerning installation and checkout. Details concerning the installation, operation, troubleshooting, and maintenance of the printer itself can be found in Data Products Corporation Technical Manual DPC-214163A (80-column printer) or DPC-215656A (132-column printer). Other publications and documents relevant to the LE8-E are:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* — DEC, 1972
b. *PDP-8/E Maintenance Manual, Volume 1*
c. LE8-E Line Printer Diagnostic, MAINDEC-8E-D2BA
d. DEC Engineering Drawing, Line Printer Control, E-CS-M841-0-1.

SECTION 2 INSTALLATION

The LE8-E Line Printer and Control are installed on site by DEC Field Service personnel. The customer should *not* attempt to unpack, inspect, install, checkout, or service the equipment.

4.1 UNPACKING

Place the LE8-E Line Printer close to the ac power source and proceed as follows:

Step	Procedure
1	Cut the two steel straps that secure the telescoping cap and stitched sleeve to the shipping skid.
2	Remove the Tri-wall clips from all four sides of the stitched sleeve.
3	Remove the four bolts, washers, and nuts securing the line printer to the shipping skid, then remove the printer from the skid and install on the site.

(continued on next page)

Step	Procedure
4	Unpack the LE8-E Control and the signal cable. Plug the LE8-E into the PDP-8/E OMNIBUS and connect it to the line printer with the cable (refer to Table 2-3, Volume 1, for information concerning module installation order). The cable connects to the control via a Berg Connector and to J1 of the line printer via a Winchester MRAC-50 Connector (refer to Section 1 of the Data Products Corporation technical manual for the location of J1).
5	Inspect both printer and control as outlined below and report any damage to the local DEC sales office. a. Inspect external surfaces of the printer and control for surface, bezel, switch, and light damage. b. Open the printer doors and inspect for internal damage. c. Inspect the wiring side of the printer logic mounting panels and the control module for bent pins, cut wire, loose external components, and foreign matter. Also inspect the signal cable for damage. d. Check equipment received against the packing list to be certain that all equipment has been unpacked.

4.2 CHECKOUT

Use the following procedure to check out the LE8-E Line Printer and Control.

Step	Procedure
1	Insert the ribbon in the printer, following the ribbon installation procedure detailed in Section 3 of the Data Products Corporation technical manual (referred to hereafter as the technical manual).
2	Load the printer with continuous-form paper, following the paper loading procedure detailed in Section 3 of the technical manual. **NOTE** **The READY indicator on the printer control panel should light 10—15 seconds after the last step of the procedure (close and latch drum gate, etc.) has been completed.**
3	See the paper positioning (vertical) procedure in Section 3 of the technical manual.
4	Check that the TOP OF FORM and PAPER STEP switches operate as in Table 3-1 of the technical manual.
5	Set the ON LINE/OFF LINE switch to the ON LINE position and check that the TOP OF FORM and PAPER STEP switches do not operate.
6	Hold the MASTER CLEAR switch in the "up" position and check that the READY and ON LINE indicators go out. Release the switch; the READY indicator should light.
7	Check the right tractor for correct adjustment and make sure that the COPIES CONTROL switch is set to the 1—2 position.
8	Set the ON LINE/OFF LINE switch to the ON LINE position and run the MAINDEC diagnostic program, starting at Part 1 of Test 1. While the program is running, adjust the vertical paper adjustment vernier.

(continued on next page)

Step	Procedure
9	Stop the program and set the PRINT INHIBIT switch to the "up" position; set the ON LINE/OFF LINE switch to the ON LINE position and restart the program from Part 1 of Test 1. The PRINT INHIBIT indicator should light and the program should run as in Step 8. Run the program for one minute.
10	Set the PRINT INHIBIT switch to the "down" position and check for printout errors.
11	Replace the continuous-form paper with single-part paper. Run all parts of the program (except Part 1 of Test 1) for one hour.
12	Inspect all printouts for errors and print quality and compare to the enclosed factory-printed samples.

SECTION 3 BLOCK DIAGRAM DESCRIPTION

Figure 4-1 is a block diagram of the LE8-E Control. OMNIBUS pin numbers and pin assignments for both ends of the signal cable can be found on engineering drawing E-CS-M841-0-1. Connector receptacle J1 on the line printer is a 20-pin connector with a return pin for each of the 10 signal pins. Figure 4-2 is a timing diagram of the control; Table 4-1 presents the LE8-E IOT instructions. Refer to the figures while reading this description.

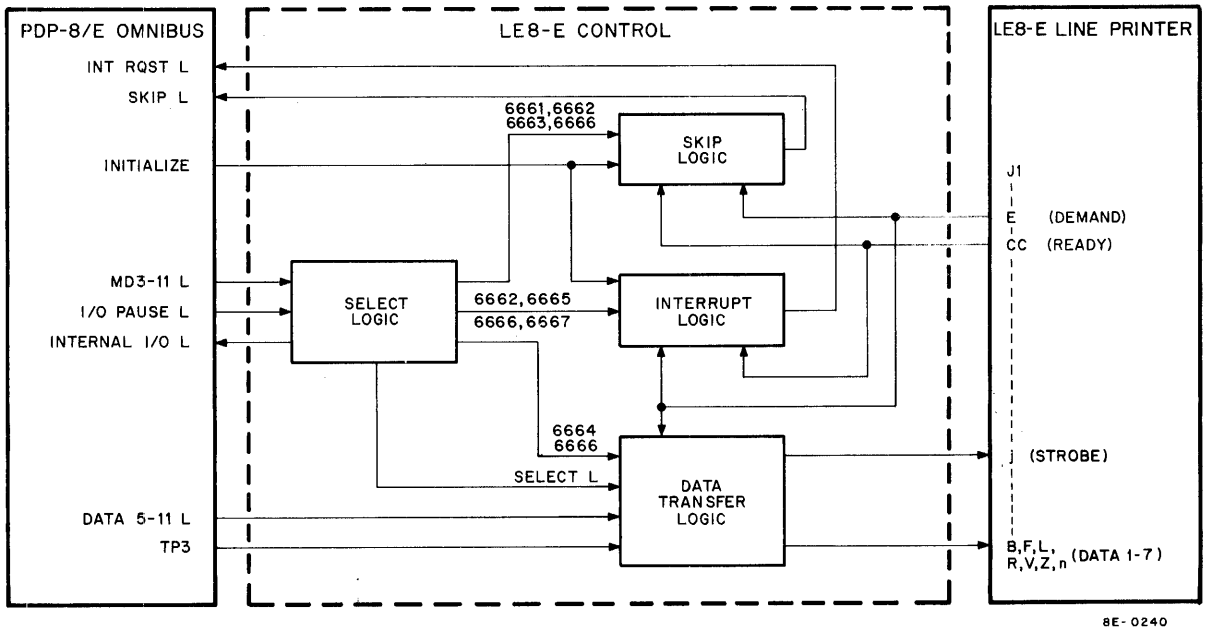


Figure 4-1 LE8-E Line Printer Control Block Diagram

When the line printer is ready to be placed on-line, a READY indicator on the line printer lights. At the same time, the READY signal is asserted. After the line printer has been placed on-line, it asserts the DEMAND signal when it is able to accept a character. The DEMAND signal sets the FLAG flip-flop in the interrupt logic. If the INT ENA flip-flop is set, the FLAG flip-flop asserts the OMNIBUS INT RQST L signal. The computer then begins to execute the interrupt servicing routine to determine the identity of the requesting device.

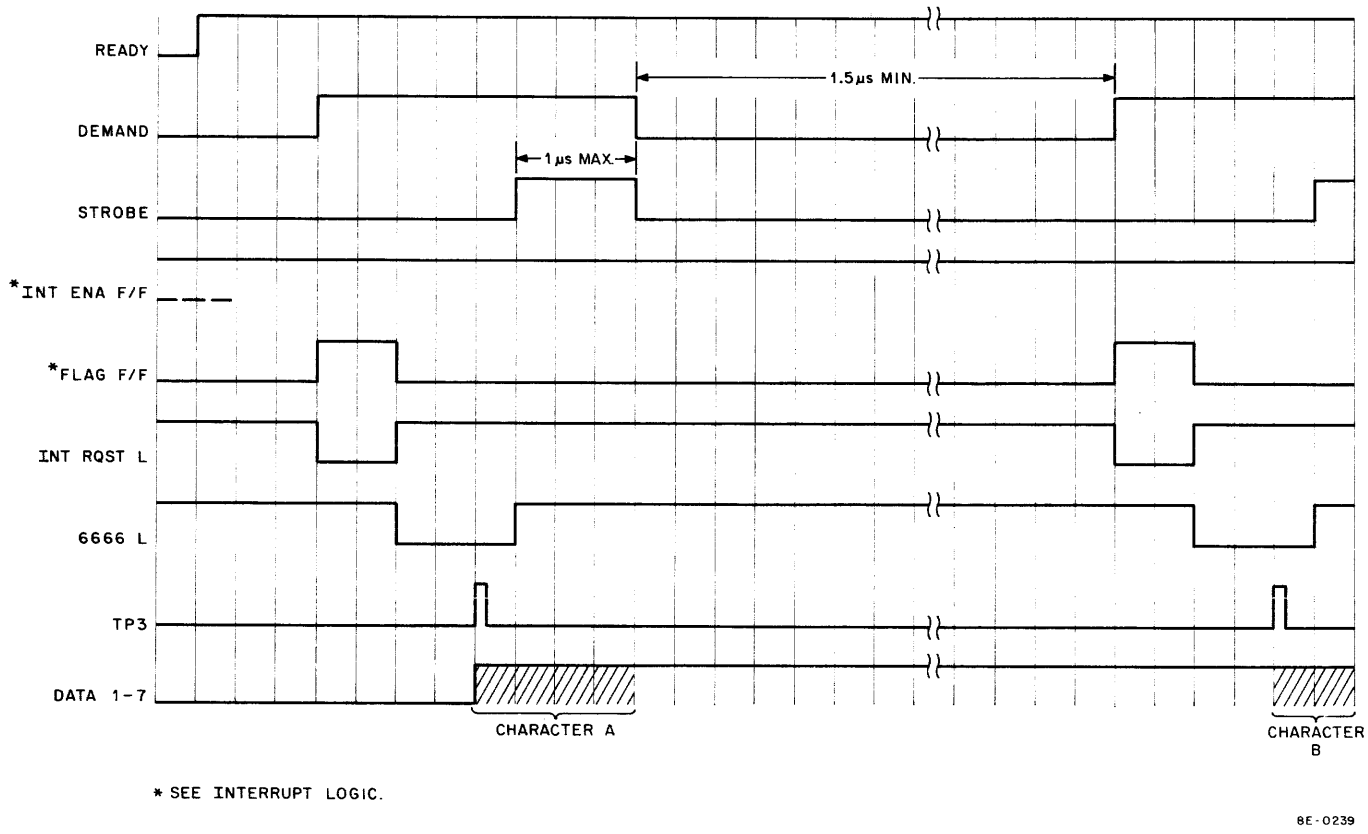


Figure 4-2 LE8-E Control Timing

Table 4-1
LE8-E IOT Instruction List

Octal Code	Mnemonic	Function
6661	PSKF	Skip on the Flag. Senses the state of the FLAG flip-flop. If it is set, the program counter is incremented so that the next sequential instruction is skipped.
6662	PCLF	Clear the Flag. Clears the FLAG flip-flop.
6663	PSKE	Skip on an Error. Senses the state of the READY signal. If it is low, indicating an error condition in the line printer, the program counter is incremented so that the next sequential instruction is skipped.
6664	PSTB	Load Line Printer Buffer Register. A character is transferred from the CPU AC Register, via the OMNIBUS DATA 5—11 lines and the Line Printer DATA 1—7 lines, to the Printer Buffer Register.
6665	PSIE	Set INT ENA flip-flop. The LE8-E is logically connected to the computer interrupt system. Both the READY signal and the DEMAND signal can cause a program interrupt.
6666	PCLF, PSTB	Clear the Flag, Load Line Printer Buffer Register. Microprogram of 6662 and 6664.
6667	PCIE	Clear INT ENA flip-flop.

When the 6661 instruction in the servicing routine is decoded, the skip logic asserts the OMNIBUS SKIP L signal. The computer then proceeds to the subroutine associated with the LE8-E. When the 6666 instruction (as an example) in the subroutine is decoded, the FLAG flip-flop is cleared and the information in the AC Register is placed on the OMNIBUS DATA 5—11 lines; at TP3 time the information is clocked into the Buffer Register of the data transfer logic. At the trailing edge of the 6666 instruction signal, the STROBE signal is generated and the information is clocked from the DATA 1—7 lines of the line printer into the 20-character Shift Register within the line printer. The DEMAND signal is then negated and, in turn, negates the STROBE signal.

SECTION 4 DETAILED LOGIC

4.3 SELECT LOGIC

The select logic is shown in Figure 4-3. Both the SELECT L and INTERNAL I/O L signals are asserted when a 666X instruction is decoded. The INTERNAL I/O L signal causes the positive I/O bus interface to ignore the IOT instruction; the SELECT L signal is gated with bits MD9—11 to provide inputs for the BCD-to-decimal decoder, E17 (refer to Appendix A, Volume 1, for details about the DEC 8251 IC). The decoder supplies the signals that represent IOT instructions 6661 through 6667.

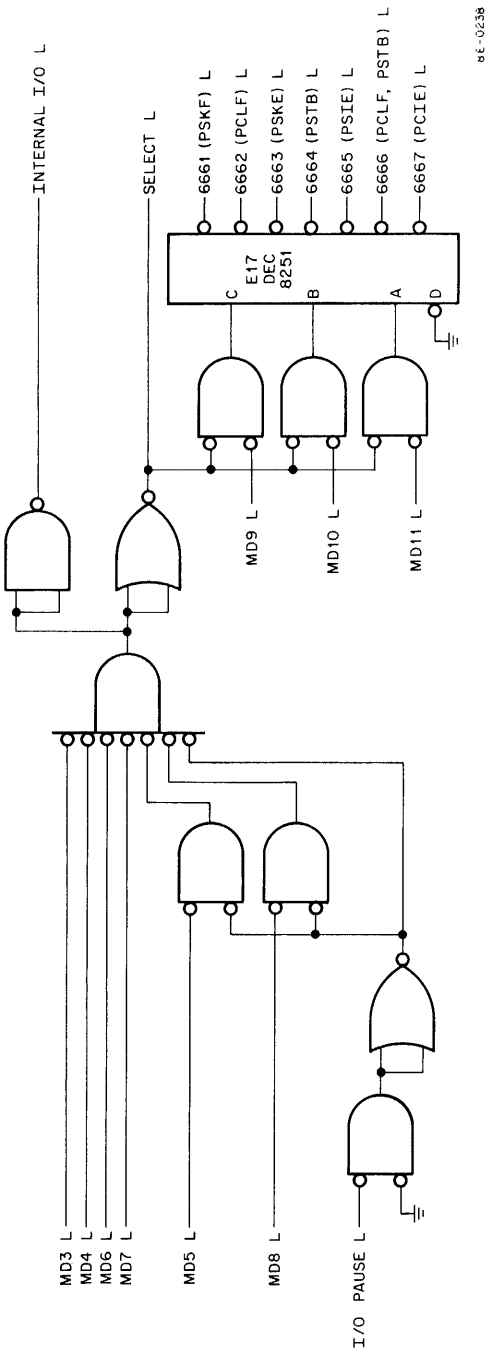


Figure 4-3 Select Logic

4.4 INTERRUPT LOGIC

The interrupt logic is shown in Figure 4-4. When the INT ENA flip-flop is set, the control is logically connected to the computer interrupt system. This flip-flop is cleared at computer power turn-on by the OMNIBUS INITIALIZE signal and can be cleared and set under program control by instructions 6667 (or 6007, CAF) and 6665, respectively.

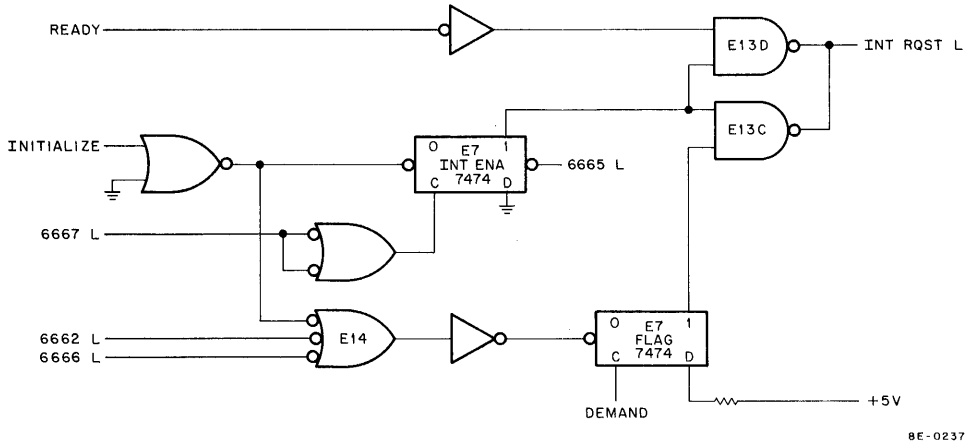


Figure 4-4 Interrupt Logic

When the INT ENA flip-flop is set, both the READY signal and the DEMAND signal can cause a program interrupt. If the READY signal is low, indicating an error condition in the line printer (drum gate open, excessive temperature in paper drive motor, insufficient drum motor speed, or printer out of paper) NAND gate E13 asserts the INT RQST L signal and the computer begins the interrupt servicing routine. Instruction 6663 senses the state of the READY line and causes a skip in the CPU program counter if READY is low (Figure 4-5).

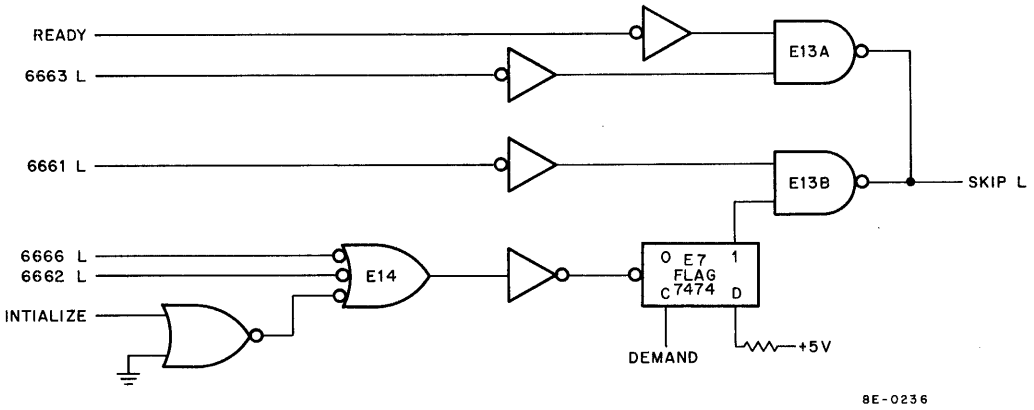


Figure 4-5 Skip Logic

The DEMAND signal causes a program interrupt by setting the FLAG flip-flop, as outlined in Section 3. Instruction 6661 senses the state of the FLAG flip-flop and causes a program skip when the FLAG is set (Figure 4-5). The FLAG flip-flop is cleared by the INITIALIZE signal and by program instructions 6662 and 6666.

4.5 DATA TRANSFER LOGIC

The data transfer logic is shown in Figure 4-6. The 7-bit code transmitted from the CPU AC Register to the printer 20-character Shift Register represents characters that appear on the 64- or 96-character printer drum (refer to the table of code/character relationship in Volume 1, Section 4). The coded information is gated from the AC Register to the OMNIBUS DATA 5—11 lines when the 6666 or 6664 instruction is decoded in the CPU. The SELECT L signal enables the DATA lines to condition the D-inputs of the 7-stage Buffer Register. When the control decodes the 6666 or 6664 instruction, the buffer is loaded at TP3 time and the coded character is placed on the printer DATA 1—7 lines.

Each character is followed by the STROBE signal that is generated when the STROBE flip-flop is set by the trailing edge of the instruction. The printer samples the DATA 1—7 lines and negates the DEMAND signal, clearing the STROBE flip-flop.

SECTION 5 MAINTENANCE

Refer to Volume 1 and the Data Products Corporation technical manual for maintenance information that pertains to both the control and the printer. The LE8-E Diagnostic, MAINDEC-8E-D2BA, should be run when an error in the LE8-E is suspected.

SECTION 6 SPARE PARTS

Table 4-2 lists recommended spare parts for the LE8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 4-2
LE8-E Recommended Spare Parts

DEC Part Number	Description	Quantity
19-05547	IC DEC 7474	1
19-05576	IC DEC 7410	1
19-05590	IC DEC 7401	1
19-09485	IC DEC 380	1
19-09594	IC DEC 8251	1
19-09686	IC DEC 7404	1
19-09704	IC DEC 314	1
19-09705	IC DEC 8881	1

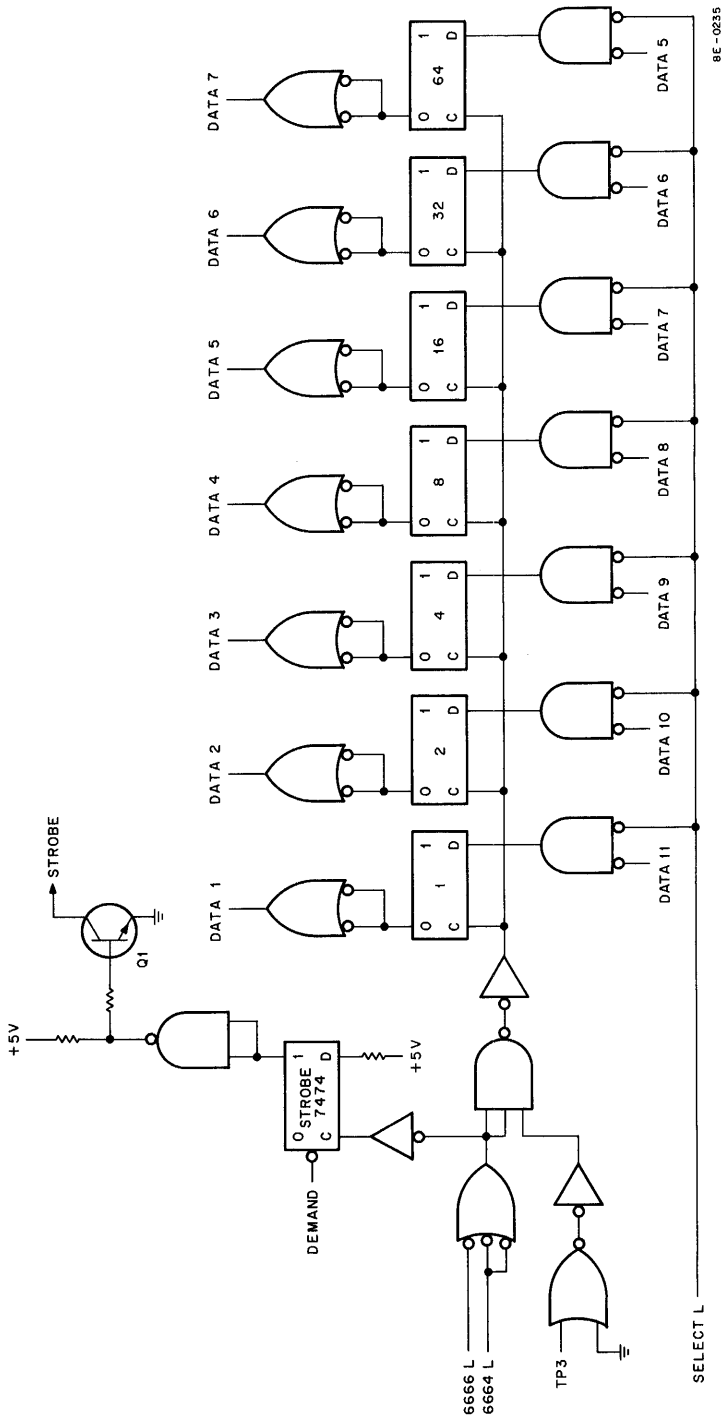


Figure 4-6 Data Transfer Logic

PART 5
DATA COMMUNICATIONS EQUIPMENT

CHAPTER 5
DP8-E SYNCHRONOUS MODEM

SECTION 1 INTRODUCTION

The PDP-8/E can communicate with remote data terminals and other computers when it is interfaced to full-duplex or half-duplex synchronous modems. A maximum of four DP8-E Synchronous Modem Interfaces can be plugged into the OMNIBUS; each interface provides a means of transferring data between the computer and a communication channel.

The interface consists of two quad modules, M839 and M866, that are connected by an H851 Edge Connector. A signal cable, supplied with the option, connects the M866 Module to the synchronous modem. The interface provides level conversion so that the computer can operate with communication channels using bipolar (EIA standard), current mode, or TTL signals. A DP8-E that interfaces bipolar or TTL signals is designated DP8-EA; one that interfaces current mode or TTL signals is designated DP8-EB. The DP8-EA Interface is designed to operate with Bell System 200-series synchronous modems, or equivalent; the DP8-EB Interface is designed to operate with Bell System 300-series modems, or equivalent. Each type of interface connects to its modem with a special cable assembly, viz., assembly BC01V for the DP8-EA and BC01W for the DP8-EB.

Data transfers between a modem and the computer are accomplished by 3-cycle data breaks, initiated and controlled by the DP8-E Interface. A modem-to-computer transfer involves a modified 3-cycle data break operation that uses seven computer timing cycles, rather than the normal three cycles. The extra four timing cycles enable the program to detect selected characters that might appear in the modem transmission.

Modems are discussed only to the extent necessary to fully describe the interface operation and to present supplementary information concerning installation and checkout of the option. Details of the installation, operation, troubleshooting, and maintenance of the modems can be found in their technical manuals. Publications and documents relevant to the DP8-E are:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* — DEC, 1972
b. *PDP-8/E Maintenance Manual, Volume 1*
c. DP8-E Diagnostic, MAINDEC-08-DHDPA-A
d. DEC Engineering Drawings, Synchronous Modem Interface, E-CS-M839-0-1 and E-CS-M866-0-1.

SECTION 2 INSTALLATION

The DP8-EA/EB Interface is installed on-site by DEC Field Service personnel. The customer should *not* attempt to unpack, install, checkout, or service the equipment.

Before the interface can be plugged into the PDP-8/E OMNIBUS, each module must be carefully checked to ensure that it is wired correctly. Each module contains many split lugs that can be selectively connected or disconnected so that the interface can meet the requirements of the PDP-8/E data break system and function with any of the compatible modems, which have diverse operating characteristics. The split lugs on each module are paired. Each pair of lugs is identified by a number, a letter, or a combination of the two (one symbol — Δ (delta) — and two words — ON and OFF — are used, also). The identification is etched on the printed circuit board between or near the two lugs and also appears on the schematics and logic diagrams.

Tables 5-1 and 5-2 list characteristics that relate to the PDP-8/E data break system and to the diversity of compatible modems. Those jumpers that connect the pairs of split lugs are also listed. Each jumper bears the same identification as the two lugs it joins. These tables show the jumpers that must be connected to achieve the desired characteristic. For example, if the modem transfers characters that have seven data bits, the M839 module jumpers B7, C7, and B78 must be connected. All other jumpers in this group (B6, B8, and C8) must be disconnected.

All the pairs of lugs, except those labeled C and Δ, are connected by machine-inserted jumpers when the boards are manufactured. Selected jumpers are then removed so that each module can be production tested. The characteristics selected for production testing are listed in paragraphs *a.* through *h.* which follow. Unless otherwise specified, the two modules are wired for these characteristics when received by the user. Therefore, the jumper selections might have to be changed to suit the user's needs.

a. The access addresses, the IOT codes, and the break priority for each interface should be assigned on the basis of channel designations, as follows:

Channel	Access Addresses	IOT Codes	Break Priority
1	7720–7730	640X, 641X	5
2	7700–7710	642X, 643X	4
3	7660–7670	644X, 645X	3
4	7640–7650	646X, 647X	2
Spare	7620–7630	—	—
Spare	7600–7610	—	—

b. 8 bits/character

c. Normal clock phase

d. EIA level conversion (DP8-EA)

e. Current mode level conversion (DP8-EB)

f. Sync code 226

g. CARRIER/AGC interrupt for both ON and OFF transitions

h. Full-duplex operation.

When correct jumper selection has been completed, insert the interface in the PDP-8/E OMNIBUS and connect the modules with the edge connector. See Table 2-3, Volume 1, for information concerning recommended module priorities (the DP8-E is a "non-memory" option).

Connect the M866 Module to the synchronous modem with the signal cable provided. Refer to Section 5 for cable and connector pin assignments.

The DP8-E option can be checked for correction operation by running the diagnostic program. If a problem arises, refer first to Section 5 for ideas. Refer then to the modem instruction manual for modem checkout procedures.

Table 5-1
Jumper Connections, M839 Module

To Select	Connect Jumper(s) (Remove Others)	Figure Reference
Bits/Character		
6	B6, C8	5-7, 5-9, 5-10
7	B7, B78, C7	
8	B78, B8 (2), C7, C8	
BRK Priority		
1	P1	5-12
2	P2	
3	P3	
4	P4	
5	P5	
6	P6	
7	P7	
Access Address		
7700–7710	A5	5-15
7720–7730	A5, A7	
7640–7650	A6	
7660–7670	A6, A7	
7600–7610	NONE	
7620–7630	A7	
Device Code		
6400–6407, 6410–6417	N6, N7	5-5
6420–6427, 6430–6437	N6, 7	
6440–6447, 6450–6457	N7, 6	
6460–6467, 6470–6477	6, 7	
Sync Code (Examples)		
000	NONE	5-9
226	S4, S7, S9, S10	
377	S4, S5, S6, S7, S8, S9, S10, S11	
Any code from 000–377 is possible by selectively connecting the 'S' jumpers		

SECTION 3 BLOCK DIAGRAM DESCRIPTION

The DP8-E includes a receive channel and a transmit channel, each of which can initiate a data break when information is to be transferred between the DP8-E and the PDP-8/E. The channels synchronize the modem and computer logic and convert computer parallel data to modem serial data, and vice-versa. Figure 5-1 is a simple block diagram showing the signals used by the interface to synchronize the modem and the computer.

Table 5-2
Jumper Connections, M866 Module

To Select	Connect Jumper(s) (Remove Others)	Figure Reference
BRK Priority		
1	NONE	
2	P1	
3	P1, P2	
4	P1, P2, P3	5-12
5	P1, P2, P3, P4	
6	P1, P2, P3, P4, P5	
7	P1, P2, P3, P4, P5, P6	
Carrier/AGC Interrupt		
ON	ON	
OFF	OFF	5-18
ON & OFF	ON, OFF	
Level Conversion		
EIA	E, CE (2)	
*Current Mode	C (6), CE (2), CT	E-CS-M866-0-1
TTL	T (2), CT	
****Clock Phase**		
Normal	N (2)	E-CS-M866-0-1
Inverted	Δ (2)	
Half-Duplex	HD	E-CS-M866-0-1

*If Bell 303 modem is used, jumpers D and X must be connected; if Bell 301 modem is used, jumpers D and X must be disconnected.

**For maintenance clock (Section 5) connect jumper F. If testing receive circuits, connect jumper Δ; if testing transmit circuits, connect jumper N.

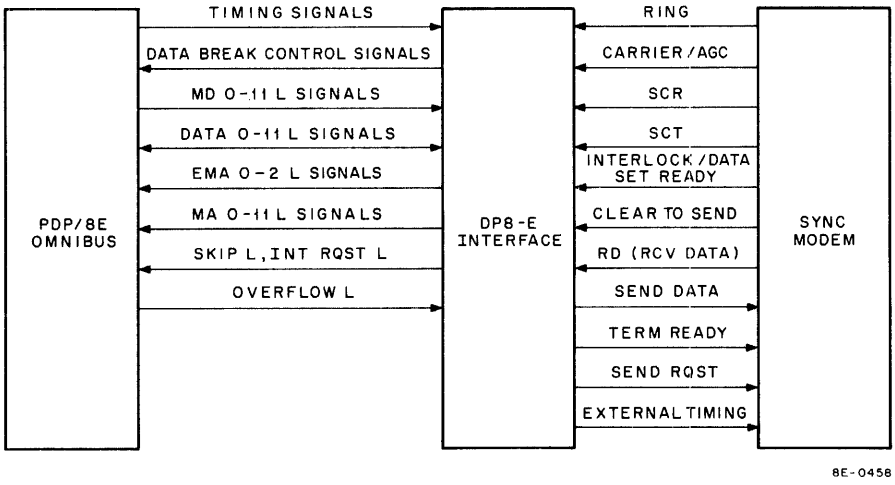


Figure 5-1 Simple Block Diagram, DP8-E

The modem generates the INTERLOCK/DATA SET READY signal when it is turned on and able to take part in a data transfer. The status of this signal can be tested in the DP8-E by the program IOT instruction, SRS1 (see Table 5-3 for a list of DP8-E IOT instructions). When the status check indicates that the modem is on, the program can issue an SLCC IOT instruction, causing the DP8-E to assert the TERM READY signal. The modem, which provides the interface with SCT (Serial Clock Transmit) pulses from the moment it is turned on, begins transmitting SCR (Serial Clock Receive) pulses when it receives the TERM READY signal.

Table 5-3
DP8-E IOT Instruction List

Octal Code	Mnemonic	Description
6400/6420 6440/6460	SSCD	Skip if character detected. Causes the program to skip the next instruction if the CHAR(acter) DET(ected) flip-flop is set. The flip-flop is set if an assembled character is found to compare to one of the stored characters in the access address locations. This instruction clears the flip-flop. If the program must identify the test character that compared to the contents of the Receive Data Register, an SRCD instruction should be used. See the SRCD instruction for details.
6401/6421 6441/6461	SCSI	Clear DP8-E. Initializes all active functions in the DP8-E.
6402/6422 6442/6462	SSRO	Skip if receive word count overflow. Skips the next instruction if the ROFLO L (receive overflow) signal is asserted, and negates the signal. The signal is asserted if, during a receive data break operation, the OMNIBUS OVERFLOW L signal is generated.
6403/6423 6443/6463	SSTO	Skip if transmit word count overflow. Skips the next instruction if the TOFLO L (transmit overflow) signal is asserted, and negates the signal. The signal is asserted if, during a transmit data break operation, the OMNIBUS OVERFLOW L signal is generated.
6404/6424 6444/6464	SGRR	Receiver go. Sets the R-GO flip-flop. The instruction implies that the program is ready to receive data from the modem, i.e., the current address (CA) and the word count (WC) have been updated. The hardware begins memory references if two consecutive synchronizing characters are received on the incoming serial data line. Memory references cease when the word count increments to 0 and SGRR is not issued in less than one character time.
6405/6425 6445/6465	SGTT	Transmitter go. Sets the T-GO flip-flop. The instruction implies that the program is ready to transmit data, i.e., the current address and the word count have been updated. If the CLEAR TO SEND signal has been asserted in response to the SEND RQST signal, the hardware begins memory references. References cease when the word count increments to 0 and SGTT is not issued within one character time. SEND RQST should be asserted by the SLCC instruction; it should not be negated until two bit times after the last bit has been transmitted, i.e., 1/ [Baud rate x (bits/character + 2)] second after word count overflow.

(continued on next page)

Table 5-3 (Cont)
DP8-E IOT Instruction List

Octal Code	Mnemonic	Description
6406/6426 6446/6466	SCSD	Clear the sync detect flip-flops. Clears the SYNC 1 and SYNC 2 flip-flops in the break request, receive logic. The instruction enables the programmer to initialize the sync detection circuits and to clear the receive circuits without initializing the DP8-E.
6407/6427 6447/6467	SRTA	Read Current/Access Address Register. Transfers the contents of the register to the AC Register. The instruction is used, primarily, for diagnostic and/or program debugging.
6410/6430 6450/6470	SSRG	Skip if the RING flip-flop is set. Skips the next instruction if the RING flip-flop is set. Clears the flip-flop.
6411/6431 6451/6471	SSCA	Skip if the C0/AGC flip-flop is set. Skips the next instruction if the C0/AGC flip-flop is set. Clears the flip-flop.
6412/6432 6452/6472	SLCC	Load control word. Transfers the contents of AC00–05 to the control word logic. AC bits 00–03 are loaded into the CNTL Register; functions selected by each bit are listed below. AC00: TERM RDY; permits the modem to enter into the data mode. AC01: IDLE; allows continuous transmission from the same location in core without program intervention. The hardware enters the Idle mode when the word count goes to 0. Word count and current address are not incremented. Access to the last transfer address continues until the SGTT instruction is issued or the Idle bit is negated. AC02: ENABLE; allows program interrupts and data break cycles. AC03: SEND RQST; activates the SEND RQST line (see SGTT instruction description). AC04: Available for customer use. When modem timing AC05: signals are used, one EIA (or current mode) transmitter is available for use with AC04 or AC05.
6413/6433 6453/6473	SLFL	Load field. Transfers the contents of AC00–AC05 to the load field logic. Bits 00–02 select the receive EMA bits 0–2, while bits 03–05 select the transmit EMA bits 0–2. The selected EMA bits, combined with the current address, form the 15-bit address to or from which data is transferred.

(continued on next page)

Table 5-3 (Cont)
DP8-E IOT Instruction List

Octal Code	Mnemonic	Description
6414/6434 6454/6474	SRS2	Transfers information from the read status logic to AC00–AC07, as follows: AC00: CO/AGC L AC01: RS (1) AC02: TERM RDY AC03: CS AC04: TEMA 0 AC05: TEMA 1 AC06: TEMA 2 AC07: RD
6415/6435 6455/6475	SRS1	Transfers information from the read status logic to AC00–AC07, as follows: AC00: RRQST L AC01: TRQST L AC02: Sync 2 L AC03: Sync 1 L AC04: REMA 0 L AC05: REMA 1 L AC06: REMA 2 L AC07: MODEM RDY L
6416/6436 6456/6476	SSBE	Skip on bus error. Skips the next instruction if the BUS ERROR flip-flop is set. Clears the flip-flop. The flip-flop is set if a transmit or receive break request is not serviced in less than 1/baud rate. This implies that the break system is overloaded or inoperative.
6417/6437 6457/6477	SRCD	Read detected character. The contents of the 2-bit register that contains the identity of the detected character are transferred to AC10 and AC11. The two bits correspond to the low-order bits of the access address where the characters for detection are stored.

Maintenance Instruction – When AC00 is logic 1, the SRCD instruction causes a single clock pulse to be generated. The pulse is placed on the maintenance clock line to the modem. In the test configuration (see Section 5, Maintenance), this line is returned as the transmit and receive clocks enabling single-step testing of the transmit and receive circuits.

5.1 TRANSMITTER-MODEM DIALOGUE

After this exchange of ready signals, a data transfer can be initiated by either the modem or the computer. A computer-to-modem transfer is initiated by the computer under program control. An SLCC instruction (either the same one that causes the TERM READY signal, or a later one) enables the modem free-running SCT pulses to set a flip-flop in the DP8-E. The setting of this flip-flop results in the SEND RQST signal being asserted by the interface. The modem responds to this signal by transmitting the CARRIER/AGC signal, followed by the CLEAR TO SEND signal. The CARRIER/AGC signal can cause the interface to generate an interrupt request,

assuming that the DP8-E has been logically connected to the interrupt system. The program proceeds to a DP8-E subroutine that initializes certain memory locations (Word Count (WC) and Current Address (CA) Registers) and issues the SGTT IOT instruction. This instruction, along with the asserted CLEAR TO SEND signal, enables the transmit channel to request a data break. During this data break, a character is transferred from memory to a shift register in the DP8-E. Subsequently, SCT pulses cause the character to be shifted from the transmit channel to the modem via the SEND DATA line. At least the first two characters transmitted must be sync characters; this requirement enables the remote receiving station to assemble each 6, 7, or 8 successive bits to form the correct character.

5.2 MODEM-RECEIVER DIALOGUE

After the initial exchange of the two ready signals, a modem can initiate a data transfer in response to a ringing signal on the transmission line. The modem generates the RING signal, thereby causing the DP8-E to generate an interrupt request. The program proceeds to a subroutine that sets up the WC and CA registers and then waits for the modem to transmit the CARRIER/AGC signal. This signal, which indicates that the modem is in the data transmission mode, causes the subroutine to issue the SGRR IOT instruction. Data transmitted by the modem on the RD line is shifted into the receive channel by SCR pulses. The IOT instruction enables the receive channel to request a data break after two successive sync characters have been recognized in the transmission (the sync characters enable the receive channel to assemble each 6, 7, or 8 successive bits thereafter into data characters). During the data break, which must be completed between 2 successive SCR pulses, the character that was shifted into the receive channel input register from the RD line prior to the data break is transferred to memory. When the data break ends, SCR pulses shift the next character in the transmission into the register.

5.3 DP8-E DATA BREAKS

A detailed block diagram of the DP8-E is shown in Figure 5-2. This block diagram illustrates the interface operation during the data break. Figures 5-3 and 5-4 are timing diagrams that relate the signals shown in the block diagram (each timing diagram depicts 6-bit character operation). All three figures should be studied and used as reference material.

Data transfers between the PDP-8/E and a synchronous modem interface are of the data break type. A data break is carried out in the Direct Memory Access (DMA) state of the CPU. This state provides direct communication between a data break device and memory by allowing the device interface to assume control of CPU major register gating. When the DP8-E interface is ready to begin a data break transfer, it asserts a number of OMNIBUS control signals to force the CPU into the DMA state. One of the first of these control signals to be asserted (at TP3 time) is the CPMA DISABLE L signal that causes the CPMA Register outputs to be disconnected from the MA lines at TP4. During TS4, the interface makes a priority check. If no higher priority device has requested a data break, the DP8-E places on the MA lines (at TP4 time) the address of the memory location that is to be accessed during the first timing cycle of the data break. At the same time, the MS, IR DISABLE L signal is asserted, forcing the next timing cycle to be carried out in the DMA state. If the synchronous modem were a 1-cycle data break device, data could be transferred, during this DMA cycle, to or from the addressed memory location. At the end of the cycle, the DP8-E would relinquish control of the CPU until a new transfer were to take place. The data break operation would be repeated as often as necessary to transfer the entire block of data words.

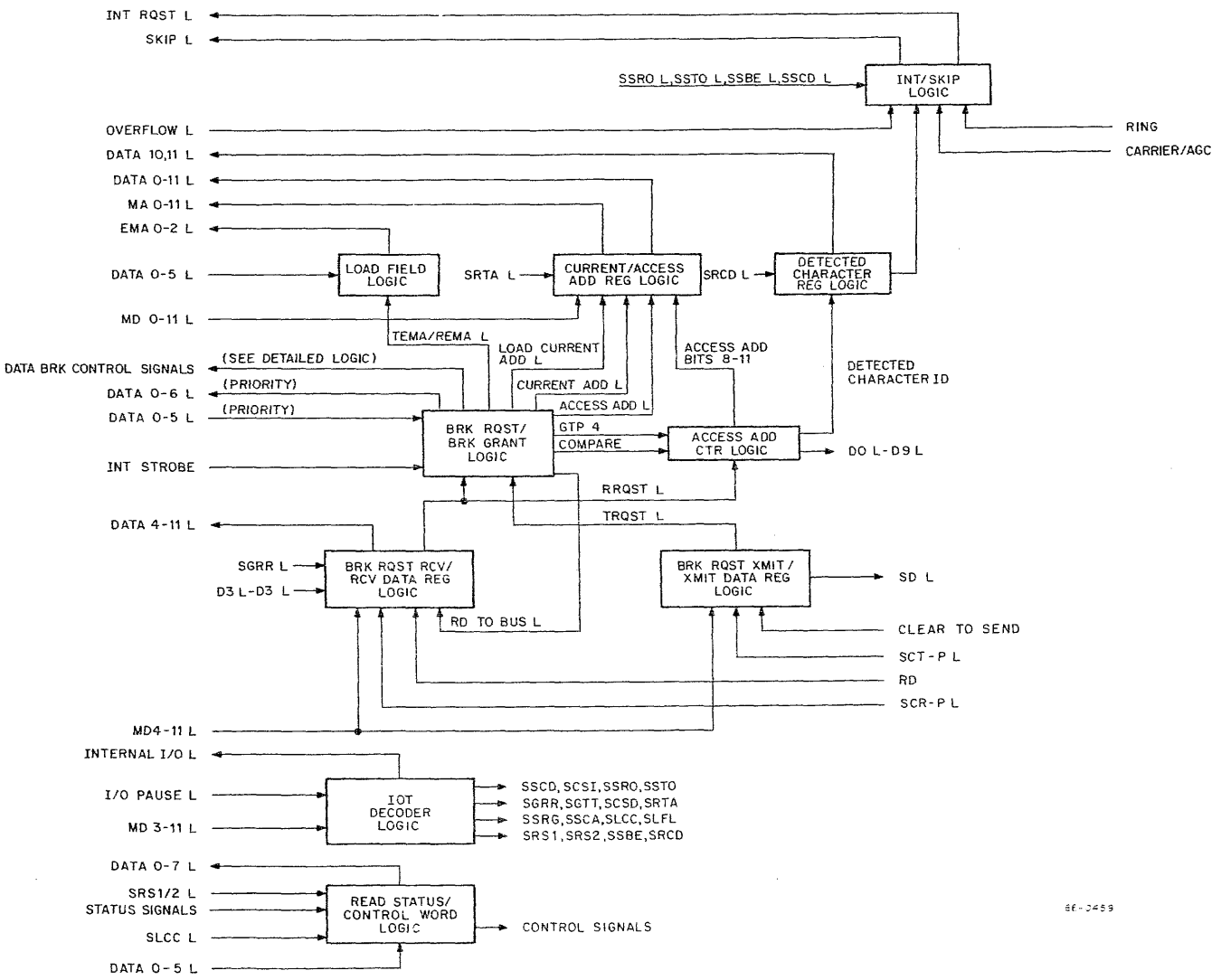


Figure 5-2 Detailed Block Diagram, DP8-E

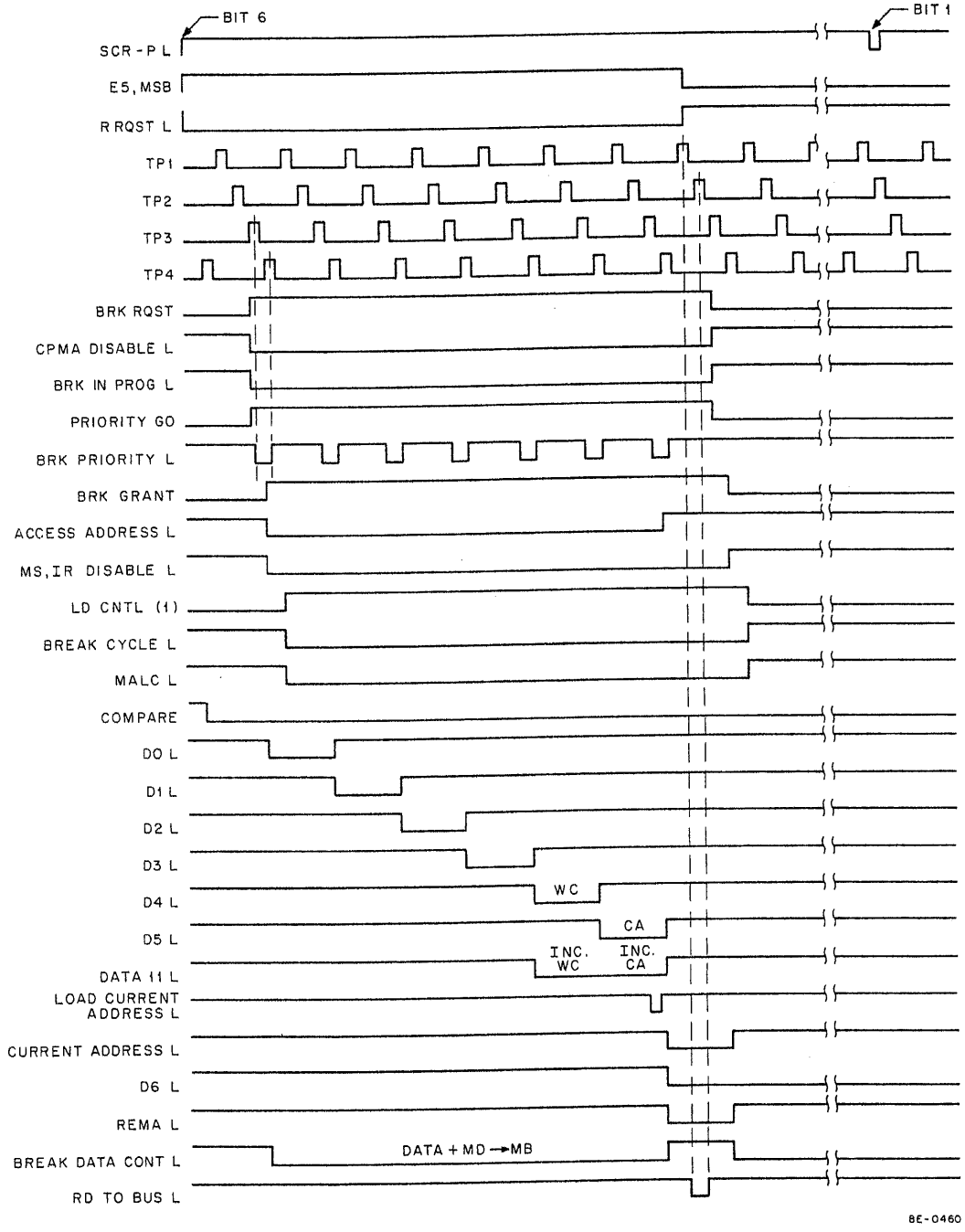


Figure 5-3 Timing, Receive Break Request

However, the synchronous modem is not a 1-cycle data break device; i.e., it does not continuously update the memory address to or from which data is transferred and, within its hardware, it does not keep track of the number of transfers made. Data break devices that do not perform these two necessary tasks are defined as 3-cycle data break devices. The transfer count and the transfer address are retained in the separate memory locations that were introduced earlier, viz., the Word Count (WC) Register and the Current Address (CA) Register,

respectively. During a data break operation, each location is addressed separately and the data in each location (the word count or the current address) is updated by the interface. A single timing cycle is required for each updating operation. Thus, three timing cycles are required for each data word transferred: the word count is updated during the first cycle; the current address is updated during the second cycle; the data word is transferred during the third cycle.

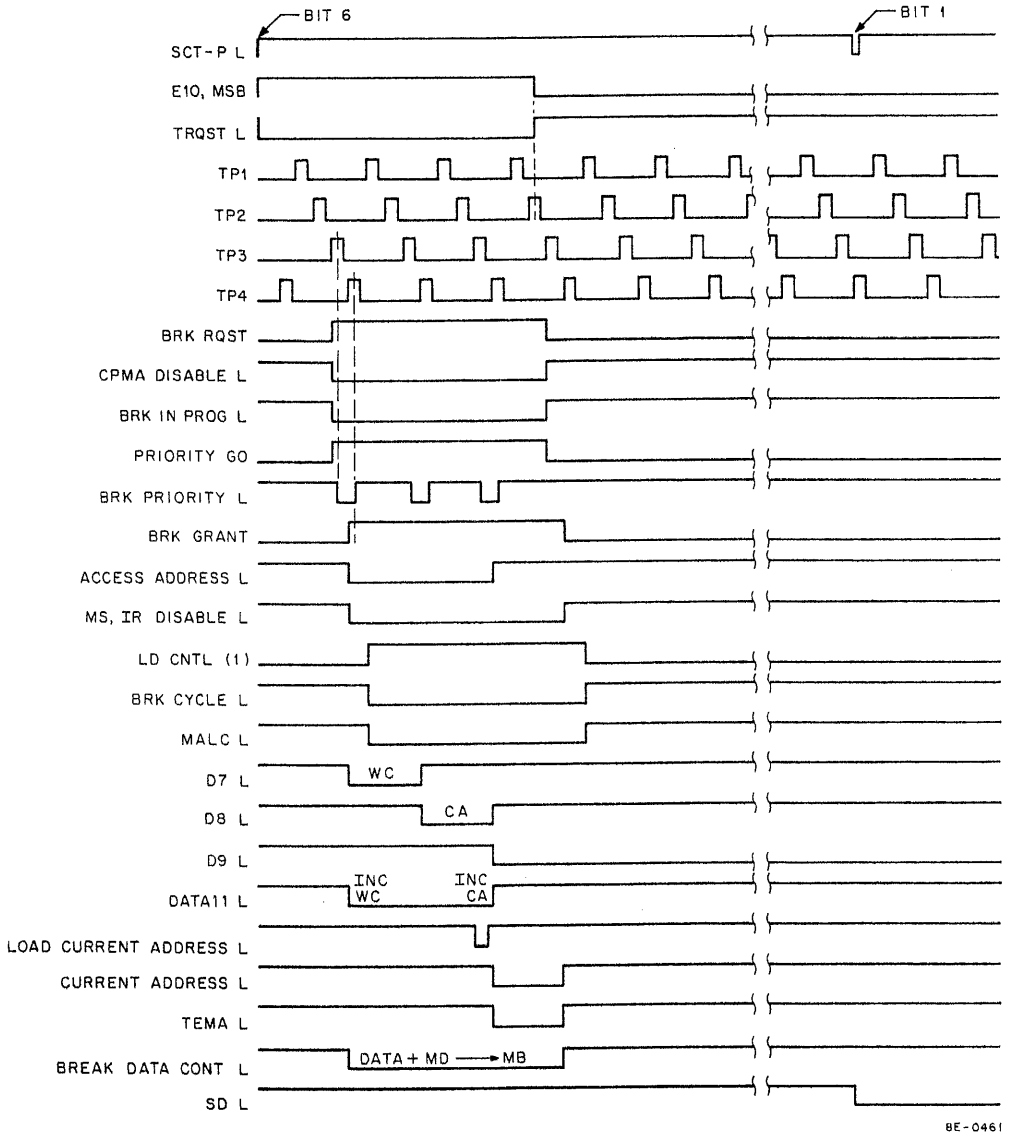


Figure 5-4 Timing, Transmit Break Request

If the data transmission is from the DP8-E to memory, the 3-cycle data break operation is modified somewhat. The DP8-E Interface is capable of identifying selected data characters that might appear in the data transmission. The identification is accomplished by comparing each data character in the transmission with a test character. Four test characters are provided; thus, the interface can identify four different data characters. The test characters are stored in four separate memory locations that are successively addressed at the beginning of the data

break operation. Each comparison requires a single timing cycle. Therefore, a receive data break operation requires seven timing cycles, rather than three, for each data word transferred. However, the operation is still considered a 3-cycle data break.

A receive data break operation can begin only after the data character has been shifted completely into the interface Receive Data Register. When the last data bit is shifted in, the interface requests a data break and asserts the CPMA DISABLE L signal to remove the CPMA Register from the MA lines. Then the interface places an "access address" on the MA lines. The memory location represented by this address is one of a group of eight special-purpose memory locations assigned to the modem/interface in question (each modem/interface occupies one communication channel). These locations are assigned to the communication channels as indicated in Section 2.

To simplify the discussion, only Channel 1 is considered. Locations 7720 through 7723 contain the four test characters; locations 7724 and 7725 contain the receive word count and current address, respectively; locations 7727 and 7730 contain the transmit word count and current address, respectively.

The first access address to be placed on the MA lines at the beginning of the receive data break operation is 7720. This address originates partly in the Current/Access Address Register logic and partly in the Access Address Counter logic. The test character stored in this location is gated to the Receive Data Register logic and compared with the received character stored there. This action can have one of three results: a) if the two characters are not equal, no further action occurs during this timing cycle; b) if the two characters are equal, an interrupt request can be generated during this timing cycle; c) if the two characters are equal, the data break operation can be terminated near the end of this timing cycle, i.e., the received character is stripped. If either a) or b) results from the comparison, the access address is incremented by the Access Address Counter logic at the end of the timing cycle. The test character in location 7721 is gated to the Receive Data Register logic during the second timing cycle and compared with the received character. This comparison can have one of the three results indicated. Again, the access address is incremented at the end of the cycle, provided the received character is not stripped. The comparison process is carried out for the four test characters. If a successful comparison occurs during the first, second, or third test cycle, the remaining test characters must still be compared. When the fourth test character has been compared, the access address increments to 7724, which represents the memory location of the word count. During the fifth timing cycle, or WC cycle, the word count is incremented. The access address then increments to 7725 and, during the sixth timing cycle, the CA cycle, the current address is incremented.

This incremented current address is the address of the location to which the received character is to be transferred during the seventh, or data transfer, timing cycle. This "current address" is placed on the MA lines at the end of the CA cycle. During the data transfer cycle, the received character is gated from the Receive Data Register to the OMNIBUS DATA lines and from the DATA lines to the location specified by the current address. At the end of this timing cycle, the data break operation is terminated.

To carry out a transmit data break operation, the DP8-E asserts the same control signals as it does during a receive data break. However, no test character timing cycles are necessary; consequently, only three timing cycles are used to transfer each data character.

Each logic block indicated in Figure 5-2 is discussed in detail in Section 4. The separate sections are arranged to present the information in the most logical progression; however, some points, because of their complexity, are covered in more than one section, albeit from a different viewpoint.

5.4 IOT DECODER LOGIC

The PDP-8/E can accommodate four separate communication channels. Hence, four sets of IOT instructions are needed. A set consists of 16 instructions, each instruction represented by an octal code and a mnemonic code. The same 16 mnemonic codes are used with each set of instructions; however, the octal codes vary from set to set. The octal codes for each channel are determined by the selective connection of certain jumpers on the M839 Module. When this module is fabricated, the octal codes are assigned to the channels as detailed in Section 2.

The IOT decoder logic portion of the M839 Module is shown in Figure 5-5. Locations are indicated on the figure where jumpers can be connected to provide the 16 octal codes for a particular channel. These locations are designated 6, 7, N6, and N7. Assume that this interface is assigned to Channel 1. Octal codes 6400 through 6407 and 6410 through 6417 must be selected. This is accomplished if jumpers are connected at locations N6 and N7. Thus, NAND gate E19 asserts the THIS CODE signal during TS3 of IOT instructions 640X and 641X.

Bit MD 8 is gated with the THIS CODE signal to provide an enabling signal for one of the DEC 8251 Decoders. If bit 8 is logic 0, E38 is enabled, and a 640X instruction can be decoded; if bit 8 is logic 1, E26 is enabled, and a 641X instruction can be decoded.

The three least significant bits of the instruction are determined by MD bits 9, 10, and 11. These bits are gated to both decoders; the enabled decoder produces the assigned octal code.

Note that the THIS CODE signal causes NAND gate E33 to assert the OMNIBUS INTERNAL I/O L signal. This signal ensures that the positive I/O bus interface ignores the IOT instruction.

5.5 CONTROL WORD LOGIC

The control word logic is shown in Figure 5-6. The SLCC instruction gates the contents of the AC Register to the DATA lines. The user can load AC bits 0–5 to assert selected DP8-E enabling signals.

The information on DATA lines 0–3 is loaded into the CNTL Register at TP3 time of the instruction. Each of the four possible enabling signals is discussed in later sections. Flip-flops E27 allow the user to enable functions of his own choosing. The 1-output of each flip-flop can be taken from the board at the "H" top connector or at connector J1, if jumpers are installed at locations FF and JJ. Note that these outputs are TTL-level rather than EIA-level signals.

5.6 BREAK RQST, RECEIVE LOGIC

The Break RQST, Receive logic is shown in Figure 5-7. When communication in the receive mode has been established between the modem and the PDP-8/E, the modem begins transmitting data to the interface. Each character bit is shifted into the Receive Data Register (Paragraph 5.7) by an SCR-P L pulse. Each SCR-P L pulse also clocks the RCV CNT binary counter, E5 in Figure 5-7 (note that the counter is wired for 6-bit/character operation). When an entire character has been shifted into the Receive Data Register, the most significant bit (MSB) of the RCV CNT counter becomes logic 1. If both the R-GO flip-flop and the SYNC 2 flip-flop are set, NAND gate E3 generates the RRQST L signal, and a data break operation can begin. During this operation, the character in the Receive Data Register is transferred to the PDP-8/E memory.

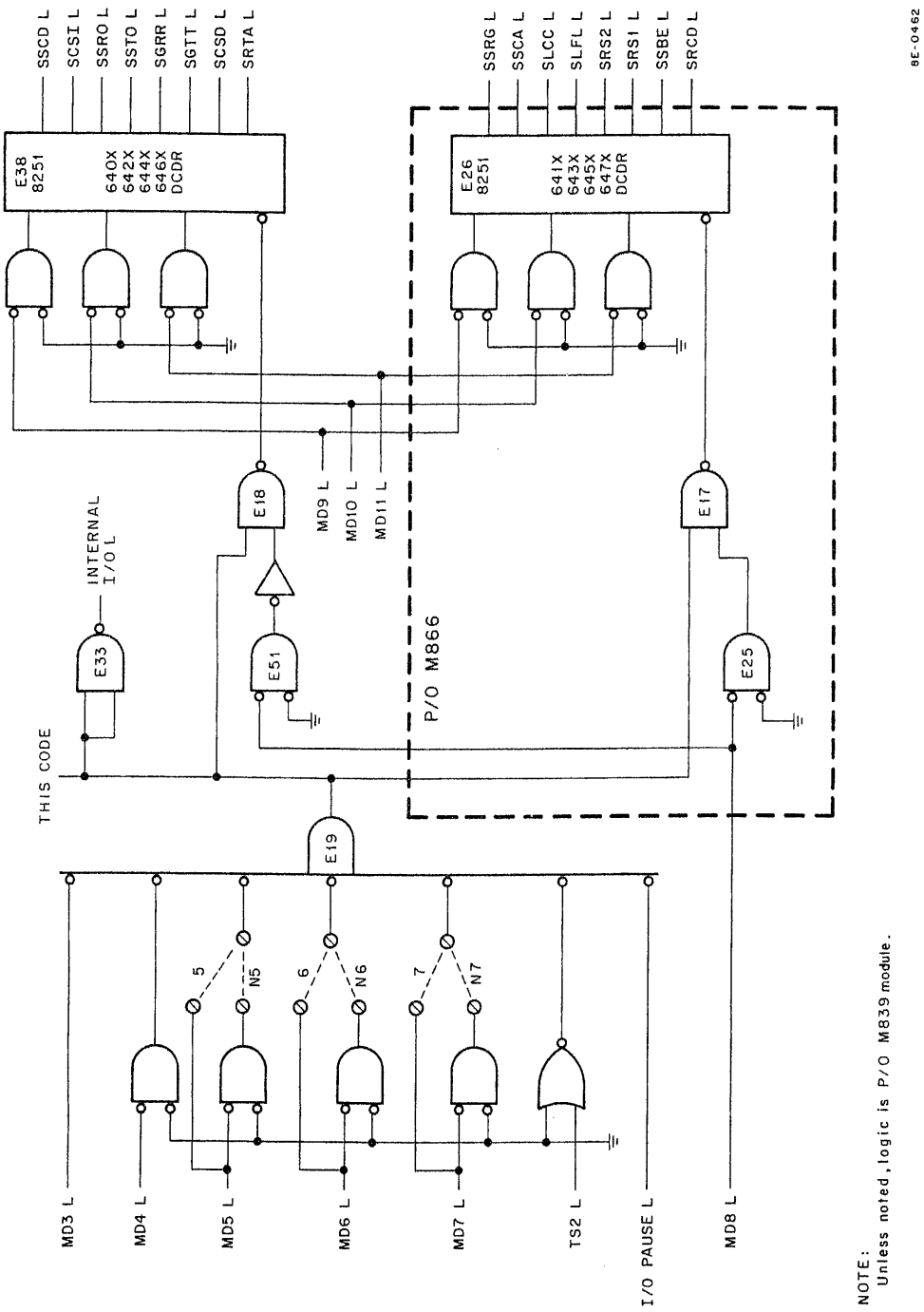


Figure 5-5 DP8-E IOT Decoder Logic

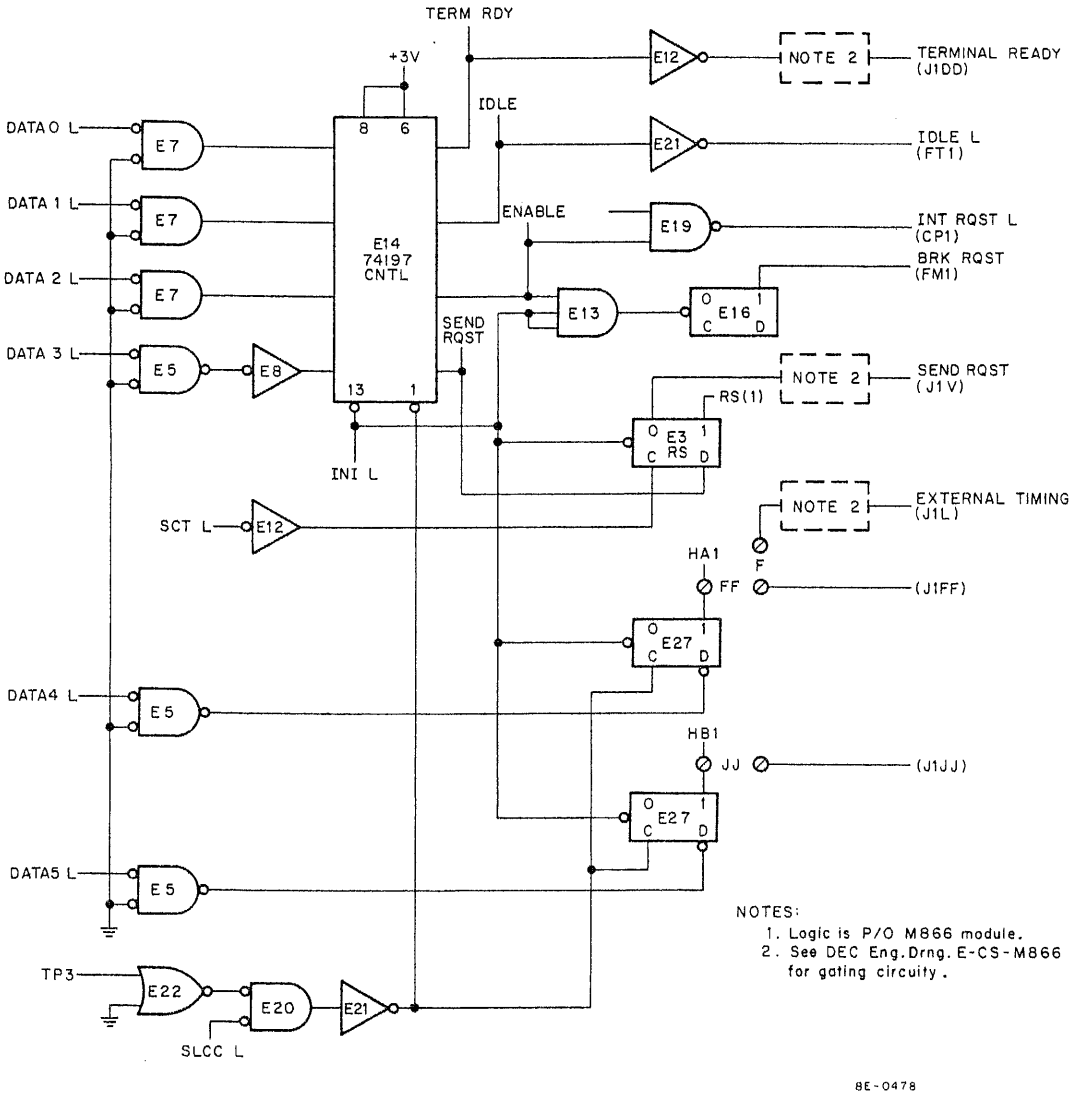


Figure 5-6 Control Word Logic

The R-GO flip-flop, which is cleared at INITIALIZE time, must be set by the SGRR IOT instruction during the time that communication is first established. The SYNC 2 flip-flop is set only when two successive sync characters have been transmitted by the modem. The detection of the sync characters is carried out by a comparison process in the Receive Data Register logic (the comparison is performed in the hardware and does not use the special break locations). The character in the Receive Data Register is compared with the jumper-selected interface sync code.

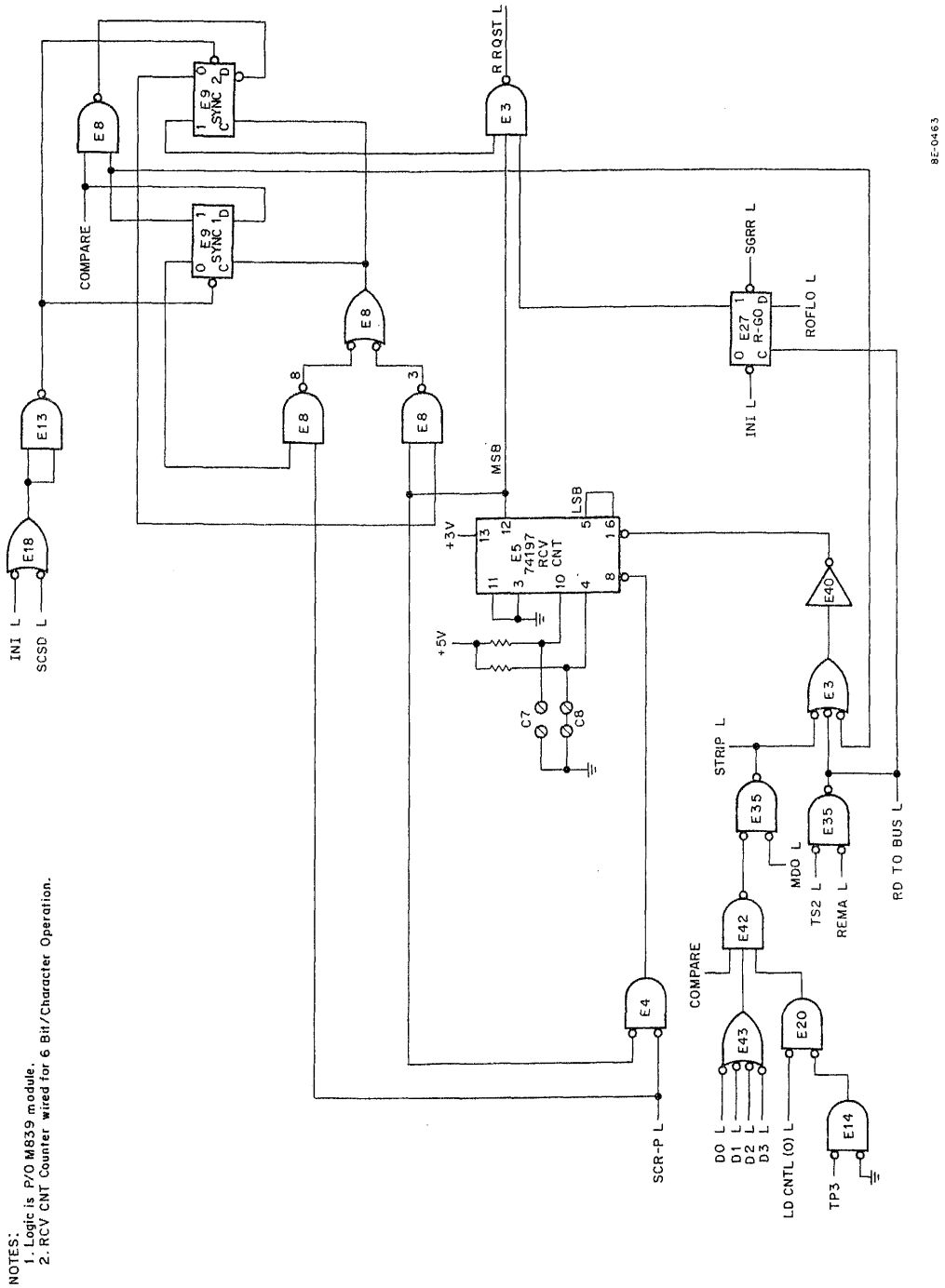


Figure 5-7 Break RQST, Receive Logic

Assume that the first character in a particular transmission is a sync character (Figure 5-8 is helpful in visualizing the sync character detection process). As the SCR-P L pulse shifts the sixth character bit into the Receive Data Register, the COMPARE signal is asserted, because each of the six character bits is the same as the corresponding sync code bit. The COMPARE signal is applied to the D-input of the SYNC 1 flip-flop, and the flip-flop is set, indicating that one sync character has been detected (the SYNC 1 flip-flop is set by the trailing edge of the SCR-P L pulse; the delay of a few nanoseconds is exaggerated in the timing diagram). Until this first character is detected, the RCV CNT counter, E5, is prevented by the 1-output of the SYNC 1 flip-flop from counting SCR-P L pulses. The 1-output causes the count/load input, pin 1, of the counter to be held low. This low not only prevents E5 from counting, but also presets E5 with a count of 0010.

When the 1-output of the SYNC 1 flip-flop goes high, E5 can begin counting pulses. If the next character shifted into the Receive Data Register is another sync character, the COMPARE signal is asserted again. The MSB output of E5 goes high with the trailing edge of the SCR-P L pulse. The low at the D-input of the SYNC 2 flip-flop enables the output pulse from NOR gate E8 to set the flip-flop. NAND gate E3 asserts the RRQST L signal.

If priority requirements are met, the receive data break operation begins at the next occurrence of a TP4 pulse. The operation takes place between the two bits indicated on the timing diagram. Even the fastest modem available is so slow compared to the computer timing cycle that approximately 15 timing cycles can occur in the time space indicated by the dashed lines. Figure 5-3 is a timing diagram of a receive data break operation. Bit 6 and bit 1 in each timing diagram correspond, to call attention to the relative timing of the computer and modem (Figure 5-3 should be referred to when considering any of the receive circuits).

If the first occurrence of a sync character is not followed by a second, the SYNC 1 flip-flop is cleared at the time that the MSB of E5 goes high. In such a case, the timing reverts to that indicated at the beginning of Figure 5-8. Therefore, two sync characters must occur successively somewhere in the transmission. When this happens, both the SYNC 1 and the SYNC 2 flip-flops remain set throughout the transmission, and can be cleared only by the SCSD IOT instruction, or at INITIALIZE time.

Each time the MSB of E5 goes high, a break request results. During the data transfer cycle the RD TO BUS L signal gates the character in the RCV DATA Register onto the OMNIBUS DATA lines. At this time, pin 1 of the RCV CNT counter is taken low, presetting the counter with a count of 0010. The MSB goes low and the RRQST L signal is negated. After six SCR-P L pulses a new break request can be generated.

Requests are generated until the last character is transferred. During the WC cycle immediately preceding the last data transfer cycle, the OMNIBUS OVERFLOW L signal is asserted, causing ROFLO (0) L to be asserted by the INT/Skip logic (Figure 5-19). The RD TO BUS L signal then clears the R-GO flip-flop, thereby disabling NAND gate E3.

Note that the RCV CNT counter can be reset to the initial count by the STRIP L signal that enables NOR gate E3. This signal is asserted when a received character has compared successfully with one of the stored test characters and the 0-bit of the test character is logic 1, i.e., MD0 is logic 1. In this case, the data break operation ends after the break cycle in which the comparison took place. Consequently, neither the word count nor the current address is incremented, and the character in the Receive Data Register is not transferred to memory. Refer to Paragraph 5.15 for a discussion of the events that occur when MD0 is logic 0.

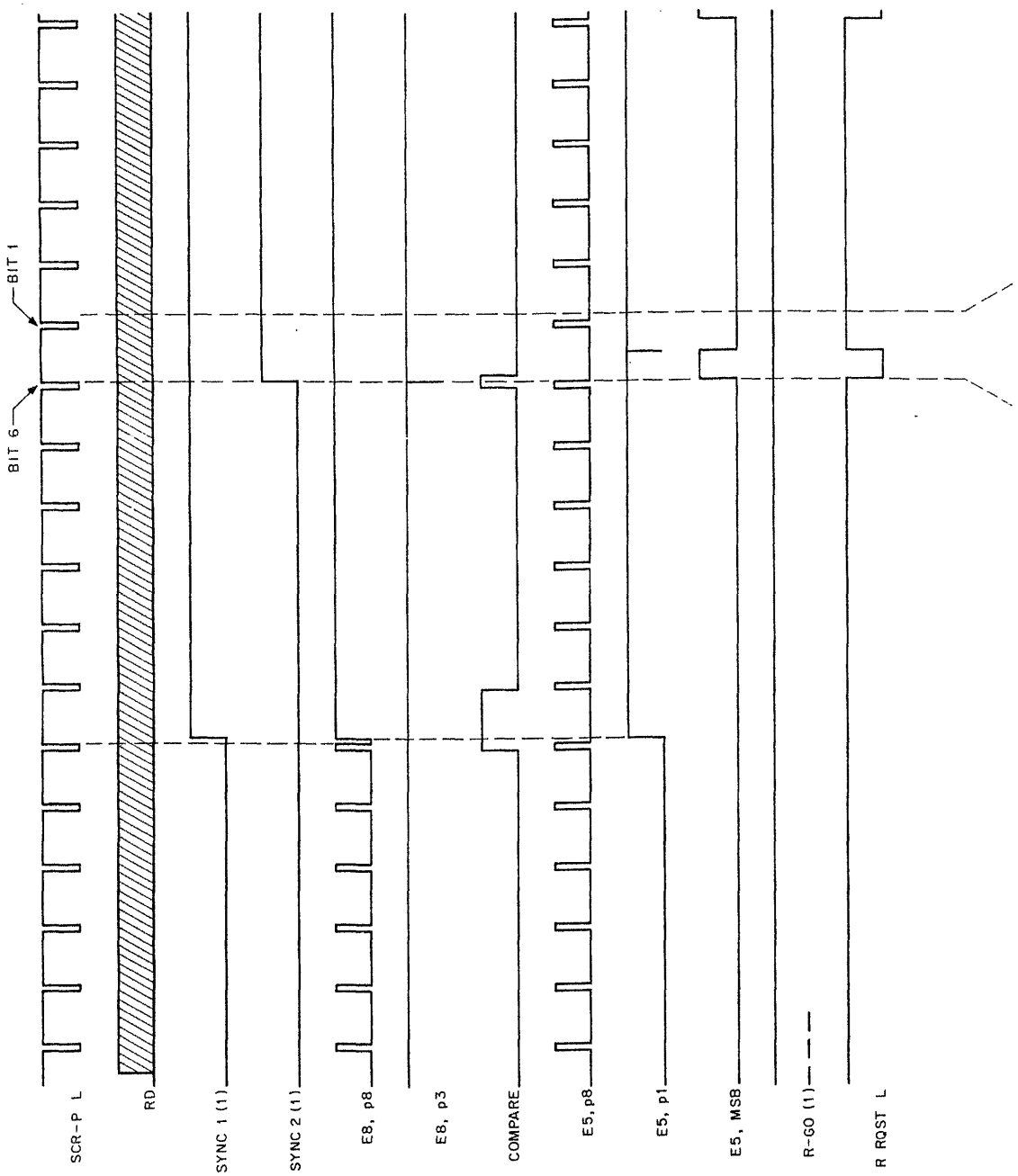


Figure 5-8 Sync Character Detection, Timing Diagram

5.7 RECEIVE DATA REGISTER LOGIC

The Receive Data Register logic is shown in Figure 5-9. The logic has two functions: a) to compare received data with either the interface sync code or test characters stored in memory; b) to transfer the received data to the OMNIBUS DATA lines.

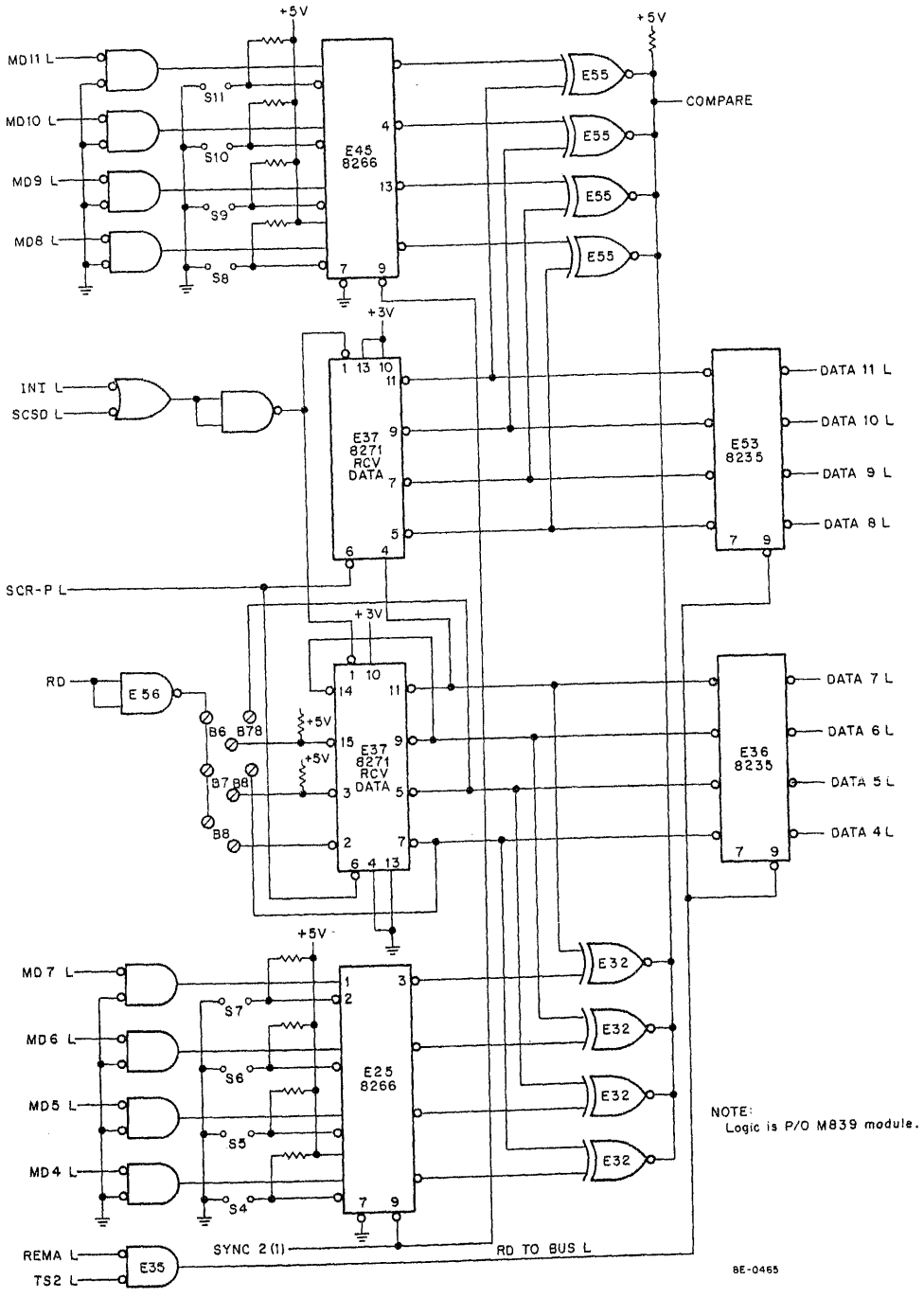


Figure 5-9 Receive Data Register Logic

The data is received in serial form as the RD signal (this signal is high, representing logic 1, when the mark condition exists). Each data bit is shifted into the Receive Data Register, E37 and E54, by its accompanying SCR-P L pulse. Jumpers B6, B7, B8, and B78 must be selectively removed or connected so that the Receive Data Register corresponds to the number of bits per character of the received data (see Table 5-1 for information concerning jumper selection). For example, if the data being received contains 6 bits per character, only jumper B6 is connected. Only two bits of the 4-bit shift register, E37, are used; thus, E37 and E54 comprise a 6-bit shift register. The register is filled each time an entire character has been received. Note that although E54 is in the "right-shift" mode, as one expects (see Volume 1, Appendix A for 8271 details), E37 is always in the "parallel-load" mode. However, because of the way E37 is externally wired, the IC operates as a right-shift register.

When an entire character has been shifted into the register, the character is compared and/or transferred to the DATA lines. A comparison is always made at the beginning of a transmission to determine if the character received is a sync character. If it is, it coincides with the interface sync code. If two successive sync characters are received, two successful comparisons are made and the interface requests a data break of the CPU.

The received character and the sync code are compared, bit for bit, by Exclusive-NOR gates E32 and E55, each of which acts as a comparator. Each bit of the received character is applied to one input of a comparator. The other comparator input is taken from E25 or E45, DEC 8266 ICs (see Volume 1, Appendix A for details). These ICs are 4-bit logic elements (multiplexers) that are used as selectors. For example, E25 provides an output at pin 3 that represents the state of the input signal at either pin 1 or pin 2. The selection is determined by the state of the control signals at pins 7 and 9. If pin 9 is low, E25 provides an output at pin 3 of the same state as the input at pin 2; if pin 9 is high, the output state at pin 3 is the inverse of the input state at pin 1.

When the received character is being compared to the interface sync code, the SYNC2 (1) signal is low. Thus, pin 3 is the same state as pin 2. The state of pin 2 depends on whether or not jumper S7 is connected. Likewise, the state of each other output pin of E25 and E45 depends on whether or not a corresponding jumper is connected. The jumpers are connected or removed to select the desired sync code. Assume that the desired sync code is 26_8 (the LSB of the sync code/character corresponds to the LSB of the PDP-8/E data word; the LSB of the received character is the first bit transmitted from the modem). Jumpers S7, S9, and S10 are connected, all others being removed. The signal at each of the following 8266 output pins is low; E25, pin 3; E45, pins 13 and 4. If the character in the Receive Data Register is a sync character, the signal at each of the following 8271 output pins is low: E37, pin 11; E54, pins 7 and 9. The input signals at each comparator coincide and, thus, the COMPARE signal is high. As the first bit of the next character is shifted into the Receive Data Register, the COMPARE signal goes low. When this next character has been shifted in completely, the COMPARE signal again goes high, assuming that this character, likewise, is a sync character. The SYNC2 (1) signal is asserted, indicating that two successive sync characters have been received from the modem, and the interface requests a data break (see Paragraph 5.6 for further details and for a timing diagram that includes the COMPARE signal and the SYNC2 (1) signal).

Any further comparisons that are made during this transmission involve the received data and a test character stored in a memory location. Because the SYNC2 (1) signal remains high throughout the entire transmission, information on the MD4–11 lines is gated through selectors E25 and E45 for comparison with the received data. This comparison process is described in detail in Section 3, and Paragraph 5.11.

The character in the Receive Data Register is transferred to the PDP-8/E memory via the OMNIBUS DATA lines during the data break operation (unless the character is to be stripped). The RD TO BUS L signal gates the data through the 8235 4-bit logic elements to the DATA 4–11 lines. Note that DATA bits 4 and 5 are negated if the received data contains 6 bits per character, as has been assumed throughout this discussion. If the data in a memory location is to be compared with a received character of 6 bits, bits 4 and 5 of the selected location must be logic 0. The same reasoning applies to bit 4 when the received data contains 7 bits per character.

5.8 BREAK RQST, TRANSMIT LOGIC

When the modem is turned on, it begins to transmit SCT pulses. After the program has issued an SLCC IOT instruction, an SCT L pulse sets the RS flip-flop in the DP8-E (see Paragraph 5.5, Control Word Logic); the resulting SEND RQST signal causes the modem to activate the CLEAR TO SEND line. The CLEAR TO SEND signal enables the Break RQST, Transmit logic, Figure 5-10, to assert the TRQST L signal.

NAND gate E3 asserts the TRQST L signal if flip-flop E2 is set and if the MSB signal is high (the third input to E3 must be high if E2 is set). E2 can be set by an SCT-P L pulse if the T-GO flip-flop is set and if the CLEAR TO SEND signal has been asserted. The SGTT instruction sets the T-GO flip-flop; consequently, the transmit synchronization process is, essentially, a program function (note that the initial count of the XMIT CNT counter, E10, is unimportant). When the last character is transferred, the T-GO flip-flop is cleared and TRQST L is negated, unless the Idle mode was previously loaded into the Control Word logic. If this was done, E13 remains enabled and the TRQST L signal remains asserted, allowing continuous transmission from the last addressed core memory location.

When the TRQST L signal is asserted, the transmit data break operation can begin at the next occurrence of a TP4 pulse. Figure 5-4 is a timing diagram of such an operation and should be referred to when considering any of the transmit circuits. During the data transfer cycle, represented by the D9 L signal, the character to be transferred from memory is gated onto the MD lines. At TP3 time, the character is parallel-loaded into the XMIT DATA Register (Paragraph 5.9). The register is shifted by each succeeding SCT-P L pulse, until all six bits, for example, have been shifted out of the interface via the SD (Serial Data) line.

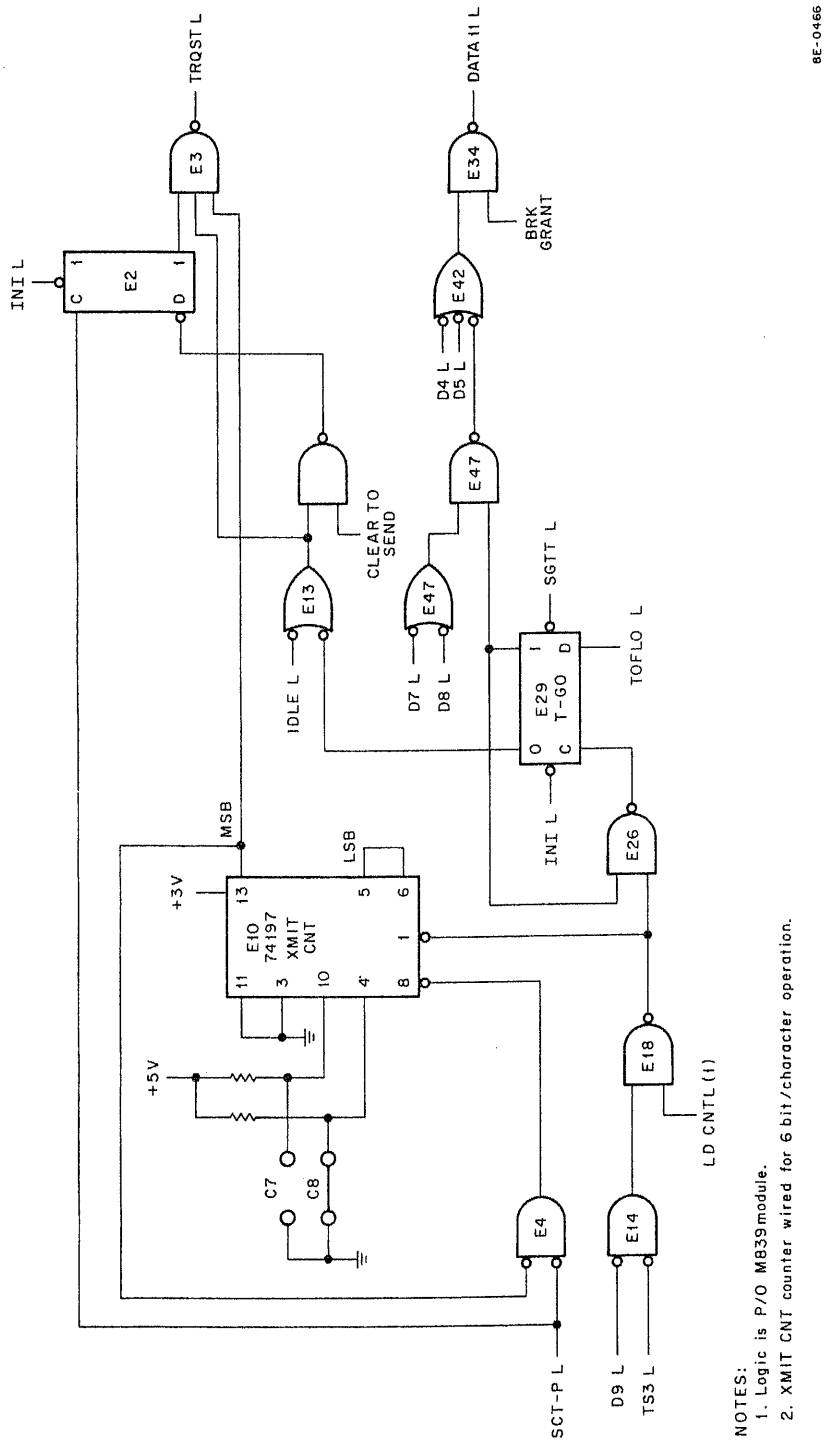
When TS3 of the data transfer cycle is first entered, the XMIT CNT counter, E10, is reset to the initial count of 0010 via NAND gate E18. Each SCT-P L pulse that shifts the XMIT DATA Register is counted by the XMIT CNT counter. Thus, the sixth pulse not only shifts the MSB of the character onto the SD line, but also causes the MSB of the counter to become logic 1. The TRQST L signal is asserted again and another break request can be generated.

Requests are generated until the last character is transferred. During the WC cycle immediately preceding the last data transfer, the OMNIBUS OVERFLOW L signal is asserted, causing the TOFLO (0) L to be asserted by the INT/Skip logic (see Figure 5-19). The T-GO flip-flop is then cleared when NAND gate E26 is enabled at the beginning of TS3. The TRQST L signal is negated, unless the Idle mode was programmed previously.

Note that when the T-GO flip-flop is set, NAND gate E34 asserts the OMNIBUS DATA 11 L signal during the CA and WC cycles (represented by the D7 L signal and the D8 L signal, respectively) of the transmit data break operation. The BRK Grant logic asserts the BREAK DATA CONT L signal throughout the transmit data break, thereby enabling the CPU gating to add MD bits and DATA bits and transfer the sum to memory. The process is represented symbolically as DATA+MD→MB. Because the MD11 L signal is asserted during the WC and CA cycles, both the word count and the current address are incremented and returned to memory.

If the Idle mode is entered after the T-GO flip-flop is cleared, a continuous transmission from the last addressed core memory location takes place. The D7 L and D8 L signals are repeatedly asserted, in turn, throughout such a transmission. Consequently, NOR gate E47 is enabled in the Idle mode. To prevent both the word count and the current address from being incremented, the 1-output of the T-GO flip-flop is applied to NAND gate E47. Thus, the word count and the current address are incremented only when T-GO is set.

The DATA 11 L signal is asserted during the CA and WC cycles (represented by the D4 L signal and the D5 L signal, respectively) of the receive data break operation, also. Again, the result is an incremented word count and transfer address. Because an Idle mode is not possible during a receive data break, the gating requires only the D4 L signal or the D5 L signal and the BRK GRANT signal to enable E34.



NOTES:
1. Logic is P/O M8039module.
2. XMIT CNT counter wired for 6 bit/character operation.

Figure 5-10 Break Request, Transmit

5.9 TRANSMIT DATA REGISTER LOGIC

The Transmit Data Register logic is shown in Figure 5-11. This logic transmits data from the OMNIBUS MD lines to the synchronous modem input.

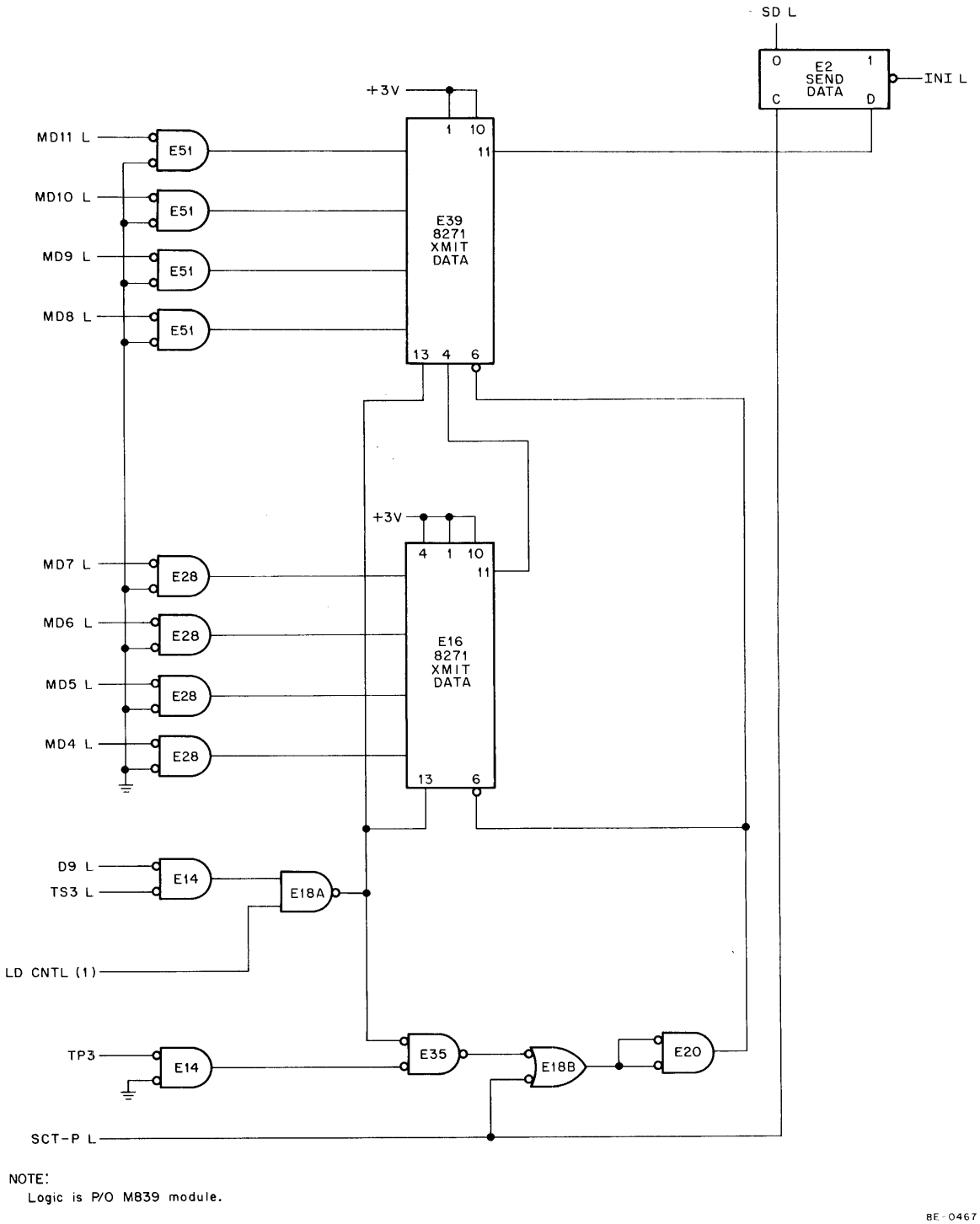


Figure 5-11 Transmit Data Register Logic

The character stored in the current address location is gated onto the MD lines during TS2 of the data transfer cycle. During TS3 of the cycle, NAND gate E18 is enabled, placing the Transmit Data Register in the parallel-load mode. At TP3 time, the register is clocked via the E35-E18B-E20 path, and the character on the MD lines is loaded into the register. When TS3 ends, 50 ns later, NAND gate E18A is disabled, placing the register in the right-shift mode. At this time the LSB of the character is applied to the D-input of the SEND DATA flip-flop. The first-occurring SCT-P L pulse after the data break ends clocks the SEND DATA flip-flop. This action places the LSB of the character on the SD L line. Simultaneously, the Transmit Data Register is right-shifted and the next character bit is applied to the SEND DATA flip-flop's D-input. Six SCT-P L pulses shift-out the register; the sixth pulse can cause the Break Request, Transmit logic to assert the TRQST L signal and another data break can begin.

5.10 BRK RQST LOGIC

The BRK RQST logic is shown in Figure 5-12. Either the RRQST L signal or the TRQST L signal can cause the INT STROBE signal to set the BRK RQST flip-flop. Note that the flip-flop is cleared when the OMNIBUS INITIALIZE signal is generated, if the ENABLE signal has been asserted by Control Word logic. If the ENABLE signal has not been asserted, the BRK RQST flip-flop is held in the clear state.

When the BRK RQST signal goes high, both the BRK IN PROG L and CPMA DISABLE L signals are asserted. The CPMA DISABLE L signal results in the CPU CPMA Register being disconnected from the OMNIBUS MA lines, while the BRK IN PROG L signal ensures that only data break devices place priority information on the OMNIBUS DATA lines during TS4.

When TS4 is entered, the BRK PRIORITY L signal is asserted; i.e., the priority of this interface is placed on the DATA BUS. Simultaneously, all other data break devices place their priorities on the DATA BUS. There can be as many as 11 other data break devices, including up to three DP8-Es, connected to the OMNIBUS via their respective interfaces. However, only six of these can have a higher priority than this modem.

Assume that there are, indeed, six data break devices that have a higher priority. This means that this DP8-E has priority 7. To establish this priority, one must ensure that the following jumpers on the two interface modules are connected: P7 on the M839 Module; P1 through P6 on the M866 Module (Figure 5-12). Thus, this interface places its priority on the DATA 6 line. The priority of all other data break devices is established by connecting selected jumpers on similar networks within the respective interfaces. The device having highest priority, which is usually the fastest device, places its priority on the DATA 0 line. The second-highest priority device uses the DATA 1 line, and so on. If, during a particular TS4, no other device is requesting a data break, or, if a requesting device is of lower priority than this interface, the DATA 0 L through DATA 5 L signals are negated. NAND gate E9 is enabled, causing E23 to assert the PRIORITY GO signal. This signal causes the break request to be granted. If any of the six higher-priority devices requests a data break at the same time as this interface, the device places its priority on its assigned DATA line. Thus, one, or more, of the DATA line signals, DATA 0 L through DATA 5 L, is asserted. NAND gate E9 is disabled and the PRIORITY GO signal remains negated. This interface must wait until the next TS4, when it again places its priority on the DATA BUS.

5.11 BREAK GRANT LOGIC

When the DP8-E asserts the PRIORITY GO signal, the Break Grant logic completes the CPU takeover process that was begun by the BRK RQST logic. The Break Grant logic is shown in Figure 5-13.

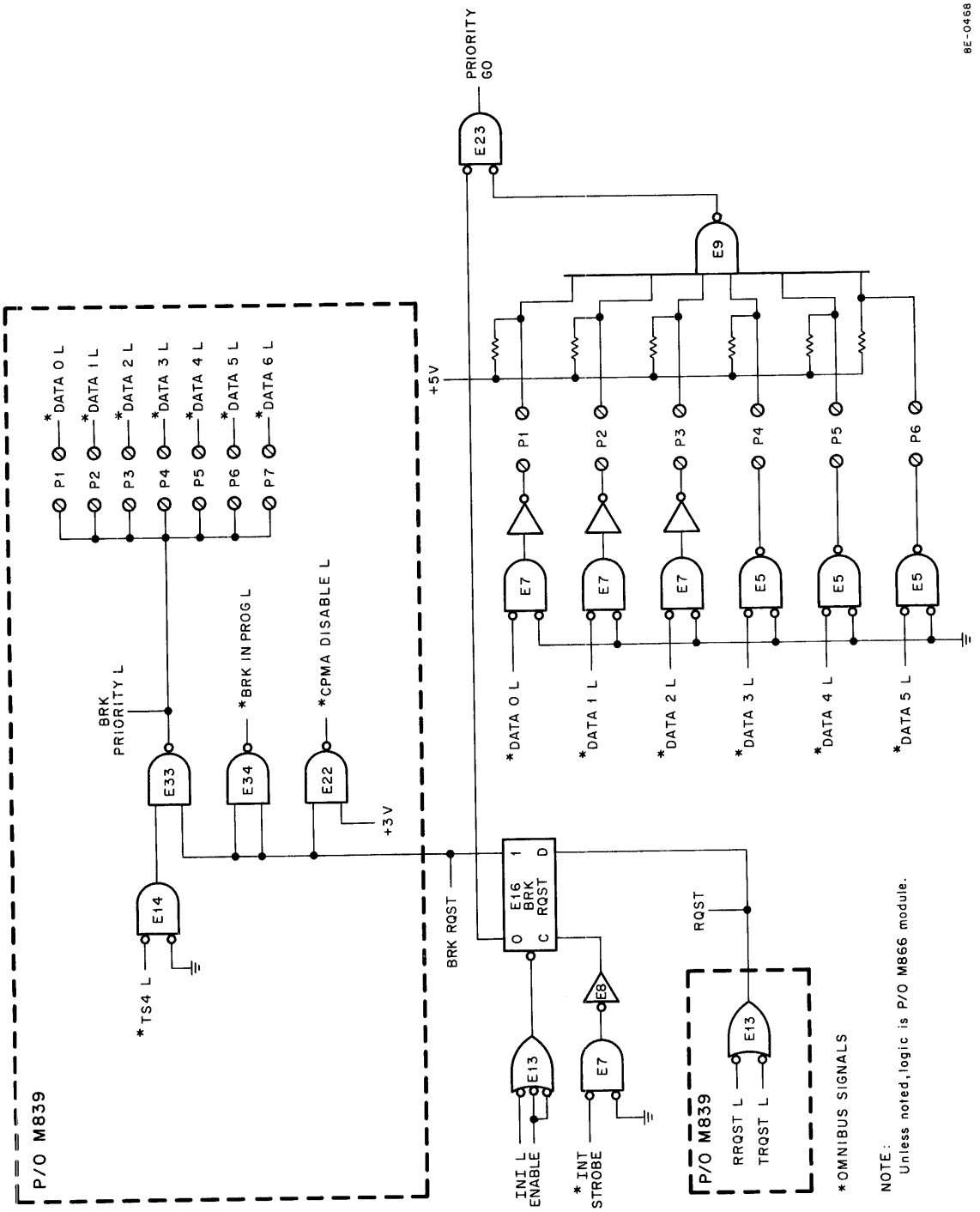


Figure 5-12 BRK RQST Logic

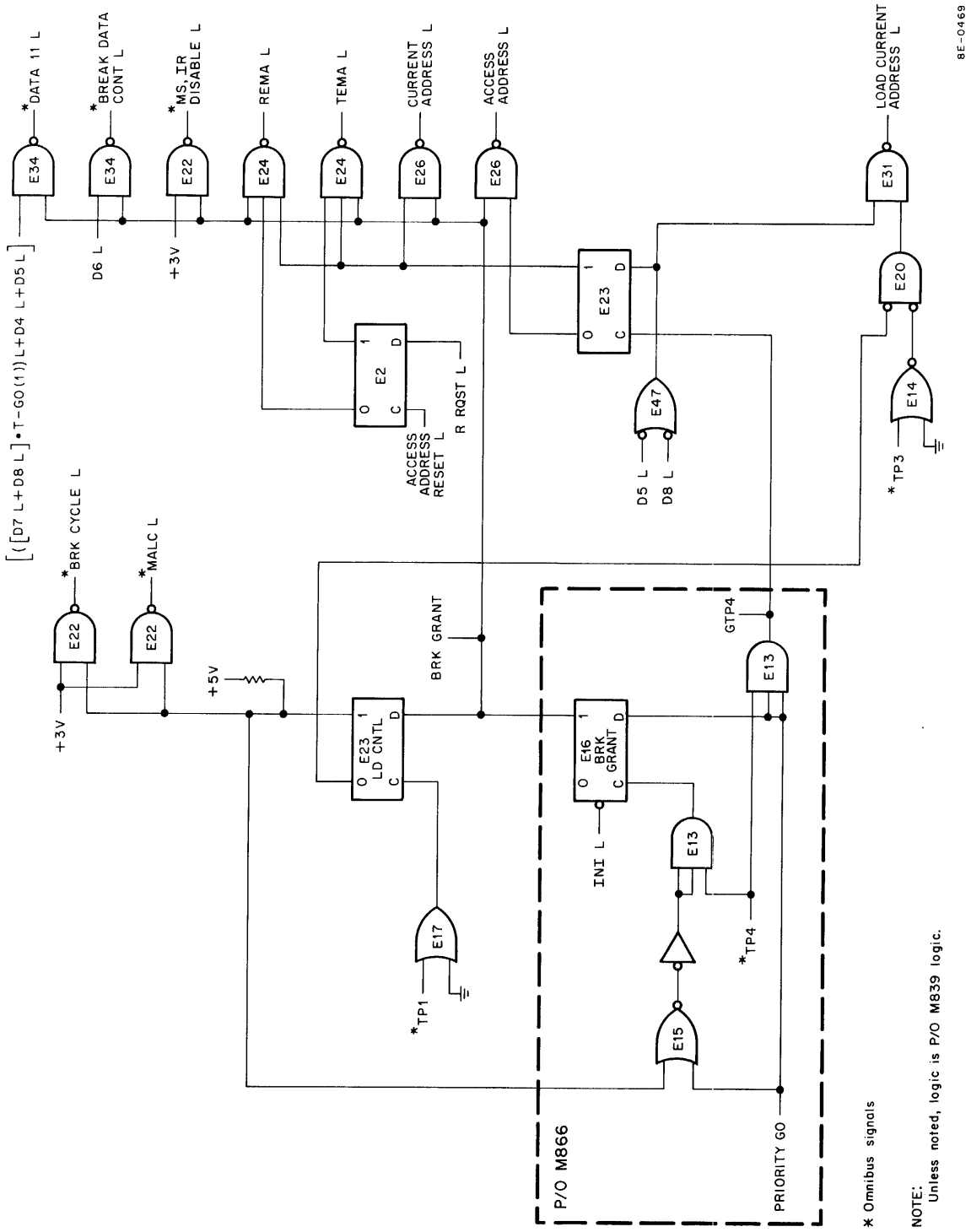


Figure 5-13 Break Grant Logic

The PRIORITY GO signal enables the TP4 pulse to set the BRK GRANT flip-flop and, also, to generate the GTP4 pulse. The 1-output of the flip-flop enables NAND gate E22 to assert the OMNIBUS MS, IR DISABLE L signal. This signal forces the CPU to enter the DMA state and disables the CPU IR Register. At the same TP4 time, the output of the CPMA Register is removed from the MA lines, the BRK RQST logic having asserted the CPMA DISABLE L signal at the previous INT STROBE time. The interface now specifies the address of the memory location that is to be affected during the next memory timing cycle, which is the first cycle of the data break operation.

This address is placed on the MA lines by the Current/Access Address Register logic, which is discussed in detail in Paragraph 5.13. Briefly, this logic places either an access address or a transfer address on the MA lines. Because the modem is a 3-cycle device, the data transfer cycle is preceded by at least 2 cycles of operation, word count (WC) and current address (CA). If the data character is to be transferred from the DP8-E to memory — a receive break request — the WC and CA cycles are preceded by 4 test character recognition cycles. Test characters, the word count, and the current address are stored in memory locations specified by access addresses. Thus, the first cycle of a Data Break operation, whether of a Receive Break Request or of a Transmit Break Request, involves an access address. Although this address is placed on the MA lines by the Current/Access Address Register logic, the Break Grant logic, by asserting either the ACCESS ADDRESS L signal or the CURRENT ADDRESS L signal, determines which type of address is selected.

Thus, when the BRK GRANT flip-flop is set at TP4 time, NAND gate E26 asserts the ACCESS ADDRESS L signal (flip-flop E23 is cleared by the GTP4 pulse). Simultaneously, NAND gate E34 asserts the BREAK DATA CONT L signal, which provides a convenient method of updating the word count and the current address, as well as re-writing recognition characters in memory. This method is explained fully later in this section.

At TP1 time of the next memory cycle, the LD CNTL (Load Control) flip-flop is set, causing NAND gates E22 to assert the BRK CYCLE L signal and the MALC L signal. The BRK CYCLE L signal is applied to the programmer's console and can be monitored on the display panel. The MALC L signal prevents the CPMA Register from being clocked during the data break operation (see Volume 1, Paragraph 3.34.1 for details). During the data break cycle begun by this TP1 pulse, the information in the access address is placed on the MD lines. The type of information depends on the type of break request that is being carried out.

If a receive break request is starting, the information on the MD lines is a test character. This character is compared to the received character in the Receive Data Register logic. When the comparison has been made, the test character is returned to memory during the write half of the timing cycle. The re-write in memory is made possible by the BREAK DATA CONT L signal that results in the CPU operation DATA+MD to the MB. Since the DATA lines carry no information at this time, only the information on the MD lines, the recognition character, is returned to the memory location. If the received character compares bit-for-bit with the test character, an interrupt request can be generated by the interface, or the received character can be stored with no other action, or the data break can be terminated immediately (the character is "stripped"). If a successful comparison is made and the character is not stripped, or if the received character and the test character differ, the data break operation continues. During each of the next three break cycles, a new access address is provided by the Access Address Counter logic (Paragraph 5.12), and a new test character is placed on the MD lines and compared to the received character. If a successful comparison occurs between the received character and one (or more) of the test characters, that fact is retained by a flip-flop in the Detected Character Register logic described in Paragraph 5.15.

During the 5th and 6th cycles of the receive break request data break, the information in the memory location defined by the access address is the word count and the current address, respectively. The word count and the current address are placed on the MD lines in turn. During each timing cycle, designated D4 L for WC and D5 L for CA, NAND gate E34 in the Break Grant logic asserts the DATA 11 L signal. Thus, the DATA+MD to the MB

operation forced by the BREAK DATA CONT L signal increments both the word count and the current address. At TP3 time of the CA cycle, the Break Grant logic asserts the LOAD CURRENT ADDRESS L signal. At TP4 time flip-flop E23 is set, causing the ACCESS ADDRESS L signal to be negated, while the CURRENT ADDRESS L signal is asserted. The combination of the LOAD CURRENT ADDRESS L signal and the CURRENT ADDRESS L signal causes the current address to be gated through the Current/Access Address Register logic to the MA lines.

During the data transfer cycle, D6 L, the RD TO BUS L signal is asserted in the BRK RQST Receive logic. The character in the Receive Data Register is gated onto the DATA lines and placed in the memory location specified by the current address. The data break ends after this timing cycle, and six more SCR-P L pulses must be received before a new break request can be generated.

If a transmit break request is carried out, only the WC and CA cycles precede the transfer cycle. The same OMNIBUS control signals are asserted by the Break Grant logic; differences occurring during the transmit operation can be noted in the timing diagram, Figure 5-4.

5.12 ACCESS ADDRESS COUNTER LOGIC

The Access Address Counter logic is shown in Figure 5-14. The logic includes the Increment Enable flip-flop, E57, the Increment Counter, E52, and a BCD-to-Decimal Decoder, E46.

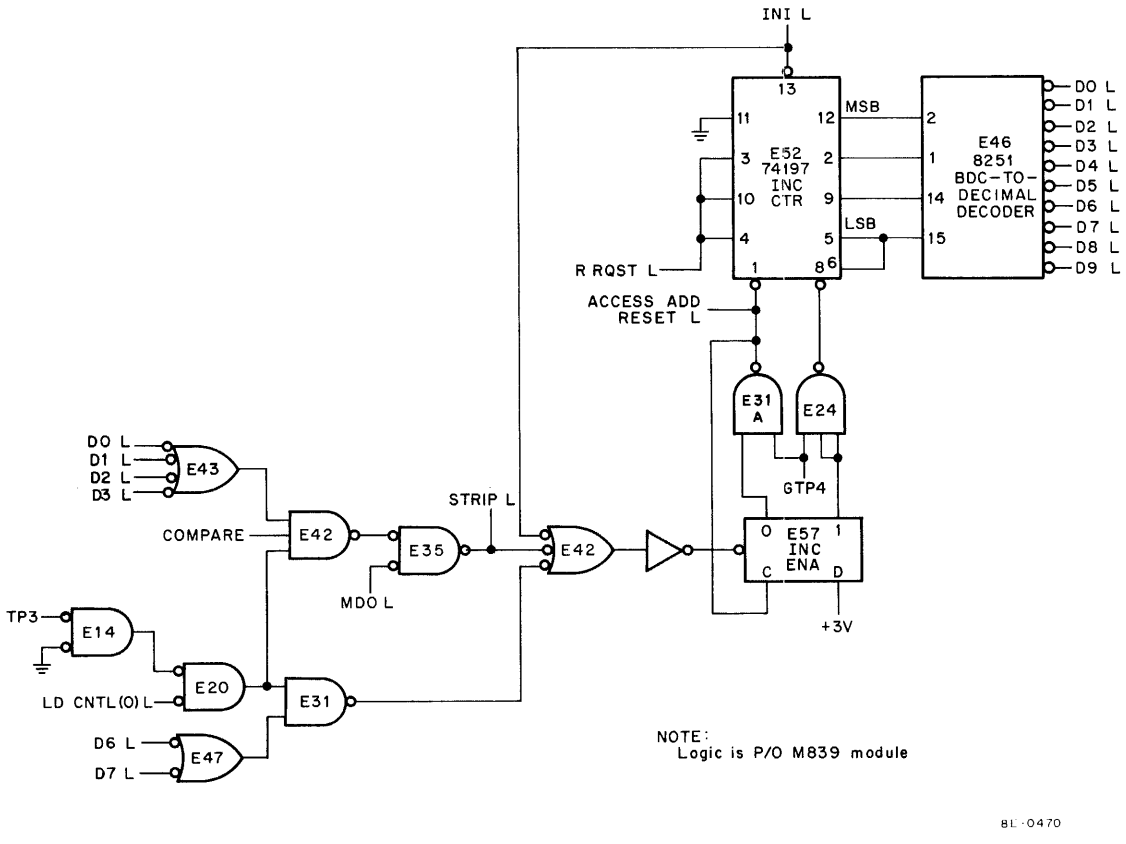


Figure 5-14 Access Add Counter Logic

When the OMNIBUS INITIALIZE signal is generated, the resulting INI L signal clears the Increment Counter and the Increment Enable (INC ENA) flip-flop. The BCD output from E52 is 0000; thus, E46 asserts the D0 L signal. Unless a break request is generated, the Increment Counter, the Decoder, and the flip-flop remain in the state described.

If the DP8-E requests a data break and has highest priority, the TP4 pulse immediately preceding the first data break cycle (the same TP4 pulse that sets the BRK Grant flip-flop) generates a GTP4 pulse. The resulting ACCESS ADDRESS RESET L signal from NAND gate E31A sets the INC ENA flip-flop. This signal is also applied to the count/load input of the Increment Counter, E52. A negative-going signal at this input loads the counter with the information present at the data inputs, pins 3, 4, 10, and 11. If this is a receive data break operation, the RRQST L signal is asserted and E52 remains in the 0000 output state. However, assume that this is a transmit data break operation. The RRQST L signal is not asserted. Therefore, E52 is loaded with a BCD count of 0111; E46 decodes this to assert the D7 L signal. When this signal is asserted, the access address 7727 is placed on the MA lines by the Current/Access Address Register logic. This is the access address of the word count location. Thus, the first cycle of the transmit data break operation is the WC cycle.

When the word count has been incremented and returned to memory, TP4 of the WC cycle generates another GTP4 pulse. Because the first GTP4 pulse sets flip-flop E57, the second GTP4 pulse enables NAND gate E24, rather than E31. E52 is clocked, the BCD count is incremented to 1000, and E46 asserts the D8 L signal. When this signal is asserted, access address 7730 is placed on the MA lines and the CA cycle is entered. The address in location 7730 is incremented to produce the current address. This address, rather than an access address, is placed on the MA lines at TP4 of the CA cycle. At the same TP4 time, E52 is again clocked, the BCD count is incremented to 1001, and E46 asserts the D9 L signal. This signal is asserted throughout the data transfer cycle and is used to gate the data character into the Transmit Data Register, to end the transmit break request (by negating the TRQST L signal), and to clear the INC ENA flip-flop at TP3 time of the transfer cycle. Because a GTP4 pulse is not generated during the data transfer cycle, the Increment Counter is not clocked at the end of this cycle. Thus, the data break operation ends with E52 holding the BCD count of 1001 and E46 asserting the D9 L signal. This condition exists until a new data break operation, either receive or transmit, is initiated.

If the next data break operation is of the transmit type, location 7727 is again addressed to begin the WC cycle. However, a receive data break request would cause the BCD count in E52 to change from 1001 to 0000 at the first GTP4 time. Therefore, location 7720, which contains a test character, is addressed by an access address. At each GTP4 time of the receive data break operation, the Increment Counter is clocked. The decoder asserts the D0 L through D6 L signals in succession. The D0 L through D3 L signals are asserted during the four test character cycles, D4 L is asserted during the WC cycle, and D5 L is asserted during the CA cycle. When D6 L is asserted, the current address, which was loaded into the Current/Access Address Register logic during the CA cycle, is placed on the MA lines. The D6 L signal is asserted throughout the data transfer cycle and enables TP3 of the cycle to clear the INC ENA flip-flop. Because a GTP4 pulse is not generated during the data transfer cycle, the Increment Counter is not clocked at the end of the cycle. Thus, the data break operation ends with E52 holding the BCD count of 0110 and E46 asserting the D6 L signal. This condition exists until a new data break operation, either receive or transmit, is initiated.

Note that the INC ENA flip-flop can be cleared in three ways. Two of these have been indicated. The third way of clearing the flip-flop is by causing a detected character to be stripped. If a test character and the received data character are the same, the COMPARE signal is asserted. If the 0-bit of the test character is logic 1, the MD0 L signal causes NAND gate E35 to assert the STRIP signal. This signal causes the receive data break operation to be terminated at the end of the current test character cycle and clears flip-flop E57. E52 and E46 remain in the state that represents the last cycle completed. For example, if the test character in location 7722 compared successfully with the received character, the data break operation would be terminated with E52 holding a BCD count of 0010 and E46 asserting the D2 L signal.

5.13 CURRENT/ACCESS ADDRESS REGISTER LOGIC

The Current/Access Address Register logic is shown in Figure 5-15. This logic places a memory address on the OMNIBUS MA lines. Since two types of addresses, Access and Current, are encountered during a data transfer, a method of selecting one or the other is required. This requirement is fulfilled by the DEC 8235 ICs E48, E21, and E1, which are 4-bit logic elements.

The type of address gated to the MA lines by these ICs depends on the control signal that is asserted by the Break Grant logic. If the CURRENT ADDRESS L control signal is asserted, pin 7 of each IC is low, and the current address, which is applied to the inverting input of the IC, is placed on the MA lines. On the other hand, if the ACCESS ADDRESS L control signal is asserted, pin 9 is low, and the access address, which is applied to the noninverting input (indicated by the circle), is placed on the MA lines.

An access address is formulated from two sources. The state of each of the first eight bits, MA0 through MA7, is determined by the logic in Figure 5-15. Each of MA bits 0 through 4 is logic 1, since the IC inputs corresponding to these MA bits are grounded. The user determines the state of each of MA bits 5, 6, and 7 by selectively connecting or removing one or more of jumpers A5, A6, and A7. The selection depends on the channel access address assignment. For example, if the logic in Figure 5-15 represents Channel 1, access addresses 7720 through 7725, 7727, and 7730 are assigned. Therefore, jumpers A5 and A7 are connected, while A6 is disconnected.

The state of each of the last four bits of the access address is determined in the Access Address Counter logic. During each data break operation, the Increment Counter in that logic counts from 0000 to 0110 (receive data break) or from 0111 to 1001 (transmit data break). The count is incremented at the end of each timing cycle of the data break. For example, consider a receive data break. The Increment Counter holds a count of 0000 just before the first timing cycle of the data break is entered. Thus, each of MA bits 8 through 11 is logic 0 (the signal at each noninverting input of E48 is high). The first memory location addressed is 7720. At the end of the first data break cycle, the Increment Counter is incremented. MA bit 11 becomes logic 1, and the second memory location addressed is 7721. In this manner, memory locations 7722, 7723, and 7724 are successively addressed.

When the Increment Counter increments to 0101 at the end of the fifth data break cycle, access address 7725 is placed on the MA lines. The next data break cycle is the CA cycle. During the CA cycle, the current address that is stored in location 7725 is gated onto the MD lines and incremented. The Break Grant logic asserts the LOAD CURRENT ADDRESS L signal that loads the current address into the register consisting of the DEC 8271 ICs E7, E12, and E50. At the end of the CA cycle, the ACCESS ADDRESS L signal is negated and the CURRENT ADDRESS L signal is asserted. The outputs from the register, which represent the current address, are placed on the MA lines. Thus, during the next (seventh) cycle a data character is transferred to the memory location specified by the current address.

Note that the contents of the register can be gated to the DATA lines by the SRTA IOT instruction. This instruction is used for maintenance and program debugging.

5.14 LOAD FIELD LOGIC

The PDP-8/E basic 4K of memory can be extended in 4K increments to a maximum of 32K. Therefore, a 15-bit address is required to specify completely a memory location. The three most significant bits of the 15-bit address are carried by the EMA 0, EMA 1, and EMA 2 lines, the EMA 0 bit being the most significant bit.

A data break option can use an extended memory address only when specifying the location that is to take part in the data transfer. The word count and the current address locations (and test character locations when considering the DP8-E) must be stored in memory field 0, the basic 4K.

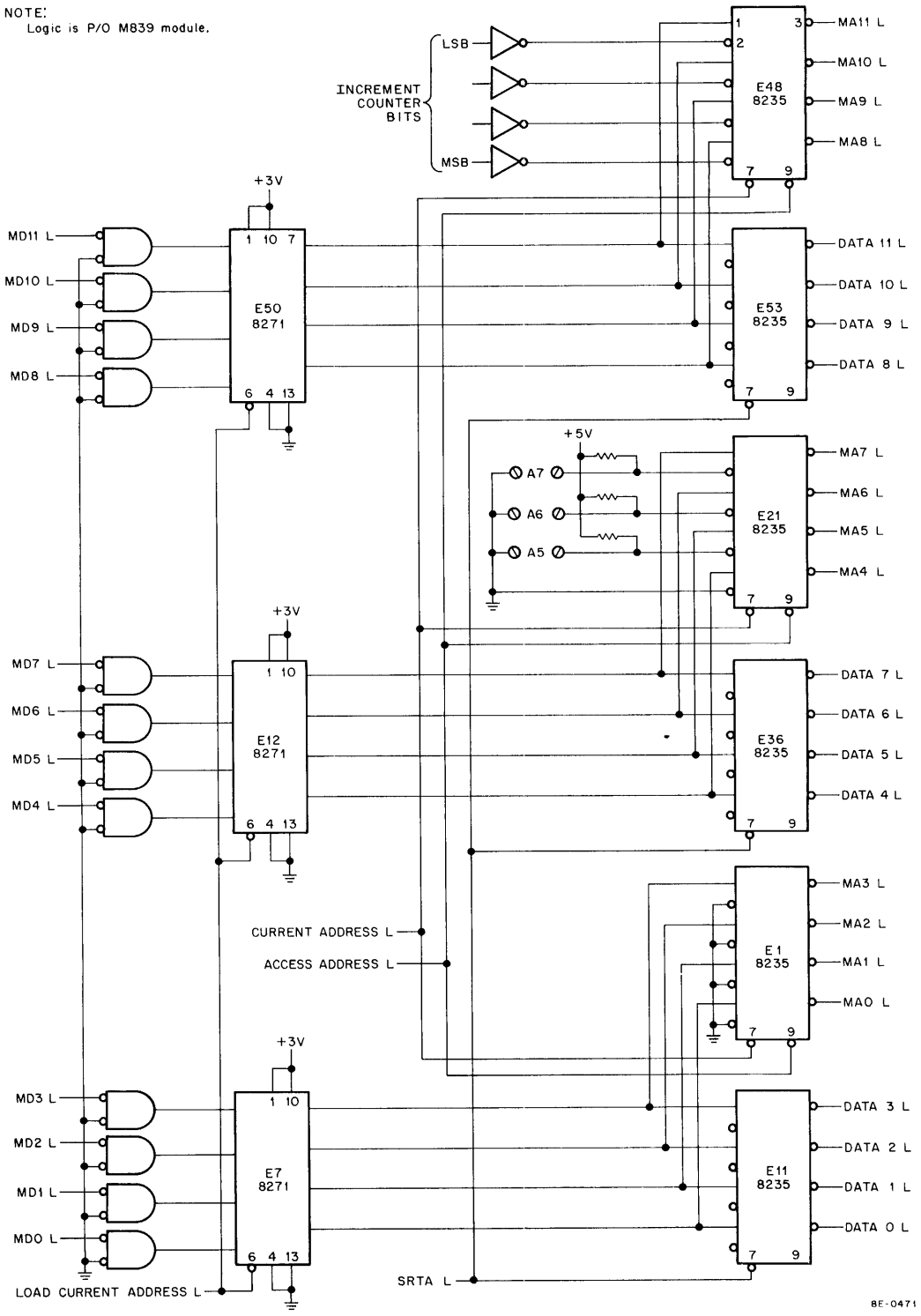


Figure 5-15 Current/Access Address Register Logic

Some data break devices can directly address an extended memory field via the EMA lines. However, if such a field is used with a synchronous modem, the field can be addressed only under program control. The load field logic, shown in Figure 5-16, enables the programmer to select the memory field to or from which a data character is to be transferred.

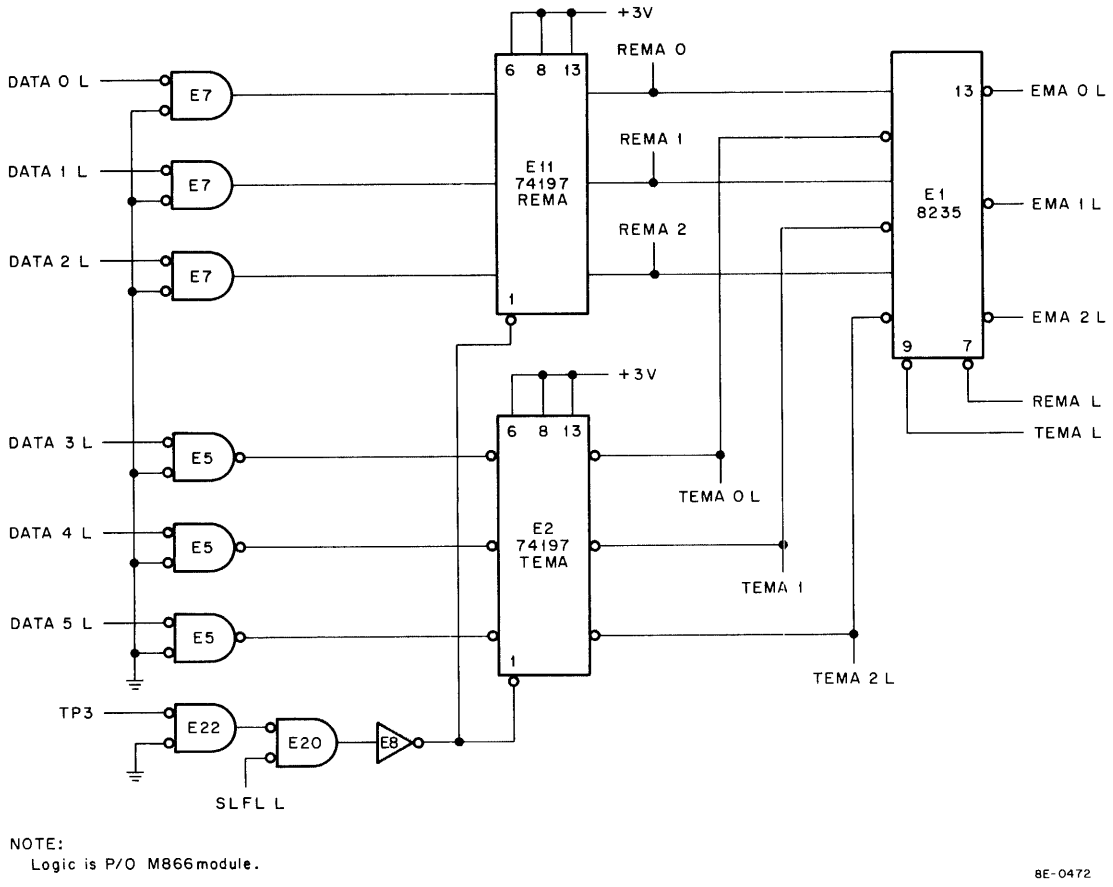


Figure 5-16 Load Field Logic

The program can specify a separate field address for the receive data break and the transmit data break operations. AC Register bits 0, 1, and 2 are loaded with the receive extended memory field address, while AC bits 3, 4, and 5 are loaded with the transmit extended memory field address. These addresses are gated onto the DATA 0–5 lines by the SLFL IOT instruction. At TP3 time of this instruction, these addresses are parallel-loaded into DEC 74197 shift registers, the receive field address into E11, and the transmit field address into E2.

If a receive data break operation is being carried out, the Break Grant logic asserts the REMA L signal throughout the timing cycle in which the received character is gated onto the DATA lines. The REMA L signal gates the outputs from E11 onto the EMA lines (the E11 outputs are inverted by selector E1). Thus, the character gated onto the DATA lines by the RCV Data Register logic is transferred to a location in the extended memory field specified by the EMA bits. If the PDP-8/E has only 4K of memory, the EMA bits are logic 0.

The TEMA L signal, asserted throughout the data transfer cycle of a transmit data break operation, gates the output from E2 onto the EMA lines. Therefore, the character to be transferred to the modem is gated onto the MD lines from an extended memory field location and shifted onto the SD line by the Transmit Data Register logic.

5.15 DETECTED CHARACTER REGISTER LOGIC

The Detected Character Register logic is shown in Figure 5-17. The logic is used to generate an interrupt request if a received character matches a test character, and to identify which test character the received character matched. For example, assume that the received character compares, bit-for-bit, with the test character stored in location 7722. This location is addressed at the same time that the D2 L signal is asserted by the Access Address Counter logic. The D2 L signal is asserted because the Increment Counter in that logic has been incremented to a count of 0010 (the Increment Counter is included in Figure 5-17 for information).

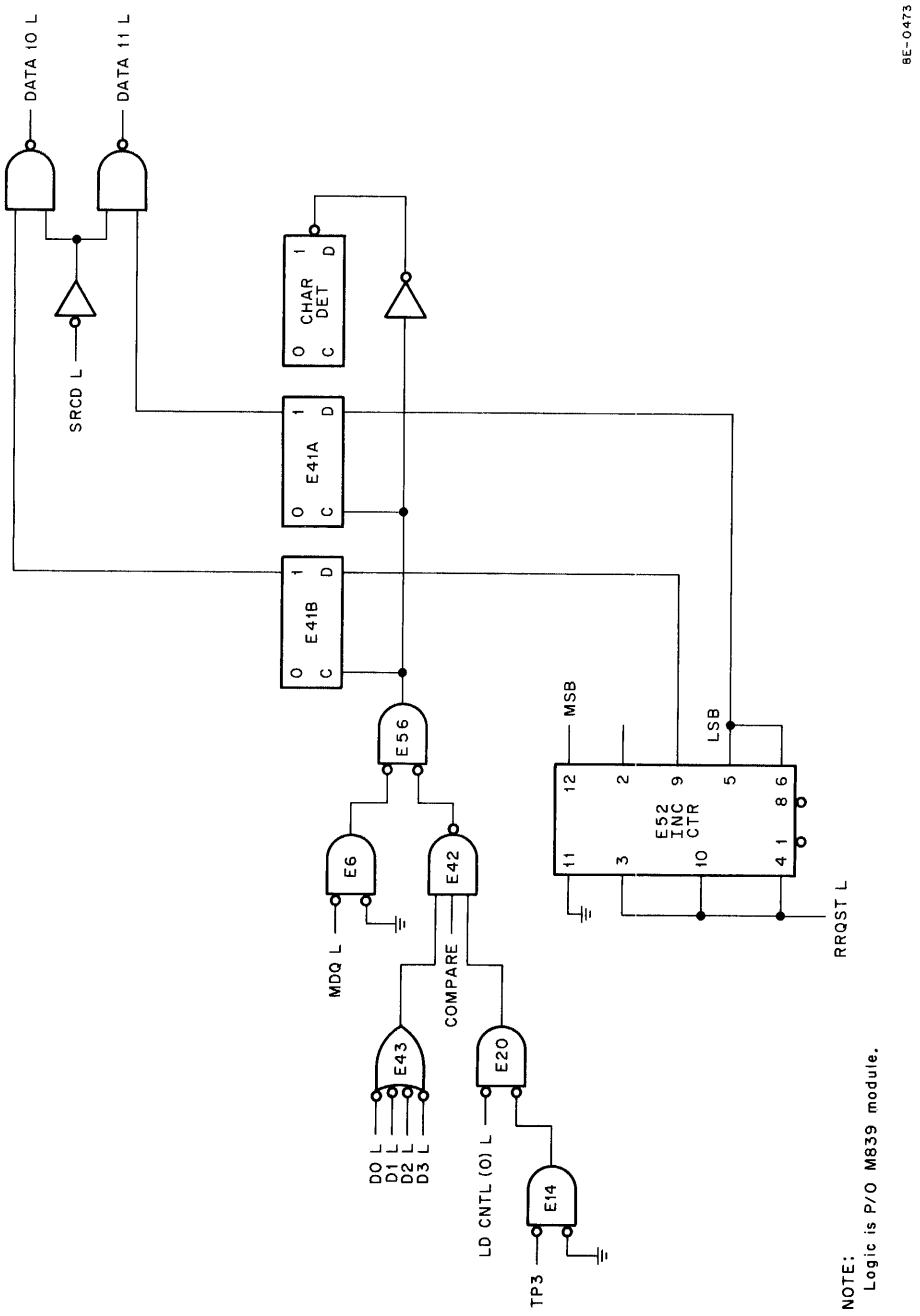
When the test character in location 7722 is gated onto the MD lines near the beginning of the third data break timing cycle, the COMPARE signal is asserted in the Receive Data Register logic. At TP3 time NAND gate E42, Figure 5-17, is enabled. If the 0-bit of the test character is logic 0 (i.e., the MD0 L signal is logic 0), the received character is to be stored. NAND gate E56 is enabled. Its output clocks the two E41 flip-flops and sets the CHAR DET flip-flop via the inverter. The D-input of E41 is high because of the count in the Increment Counter; therefore, the E41B flip-flop is set. The E41 flip-flops hold the count of 10 for one character period; i.e., until a new character has been completely shifted into the Receive Data Register. Note that if the received character is to be stripped, none of the three flip-flops is set. If the same test character is stored in more than one location, and if the received character matches this test character and is to be stored, the E41 flip-flops contain the highest location.

The 0-output of the CHAR DET flip-flop can cause an interrupt request to be generated when the data break has ended. An appropriate program routine is entered, and the SRCD IOT instruction gates the identifying count onto the DATA 10 and DATA 11 lines for further action.

5.16 INT/SKIP LOGIC

The INT/Skip logic (RING, CARRIER/AGC) is shown in Figure 5-18. The logic enables the RING and CARRIER/AGC signals to cause program interrupts and/or program instruction skips.

When the DP8-E senses a ringing signal from the modem, it generates a Ring flag, indicating that a modem-to-computer transmission is to take place. This signal is applied to the interface at pin J1X. If a jumper is in place at location X (the jumper is removed if the modem is a Bell 301 type), NAND gate E18 is disabled. The positive transition at the output of the gate sets the RING flip-flop. If the interface has been enabled under program control, setting the RING flip-flop causes NAND gate E19D to assert the OMNIBUS INT RQST L signal. The computer enters the interrupt servicing routine to determine the identity of the requesting device. The SSRG instruction in the routine causes the IOT Decoder logic to generate the SSRG L signal throughout TS3 of the instruction. The SSRG L signal causes NAND gate E19C to assert the OMNIBUS SKIP L signal; thus, at TP3 time the CPU SKIP flip-flop is set and the program instruction following SSRG is skipped. When the SSRG L signal is negated at the end of TS3, the RING flip-flop is cleared. The program proceeds to a subroutine that sets up the WC and CA Registers and then either waits for the modem to generate a CARRIER/AGC signal or exits the subroutine.



NOTE:
Logic is P/O M839 module.

Figure 5-17 Detected Character Register Logic

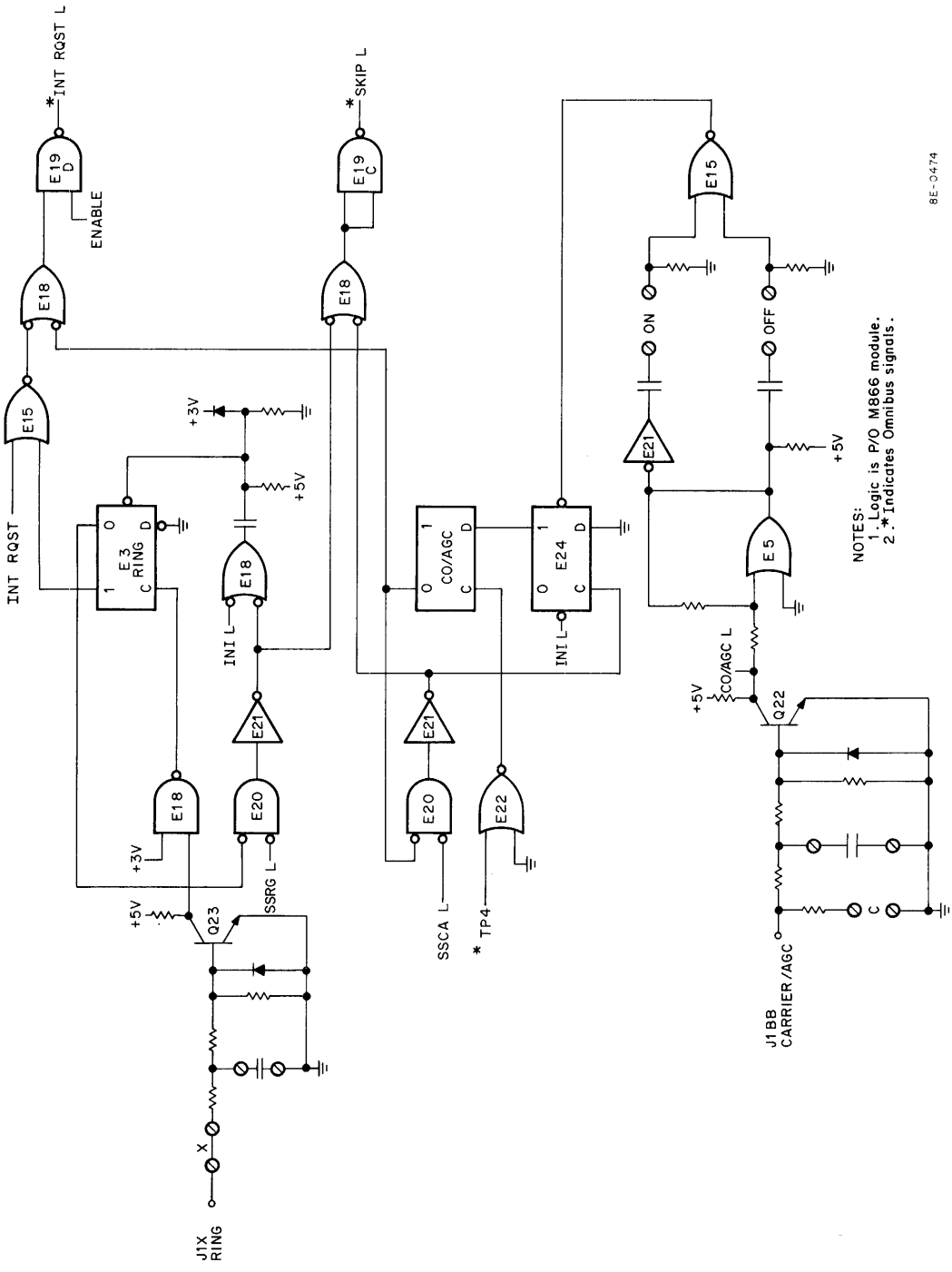


Figure 5-18 INT/Skip Logic (RING, CARRIER/AGC)

If a computer-to-modem transmission is to take place, a RING signal is not generated. Instead, a program subroutine sets up the registers and then enables the modem SCT L signal to set the RS flip-flop in the Control Word logic. The setting of this flip-flop causes the interface to generate the SEND RQST signal that is applied to the modem. The program then either waits for the modem to generate a CARRIER/AGC signal or exits the subroutine.

When the modem generates the CARRIER/AGC signal, whether a transmit or receive operation, the CO/AGC L signal is applied to Schmitt trigger E5. The output signal from E5 takes two paths; only the path to the ON jumper is significant when the CARRIER/AGC signal is generated at the beginning of a transmission. If the jumper is in place, NOR gate E15 is enabled, and its output sets flip-flop E24. The path leading to the OFF jumper is significant when the CARRIER/AGC signal is negated. This happens when TERM READY has been negated by either receiver or transmitter, or when a modem malfunction has interrupted the data stream. If the jumper is in place when this occurs, NOR gate E15 is enabled and flip-flop E24 is set again. Thus, the circuit can respond to either or both transitions of the CARRIER/AGC signal.

When E24 is set, the next occurring TP4 pulse sets the CO/AGC flip-flop, and E19D can assert the INT RQST L signal. When the SSCA L signal goes low, the SKIP L signal is asserted, and the CPU SKIP flip-flop is set at TP3 time. The SSCA L signal is negated at the end of TS3, causing flip-flop E24 to be cleared. At TP4 time the CO/AGC flip-flop is cleared, causing the INT RQST L signal to go high.

The INT/Skip logic (WC overflow, character detected, and bus error) is shown in Figure 5-19. The logic enables an interrupt request to be generated when one of the events in the parentheses occurs.

During the WC cycle immediately preceding the last data transfer cycle, the OVERFLOW L signal is asserted by the CPU. One or the other of AND gates E49A and E49C is enabled, setting either flip-flop E27 or flip-flop E29, respectively. The 0-output of the set flip-flop enables NOR gate E43 to assert the INT RQST signal. This signal causes NAND gate E19D, Figure 5-19, to assert the OMNIBUS INT RQST L signal. The interrupt request is recognized by the CPU during the first timing cycle following the data transfer cycle, provided another data break device does not assume control of the CPU. When the program enters the interrupt servicing routine, either the SSRO or the SSTO IOT instruction causes the SKIP L signal to be asserted and clears the flip-flop that caused the interrupt request. The program then proceeds to a subroutine that services the request.

If a test character has been detected in the transmission, the CHAR DET flip-flop is set; the 0-output enables NOR gate E43. When the data break has ended, the SSCD IOT instruction in the servicing routine causes an instruction skip after clearing the CHAR DET flip-flop. The program proceeds to a subroutine to determine the identity of the detected character.

The third event that can cause an interrupt request is a bus error. If either the TRQST L signal or the RRQST L signal is asserted and a serial clock pulse is received by the interface, the BUS ERROR flip-flop is set. Such an occurrence indicates that the particular break request was not serviced by the computer because of an overloaded or inoperative break system. Again, an IOT instruction, SSBE, in the servicing routine causes the SKIP L signal to be asserted and clears the flip-flop that caused the interrupt request.

5.17 READ STATUS/TEST PULSE LOGIC

The Read Status logic is shown in Figure 5-20. Significant signals in the interface are gated onto DATA lines 0 through 7 by either of two control signals, SRS1 L and SRS2 L. The information on the DATA lines is loaded into the AC Register at TP3 time. The logic and IOT instructions SRS1 and SRS2 are intended primarily for maintenance and program debugging, but can be used to monitor the state of CARRIER, EMA, etc.

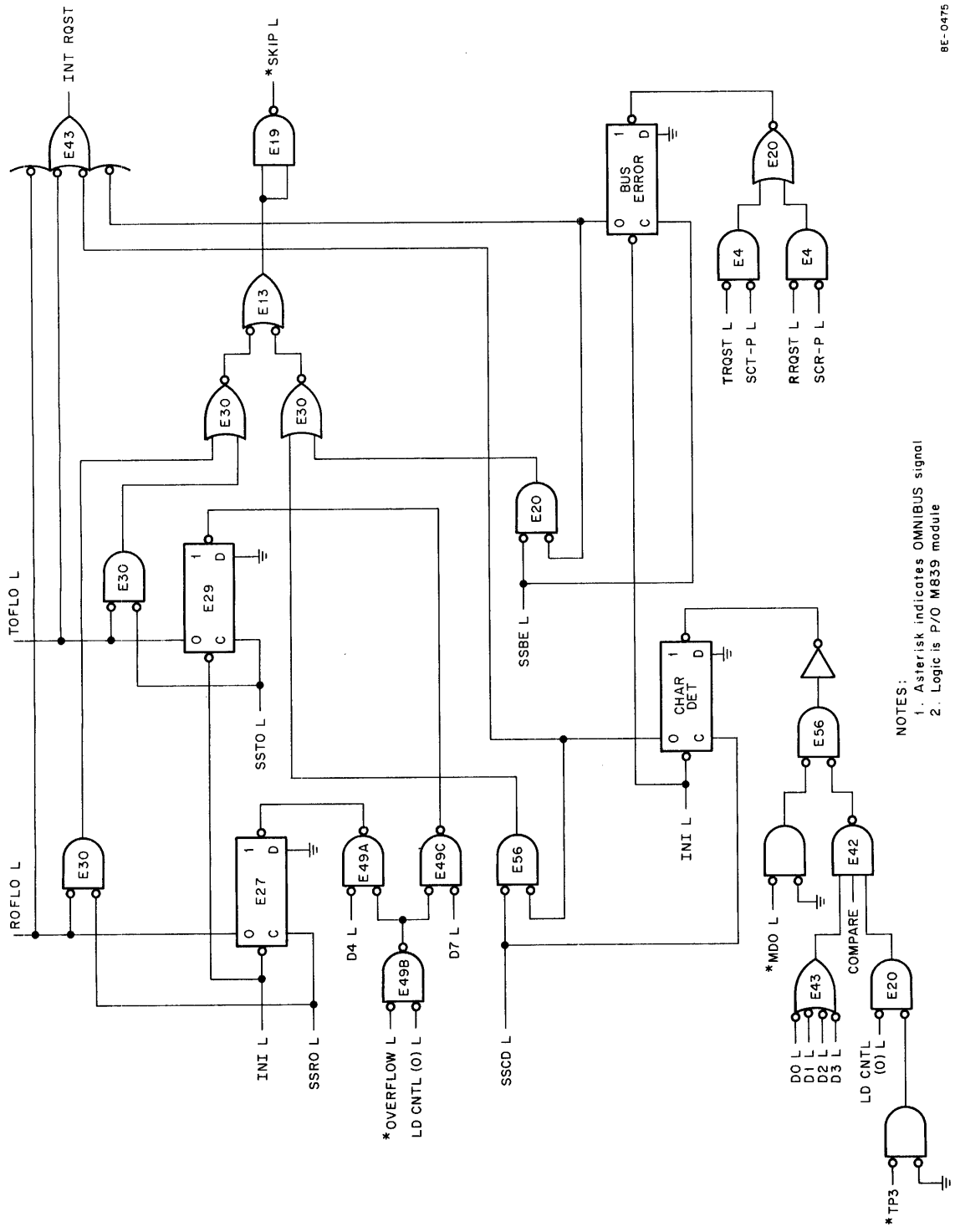


Figure 5-19 INT/Skip Logic (Character Detected, Bus Error, WC Overflow)

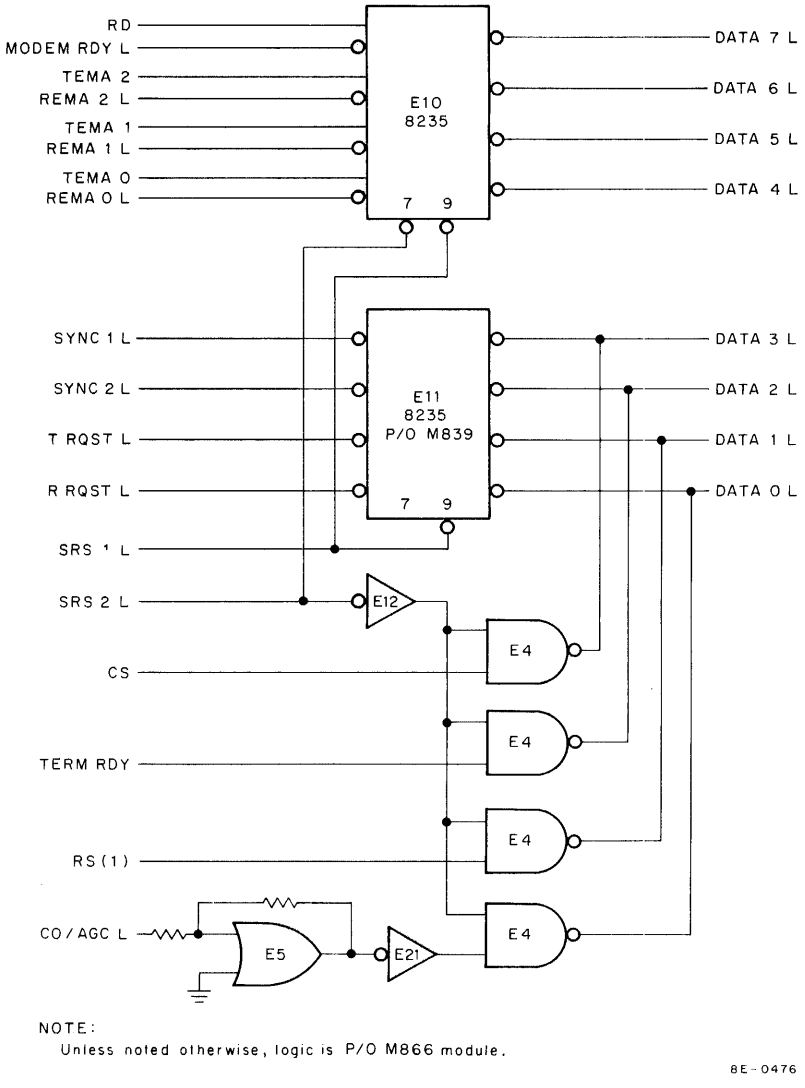


Figure 5-20 Read Status Logic

Another instruction that can be used during maintenance is the SRCD instruction that is normally used to gate detected character information onto the DATA 10 and DATA 11 lines. When used with the Test Pulse logic, shown in Figure 5-21, the SRCD instruction can cause a single clock pulse to be generated. This pulse is routed through a test connector and returned to both the SCR and SCT input lines of the interface, enabling single-step testing of the receive and transmit circuits.

The AC0 bit must be logic 1 when the SRCD instruction is issued. NAND gate E23, Figure 5-21, sets the E23 NOR-gate flip-flop. This flip-flop is cleared by the BTP4 pulse; thus, a negative pulse of approximately 600-ns width is produced at the emitter of Q1 and gated to the emitter of Q2, as a positive pulse. If a jumper is in place at location F, and if the test connector P1 is connected to J1, the pulse is returned on the SCR and SCT lines (see Section 5, Maintenance, for further information about the test connector).

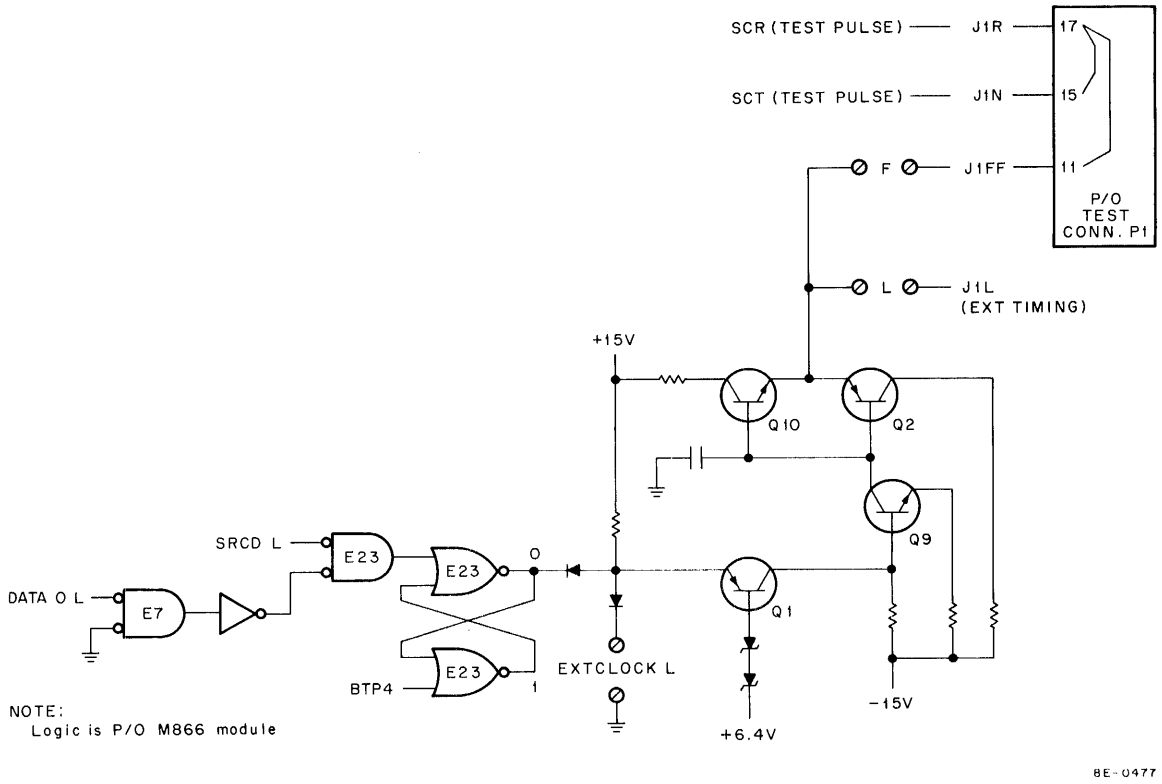


Figure 5-21 Test Pulse Logic

The four-transistor gating circuit can also be used to gate an external clock to the modem, which has an external timing mode. The external clock is applied at the input designated EXT CLOCK L (etched on the printed circuit board as EXT CLOCK), and a jumper must be installed at location L.

5.18 LEVEL CONVERSION CIRCUITS

The M866 Module contains the DP8-E level conversion circuits. Figure 5-22 illustrates the method used to convert either EIA or current mode signals to the TTL levels required by the DP8-E. The CLEAR TO SEND signal conversion circuit is used as an example.

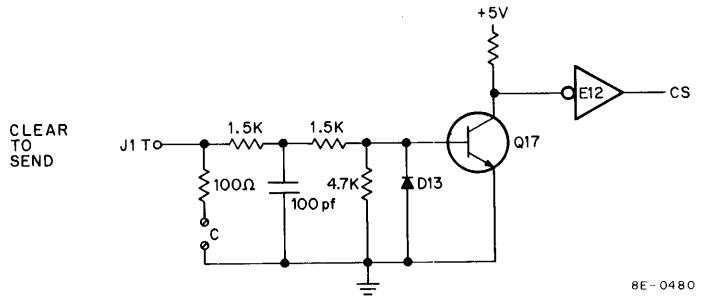


Figure 5-22 DP8-E Input Circuit (Receiver)

If the CLEAR TO SEND signal is an EIA-type signal (bipolar), a "mark" is represented by a voltage level of -5V to -15V; a "space" is represented by a voltage level of +5V to +15V. A mark, which indicates that the CLEAR TO SEND signal is not asserted, turns off Q17, and the CS signal is negated (logic 0); a space turns on Q17, thereby asserting the CS signal.

If the CLEAR TO SEND signal is a current mode signal, a jumper is connected at location C. An input current of less than 5 mA represents a mark, which indicates that the CLEAR TO SEND signal is negated. Q17 is nonconducting, and the CS signal is low. A space is represented by an input current of greater than 23 mA, which produces a base voltage sufficiently high to turn on Q17, thereby asserting the CS signal.

Figure 5-23 illustrates the method used to convert the DP8-E TTL signals to either EIA or current mode signals. The SEND DATA L signal conversion circuit is used as an example.

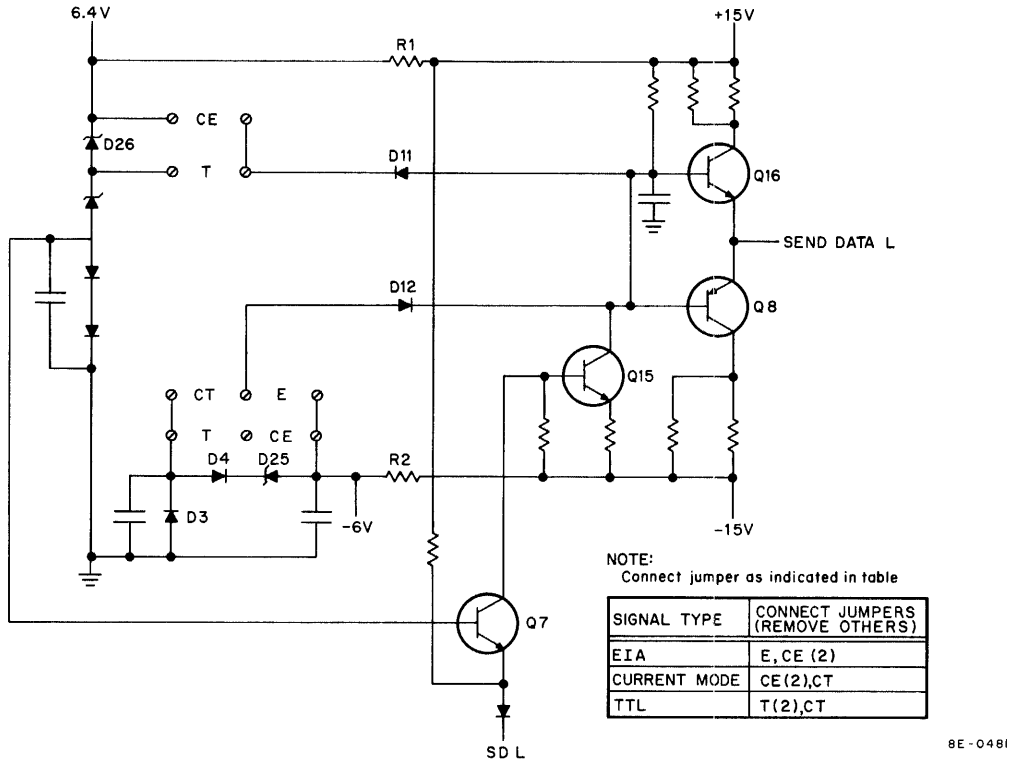


Figure 5-23 DP8-E Output Circuit (Driver)

The output transistors, Q8 and Q16, are connected for push-pull operation and are controlled by transistors Q7 and Q15. As the table in Figure 5-23 indicates, jumpers E and CE are connected for TTL-to-EIA level conversion. If the SD L signal is high, logic 0, both Q7 and Q15 are nonconducting. Diode D12 is reverse-biased, while D11 is forward-biased. Thus, Q16 connects the SEND DATA line to a voltage that varies between 5V and 15V, depending on the load.

If the SEND DATA L signal must be current mode, the CE and CT jumpers are connected. If the SD L signal is high, logic 0, Q16 provides the load current of greater than 23 mA, indicating a space condition. When the SD L signal is asserted, diode D12 is forward-biased; Q8 provides the load current of less than 5 mA, indicating a mark

condition on the SEND DATA line. Note that the CT jumper, by placing D12's plate just below ground rather than at -6V, changes the operating point of Q8 from what it was during EIA conversion.

Table 5-4 lists the control signals and data signals and relates the two types to mark/space, logic 1/logic 0, etc. Table 5-5 lists the EIA and current mode specifications for reference.

Table 5-4
Signal Level Terminology

Control Signals	Data Signals	Mark/ Space	High/ Low	Asserted Not Asserted
RING CARRIER/AGC SCR SCT INTERLOCK/DATA SET READY CLEAR TO SEND TERMINAL READY SEND REQUEST EXTERNAL TIMING		Mark Space	Low High	Not Asserted Asserted
	RECEIVE DATA L SEND DATA L	Mark Space	Low High	Asserted Not Asserted

Table 5-5
EIA/Current Mode Electrical Specifications

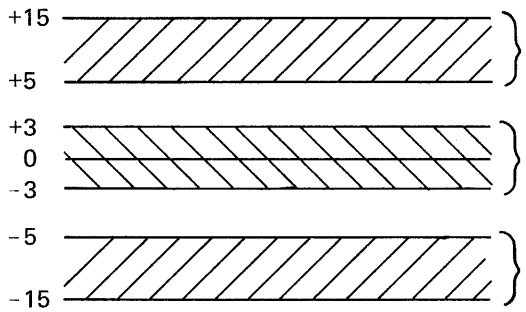
Current mode specifications (applicable to Bell 300 Series Modem, or equivalent).

EIA (RS-232-C) Electrical Specifications

Driver output logic levels with 3K to 7K load	$15V > V_{oh} > 5V$ $-5V > V_{ol} > -15V$
Driver output voltage with open circuit	$V_o < 25V$
Driver output impedance with power off	$Z_o > 300\Omega$
Output short circuit current	$I_o < 5A$
Driver slew rate	$\frac{dv}{dt} < 30V/\mu s$
Receiver input impedance	$7\ k\Omega > R_{in} > 3\ k\Omega$
Receiver input voltage	±15V compatible w/driver
Receiver output with open circuit input	Mark
Receiver output with 300Ω to ground on input	Mark
Receiver output with +3V input	Space
Receiver output with -3V input	Mark

(continued on next page)

Table 5-5 (Cont)
EIA/Current Mode Electrical Specifications



Current Mode Electrical Specifications (Applicable to the Bell 300 Series Modem or equivalent)

Receiver Input Current/Voltage levels with 100Ω Termination	Mark 5 mA ($-0.7 < Ew < 1$)
Driver Output Impedance with Power Off	Not Specified
Driver Output Short Circuit Current	Not Specified
Driver Slew Rate between the 7 mA and the 21 mA levels	Typical 14 mA/100 ns Maximum 14 mA/50 ns Minimum 14 mA/200 ns
Receiver Input Impedance	$120 > Z_{in} > 90$
Receiver Output with Open Circuit Input	Logic 1 – Mark–Off
Receiver Output with Input > 23 mA	Logic 0 – Space–On
Receiver Output with Input < 5 mA	Logic 1 – Mark–Off
Driver Distortion Limits	Mark to Space or Space to Mark must be achieved within 25% of bit interval
Receiver Open Circuit Voltage	-0.8V to -1.3V

SECTION 5 MAINTENANCE

General instructions concerning preventive and corrective maintenance are given in Volume 1, Chapter 4. Two maintenance aids are available when corrective maintenance of the DP8-E is required. One, the diagnostic program, MAINDEC-08-DHDPA-A, can help the technician to determine the nature of the problem. The other, a self-test feature, enables the technician to single-step test both the receive and transmit logic.

To use the self-test feature, the technician must connect the test connector to the plug on the modem side of the interconnecting cable. The internal wiring of the test connector enables software simulation of the modem-interface signals. Figure 5-24 is a pictorial representation of the signals involved in the self-test feature. Note that the M866 "F" jumper and either the "N" or "Δ" jumper (Table 5-2) must be connected. When the technician wishes to check the receive or transmit logic, he can, by careful selection of IOT instructions, assert or negate any of the signals shown in Figure 5-24. The SRCD instruction generates a single clock pulse that is returned on both the SCR and SCT lines, thereby enabling all other signals to be generated. See Paragraph 5.16 for additional information concerning the self-test feature.

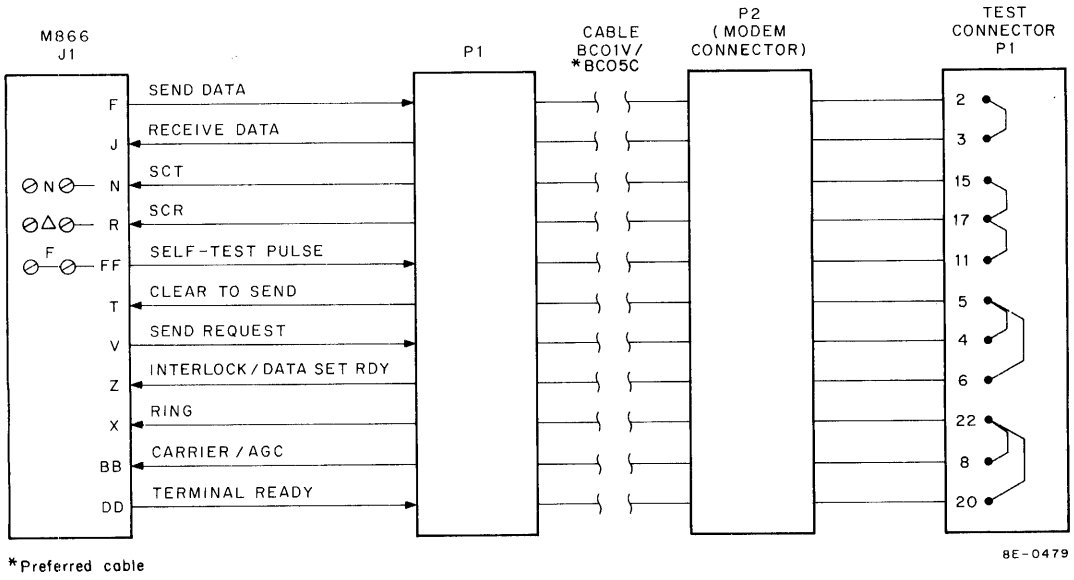


Figure 5-24 Self-Test Interconnection

When performing corrective maintenance, the technician should refer to the option schematics, E-CS-M839-0-1 and E-CS-M866-0-1, rather than to the logic extracts in this volume. Table 5-6 lists the modem-interface signals and the corresponding cable connector pin information. Top-connector "H" on the M866 Module, an alternate input/output connector, is shown in parentheses with the J1 pin number. Table 5-7 lists the M866-M839 Module interconnecting signals and indicates the source module.

Table 5-6
Modem-Interface Cable Pin Information

Signal Name	J1 (H) M866	P1 40-Pin Berg	P2 (DP8-EA) 25 Pin Cinch	P2 (DP8-EB) 12-Pin Burndy
SEND DATA	F (HE2)	F	2	E
RECEIVE DATA L	J (HF2)	J	3	K
EXTERNAL TIMING	L (HH1)	L	24	H
SCT	N (HH2)	N	15	J
SCR	R (HJ2)	R	17	L
CLEAR TO SEND	T (HK2)	T	5	C
SEND REQUEST	V (HL2)	V	4	D
RING	X (HM2)	X	22	No Connection (Bell 301) F-Shield (Bell 303)
INTERLOCK/DATA SET READY	Z (HN2)	Z	6	F
CARRIER/AGC	BB (HP2)	BB	8	M

(continued on next page)

Table 5-6 (Cont)
Modem-Interface Cable Pin Information

Signal Name	J1 (H) M866	P1 40-Pin Berg	P2 (DP8-EA) 25 Pin Cinch	P2 (DP8-EB) 12-Pin Burndy
TERMINAL READY	DD (HR2)	DD	20	No Connection (Bell 301) M-Shield (Bell 303)
USER FUNCTION AND SELF-TEST PULSE	FF (If Jumpered) (HA1)	FF	11	–
USER FUNCTION	JJ (If Jumpered) (HB1)	JJ	12	–
FRAME/SIGNAL GROUND	C VV (HT1, HC2)	C VV	25 7	–
-6V	(HC1) No J1 Connection	–	–	–
6.4V	(HS2) No J1 Connection	–	–	–
EXTERNAL TIMING, TTL LEVEL	(HV2) No J1 Connection	–	–	–

Table 5-7
M866-M839 Top-Connector Signals

Signal Name	"F" Connector Pin Number	Source Module	
		M839	M866
SRCD L	FA1		*
THIS CODE	FB1	*	
INT RQST	FC1	*	
RD	FD1		*
REMA L	FE1	*	
TEMA L	FF1	*	
SCR-P L	FH1		*
BREAK GRANT	FJ1		*
INI L	FK1	*	
GTP4	FL1		*
BREAK RQST	FM1		*
SSBE L	FN1		*
SCT-P L	FP1		*
CS	FR1		*
SD L	FS1	*	
IDLE L	FT1		*
RQST	FU1	*	
SRS1 L	FV1	*	
GROUND	FA2		
⋮	⋮		
GROUND	FV2		

Table 5-8
Equivalent EIA and CCITT Circuit Designations

DP8-E Signal Name	P2 (DP8-EA) Pin Number	EIA Circuit	CCITT Circuit	EIA/CCITT Circuit Description
FRAME/SIGNAL GROUND	1	AA	101	PROTECTIVE GROUND
	7	AB	102	SIGNAL GROUND/COMMON RETURN
SEND DATA	2	BA	103	TRANSMITTED DATA
RECEIVE DATA L	3	BB	104	RECEIVED DATA
SEND RQST	4	CA	105	REQUEST TO SEND
CLEAR TO SEND	5	CB	106	CLEAR TO SEND
INTERLOCK/DATA SET READY	6	CC	107	DATA SET READY
TERMINAL READY	20	CD	108.2	DATA TERMINAL READY
RING	22	CE	125	RING INDICATOR
CARRIER/AGC	8	CF	109	RECEIVED LINE SIGNAL DETECTOR
NOT USED IN DP8-E	21	CG	110	SIGNAL QUALITY DETECTOR
	23	CH	111	DATA SIGNAL RATE SELECTOR (DTE)
		CI	112	DATA SIGNAL RATE SELECTOR (DCE)
EXTERNAL TIMING (IF JUMPER 'L' IS CONNECTED)	24	DA	113	TRANSMITTER SIGNAL ELEMENT TIMING (DTE)
	15	DB	114	TRANSMITTER SIGNAL ELEMENT TIMING (DCE)
SCR	17	DD	115	RECEIVER SIGNAL ELEMENT TIMING (DCE)
NOT USED IN DP8-E	14	SBA	118	SECONDARY TRANSMITTED DATA
	16	SBB	119	SECONDARY RECEIVED DATA
	19	SCA	120	SECONDARY REQUEST TO SEND
	13	SCB	121	SECONDARY CLEAR TO SEND
USER FUNCTION	12	SCF	122	SECONDARY RECEIVED LINE SIGNAL DETECTOR
USER FUNCTION AND SELF-TEST PULSE	11	11, 18, 15 ARE UNASSIGNED.		
NOT USED IN DP8-E	9, 10, 18	9, 10 ARE RESERVED FOR DATA SET TESTING.		
FRAME/SIGNAL GROUND	25			

Table 5-8 relates the DP8-E interface signal designations to both the equivalent EIA (RS-232-C) and the equivalent CCITT circuit designations. For example, the DP8-E signal called SEND DATA is brought out to pin 2 of P2 (DP8-EA). The EIA circuit designation for this signal is "BA", while the CCITT circuit designation is "103".

SECTION 6 SPARE PARTS

Table 5-9 lists the recommended spare parts for the DP8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 5-9
DP8-E Recommended Spare Parts

DEC Part Number	Description	Quantity
19-09667	IC 74H74	1
19-10035	IC 74197	1
19-09057	IC 74H10	1
19-09931	IC 74H04	1
19-09056	IC 74H00	1
19-09935	IC 8235	3
19-09934	IC 8266	1
19-09712	IC 8242	1
19-09705	IC 8881	2
19-09704	IC 314	1
19-09686	IC 7404	1
19-09615	IC 8271	3
19-09854	IC 8251	1
19-09486	IC 384	1
19-09485	IC 380	2
19-09004	IC 7402	2
19-05577	IC 7420	1
19-05576	IC 7410	1
19-05575	IC 7400	2
19-05547	IC 7474	3
19-09267	IC 74H11	1
19-05578	IC 7430	1
19-09373	IC 9601	1
11-00114	Diode, D664	5
11-00113	Diode, D662	2
15-03100	Transistor, 3009B	5
15-03409-2	Transistor, 7534C	4
11-01938	Diode, 1/4M, 2.4 AZ	1
11-00124	Diode, IN750A, 1/4W 4.7J	1

CHAPTER 6
KG8-E GENERATOR/DETECTOR

SECTION 1 INTRODUCTION

The KG8-E BCC Generator/Detector option consists of a single quad module that plugs into the PDP-8/E OMNIBUS. The option operates under program control to provide the computer with a parity-check capability. Although intended to be used with data communication equipment, the option is independent of such equipment and can be used with other devices.

Parity checks are carried out in the KG8-E on data characters that are transferred from the PDP-8/E memory by a programmed I/O transfer. The KG8-E can perform three types of parity checks: a vertical redundancy check (VRC) can be performed on a 6-, 7-, or 8-bit character; a longitudinal redundancy check (LRC) can be made on a message consisting of 6-, 7-, 8-, 12-, or 16-bit characters; and a cyclic redundancy check (CRC) can be carried out on a message consisting of 6-, 8-, 12-, or 16-bit characters. A VRC can be performed separately or as part of either an LRC or a CRC.

Publications and documents that are relevant to the KG8-E are:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* — DEC, 1972
b. *PDP-8/E Maintenance Manual, Volume 1*
c. KG8-E Diagnostic Program, MAINDEC-8E-D8CA
d. DEC Engineering Drawing, E-CS-M884-0-1.

SECTION 2 INSTALLATION AND CHECKOUT

The KG8-E option is installed on site by DEC Field Service personnel. The customer should *not* attempt to unpack, install, checkout, or service the equipment.

Insert the module in the PDP-8/E OMNIBUS. See Table 2-3, Volume 1, for information concerning recommended module priorities (the KG8-E is a "non-memory" option).

The KG8-E can be checked for correct operation by running the diagnostic program. If maintenance is necessary, refer to Chapter 4, Volume 1.

SECTION 3 PARITY CHECK/BLOCK DIAGRAM

6.1 PARITY CHECK

The three types of parity checks performed by the KG8-E are VRC, LRC, and CRC. A general description of each type follows.

6.1.1 VRC Parity Check

A VRC is carried out on each character of a message. The summation of all logic-1 bits within the character must be even or odd, whichever is desired. The KG8-E examines each character: when the character is part of a message that is to be transmitted to some external device from memory, the option adds a parity bit (logic 1), if one is needed; when the character is part of a message transmitted from an external source to memory, an error-detecting software routine is entered, if the character does not exhibit the correct parity. In one instance parity is generated; in the other, parity is tested. Although each operation is different, the terms VRC and parity check are used to refer to either operation. The logic implementation of a VRC is detailed in Paragraph 6.5.

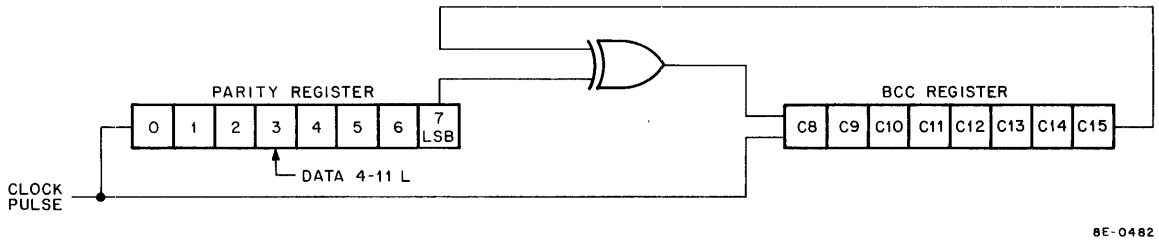
6.1.2 LRC Parity Check

A distinction similar to that expressed in the preceding paragraph is unnecessary when either an LRC or a CRC is performed. Each of these parity checks is the same, regardless of the direction of the message transfer. The LRC parity check is based on the accumulation of a block check character (BCC). The KG8-E generates this BCC by Exclusive-ORing the contents of corresponding bit positions in each character of the message. For example, consider a message consisting of the following four 8-bit characters:

	MSB							LSB	
Character 1	0	1	1	0	0	0	1	0	
Character 2	1	0	0	1	0	0	0	1	
Character 3	1	1	1	0	0	0	0	0	
Character 4	1	0	0	1	1	0	1	0	
	1	0	0	0	1	0	0	1	BCC

If one Exclusive-ORs corresponding bit positions, the BCC shown results. Figure 6-1 illustrates how Exclusive-ORing is implemented by the KG8-E logic; the chart shows the state of the BCC Register at various stages of BCC accumulation for the four characters.

The first character is parallel-loaded into the Parity Register from the DATA lines by a program instruction. Clock pulses shift the character into the BCC Register (although shown as an 8-bit register, for convenience, the BCC Register is 16 bits in length; characters are loaded into the register in a right-justified format). With each clock pulse, the bit in the LSB position of the Parity Register is Exclusive-ORed with the bit in the LSB position of the BCC Register. The result is shifted into the MSB of the BCC Register by the next clock pulse. Eight clock pulses shift the entire character into the BCC Register. The second character is then loaded into the Parity Register, although an appreciable amount of time might pass before this happens (because data transfers between the KG8-E and memory are of the programmed I/O type, the operation can be interrupted by program interrupts or data breaks after each character transfer).



CHARACTER 1: 01100010
CHARACTER 2: 10010001
CHARACTER 3: 11100000
CHARACTER 4: 10011010

CHARACTER/BIT LOADED	CLOCK PULSE	BCC REGISTER CONTENTS							
		C8	C9	C10	C11	C12	C13	C14	C15
	START	0	0	0	0	0	0	0	0
CHARACTER 1, BIT 1	1	0	0	0	0	0	0	0	0
CHARACTER 1, BIT 2	2	1	0	0	0	0	0	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
CHARACTER 1, BIT 8	8	0	1	1	0	0	0	1	0
CHARACTER 2, BIT 1	9	1	0	1	1	0	0	0	1
CHARACTER 2, BIT 2	10	1	1	0	1	1	0	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
CHARACTER 2, BIT 8	16	1	1	1	1	0	0	1	1
CHARACTER 3, BIT 1	17	1	1	1	1	1	0	0	1
CHARACTER 3, BIT 2	18	1	1	1	1	1	1	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
CHARACTER 3, BIT 8	24	0	0	0	1	0	0	1	1
CHARACTER 4, BIT 1	25	1	0	0	0	1	0	0	1
CHARACTER 4, BIT 2	26	0	1	0	0	0	1	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
CHARACTER 4, BIT 8	32 → BCC	1	0	0	0	1	0	0	1

Figure 6-1 LRC BCC Accumulation for Four 8-Bit Characters

When all four characters have been shifted into the BCC Register (32 clock pulses), the result in the register is the BCC. If the message is to be transmitted from memory, the BCC is transmitted as the last character of the message. Similarly, if the message was received from an external device, the four characters already considered are followed by a BCC that was generated in the transmitting device. The BCC is treated as a character and loaded into the Parity Register. When it has been shifted into the BCC Register by eight clock pulses, the register contents will be zero, if the message has been received free of error. If not, an error detecting software routine is entered by the computer.

Note that there is no reason why a VRC cannot be performed before an LRC (or before a CRC, for that matter). Such a procedure enhances the error-detecting capability provided by the KG8-E. In such a case, bit position 0 or 7 of the example would contain the parity bit. Although the example illustrates the LRC BCC accumulation for an 8-bit character, the LRC can be carried out for 6-, 7-, 12-, and 16-bit characters, as well. The procedure is the same, as will be demonstrated in Paragraph 6.8.

6.1.3 CRC Parity Check

A CRC is also based on the accumulation of a BCC; however, the generation of the BCC is more intricate than during an LRC. A number of different CRC codes can be used, but the KG8-E implements only two, viz., CRC-12 and CRC-16. Unlike LRC, CRC concepts are best understood through a mathematical background, followed by a description of the logical implementation of the mathematics.

A CRC code message consists of a specific number of data bits and a BCC that is generated by the KG8-E. Let n equal the total number of bits in the message and k equal the number of data bits; then, n-k equals the number of bits in the BCC. The code message is derived from two polynomials that are algebraic representations of two binary words. The generator polynomial, P (X), reflects the type of code used (CRC-12, CRC-16), and the message polynomial, G (X), represents the string of serial data bits. The polynomials are usually represented algebraically by a string of terms in powers of X, as $X^n+...+X^3+X^2+X+1$. In binary form, a 1 is placed in each position that contains a term; the absence of a term is indicated by a 0. The convention followed in this manual is to place the LSB (X^0, or 1) at the right. For example, if a polynomial is given as X^4+X+1, its binary representation is 10011 (third and second degree terms are not present).

Given a message polynomial, G (X), and a generator polynomial, P (X), the objective is to construct a code message polynomial, F (X), that is evenly divisible by P (X). This is accomplished as follows:

a. Multiply the message, G (X), by X^{n-k}, where n-k is the number of bits in the BCC.
b. Divide the resulting product, $X^{n-k}G(X)$, by the generator polynomial, P (X).
c. Discard the quotient; add (binary addition) the remainder, C (X), to the product of Step *a.*
d. The result is the code message polynomial, F (X), represented by $X^{n-k}G(X)+C(X)$.

The division is performed in binary without carries or borrows. In this case, the remainder is always one bit less than the divisor. The remainder is the BCC, and the divisor is the generator polynomial. Thus, the bit length of the BCC is always one less than the number of bits in the generator polynomial. A simple example is carried out in the following steps:

a. Given: Message polynomial, G (X) = 110011 (X^5+X^4+X+1)
Generator polynomial, P (X) = 11001 (X^4+X^3+1)
G (X) contains 6 data bits; P (X) contains 5 bits and yields a BCC of 4 bits; thus, n-k=4.

b. Multiplying G (X) by X^{n-k} gives

$$X^{n-k}G(X) = X^4(X^5+X^4+X+1) = X^9+X^8+X^5+X^4$$

The binary equivalent of the product is 1100110000.

c. Dividing the product by P (X) gives

```
                  100001  ← Quotient
P (X) → 11001 ⌈ 1100110000 ← X^(n-k)G (X)
              11001
                  10000
                  11001
                   1001  ← Remainder = C (X) = BCC
```

(continued on next page)

d. Adding the BCC to the product of Step *b.* gives

F (X) = 1100111001

The code message polynomial is transmitted. The receiving station divides it by the same generator polynomial. If there is no error, the division produces no remainder. A remainder indicates an error. The result of the division is shown below, with the result indicating an error-free message.

```
                  100001
P (X) → 11001  ⌈1100111001 ← F (X)
               11001
                   11001
                   11001
                   00000 ← Remainder of 0
```

A more practical example, the mathematical derivation of a CRC-12 BCC, is now detailed. This example derives the BCC of a 2-character message. The KG8-E logic implementation of the mathematics is then presented.

The message characters are: character 1, 000 000 000 101; and character 2, 000 000 001 000 (PDP-8/E convention is followed throughout; i.e., LSB position is on the right). When a character is transferred to the KG8-E from memory, the LSB of character 1 is the first bit shifted into the BCC Register. Therefore, G (X) = $X^{15}+X^2+1$ (000 000 001 000 000 000 000 101). P (X) for CRC-12 is $X^{12}+X^{11}+X^3+X^2+X+1$ (1100000001111). The BCC is always one bit less than the P (X); thus, the quantity n-k is 12. Because of the way that the KG8-E implements the mathematical derivation, the message polynomial, G (X), is modified and re-designated G′ (X). The modification merely reverses the order of the character bits of G (X). Thus, G′ (X) in this example is $X^{23}+X^{21}+X^8$ (101 000 000 000 000 100 000 000). The quantity $G'(X)X^{n-k} = (X^{23}+X^{21}+X^8)\ X^{12} = X^{35}+X^{33}+X^{20}$. The long division of $G'(X)X^{n-k}$ by P (X) follows.

```
                                                  110 000 000 111 100 111 001 100
1100000001111  ⌈101 000 000 000 000 100 000 000 000 000 000 000
                 110 000 000 111 1
                  11 000 000 111 10
                  11 000 000 011 11
                             100 010 100 000 0
                             110 000 000 111 1
                              10 010 100 111 10
                              11 000 000 011 11
                               1 010 100 100 010
                               1 100 000 001 111
                                 110 100 101 101 0
                                 110 000 000 111 1
                                     100 101 010 100 0
                                     110 000 000 111 1
                                      10 101 010 011 10
                                      11 000 000 011 11
                                       1 101 010 000 010
                                       1 100 000 001 111
                                           1 010 001 101 000
                                           1 100 000 001 111
                                             110 001 100 111 0
                                             110 000 000 111 1
                                                 001 100 000 100 ← BCC
                                                 ↑
                                                 LSB
```

The remainder is the BCC of the two-character message. Note that the LSB is on the left. The BCC is logically added to the quantity $G'(X)X^{n-k}$ (MSB is added to MSB) to obtain the code message polynomial, F (X), as shown below.

$$F(X) = G'(X)X^{n-k} + BCC = X^{35}+X^{33}+X^{20}+X^{9}+X^{8}+X^{2}$$

The F (X) is transmitted. The receiving station divides the F (X) by the P (X). An errorless transmission results in a remainder of zero (this division is not shown; the reader can verify the fact that the division produces a zero remainder).

Figure 6-2 is a representation of the BCC Register in its CRC-12 configuration (the configuration is different for CRC-16). The accompanying chart indicates the content of the register after selected bits of the two example characters have been shifted into the register (space limitations prevent each step from being shown). The bit in the LSB position of the character is Exclusive-ORed with the bit in the LSB position of the BCC Register. The result is either shifted directly into the register or Exclusive-ORed again and then shifted. Either way, the shift takes place after the Exclusive-OR has been accomplished. The chart carries the process through 36 clock pulses. The first 24 pulses shift the two characters into the register. After the 24th clock pulse, the BCC has been accumulated, as shown. Note that the LSB is on the right.

If the message is to be transmitted, the BCC is added to the $G'(X)X^{n-k}$, as indicated earlier; then, the F (X) is transmitted. However, if the message was received from an external source, the two characters are followed by the BCC computed by the external device. In this case, the BCC is shifted into the KG8-E BCC Register by the next 12 clock pulses, as illustrated in the chart. The result, zero, indicates no error in the transmission.

The procedure is the same for CRC-16, except that the P (X) is different. The BCC Register logic is manipulated by control signals to implement the mathematical derivation. The logic is explained in detail in Paragraph 6.8.

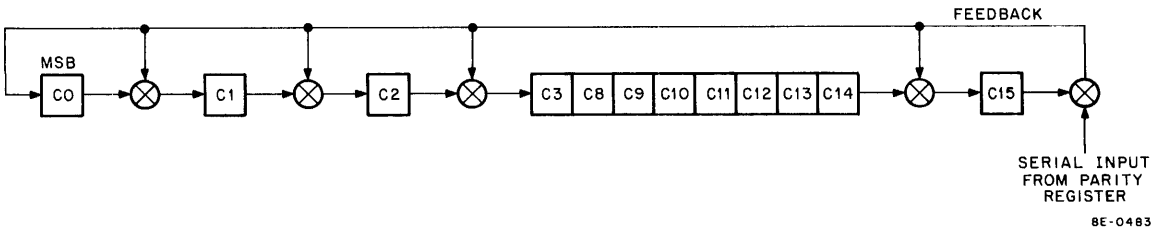
6.2 BLOCK DIAGRAM

The block diagram of Figure 6-3 presents the various logic sections of the KG8-E and illustrates their interrelationship. A detailed discussion of each section follows the block diagram description.

The IOT Decoder logic decodes bits MD3—11 to generate the IOT signals shown in the figure (see Table 6-1 for a complete list of the KG8-E IOT instructions). The type of parity check carried out by the KG8-E is determined, basically, by the IOT instruction issued, viz., RCCV, RCGB, or RCTV. The way that the selected type of check is performed is determined by control signals generated in the Control Register logic.

The Control Register logic is loaded from the AC Register, via DATA lines 5—11, by the RCLC instruction. This instruction is issued before the type of parity check is selected. The control signals generated in response to the RCLC instruction determine how the parity check is carried out: the PARITY signals (2 signals) determine where a generated parity bit is placed in a character during a VRC; the VRC (RCGB) signals (3 signals) are generated when a VRC is to be carried out along with an LRC/CRC; the CRC/LRC (0) signal manipulates the BCC Register so that either an LRC or a CRC is carried out; finally, the BIT signals select the BCC Register configuration and the number of clock pulses per burst appropriate for the message character bit length.

A character is transferred from the AC Register, via DATA lines 4—11, to the VRC logic in response to either an RCCV instruction or an RCGB instruction. If a VRC check (as opposed to a test) is carried out, the generated parity bit and the character are returned to the AC Register, again on DATA lines 4—11. The COMPUTE VRC signal is asserted and applied to the I/O XFER logic to control CPU timing during the return transfer. If a VRC test is performed, the character is not returned to the AC; rather, the PARITY signal is used to check that the character exhibits the correct parity.



MSB ↓ LSB ↓

CHARACTER 1: 000 000 000 101
CHARACTER 2: 000 000 001 000

CLOCK PULSE	C0	C1	C2	C3	C8	C9	C10	C11	C12	C13	C14	C15	SERIAL INPUT	FEEDBACK
	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	1	1	1	0	0	0	0	0	0	0	1	0	1
2	1	0	0	0	1	0	0	0	0	0	0	1	1	0
3	0	1	0	0	0	1	0	0	0	0	0	0	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
11	1	0	0	0	1	0	0	0	0	1	0	1	0	1
12	1	0	1	1	0	1	0	0	0	0	1	1	0	1
13	1	0	1	0	1	0	1	0	0	0	0	0	0	0
14	0	1	0	1	0	1	0	1	0	0	0	0	0	0
15	0	0	1	0	1	0	1	0	1	0	0	0	1	1
16	1	1	1	0	0	1	0	1	0	1	0	1	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
23	0	1	0	0	0	0	0	1	1	0	0	0	0	0
24	0	0	1	0	0	0	0	0	1	1	0	0	0	0
			↑ BCC											
25	0	0	0	1	0	0	0	0	0	1	1	0	0	0
26	0	0	0	0	1	0	0	0	0	0	1	1	1	0
27	0	0	0	0	0	1	0	0	0	0	0	1	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
32	0	0	0	0	0	0	0	0	0	0	1	0	0	0
33	0	0	0	0	0	0	0	0	0	0	0	1	1	0
34	0	0	0	0	0	0	0	0	0	0	0	0	0	0
35	0	0	0	0	0	0	0	0	0	0	0	0	0	0
36	0	0	0	0	0	0	0	0	0	0	0	0		

NOTES:

1. □ = BCC Register Stage; C-Number refers to the bit used (see Paragraph 6.8)
2. ⊕ = Exclusive-OR operation
3. $P(X) = X^{12}+X^{11}+X^3+X^2+X+1$

Figure 6-2 CRC BCC Accumulation for Two 12-Bit Characters

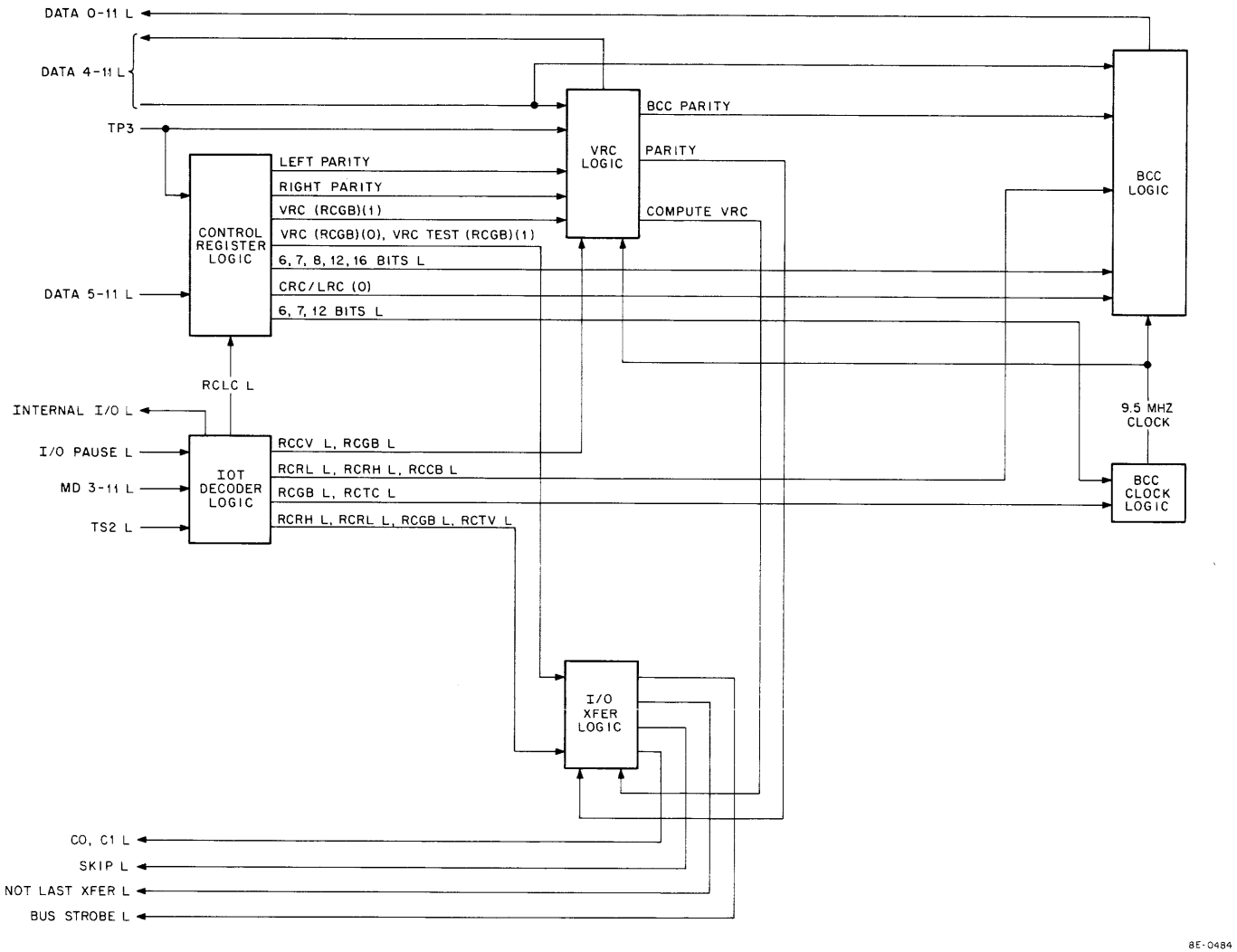


Figure 6-3 KG8-E Block Diagram

Table 6-1
KG8-E IOT Instruction List

Octal Code	Mnemonic	Function
6110	RCTV	Test VRC and Skip. If the VRC logic is wired for an odd parity check, the next program instruction is skipped when the character exhibits odd parity; if the logic is wired for an even parity check, the next program instruction is skipped when the character does *not* exhibit even parity.
6111	RCRH	Read BCC high. Jam-transfers the 8 most significant bits of a BCC to AC4–11 (the MSB goes to AC4); used for a 16-bit accumulation.
6112	RCRL	Read BCC low. Jam-transfers the BCC to the AC Register. The number of bits involved depends on the type of parity check performed. The LSB of the BCC is transferred to AC11.
6113	RCCV	Compute VRC. Transfers a character from AC4–11 to the Parity Register and clears the AC; causes the VRC logic to check for odd or even parity and add a parity bit to the character if necessary; returns the character to the AC with the parity bit being jammed into either AC4 or AC11.
6114	RCGB	Generate BCC. Generates an LRC or CRC BCC; the BCC is either transmitted as part of the message or compared to a BCC that has been received. This instruction causes the RCTV and RCCV operations to be carried out before the BCC generation, providing the Control Register logic has been properly programmed (see the RCLC instruction).
6115	RCLC	Load Control Register. Defines the type of parity check carried out, and programs the logic for the correct number of bits per character. See the Control Register logic, Paragraph 6.4, for the relation between AC bit and Control Register function.
6116	RCCB	Clear BCC Register. Clears the 16-bit BCC Register.
6117	RCTC	Maintenance Test Clock. If test point DA1 on the module is grounded, this instruction causes a single clock pulse to be applied to the logic; the technician can use this pulse for single-step testing of the KG8-E.

When a CRC/LRC follows the VRC, or when such a check is performed alone, each character is first loaded into the VRC logic Parity Register. 9.5 MHz clock pulses shift the character from the VRC logic, via the BCC parity line, to the BCC logic. A BCC is accumulated in the BCC Register in either CRC or LRC format. The generated BCC is transferred to the AC Register on DATA lines 0–11 in a format determined by the type of check performed and by the number of bits per message character. The transfer is directed by either the RCRL instruction or the RCRH instruction, or both.

6.3 IOT DECODER LOGIC

The IOT Decoder logic is shown in Figure 6-4. Bits MD3–8 are gated with the I/O PAUSE L signal to generate the 611X signal. NAND gate E3 asserts the OMNIBUS INTERNAL I/O L signal, causing the positive I/O bus interface to ignore the IOT instruction. During TS3, the 611X signal is gated with bits MD9–11 in the 8251 BCD-to-decimal decoder to produce the listed IOT signals.

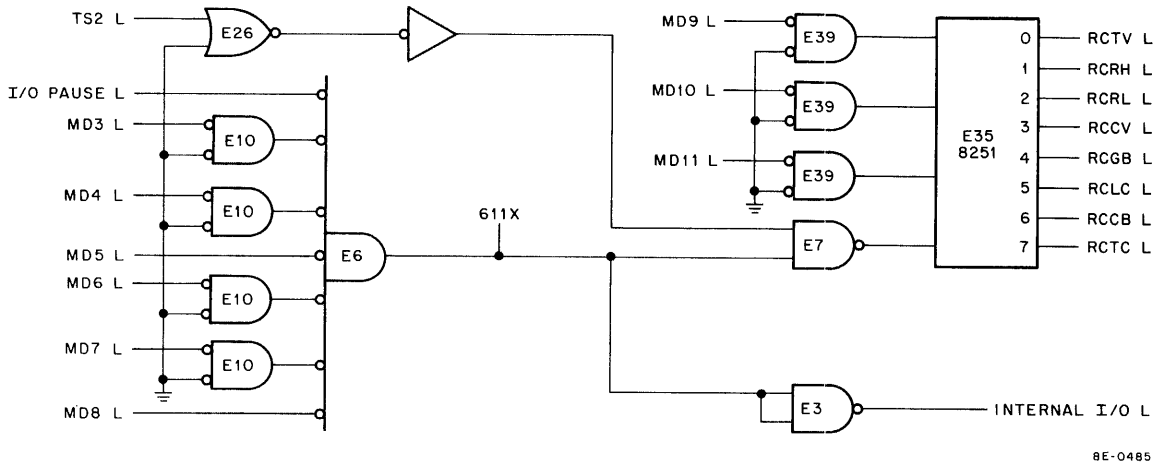


Figure 6-4 IOT Decoder Logic

6.4 CONTROL REGISTER LOGIC

The Control Register logic is shown in Figure 6-5. The logic includes seven flip-flops and a BCD-to-decimal decoder, E8. When the RCLC IOT instruction is issued, the information in the AC Register is gated onto the DATA lines during TS2; the information remains on the lines for the rest of TS2 and throughout TS3. At TP3 time, all seven flip-flops in the logic are clocked. The resulting state of each flip-flop depends on the state of the appropriate AC Register bit. The AC Register bits are related to the control signal functions as follows:

AC5 = 1: CRC BCC
0: LRC BCC

AC 6 7 8
0 0 0 16-bit BCC
0 0 1 12-bit BCC
0 1 0 8-bit BCC
0 1 1 7-bit BCC
1 0 0 6-bit BCC

AC9 = 1: Generated parity bit to AC11
0: Generated parity bit to AC4

AC10 = 1: A VRC check (RCCV) is performed prior to a BCC accumulation.

AC11 = 1: A VRC test (RCTV) is performed prior to a BCC accumulation.

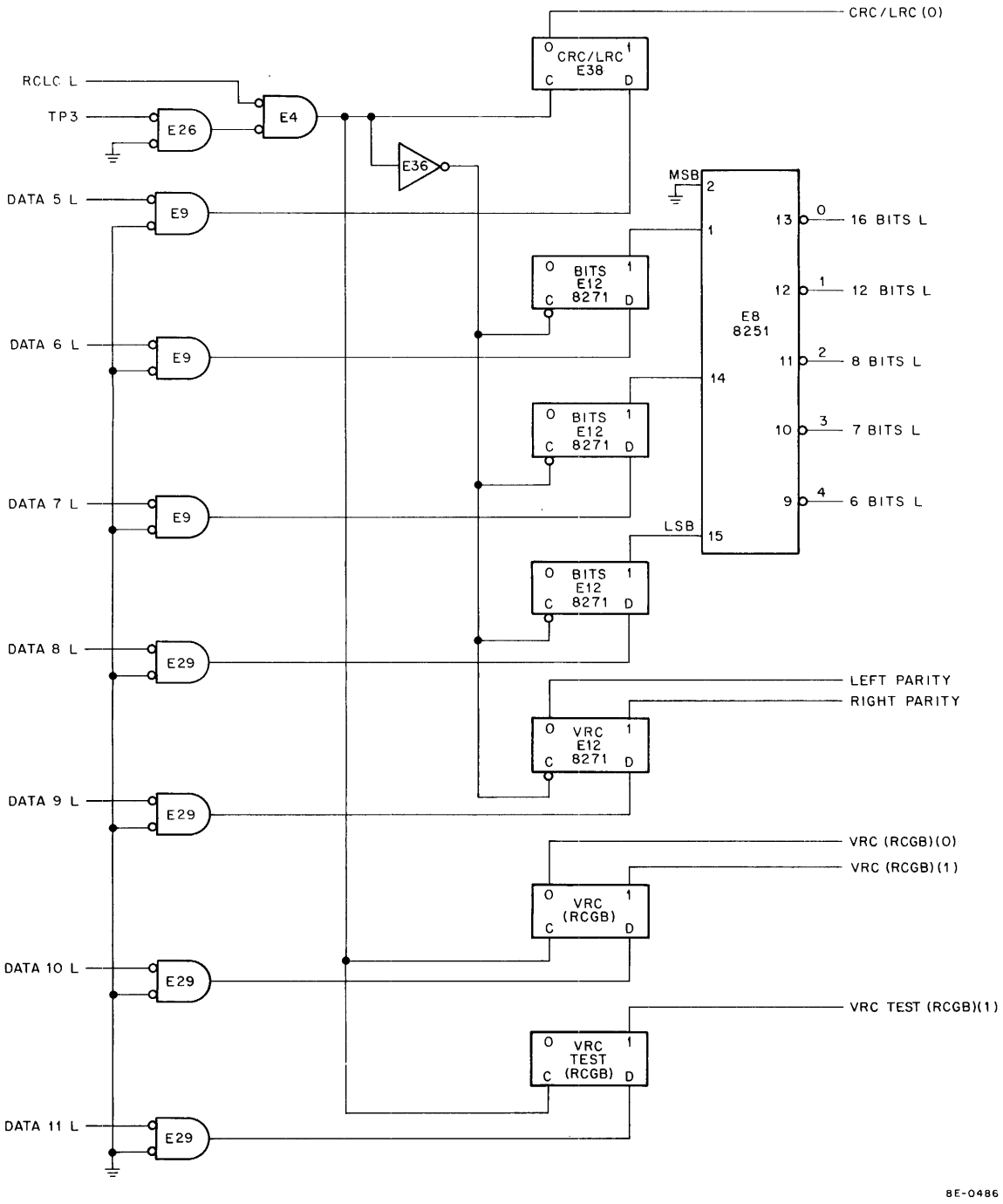


Figure 6-5 Control Register Logic

6.5 VRC LOGIC

The VRC logic is shown in Figure 6-6. The logic includes an Exclusive-OR circuit, comprising gates E16, E20, and E1, and jumper locations E and O, and an 8-bit Parity Register, comprising ICs E14 and E34. Both the Exclusive-OR circuit and the Parity Register are used when an RCCV instruction is issued. This instruction causes a character to be gated from the AC Register onto the DATA lines. The Exclusive-OR logic examines the character and generates a parity bit, if one is required. The character and the parity bit are then loaded into the Parity Register (the parity bit is loaded into either bit position 4 or bit position 11), gated from the register onto the DATA lines, and returned to the AC Register.

Only the Exclusive-OR circuit is used when an RCTV instruction is issued. This instruction also causes a character to be gated from the AC Register to the DATA lines and examined by the Exclusive-OR circuit. However, a parity bit is not generated, and the Parity Register is not loaded. Rather, the I/O Transfer logic monitors the PARITY signal to determine if a program instruction must be skipped (Paragraph 6.7). Thus, the RCCV instruction is used to provide the correct parity for characters that are to be transmitted from memory; conversely, the RCTV instruction is used to check the parity of characters that have been received and stored in memory (the term "a VRC" is used to indicate the execution of either an RCCV or an RCTV instruction). The RCTV instruction logic is described in Paragraph 6.7; the discussion that follows details how the VRC logic provides the correct parity for characters destined for transmission.

A VRC can be performed independently or in conjunction with either an LRC or a CRC. If only a VRC of a character is to be made, the program issues an RCCV IOT instruction. This instruction gates the character from the AC Register onto the DATA lines and causes the IOT Decoder logic to generate the RCCV L signal. This signal enables NOR gate E28 (Figure 6-6) to assert the COMPUTE VRC signal and causes the Parity Register to be placed in parallel-load mode (pin 13 of both E14 and E34 is taken low).

The VRC flip-flop in the Control Register logic will have been set or cleared by a previous RCLC instruction. Therefore, either the LEFT PARITY signal or the RIGHT PARITY signal is high when the COMPUTE VRC signal is asserted. This discussion assumes that the LEFT PARITY signal has been asserted; thus, the character bits on DATA lines 5—11 are gated to the parallel-load inputs of the Parity Register and to the Exclusive-OR circuit, which checks for odd or even parity (the state of the DATA 4 line is immaterial, because NAND gate E9A is disabled). The discussion assumes that an odd-parity check is desired; thus, jumper 0 is connected. If the character contains an odd number of 1s in bits 5—11 (odd parity), the PARITY signal is asserted; the DATA 4-bit input of E14 (pin 3) is low, i.e., a parity bit need not be added to the character. However, if the character contains an even number of 1s in bits 5—11, the PARITY signal is negated. AND-NOR gate E32B is enabled, and pin 3 of E14 is high. The Parity Register is loaded with an odd number of 1s, a parity bit being loaded into the bit 4 position.

If an even-parity check is desired, the E jumper, rather than the O jumper, is connected; if the character gated from the AC Register contains an odd number of 1s, a parity bit is added. The parity bit can be loaded into the bit 11 position if the RIGHT PARITY signal, rather than the LEFT PARITY signal, is asserted.

The Parity Register is loaded at TP3 time of the RCCV instruction, on the leading edge of the pulse at pin 6 of both E14 and E34. At the same TP3 time, but on the trailing edge, the VRC XFER CNTL flip-flop is set, gating the character in the Parity Register onto the DATA lines. The character is gated to the AC Register and loaded into the register at BUS STROBE time (see Paragraph 6.7 for details).

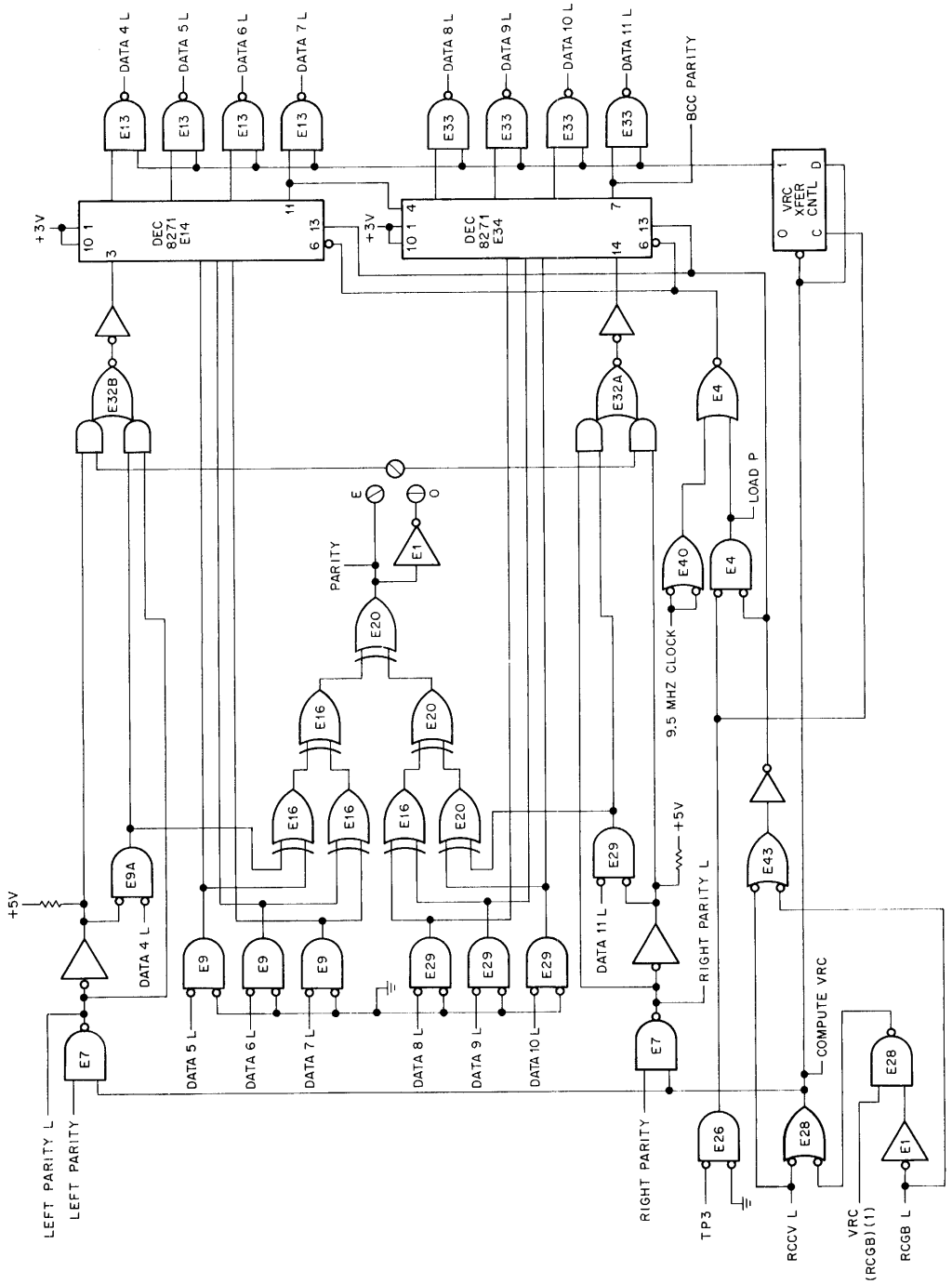


Figure 6-6 VRC Logic

As noted earlier, a VRC can be performed in conjunction with either an LRC or a CRC. The VRC (RCGB) flip-flop in the Control Register logic must be set by an RCLC IOT instruction. Then, an RCGB instruction causes the IOT Decoder logic to generate the RCGB L signal. This signal causes the COMPUTE VRC signal to be generated (via NAND gate E28 and NOR gate E28) and the Parity Register to be placed in the parallel-load mode. Thus, the VRC is carried out in the same way as the RCCV instruction. However, after the character in the Parity Register has been gated to the AC Register and loaded, the same character must be transferred to the BCC Register so that a BCC can be computed. When the RCGB L signal goes high, pin 13 of both E14 and E34 goes high, placing the Parity Register in the right-shift mode. The BCC Clock logic (Paragraph 6.6) begins generating 9.5 MHz clock pulses; each pulse shifts the Parity Register. As a bit is shifted out of the Parity Register, it is shifted into the LSB position of the BCC Register. After eight clock pulses, for example, the character has been shifted out of the Parity Register and into the BCC Register. Figure 6-7 is a timing diagram that includes the important signals of the VRC logic. Some of the signals shown have yet to be explained in detail; however, this diagram is helpful in understanding VRC logic operation.

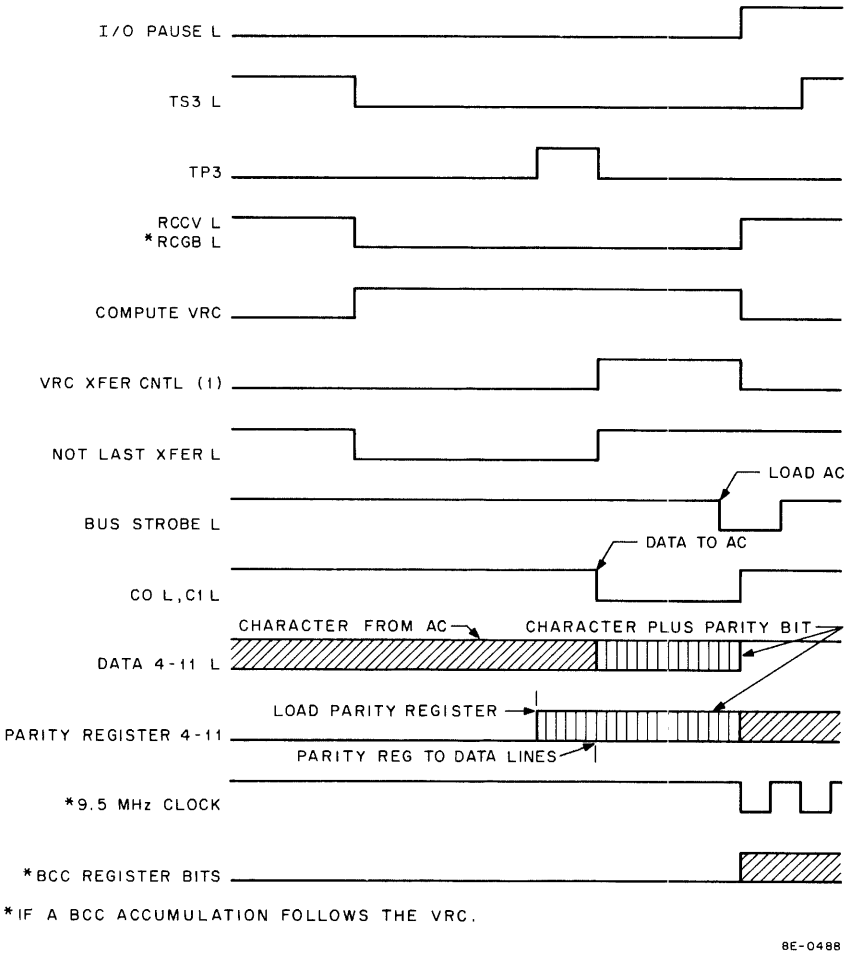


Figure 6-7 VRC Logic Timing

If the VRC (RCGB) flip-flop in the Control Register logic is not set by an RCLC instruction, the COMPUTE VRC signal cannot be asserted when the RCGB instruction is issued (NAND gate E28 is disabled). Thus, a VRC is not performed; rather, an LRC or a CRC, alone, is carried out, and the VRC logic is used as the input network for the BCC logic. When the RCGB instruction is issued, it causes a character to be placed on the DATA lines. Neither the LEFT PARITY L signal nor the RIGHT PARITY L signal is asserted; consequently, the character bits on DATA lines 4–11 (if the character contains eight data bits) are gated to the Parity Register inputs, and the output of the Exclusive-OR circuit is ignored by the logic. As before, the register is parallel-loaded at TP3 time; however, because the VRC XFER CNTL flip-flop is not set, the register outputs are not gated onto the DATA lines. When the RCGB L signal goes high, 9.5 MHz clock pulses begin shifting the Parity Register contents to the BCC Register.

6.6 BCC CLOCK LOGIC

The BCC Clock logic is shown in Figure 6-8. The logic generates clock pulses that shift both the Parity Register and the BCC Register. Figure 6-9 is a timing diagram that helps explain the logic operation.

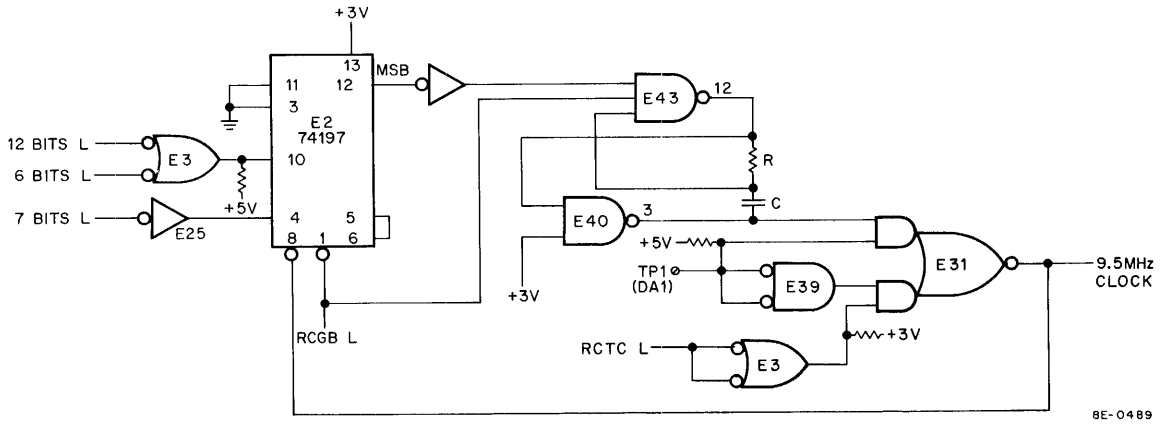


Figure 6-8 BCC Clock Logic

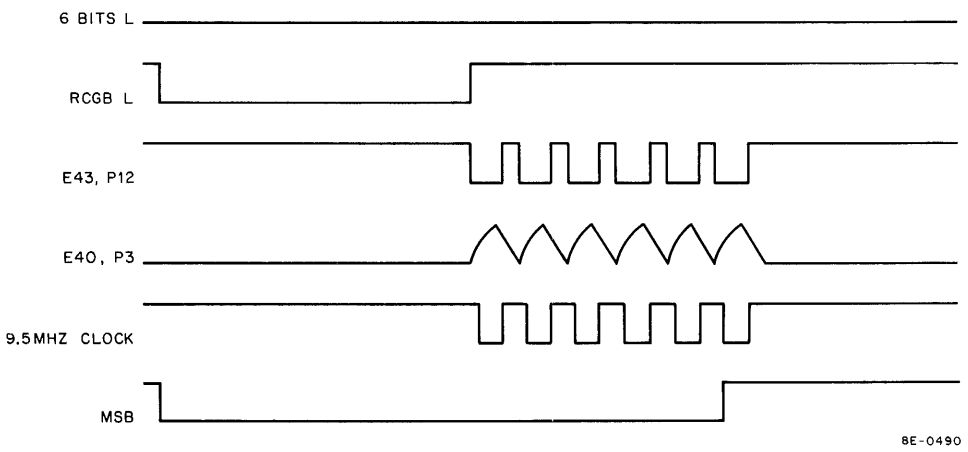


Figure 6-9 9.5 MHz Clock Pulse Generation

The logic includes a 4-bit binary counter, E2, and a free-running multivibrator, comprising NAND gates E43 and E40, and the RC network. The binary counter is preset with a count that is determined by the signals at the parallel inputs. Figure 6-9 indicates that the 6 BITS L signal has been asserted by the Control Register logic. Thus, when the RCGB L signal goes low, E2 is preset with a binary count of 0010. When the RCGB L signal goes high, the free-running multivibrator is triggered. The multivibrator output alternately enables and disables AND-NOR gate E31, thereby producing clock pulses at a frequency of approximately 9.5 MHz. Six clock pulses advance the binary count in E2 to 1000, at which count the MSB signal is asserted. This signal cuts off the multivibrator and no more clock pulses are generated.

The RCTC L signal is generated by the IOT Decoder logic when the maintenance test clock instruction, RCTC, is issued. If test point DA1 is grounded, the RCTC L signal causes a single pulse to be produced; thus, single-step testing of the BCC generating logic is possible.

6.7 I/O TRANSFER LOGIC

The I/O Transfer logic is shown in Figure 6-10. The logic asserts OMNIBUS control signals to enable transfers of data characters and BCCs from the KG8-E to the AC Register. In addition, the logic is used to assert the OMNIBUS SKIP L signal when odd parity is detected during a character parity test (RCTV).

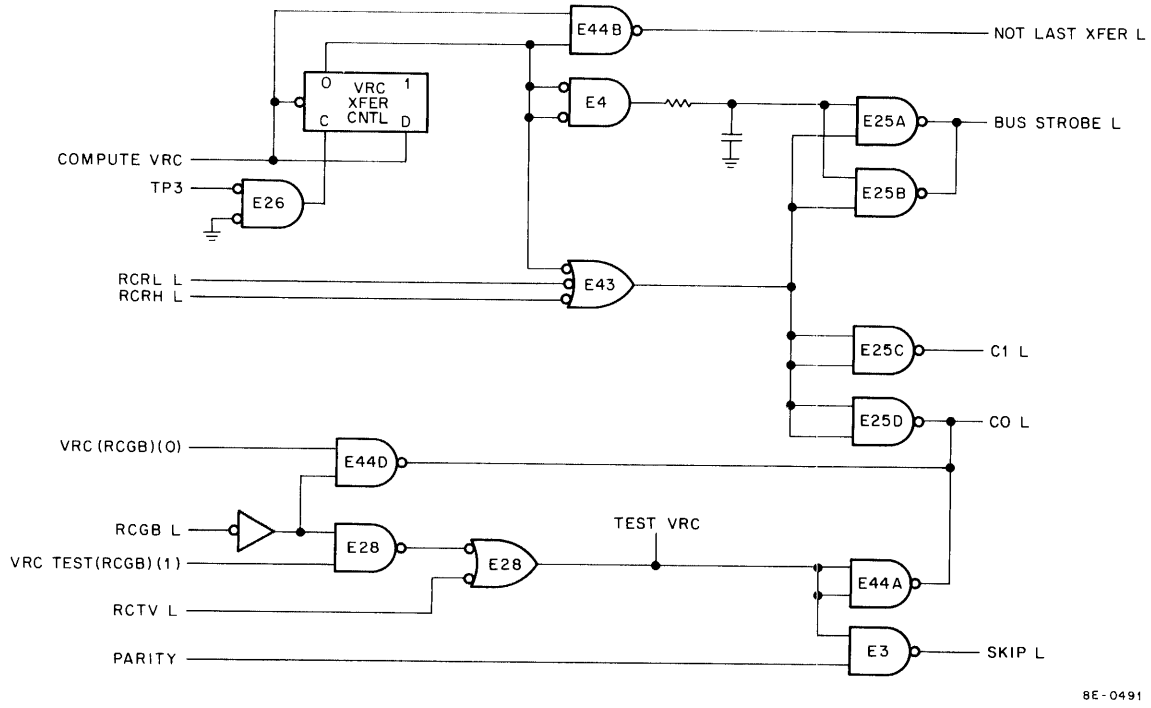


Figure 6-10 I/O Transfer Logic

When a VRC is performed on a character transferred from the AC Register (as a result of an RCCV instruction or an RCGB instruction), the character and the parity bit must be returned to the AC from the Parity Register. In normal operation, the AC Register is loaded at TP3 time. However, the Parity Register outputs are not gated onto the DATA lines until TP3 time; consequently, with normal computer timing, the information on the DATA lines would appear at the AC Register data inputs too late to be loaded into the register. The I/O Transfer logic

solves this difficulty by asserting the NOT LAST XFER L signal. This signal prevents the AC Register from being loaded at TP3 time; instead, the register is loaded when the I/O Transfer logic asserts the BUS STROBE L signal (see Volume 1, Section 6, for more details).

The timing diagram of Figure 6-7 demonstrates how the NOT LAST XFER L signal affects the character transfers from the Parity Register. The NOT LAST XFER L signal is asserted by NAND gate E44B, Figure 6-10, when the VRC logic asserts the COMPUTE VRC signal. At TP3 time (trailing edge), the VRC XFER CNTL flip-flop is set, gating the Parity Register outputs onto the DATA lines (see VRC logic) and causing E44B to negate the NOT LAST XFER L signal. At the same time, both the C0 L signal and the C1 L signal are asserted, via NOR gate E43, and NAND gate E4 is enabled. The output of E4 rises exponentially until, approximately 200 nanoseconds later, it causes the BUS STROBE L signal to be asserted. Because the C1 L and C0 L signals are asserted, the BUS STROBE L signal jam transfers into the AC the information on the DATA lines. The long delay in asserting the BUS STROBE L signal ensures that the AC Register input lines have settled before the register is clocked.

When an LRC or a CRC is performed on a message, the generated BCC must be transferred to the AC Register. This is accomplished by the RCRL instruction, alone, or by both the RCRL and RCRH instructions. Either instruction generates a signal that enables NOR gate E43. The output of this gate enables NAND gates E25C and D to assert the C1 L and C0 L signals. The BCC is gated onto the DATA lines and jam transferred into the AC Register at TP3 time of the RCRL or RCRH instruction (the BUS STROBE L signal is not asserted by the I/O Transfer logic).

A VRC can be carried out on a character in response to an RCTV instruction; i.e., a parity test is made on the character. This instruction causes the RCTV L signal to be asserted, thereby enabling NOR gate E28. The resulting TEST VRC signal enables NAND gate E3 to pull the OMNIBUS SKIP line low, if the PARITY signal is asserted by the VRC logic. Remember that the PARITY signal, when asserted, indicates that the tested character either does exhibit correct parity (VRC logic wired for an odd parity check) or does not exhibit correct parity (VRC logic wired for an even parity check). Therefore, in the case of an odd parity check, the asserted PARITY signal would cause the program to skip *over* an error-handling instruction; in the case of an even parity check, the asserted PARITY signal would cause the program to skip *to* an error-handling instruction.

Note that the TEST VRC signal also asserts NAND gate E44A, thereby asserting the C0 L signal. This action results in the AC Register being cleared at TP3 time of the RCTV instruction (to be exact, the AC is loaded with zeros at TP3 time). Because the character is merely tested by the RCTV instruction, it need not be returned to the AC, as is the case with the RCCV instruction. A similar situation exists when only an LRC or a CRC is performed. Each character is transferred from the AC Register to contribute to the BCC generation. The character need not be returned to the AC. Consequently, the RCGB L signal causes NAND gate E44D to be enabled, thereby asserting the C0 L signal (remember that the VRC (RCGB) flip-flop is set only if a VRC is to be initiated by the RCGB instruction).

6.8 BCC LOGIC

A block diagram of the BCC logic is shown in Figure 6-11. The logic is used to generate a BCC for either an LRC or a CRC. Each character that contributes to the BCC accumulation is parallel-loaded into the 8-bit Parity Register at TP3 time of the RCGB IOT instruction. The character is then shifted from the Parity Register into the 16-bit BCC Register by 9.5 MHz clock pulses. The accumulation is held in the BCC Register until either an RCRL or an RCRH IOT instruction is issued.

Each bit of the character in the Parity Register is Exclusive-ORed with the bit in the LSB position of the BCC Register. The result is placed on the SERIAL QUOTIENT line and shifted into the BCC Register. The particular bit position into which the SERIAL QUOTIENT signal is shifted depends on the state of the control signals

shown in the bottom of the figure. The LRC/CRC (0) signal manipulates the register for an LRC or a CRC, while the X BITS L signal produces the correct gating configuration for the bit length of the characters.

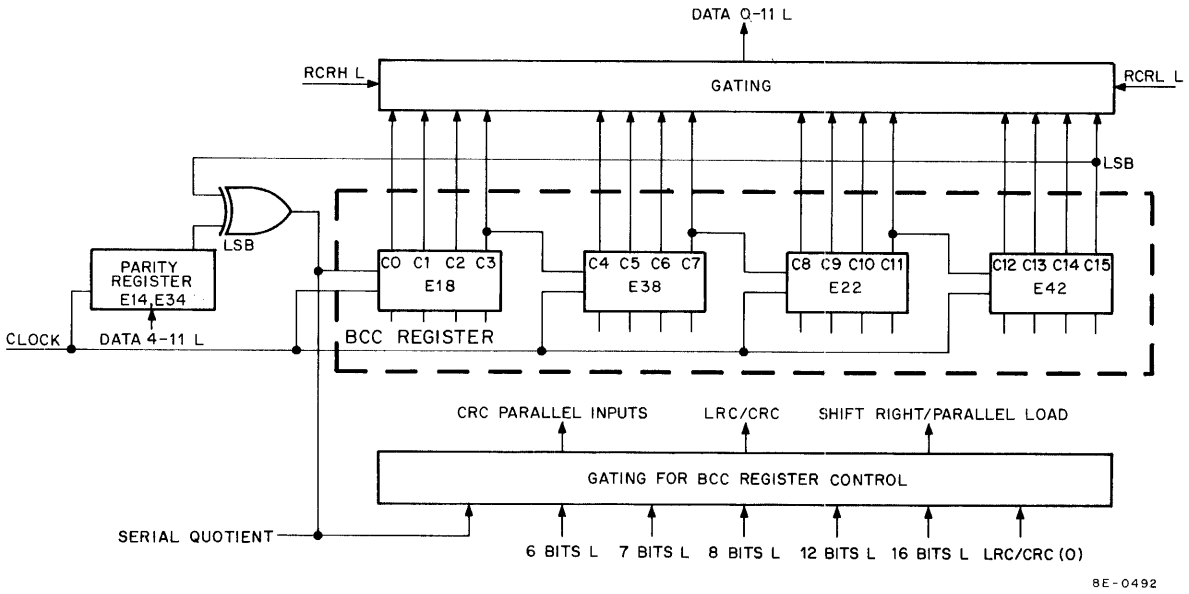


Figure 6-11 BCC Logic, Block Diagram

Consider an LRC parity check, which can be carried out on 6-, 7-, 8-, 12-, and 16-bit characters. The BCC is accumulated in the BCC Register with the LSB right-justified. Therefore, a number of left-most bit positions in the BCC Register must be ignored when a BCC of less than 16 characters is accumulated. For example, the 8 left-most bit positions (C0—C7 in Figure 6-11) must be disregarded when an 8-bit BCC is accumulated. This configuration is illustrated in Figure 6-12, a logic-block diagram that also shows the configuration for 6- and 7-bit characters.

When the character is parallel-loaded into the Parity Register, the LSB of the character is Exclusive-ORed with the bit in the C15 position (E42). The result is placed on the SERIAL QUOTIENT line. The first clock pulse of the burst (see the VRC logic and the BCC clock logic) shifts the SERIAL QUOTIENT bit into either the C8, C9, or C10 position of E22, while at the same time shifting the next character bit into the LSB position of the Parity Register.

Assume that the data character loaded into the Parity Register is 6 bits in length. The 6 BITS L signal and the CRC/LRC (0) signal are asserted by the Control Register logic (consequently, the 16 BITS L signal is negated). Therefore, each SERIAL QUOTIENT bit is shifted into the C10 position of the BCC Register and shifted right by each succeeding clock pulse (note that although E22 is in the parallel-load mode, a right-shift operation is carried out because of the IC's external wiring). After six clock pulses, the character has been shifted out of the Parity Register. Each bit of the character has been Exclusive-ORed and shifted into the 6 most significant bit positions of the BCC Register. Each character of the message is handled in the same way. When the last character has been operated on, the BCC has been accumulated. The RCRL instruction can then be issued, causing the character to be gated to the AC Register via DATA lines 4 through 11, as shown. If the last character of the message is a BCC accumulated by a transmitting station, the final content of the BCC Register is 0, if no errors occurred.

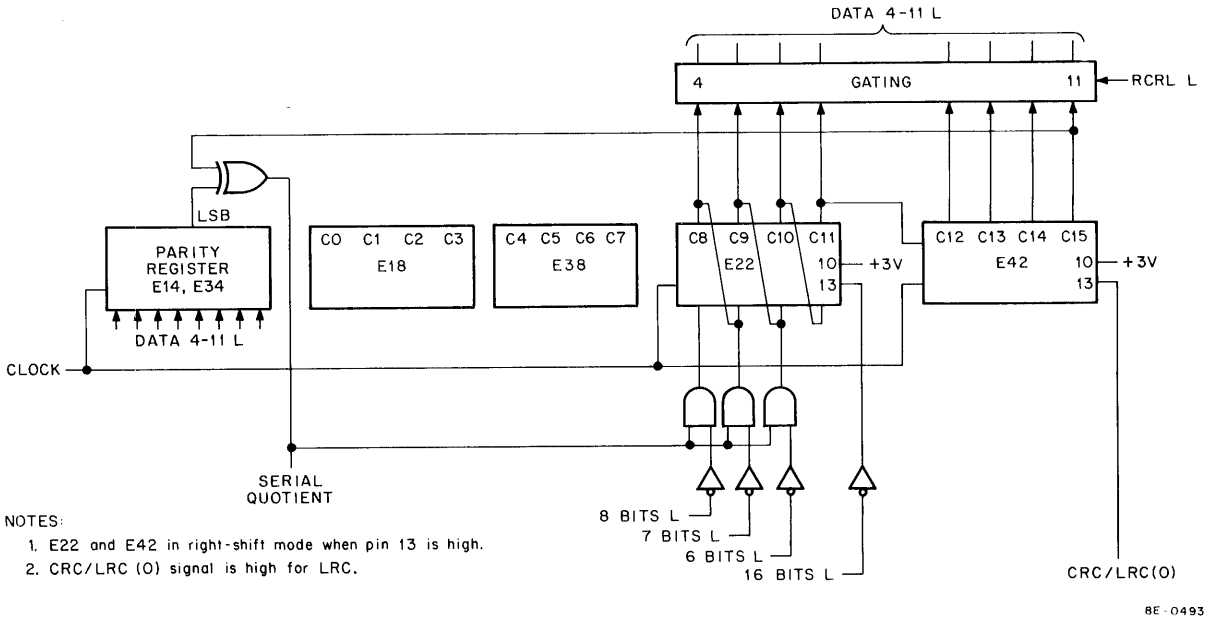


Figure 6-12 6-, 7-, and 8-Bit LRC BCC Accumulation

Figure 6-13 shows the actual logic involved in the 6-bit LRC BCC accumulation. Note that many connections shown have been left off the logic block diagram of Figure 6-12. One should study Figure 6-13 thoroughly to pick up fine points not illustrated in the logic block diagram. Refer to engineering drawing no. E-CS-M884-0-1 for the complete logic presentation.

An LRC can be used to accumulate a 12-bit or 16-bit BCC, also. The BCC Register configuration in each case is shown in Figure 6-14. Consider the 12-bit BCC first.

To accumulate such a BCC, the 12 BITS L signal and the CRC/LRC (0) signal are asserted by the Control Register logic. Therefore, ICs E18 and E42 are placed in the right-shift mode, while E22 is in the parallel-load mode. IC E38 is wired so that it is always in the right-shift mode. The output of E38, the C7 bit, is applied to the serial input line of E22. However, E22 is in the parallel-load mode and ignores the output of E38. Instead, the C3 bit is gated to pin 10 of E22, the parallel-load input of the C8 bit. Thus, the 12 register bits used for the 12-bit BCC are C0—C3 and C8—C15.

To fill these 12 register bits, a 12-bit character must be transferred from the PDP-8/E memory. Because the Parity Register can accommodate only 8 bits, one must use the following technique:

a. The 12-bit character is brought from memory and loaded into the AC Register by a TAD instruction.

b. The RCGB instruction is issued, causing the character to be gated via the DATA lines to the Parity Register. At TP3 time, the 8 least significant bits are loaded into the Parity Register (bit 11 of the character is loaded into the LSB position). The AC Register is cleared (see the I/O XFER logic).

c. The BCC Clock logic generates a burst of 6 clock pulses, shifting the 6 least significant bits of the character into the 6 most significant bit positions of the BCC Register (C0—C3, C8, C9).

d. While the registers are being shifted, another TAD instruction loads the same character into the AC Register.

(continued on next page)

e. A BSW instruction (swap bytes in AC) is issued, causing the 6 most significant bits of the character to be placed in the 6 least significant bit positions of the AC (the MSB of the character goes to AC bit 6).

f. Another RCGB instruction is issued. Now the Parity Register is loaded with the 6 most significant bits of the character; bit 0 of the character is loaded into the Parity Register LSB position. The AC Register is cleared.

g. Six clock pulses shift the 6 most significant bits of the character into the BCC Register and shift the 6 least significant bits of the character to the right.

h. The 12-bit character is now contained in the 12-bit BCC Register. Each succeeding character is handled in the same way.

When the BCC has been accumulated, the RCRL instruction causes the character to be gated to the AC Register. The 4 most significant bits are gated via DATA lines 0 through 3, as shown. If the last character of the message is a BCC accumulated by a transmitting station, the final content of the BCC Register is 0, providing no errors occurred in transmission.

When a 16-bit BCC is accumulated, all 16-bit positions of the BCC Register are used, and each IC is placed in the right-shift mode, as Figure 6-14 illustrates. Because the PDP-8/E cannot store an entire 16-bit character in one memory location, two locations are required. The 8 most significant bits of the character are stored in location "A", in a right-justified format, while the 8 least significant bits of the character are stored in location "B", also in right-justified format. A TAD instruction brings the contents of location B to the AC Register first. An RCGB instruction transfers the 8 least significant bits to the Parity Register; clock pulses then shift the bits into the 8 most significant bit positions of the BCC Register. Another TAD instruction brings the contents of location A to the AC. A second RCGB instruction results in the 8 most significant bits of the character being shifted into the 8 most significant bit positions of the BCC Register. At the same time, the 8 least significant bits of the character are right-justified into the 8 least significant bit positions. As Figure 6-14 indicates, the 8 least significant bits of the BCC are transferred to the AC Register via DATA lines 4 through 11 by the RCRL instruction, while the 8 most significant bits are transferred by the RCRH instruction.

The BCC accumulation during a CRC parity check is basically the same as during an LRC: the message characters are parallel-loaded into the Parity Register; the bits in the LSB positions are Exclusive-ORed; the result is placed on the SERIAL QUOTIENT line and shifted into the BCC Register. However, to implement the generating polynomial, P (X), additional Exclusive-ORing is carried out, as illustrated in Figure 6-15.

The logic block diagrams shown in Figure 6-15 illustrate Exclusive-OR gating for both CRC-12 and CRC-16. The gating enables the logic to implement the two generating polynomials. For industry-compatible application, CRC-12 is used with 6-bit characters, while CRC-16 is used with 8-bit characters. CRC-12 could be used to generate the BCC of a message consisting of 12-bit characters, but this would require the same sort of program manipulation as described for LRC-12. The same can be said when considering CRC-16 with 16-bit characters. Because the CRC logic is so similar to the LRC-12 and LRC-16 logic, no further logic description is presented.

SECTION 5 MAINTENANCE

See Volume 1 for maintenance information that can be applied to the KG8-E option. The diagnostic program and the single-step test feature should be used to isolate problems that are traced to the KG8-E.

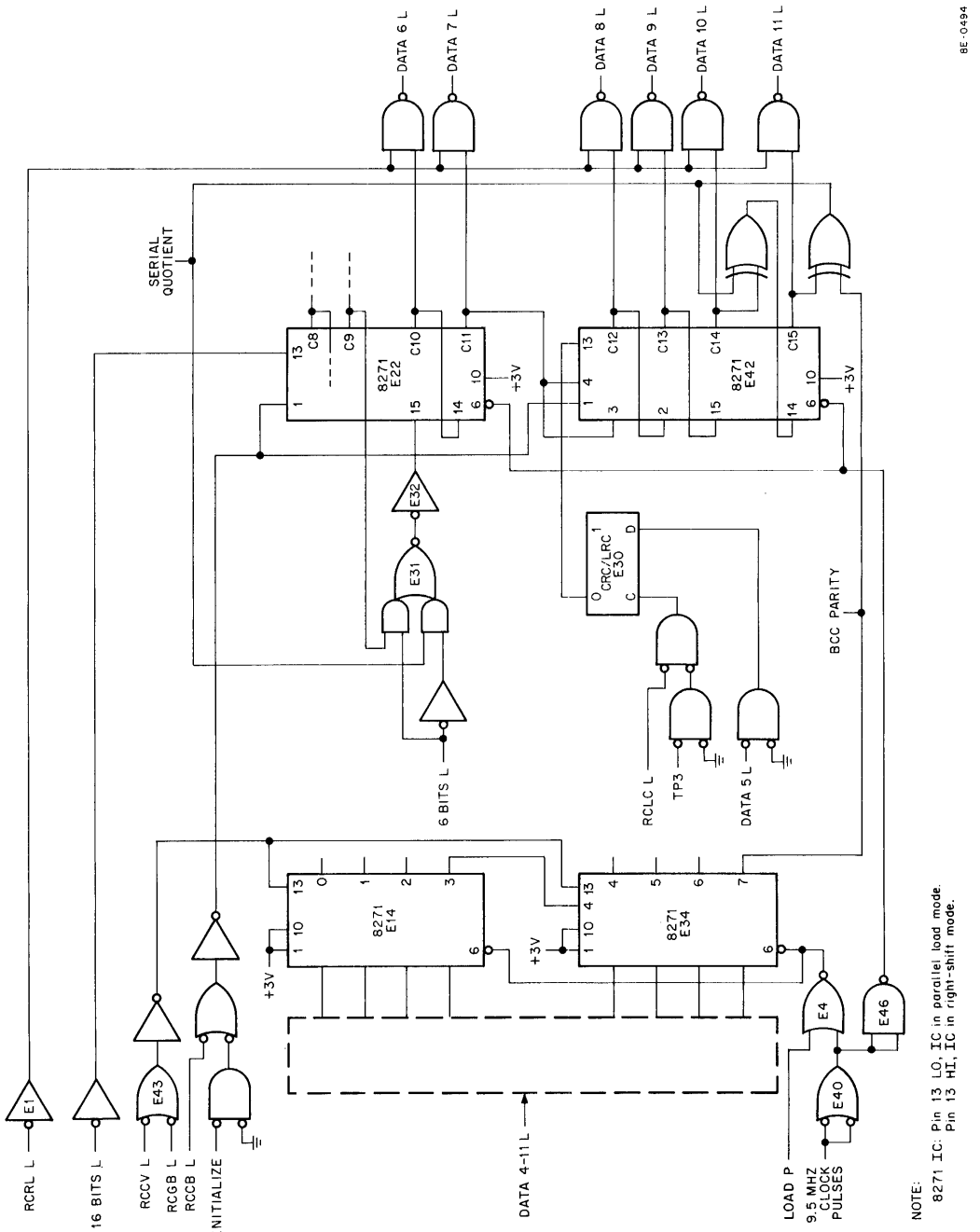


Figure 6-13 BCC Generating Logic (Using LRC Technique – 6-Bit Character)

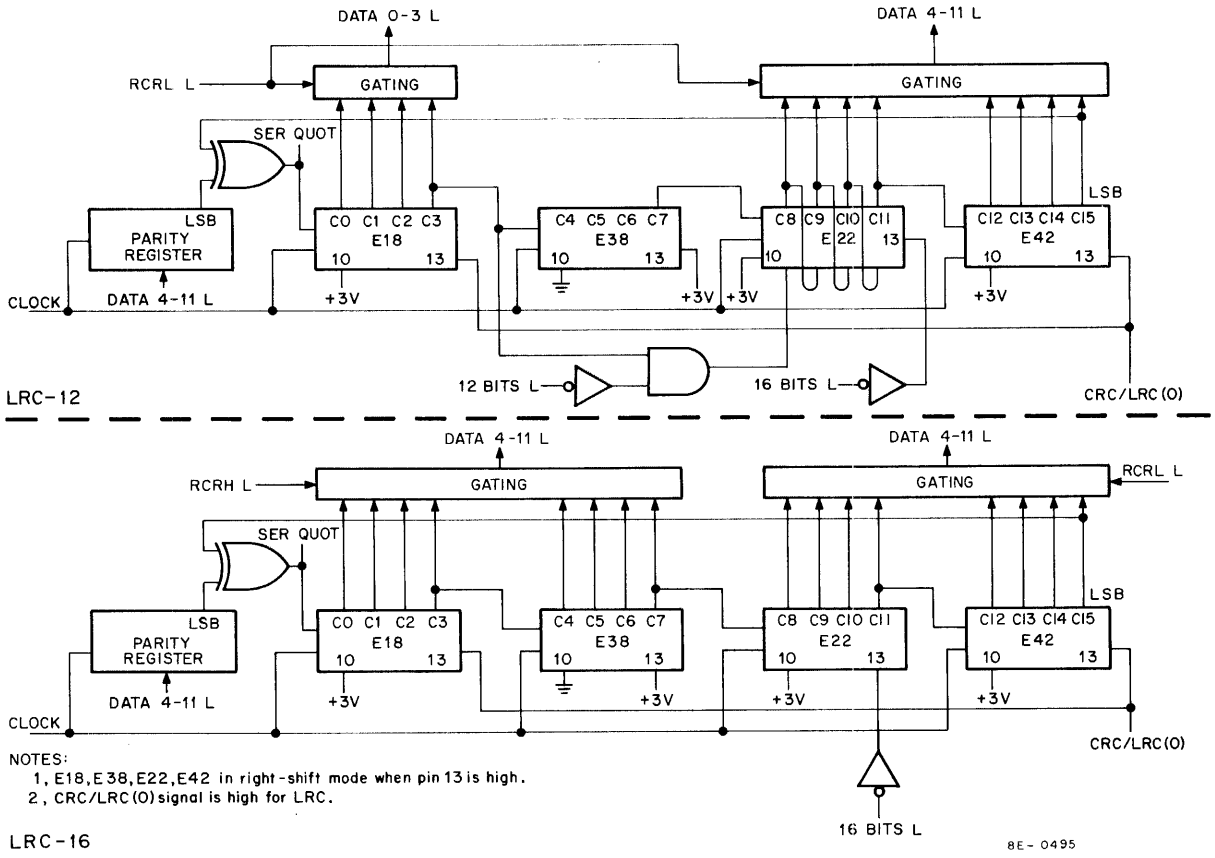
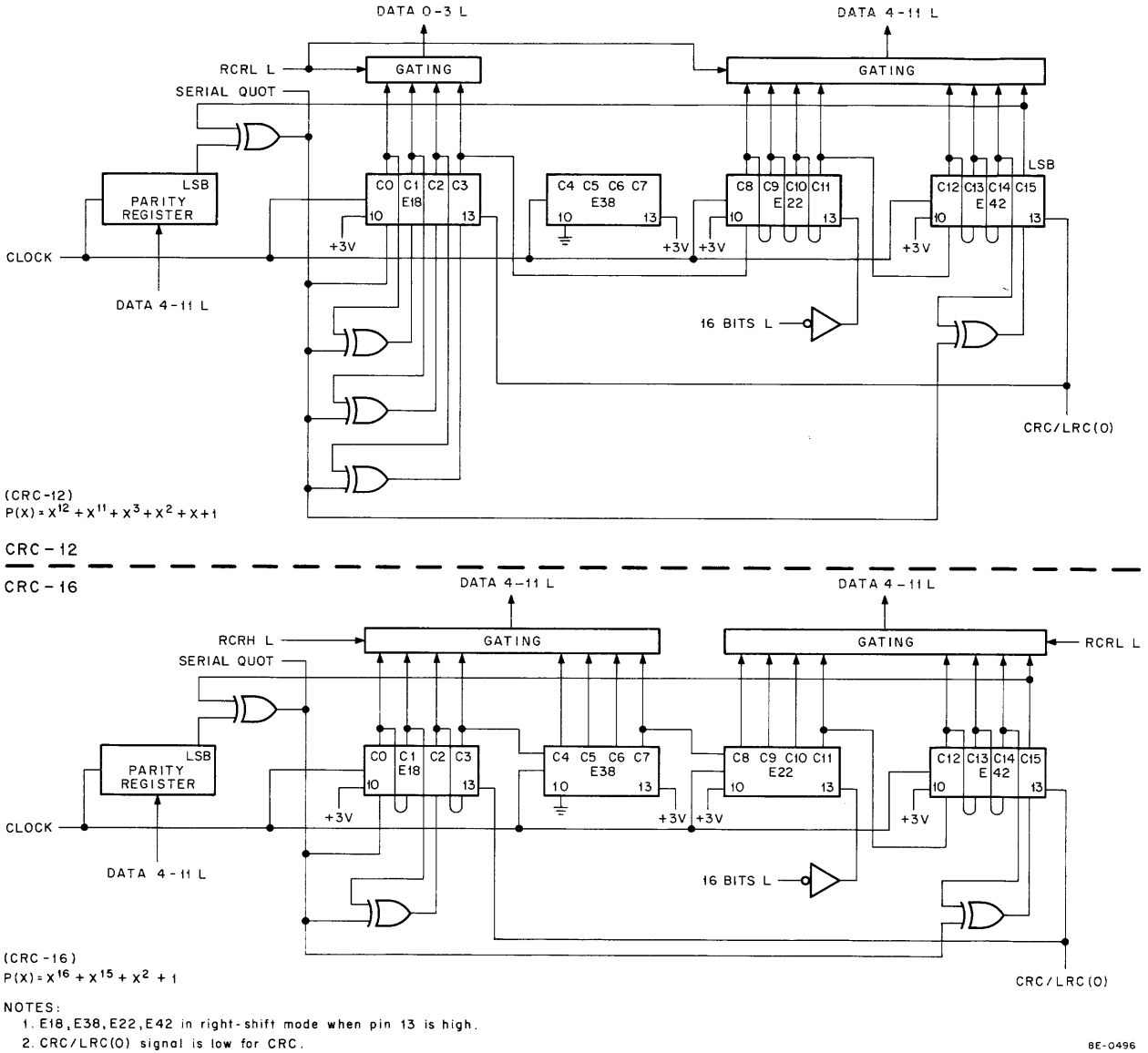


Figure 6-14 Logic Block Diagram: LRC-12, LRC-16

SECTION 6 SPARE PARTS

Table 6-2 lists recommended spare parts for the KG8-E. These spare parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.



NOTES:
1. E18, E38, E22, E42 in right-shift mode when pin 13 is high.
2. CRC/LRC(0) signal is low for CRC.

8E-0496

Figure 6-15 Logic Block Diagram: CRC-12, CRC-16

Table 6-2
KG8-E Recommended Spare Parts

DEC Part Number	Description	Quantity
19-09704	IC DEC 314	1
19-09485	IC DEC 380	1
19-05575	IC DEC 7400	1
19-09004	IC DEC 7402	1
19-09686	IC DEC 7404	1
19-05576	IC DEC 7410	1
19-05580	IC DEC 7450	1
19-05547	IC DEC 7474	1
19-10011	IC DEC 7486	1
19-09594	IC DEC 8251	1
19-09615	IC DEC 8271	2
19-09705	IC DEC 8881	2
19-10035	IC DEC 74197	1
10-00016	Capacitor, 100 pF, 100V, 5%	1
10-01610	Capacitor, 0.01 μF, 100V, 20%, DISC	5
10-00027	Capacitor, 820 pF, 100V, 5%	1
13-00293	Resistor, 330Ω, 1/4W, 10%	1
13-01401	Resistor, 750Ω, 1/4W, 5%	1
13-00271	Resistor, 220Ω, 1/4W, 5%	1

PART 6
CARD READERS

CHAPTER 7
CM8-E/CR8-E CARD READERS

SECTION 1 INTRODUCTION

Two card reader options are available for use with the PDP-8/E. Both transfer data from EIA-standard data cards to the CPU AC Register. The CM8-E Optical Mark Card Reader option reads data from pencil-marked or punched-hole data cards; the CR8-E Card Reader option reads only from punched-hole cards. Each option uses the same control module to interface the card reader and the computer. This module, DEC M843, plugs into the OMNIBUS and connects to the external card reader via a signal cable that is supplied with the option.

The card reader used with the CM8-E option is the GDI Model 100-M Optical Mark Reader. That used with the CR8-E option is the Documation Model M200 Card Reader. These card readers are discussed only to the extent necessary both to fully describe the control operation and to present supplementary information concerning installation and checkout of the option. Details of the installation, operation, troubleshooting, and maintenance of the card reader, itself, can be found in the respective technical manual. Other publications and documents relevant to the CM8-E and CR8-E are:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* — DEC 1972
b. *PDP-8/E Maintenance Manual, Volume 1*
c. CM8-E Diagnostic, MAINDEC-8E-D2DA, CR8-E Diagnostic, MAINDEC-8E-D2EA
d. DEC Engineering Drawing, Card Reader Control, E-CS-M843-0-1.

SECTION 2 INSTALLATION

The CR8-E/CM8-E Card Reader option is installed on site by DEC Field Service personnel. The customer should not attempt to unpack, install, checkout, or service the equipment.

Insert the option control module (DEC M843) into the PDP-8/E OMNIBUS. Refer to Table 2-3, Volume 1, for information concerning recommended module priorities (the CR8-E/CM8-E is a "non-memory" option).

Connect the control to the card reader with the signal cable provided. J1 of the control connects either to J2 (CR8-E) or to J5 (CM8-E) of the card reader. See Section 5 for cable and connector pin assignments.

The CR8-E/CM8-E option can be checked for correct operation by running the appropriate diagnostic program. Refer to the respective card reader instruction manual for card reader checkout procedures.

SECTION 3 BLOCK DIAGRAM DESCRIPTION

Figure 7-1 is a block diagram of the CR8-E/CM8-E Control. OMNIBUS pin numbers can be found on DEC engineering drawing E-CS-M843-0-1. The pin assignments for connector receptacle J1 are given in Table 7-4.

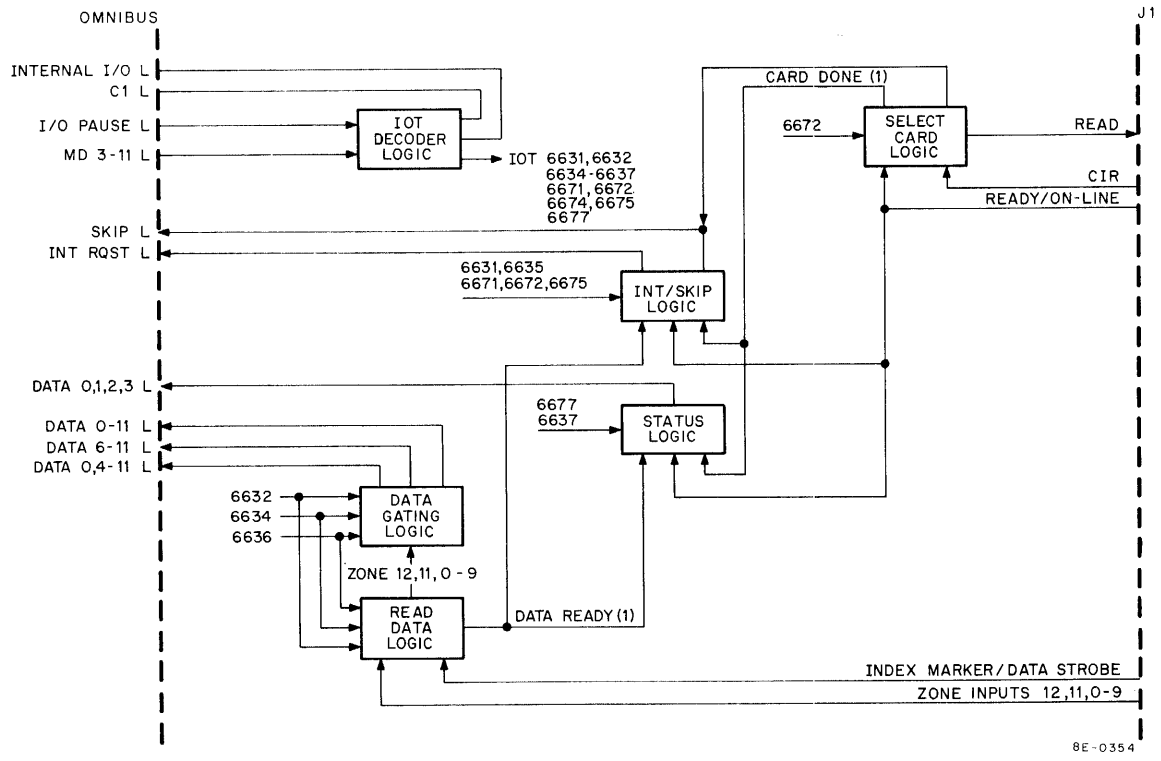


Figure 7-1 CR8-E/CM8-E Control Block Diagram

The signals shown on the block diagram are related in the timing diagram, Figure 7-2. The IOT instructions are listed in Table 7-1 (the same instruction set is used by both the CR8-E and the CM8-E; thus, the two card readers cannot be used in the same system). Refer to Figures 7-1 and 7-2 and Table 7-1 while reading the block diagram description.

The card reader asserts the signal READY/ON LINE when the reader is clear of errors and ready to receive a card read command. When the 6672 instruction is issued, the control's IOT decoder logic asserts the 6672 L signal. At TP3 time, the select card logic asserts the READ signal that initiates the card pick cycle in the card reader. A card is brought into the reader card track and advanced toward the read station. The CIR signal is asserted by the reader when the card has arrived at the read station.

The card columns pass sequentially before the read station sensors beginning with column 1 (note that an 80-column card is illustrated in the timing diagram; this applies only to the CR8-E, the CM8-E being limited to use with 40-column cards). The information in the 12 data rows of the column is transferred, via the Zone Input lines, to the 12-bit Zone Register of the read data logic. The reader generates an INDEX MARKER/DATA STROBE signal for each card column; this signal clocks the information on the Zone Input lines into the Zone Register. At the same time, INDEX MARKER STROBE causes the read data logic to assert the DATA READY (1) signal.

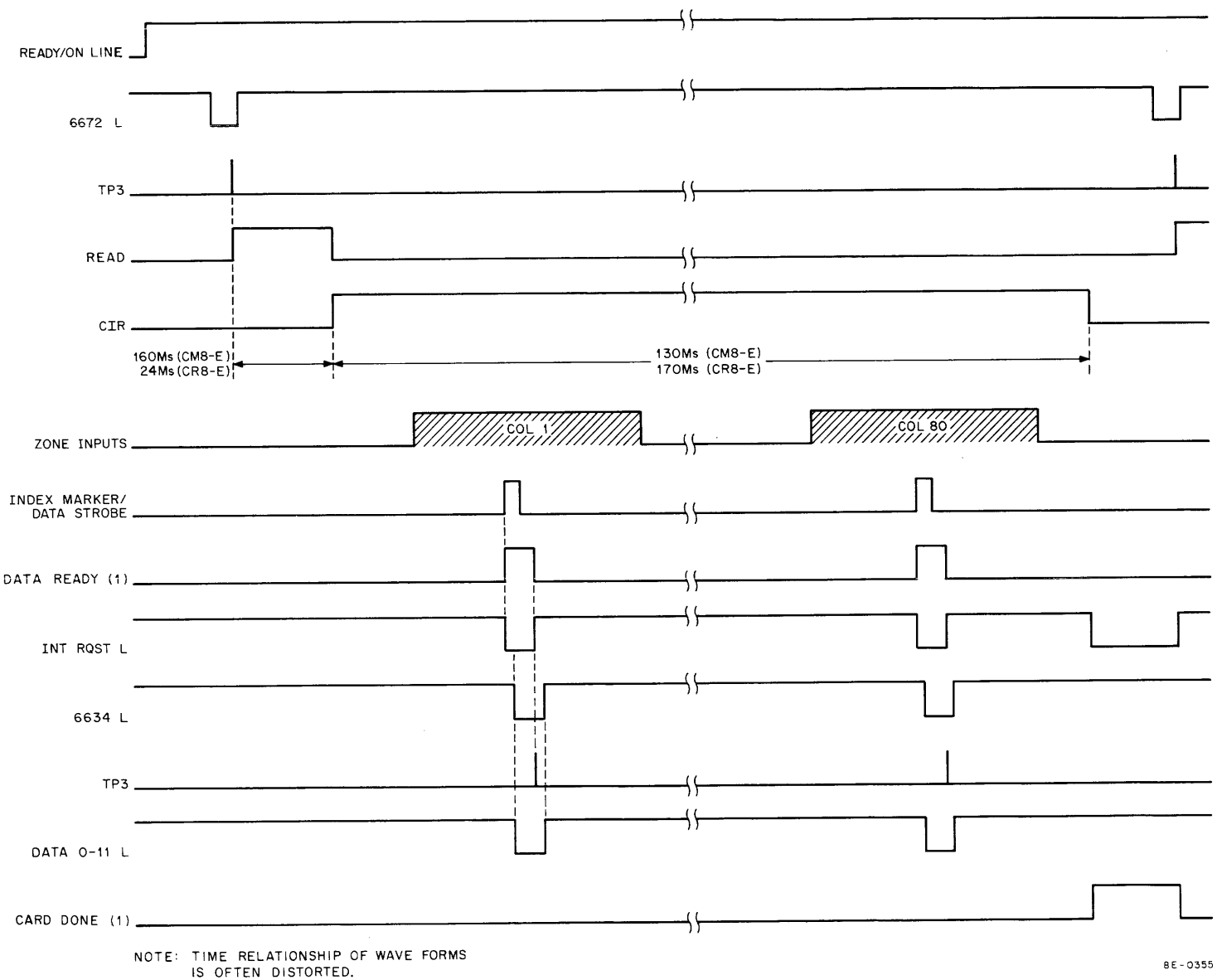


Figure 7-2 Timing, CR8-E/CM8-E Control

Table 7-1
CM8-E/CR8-E Instruction List

Octal Code	Mnemonic	Function
6631	RCSF	Skip on the Data Ready flag. Senses the state of the DATA READY flip-flop. If the flip-flop is set, the program counter is incremented so that the next sequential instruction is skipped.
6632	RCRA	Read alphanumeric. Causes a 6-bit alphanumeric code, which is translated from the 12-bit code of a card column, to be gated to AC bits 6–11. Clears the DATA READY flip-flop.
6634	RCRB	Read binary. Causes the 12-bit code of a card column to be gated to AC bits 0–11 (column rows 12, 11, and 0 are gated to AC0, 1, and 2, respectively; rows 1–9 are gated to AC3–11, respectively). Clears the DATA READY flip-flop.
6635	RCNO	Read conditions out to card reader. Selectively sets or clears two flip-flops that control the INT/skip logic. If AC11 is logic 1, the RCNO instruction sets the DATA AND CARD INT flip-flop, thereby enabling the DATA READY flip-flop and the CARD DONE flip-flop to cause a program interrupt and an instruction skip. If AC10 is logic 1, the RCNO instruction sets the RDY/TROUBLE INT flip-flop, thereby enabling a transition in the READY/ON LINE signal to cause a program interrupt and an instruction skip.
6636	RCRC	Read compressed. Causes an 8-bit code, which is translated from the 12-bit code of a card column, to be gated to AC bits 4–11. Gates a logic 1 into AC bit 0, if a hardware validity-check circuit has detected more than one hole or mark in rows 1–7 of a card column. Clears the DATA READY flip-flop.
6637	RCNI	Read conditions in from card reader. Causes the state of the DATA READY flip-flop and the state of the CARD DONE flip-flop to be placed on DATA lines 0 and 1, respectively. Causes the transition of the READY/ON LINE signal to be represented by DATA bits 2 and 3. If the signal has gone high, the DATA 3 L signal is asserted, while the DATA 2 L signal is negated; if the signal has gone low, the DATA 3 L signal is negated, while the DATA 2 L signal is asserted.
6671	RCSD	Skip on Card Done flag. Senses the state of the CARD DONE flip-flop. If the flip-flop is set, the program counter is incremented so that the next sequential instruction is skipped.
6672	RCSE	Select card and skip if ready. If the card reader has asserted the READY/ON LINE signal, the program counter is incremented so that the next sequential instruction is skipped; a card is started toward the read station. Clears the CARD DONE flip-flop.

(continued on next page)

Table 7-1 (Cont)
CM8-E/CR8-E Instruction List

Octal Code	Mnemonic	Function
6674	RCRD	Clear Card Done flag. Clears the CARD DONE flip-flop.
6675	RCSI	Skip if interrupt being generated. If any one of four conditions has caused a program interrupt, the program counter is incremented so that the next sequential instruction is skipped.
6677	RCTF	Clear Transition flag. Clear the TRANSITION flip-flop in the status logic.

If the control is programmed to operate in the interrupt mode, as the timing diagram illustrates, DATA READY (1) causes the INT/skip logic to assert the OMNIBUS INT RQST L signal. The computer then begins to execute the interrupt servicing routine. When the appropriate instruction (6631 in this example) in the servicing routine is decoded, the INT/skip logic asserts the OMNIBUS SKIP L signal. The computer proceeds to an appropriate subroutine to transfer the data from the read data logic to the OMNIBUS DATA lines, via the data gating logic. The 6634 instruction is used in the present example to transfer the data; this instruction is decoded and the resulting signal, 6634 L, gates the data through the data gating logic to the DATA 0—11 lines. At TP3 time, the information is loaded into the AC Register and the DATA READY (1) signal is negated. When the data from all columns has been transferred, the CIR signal is negated and the select card logic asserts the CARD DONE (1) signal. This signal asserts the INT RQST L signal, the card pick subroutine is entered, and a new 6672 instruction is decoded.

The control status logic allows the program to check the status of the DATA READY (1) signal, the CARD DONE (1) signal, and the READY/ON LINE signal. The significance of this status logic is explained in detail in Paragraph 7.5.

SECTION 4 DETAILED LOGIC

7.1 IOT DECODER LOGIC

The IOT decoder logic is shown in Figure 7-3. Bits MD3—8 are decoded by NAND gates E12 and E16 to produce signals 667X, and 663X, respectively. Each of these signals causes the OMNIBUS INTERNAL I/O L signal to be asserted, ensuring that the positive I/O bus interface ignores the IOT instruction. Also, each signal is gated with bits MD 9, 10, and 11 in decoder E3 to produce the IOT signals shown. The inverted 663X signal, likewise, is gated with bits MD 9, 10, and 11, but in decoder E2. This decoder produces the six IOT signals shown, four of which cause the OMNIBUS C1 L signal to be asserted. When the C1 L signal is asserted, information placed on the DATA lines is gated through the CPU Major Register Gating and ORed into the AC Register (a jam transfer is unnecessary because a card reader program always clears the AC Register before data is transferred from the card reader control).

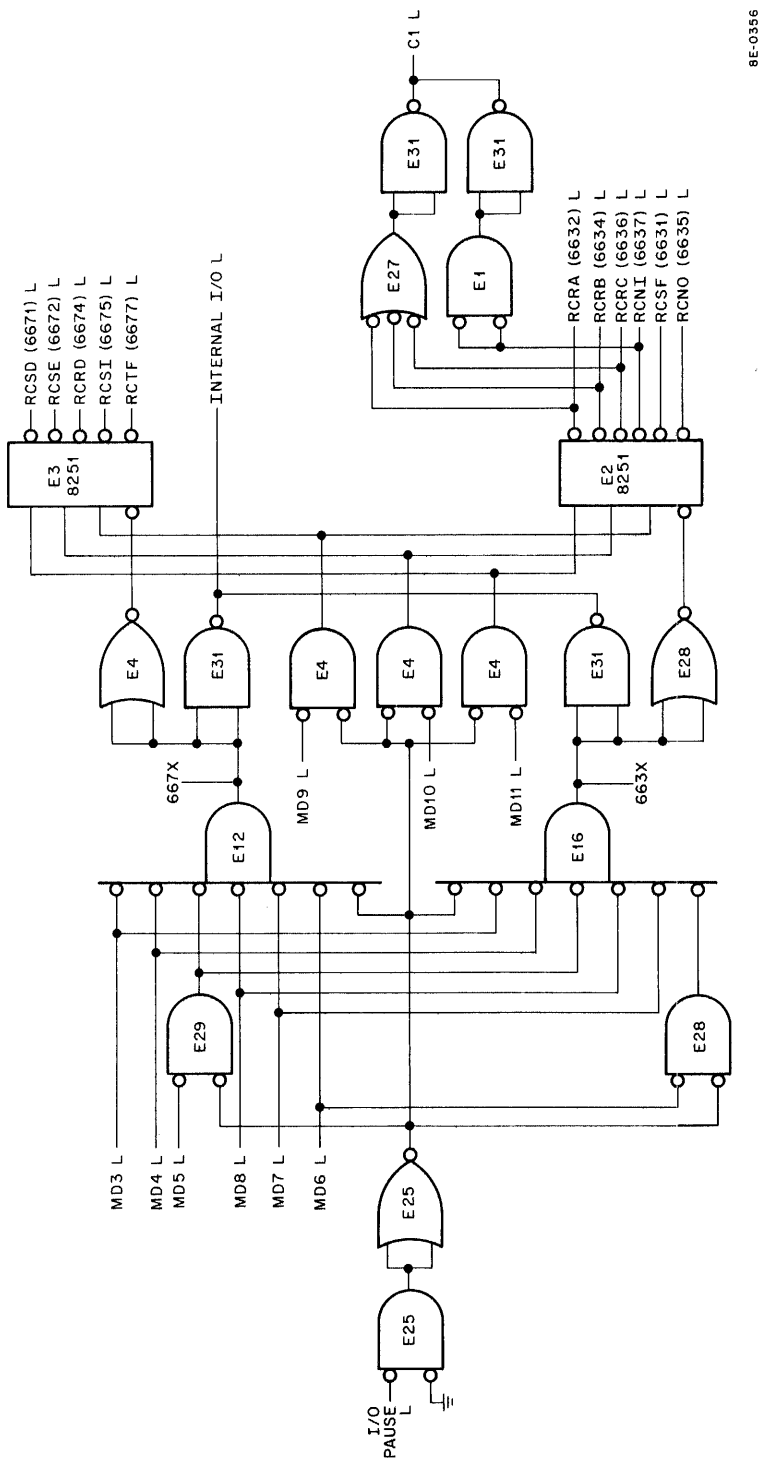


Figure 7-3 IOT Decoder Logic

7.2 SELECT CARD LOGIC

The select card logic is shown in Figure 7-4. When the 6672 IOT instruction is decoded, the IOT decoder logic generates the RCSE L signal. If the card reader is ready, the signal at pin J1J, READY or ON LINE, is high and NAND gate E20 asserts OMNIBUS SKIP L. The two E40 NAND gates at the READY/ON LINE input comprise a Schmitt trigger that prevents noise on the input line from triggering the select card logic (a Schmitt trigger is placed in the J1N input for the same reason).

At TP3 time of the 6672 instruction NAND gates E24 and E27 are enabled. Thus, the CARD DONE flip-flop is cleared and the READ flip-flop is set, the latter flip-flop causing NOR gate E39 to assert the READ signal. This signal causes the card reader to begin processing the data card. When the card is in the read station, the signal at pin J1N, CIR (Card In Reader), goes high, clearing the Read flip-flop. When the card has been processed the CIR signal is negated. The negative-going edge of the signal sets the CARD DONE flip-flop.

Note that both the CARD DONE flip-flop and the READ flip-flop are cleared by the OMNIBUS INITIALIZE signal via NOR gate E29. The CARD DONE flip-flop, in addition to being cleared by this signal and by the RCSE instruction, can be cleared by the RCRD instruction (Clear Card Done flag). Normally, the CARD DONE flip-flop generates an interrupt request when it is set; the result of the program interrupt is a re-issue of the RCSE instruction. Thus, another card is fed into the read station and processed. However, the programmer might wish to halt the reading operation when a particular card has been processed. Such a halt can be carried out easily by a subroutine; but, the subroutine must issue the RCRD instruction so as to clear the CARD DONE flip-flop and remove the ground signal from the OMNIBUS INT RQST line.

The READ flip-flop can also be cleared by a signal other than INITIALIZE. This other signal is taken from the J1J input Schmitt trigger, as Figure 7-4 illustrates. Thus, when the READY/ON LINE signal goes low, the READ flip-flop is cleared, negating the READ signal. This action prevents an uncontrolled start of the card reading operation when the reader is manually re-started following a trouble condition.

7.3 READ DATA LOGIC

As each card column passes the read array in the card reader, 12 data row bit signals and one INDEX MARKER/DATA STROBE signal can be generated (a data row bit signal is generated if a hole/optical mark is present in a data row). The data row bit signals are transferred to the Zone Register in the read data logic, as illustrated in Figure 7-5. Each bit is applied to the data (D) input of the corresponding Zone Register flip-flop; i.e., the Data Row 12 bit is applied to the ZONE 12 flip-flop, the Data Row 0 bit is applied to the Zone 0 flip-flop. The INDEX MARKER/DATA STROBE signal is also transferred to the read data logic. However, before it is applied to the clock (C) input of the Zone Register flip-flops, it is delayed for approximately 2 μs by a network that includes the one-shot multivibrators E32 and E45. This network ensures that the D-input lines of the Zone Register flip-flops have settled before the flip-flops are clocked by the INDEX MARKER/DATA STROBE signal. This precaution must be taken because some card readers do not provide a sufficient amount of time between generation of the Data Row bit signals and the INDEX MARKER/DATA STROBE signal (those listed in Section 1 do provide sufficient time; see the various card reader instruction manuals for clarification).

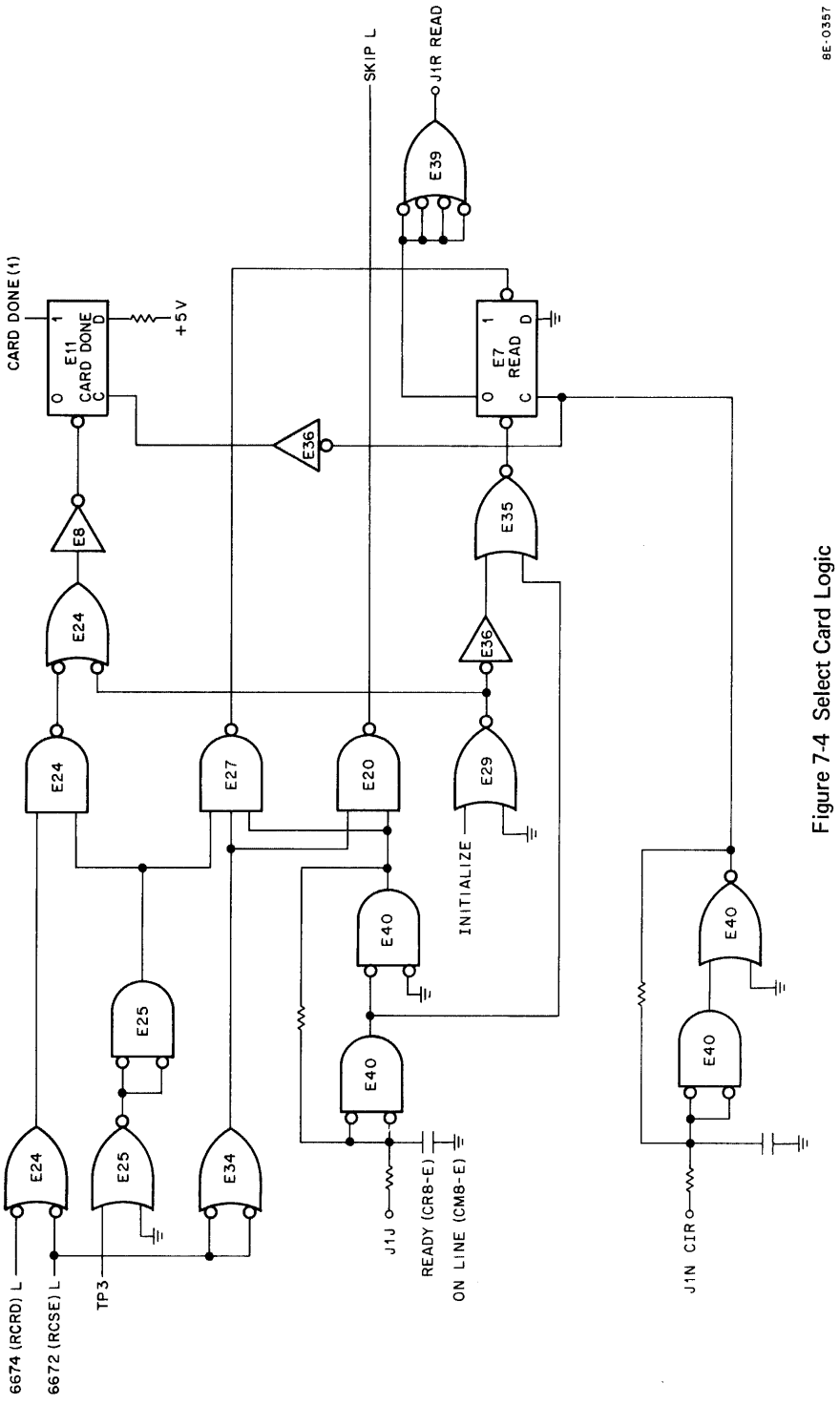


Figure 7-4 Select Card Logic

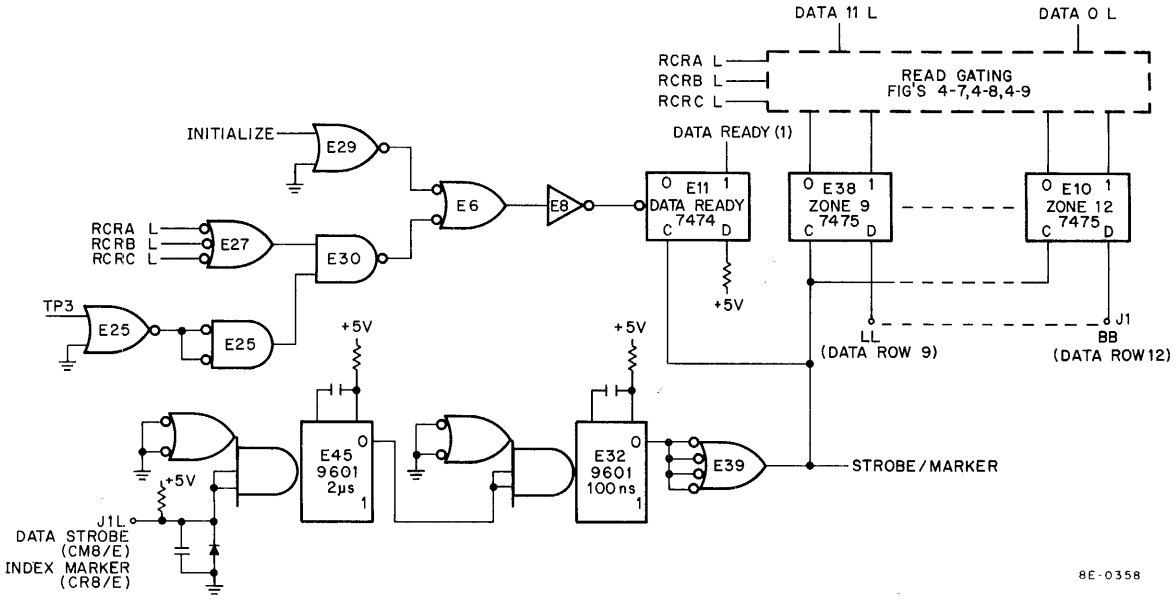


Figure 7-5 Read Data Logic

The INDEX MARKER/DATA STROBE signal clocks not only the Zone Register flip-flops, but also the DATA READY flip-flop. Thus, when the data from a card column is loaded into the Zone Register, the DATA READY (1) signal is asserted. The state of this signal can be tested by a program instruction or by using the interrupt mode. In either case, the program then enters a subroutine that contains one of the read instructions, RCRA, RCRB, or RCRC. As illustrated in Figure 7-5, these instructions generate signals that cause the data in the Zone Register to be gated through the read gating logic to the OMNIBUS DATA lines. At TP3 time of the instruction the DATA READY flip-flop is cleared and the procedure is repeated for the next card column of data.

7.4 INTERRUPT/SKIP LOGIC

Four conditions in the Card Reader option can cause a program interrupt; viz., the data from a card column is ready to be placed on the DATA lines, all columns of the present card have been read, the READY/ON LINE signal has gone high, the READY/ON LINE signal has gone low. The first two conditions are represented, respectively, by the set state of the DATA READY flip-flop and of the CARD DONE flip-flop; the last two conditions are represented by the set state of the TRANSITION flip-flop. These three flip-flops are illustrated in Figure 7-6.

Also shown in Figure 7-6 are two interrupt control flip-flops, identified as DATA AND CARD INT and RDY/ TROUBLE INT. These two flip-flops are set under program control and enable the three condition flip-flops to assert the OMNIBUS INT RQST L and SKIP L signals. Specifically, consider the DATA AND CARD INT flip-flop, E23A. This flip-flop can be set at TP3 time of the RCNO instruction, if the AC11 bit is logic 1 (this flip-flop is set by the INITIALIZE signal for program compatibility with other PDP-8 family computers; if the programmer does not want the set state, he must clear the flip-flop by programming the RCNO instruction with a logic 0 in the AC11 bit). The 1-output of E23A is applied to two NAND gates, E15, and an AND/NOR gate, E19. The E15 gates enable the CARD DONE flip-flop and the DATA READY flip-flop to assert the INT RQST L signal. Gate E19 enables the same two flip-flops to assert the SKIP L signal when an RCSI instruction is issued. The RDY/ TROUBLE INT flip-flop, E23B, operates like E23A. It, too, is under program control of the RCNO instruction;

however, AC bit 10 determines if the flip-flop is set or cleared (note that this flip-flop is cleared, rather than set, by the INITIALIZE signal). Its 1-output is also applied to gates E15 and E19; however, in this case, E15 and E19 are enabled by the TRANSITION flip-flop rather than by the DATA READY or CARD DONE flip-flops.

As with many other PDP-8/E options, the Card Reader option can engage in a programmed I/O transfer of data or it can operate in the more efficient interrupt mode of data transfer. If the interrupt control flip-flops, E23A and E23B, are not set, a background program must execute a loop that tests for a desired condition. For example, the program can repeatedly test the DATA READY flip-flop with the RCSF instruction. When the flip-flop is set the RCSF L signal causes NAND gate E20 to assert the SKIP L signal. The program then proceeds to an appropriate subroutine. The same method can be used to test the CARD DONE flip-flop with the RCSD instruction, and to test the READY/ON LINE signal with the RCSE instruction.

If the programmer wishes to use the interrupt mode, he can proceed in a number of ways. For example, if E23A is set, the DATA READY flip-flop, when set, causes NAND gate E15 to assert the INT RQST L signal. The program executes the interrupt servicing routine; the RCSF instruction in the routine results in a jump to the appropriate subroutine. The same method can be used for the CARD DONE flip-flop. However, note that the READY/ON LINE signal does not directly cause an interrupt request. Rather, the TRANSITION flip-flop, which reflects the state of the READY/ON LINE signal, is used to assert the INT RQST L signal. Thus, if E23B is set, the TRANSITION flip-flop, when set in response to a transition of the READY/ON LINE signal, causes NAND gate E15 to assert the INT RQST L signal; the appropriate subroutine is ultimately carried out.

Perhaps the most efficient way of using the interrupt capability of the Card Reader option is that which tests all the interrupt flip-flops simultaneously with the RCSI instruction. If both E23A and E23B are set, AND/NOR gate E19 is enabled when any of the interrupt flip-flops is set. The RCSI instruction in the interrupt servicing routine causes NAND gate E20 to assert the SKIP L signal. A card reader routine is then entered and the specific reason for the interrupt request must be determined. This determination involves testing with the skip instructions, which is a satisfactory method in the case of the CARD DONE and DATA READY flip-flops. However, when the TRANSITION flip-flop has caused an interrupt request another method is necessary. Because the flip-flop is set by a transition of the READY/ON LINE signal, the program must also determine if the signal went from low to high or vice-versa. The RCSE instruction could determine a low to high transition by causing an instruction skip via NAND gate E20; however, the opposite transition could be detected only if the absence of such a skip caused an error routine to be entered. Another method of making the transition determination is provided by the status logic, shown in Figure 7-7 and discussed in the following paragraphs.

7.5 STATUS LOGIC

As detailed in Paragraph 7.4, any of four conditions can cause a card reader interrupt request. Two conditions involve the READY/ON LINE signal; the status logic has been devised, primarily, to deal effectively with these two conditions. The READY/ON LINE signal is applied to the Schmitt trigger, E40 (Figure 7-7). The Schmitt trigger provides an input signal for NAND gate E5D and for a delay network consisting of inverter E8, delay line DL1, and AND/NOR gate E19. The delay network gates the Schmitt trigger output in such a way that gate E19 is enabled when the READY/ON LINE signal undergoes a transition. Figure 7-8 is a timing diagram illustrating how the output is obtained.

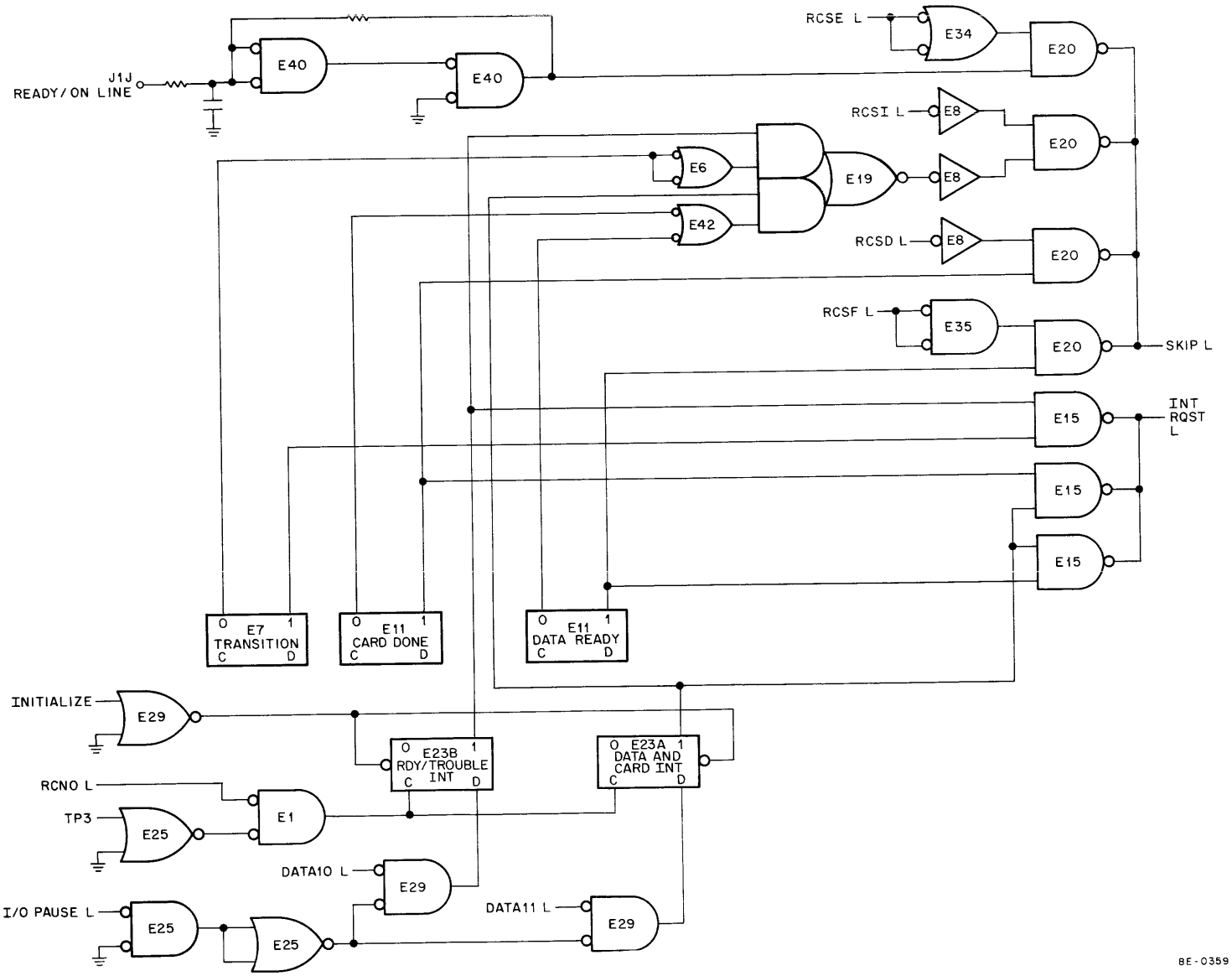


Figure 7-6 INT/Skip Logic

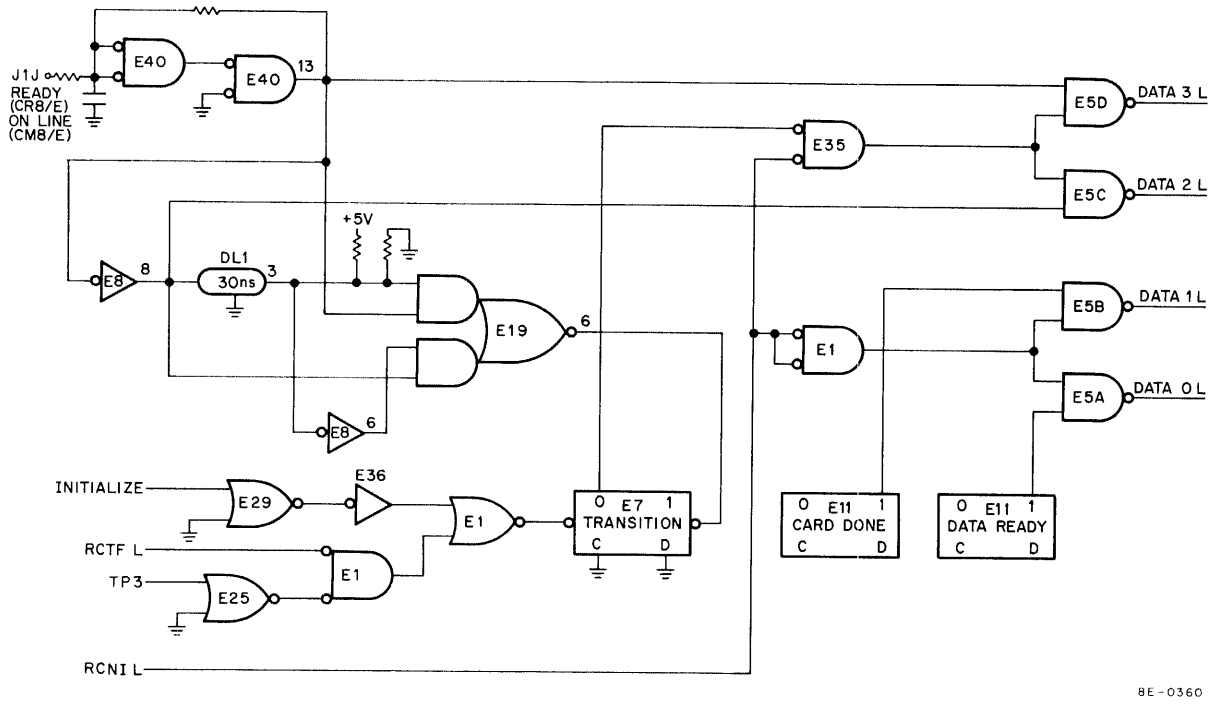


Figure 7-7 Status Logic

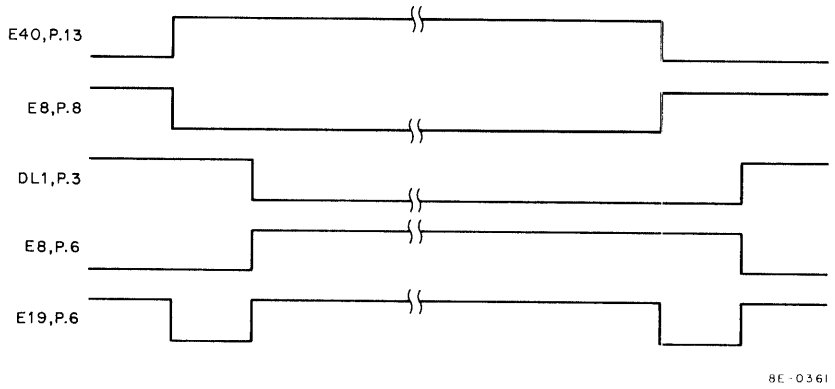


Figure 7-8 Timing, Transition Network

When a change in the READY/ON LINE signal occurs, the output from E19 sets the TRANSITION flip-flop, E7. The 0-output of E7 is one input of NAND gate E35. The other input of E35 is asserted when the RCNI instruction is issued. When E35 is enabled, NAND gate E5C or E5D is enabled, depending on the direction of the READY/ON LINE signal transition. For example, if the READY/ON LINE signal has gone from low to high, E5D asserts the DATA 3 L signal when the RCNI L signal enables E35. Note that the RCNI L signal also enables NAND gate E1. This gate, in turn, can enable gates E5A and/or E5B, depending on the state of the CARD DONE flip-flop and the DATA READY flip-flop. Thus, a signal representing the status of each of the card reader

conditions can be placed on a DATA line by the RCNI instruction. The DATA line information is then gated to the AC Register and loaded at TP3 time. Although the status logic is more sensibly applied in the interrupt mode, it could be used to advantage in the programmed I/O transfer mode, particularly when the DATA READY flip-flop is considered. For example, the program could concern itself with a task, periodically issuing a RCNI instruction, followed by a SMA Operate microinstruction. If the DATA READY flip-flop were set, the AC0 bit would become logic 1 at TP3 time of the RCNI instruction. This is defined as a "minus AC"; thus, a program instruction would be skipped and a subroutine could be entered. This procedure could conceivably be extended to the other three DATA bits (1, 2, and 3) by making use of the rotate microinstructions.

The status logic is more efficient when used in the interrupt mode. The program can be interrupted when one of the card reader conditions becomes true. The RCSI instruction can then direct the program to a card reader routine that checks each bit of the status word with the rotate microinstructions. This method is particularly effective in monitoring the state of the READY/ON LINE signal.

7.6 READ GATING LOGIC

The read gating logic is illustrated in Figures 7-9, 7-10, and 7-11. Each figure shows the logic for one of the three read instructions, RCRA, RCRB, and RCRC.

The simplest form of reading is that which is accomplished by the RCRB instruction, Read Binary. This logic is shown in Figure 7-9. The RCRB L signal gates the Zone Register bits through the 12 NAND gates to the DATA lines; the bit-for-bit correspondence is as indicated. The DATA bits are gated to the AC Register and loaded at TP3 time.

A more complex form of reading is that which is accomplished by the RCRA instruction, Read Alphanumeric. This form of reading converts the code represented by the holes or marks of each card column to a 6-bit alphanumeric code. The alphanumeric code is gated onto DATA lines 6 through 11 by the RCRA L signal (Figure 7-10) and loaded into the AC Register at TP3 time.

The data card can be punched or pencil-marked to represent any code desired by the user. However, the most common code in use, particularly with punched cards, is the Hollerith code. The 47 characters of the Hollerith code can be converted easily to the 6-bit alphanumeric code, thereby minimizing the size of translation tables. Table 7-2 shows the relationship between the Hollerith code and the alphanumeric code carried by the DATA lines. Each character of the topmost group, numerals 1 through 9, is translated into an alphanumeric code as follows: The numeral is represented in BCD code in the four least-significant DATA bits; the two most significant DATA bits are logic 0. The next three groups of characters are translated in a similar manner; the BCD code for numerals 1 through 9 is repeated (the fourth group repeats 2 through 9) in each group, but DATA bits 6 and 7 are changed. The last group is translated with less extensive but still noticeable similarities.

The third form of reading, RCRC (Read Compressed), is accomplished by the logic shown in Figure 7-11. This form of reading is designed to handle a proposed expansion of the Hollerith code. The expanded Hollerith code is converted to a 9-bit compressed code that features a validity-check bit. The 9-bit compressed code is gated onto DATA lines 0 and 4 through 11 by the RCRC L signal and loaded into the AC Register at TP3 time.

Table 7-3 shows the relationship between the Hollerith code (excluding whatever characters may be added as a result of expansion) and the compressed code. Note that DATA bit 0 is always logic 0. This bit is the validity-check bit. Only one of rows 1 through 7 in a card column can contain a hole or mark. If more than one row is punched or marked, an error exists and the DATA 0 bit becomes logic 1. This error condition could be checked by the program, for instance, with a SMA Operate microinstruction.

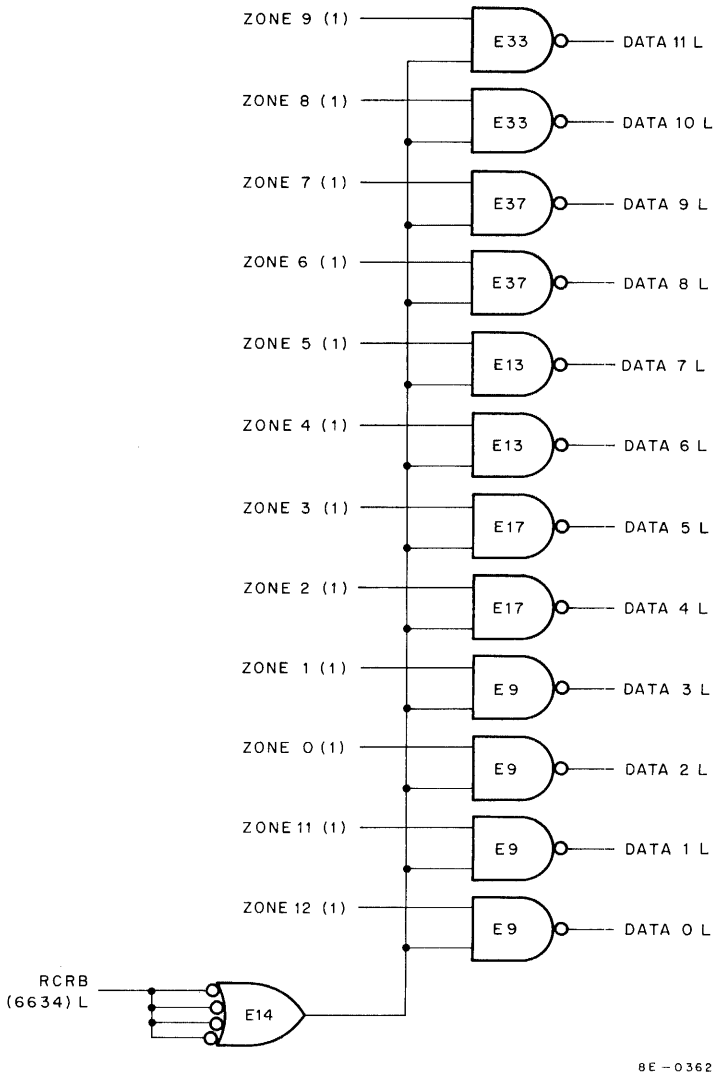


Figure 7-9 Data Gating, RCRB Instruction

DATA bits 4 through 11 represent the Hollerith code characters in compressed code. Each character of the top-most group, numerals 1 through 9, is translated into compressed code as follows: numerals 1 through 8 are represented in BCD code in the four least-significant DATA bits (all other bits are logic 0); numeral 9 is represented by logic 1 in DATA bit 4. The next three groups of characters are translated in a similar manner; the code for numerals 1 through 9 is repeated (the fourth group repeats 2 through 9) in each group, but DATA bits 5, 6, and 7 are changed. The last group is translated with less extensive but still noticeable similarities.

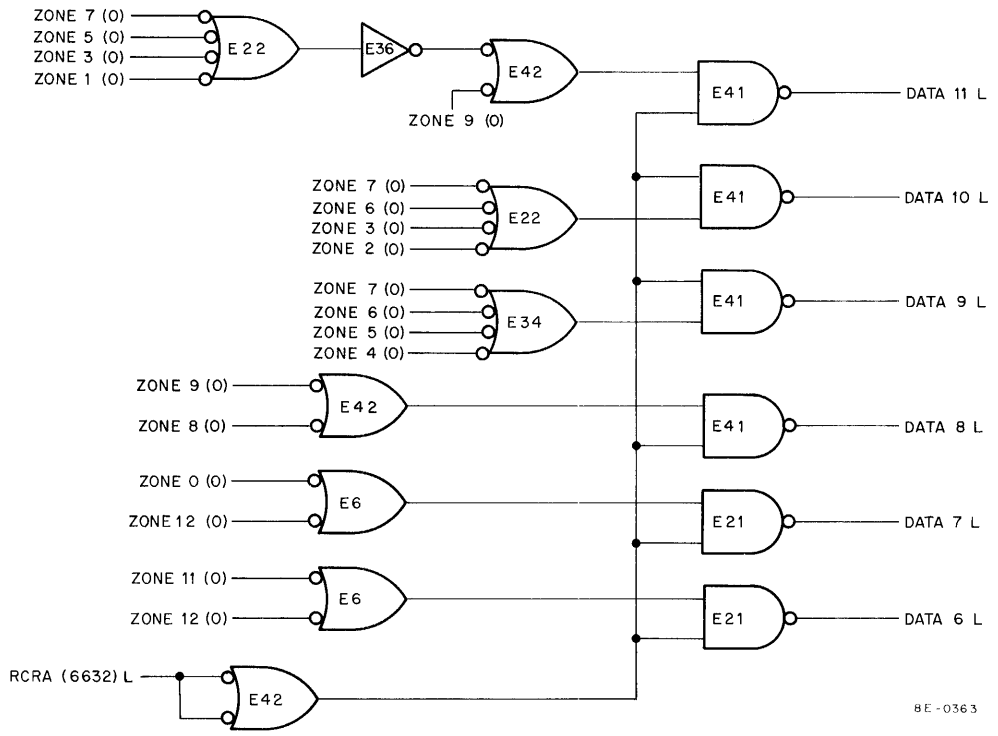


Figure 7-10 Data Gating, RCRA Instruction

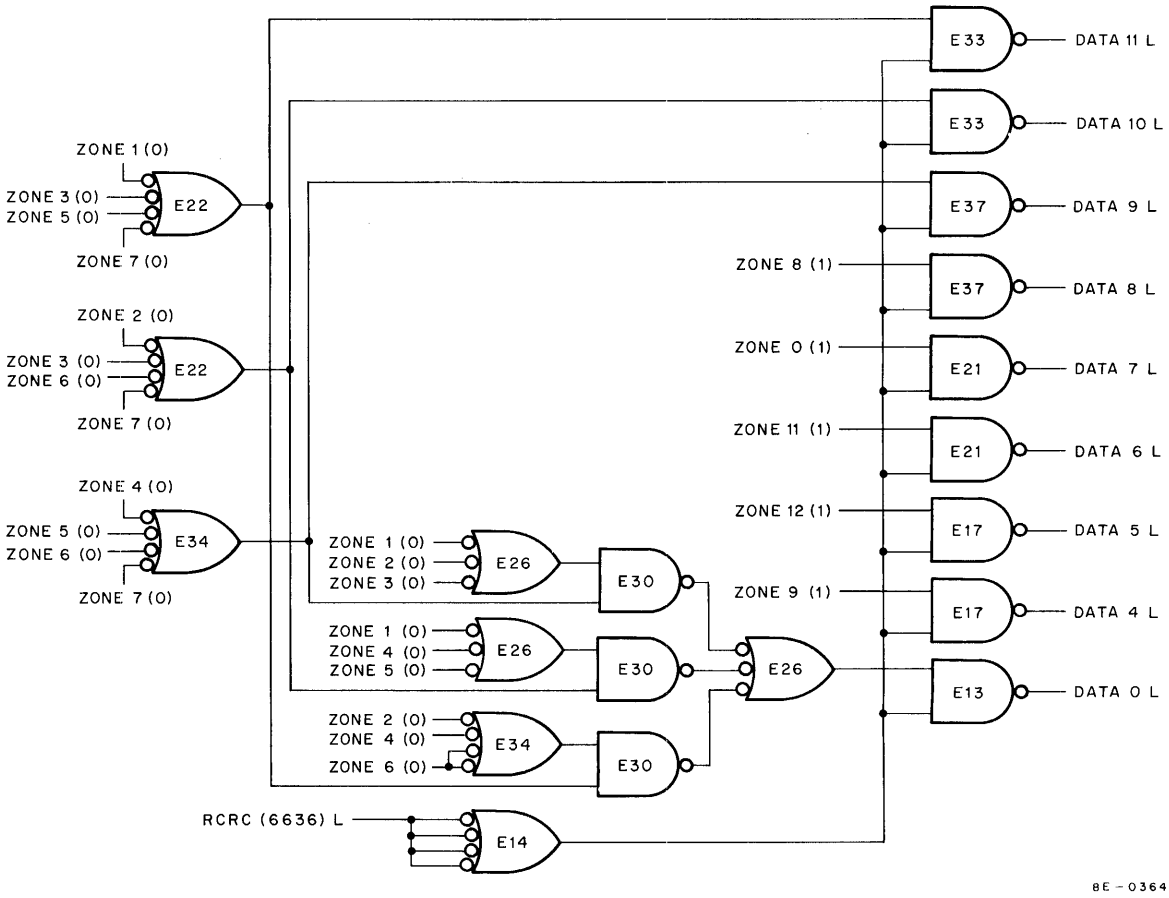


Figure 7-11 Data Gating, RCRC Instruction

Table 7-2
Translation, Hollerith Code – Alphanumeric Code

Character	Hollerith Code (card row punched or marked)	DATA Bit					
		6	7	8	9	10	11
1	1	0	0	0	0	0	1
2	2	0	0	0	0	1	0
3	3	0	0	0	0	1	1
4	4	0	0	0	1	0	0
5	5	0	0	0	1	0	1
6	6	0	0	0	1	1	0
7	7	0	0	0	1	1	1
8	8	0	0	1	0	0	0
9	9	0	0	1	0	0	1
A	12,1	1	1	0	0	0	1
through	through			through			
I	12,9	1	1	1	0	0	1
J	11,1	1	0	0	0	0	1
through	through			through			
R	11,9	1	0	1	0	0	1
S	0,2	0	1	0	0	1	0
through	through			through			
Z	0,9	0	1	1	0	0	1
0	0	0	1	0	0	0	0
/	0,1	0	1	0	0	0	1
=	3,8	0	0	1	0	1	1
,	0,3,8	0	1	1	0	1	1
&	11,3,8	1	0	1	0	1	1
.	12,3,8	1	1	1	0	1	1
	4,8	0	0	1	1	0	0
(	0,4,8	0	1	1	1	0	0
*	11,4,8	1	0	1	1	0	0
)	12,4,8	1	1	1	1	0	0
+	12	1	1	0	0	0	0
-	11	1	0	0	0	0	0

SECTION 5 MAINTENANCE

Refer to Volume 1 and the respective card reader instruction manuals for maintenance information that pertains to both the control and the card readers. The diagnostic program should be used to isolate problems that occur in the system.

Table 7-4 shows the connector pin assignments for the control and the respective card reader.

SECTION 6 SPARE PARTS

Table 7-5 lists recommended spare parts for the CR8-E/CM8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 7-3

Translation, Hollerith Code – Compressed Code

Character	Hollerith Code (card row punched or marked)	DATA Bit								
		0	4	5	6	7	8	9	10	11
1	1	0	0	0	0	0	0	0	0	1
2	2	0	0	0	0	0	0	0	1	0
3	3	0	0	0	0	0	0	0	1	1
4	4	0	0	0	0	0	0	1	0	0
5	5	0	0	0	0	0	0	1	0	1
6	6	0	0	0	0	0	0	1	1	0
7	7	0	0	0	0	0	0	1	1	1
8	8	0	0	0	0	0	1	0	0	0
9	9	0	0	0	0	0	0	0	0	0
A	12,1	0	1	0	0	0	0	0	0	1
through	through	through								
H	12,8	0	0	1	0	0	1	0	0	0
I	12,9	0	1	1	0	0	0	0	0	0
J	11,1	0	0	0	1	0	0	0	0	1
through	through	through								
Q	11,8	0	0	0	1	0	1	0	0	0
R	11,9	0	1	0	1	0	0	0	0	0
S	0,2	0	0	0	0	1	0	0	1	0
through	through	through								
Y	0,8	0	0	0	0	1	1	0	0	0
Z	0,9	0	1	0	0	1	0	0	0	0
0	0	0	0	0	0	1	0	0	0	0
/	0,1	0	0	0	0	1	0	0	0	1
=	3,8	0	0	0	0	0	1	0	1	1
,	0,3,8	0	0	0	0	1	1	0	1	1
&	11,3,8	0	0	0	1	0	1	0	1	1
.	12,3,8	0	0	1	0	0	1	0	1	1
	4,8	0	0	0	0	0	1	1	0	0
(	0,4,8	0	0	0	0	1	1	1	0	0
*	11,4,8	0	0	0	1	0	1	1	0	0
)	12,4,8	0	0	1	0	0	1	1	0	0
+	12	0	0	1	0	0	0	0	0	0
-	11	0	0	0	1	0	0	0	0	0

Table 7-4

Connector Pin Assignments, J1—J5, J1—J2

M843 Module J1 (DEC 1209941)		GDI 100M J5 (AMPHENOL 57-40240)		Documation M200 J2 (ELCO 00-8016-038-000-707)	
Pin	Signal	Pin	Signal	Pin	Signal
J	READY/ON LINE	15	ON LINE X+	BB	RDY (Ready)
L	INDEX MARKER/ DATA STROBE	13	DATA STROBE X+	AA	IM (Index Mark)
N	CIR	23	CARD IN READER X+	MM	BSY (Busy)
R	READ	14	READ COMMAND X+	LL	PC (Pick Command)
BB	ZONE INPUT 12	12	DATA ROW 12 X+	A	D12
V	ZONE INPUT 11	11	DATA ROW 11 X+	B	D11
JJ	ZONE INPUT 0	10	DATA ROW 10 X+	C	D0
T	ZONE INPUT 1	1	DATA ROW 1 X+	D	D1
DD	ZONE INPUT 2	2	DATA ROW 2 X+	K	D2
X	ZONE INPUT 3	3	DATA ROW 3 X+	L	D3
FF	ZONE INPUT 4	4	DATA ROW 4 X+	M	D4
Z	ZONE INPUT 5	5	DATA ROW 5 X+	N	D5
TT	ZONE INPUT 6	6	DATA ROW 6 X+	U	D6
RR	ZONE INPUT 7	7	DATA ROW 7 X+	V	D7
NN	ZONE INPUT 8	8	DATA ROW 8 X+	Y	D8
LL	ZONE INPUT 9	9	DATA ROW 9 X+	Z	D9

Table 7-5

CR8-E/CM8-E Recommended Spare Parts

DEC Part Number	Description	Quantity
19-9971	IC DEC 6380	1
19-9705	IC DEC 8881	1
19-9704	IC DEC 314	1
19-9373	IC DEC 9601	1
19-9686	IC DEC 7404	1
19-9594	IC DEC 8251	1
19-9050	IC DEC 7475	1
19-9004	IC DEC 7402	1
19-5580	IC DEC 7450	1
19-5579	IC DEC 7440	1
19-5577	IC DEC 7420	1
19-5576	IC DEC 7410	1
19-5575	IC DEC 7400	1
19-5547	IC DEC 7474	1

(continued on next page)

Table 7-5 (Cont)
CR8-E/CM8-E Recommended Spare Parts

DEC Part Number	Description	Quantity
16-5528	Delay Line, 30 ns	1
10-0025	Capacitor, 560 pF, 100V, 5% DM	1
10-0016	Capacitor, 100 pF, 100V, 5% DM	1
10-0067	Capacitor, 6.8 μF, 35V, 20% S. TANT.	1
10-1610	Capacitor, 0.01 μF, 100V, 20% DISK	1
70-7252	Cable, Card Reader Interface	1

PART 7
MAGNETIC TAPE

CHAPTER 8
TD8-E DECTAPE CONTROL

SECTION 1 INTRODUCTION

The TD8-E Simple DECtape Control is used to control a TU56M or TU56MH Tape Drive Unit (Figure 8-1). The TD8-E controls the assembly and disassembly of data to be read from or written onto the DECtape and provides control signals to the drive unit. The TD8-E logic is on one quad board, Module M868, that is inserted into the PDP-8/E OMNIBUS and connected to a single or dual TU56M Tape Drive by a 7008447 cable.

The TD8-E controls the direction and motion of the tape drive unit with signals generated by flip-flops in the Command Register. The Command Register allows the TD8-E to select even or odd tape drive, start and stop, move forward or reverse, and read or write by changing the state of four flip-flops. These flip-flops are controlled by an instruction (SDLC) that loads the Command Register with four bits of data from the AC.

The assembly and disassembly of the 12 data bits takes place in the Data Register. The Data Register contains the gating and register necessary to receive data from and place data on the OMNIBUS. The Data Register takes serial data from the tape during a read operation and puts serial data on the tape during a write operation.*

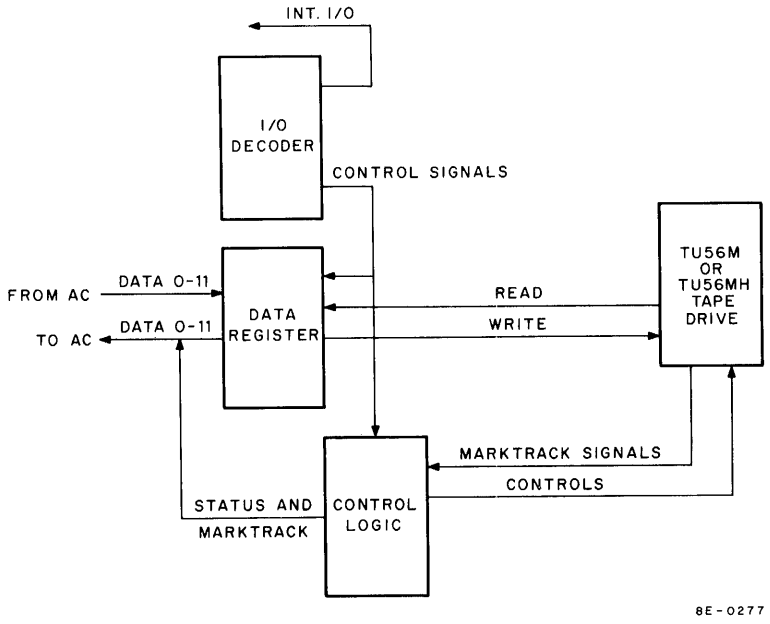


Figure 8-1 TD8-E Block Diagram

*See the *PDP-8/E & PDP-8/M Small Computer Handbook,* page 7-161, for more detailed information on DECtape formatting.

SECTION 2 INSTALLATION

The TD8-E is installed on site by DEC Field Service personnel. The customer should not attempt to unpack, inspect, install, checkout, or service the equipment until a Field Service representative is present.

8.1 INSTALLATION

Perform the following to install the TD8-E System.

Step	Procedure
1	Ensure power is off.
2	Ensure jumpers are installed on the M868 to select the correct I/O code for this TD8-E System (see Table 8-3 for a list of device code jumpers to be installed and unit numbers).
3	Insert the M868 Module into the OMNIBUS (see Volume 1 for module priority).
4	Ensure that the jumpers are installed on the M960 Module (Table 8-2).
5	Connect the 7008447 cable. P3 goes to J1 on the M868 Module and P1 to location A6 or A7 and P2 to location AB10 or AB11 in the TU56M (Table 8-1).
6	Ensure that the G742 Module has been installed in place of the M531 and the G888s are installed in the TU56M Drive Unit.
7	Ensure that the power is wired according to power wiring print TD8-E-3 for the configuration used.

8.2 ACCEPTANCE TEST

Perform the following to check the TD8-E System.

Step	Procedure
1	Run the Formatter Program (DEC-8E-EUZC-D) on each drive. Follow instructions in the formatter document. If testing a TU56M (Dual Drive) swap the formatted tapes from one drive to the other to run the diagnostic test. **NOTE** **The Formatter will run only on TD8-Es with device code 677X (only on units 0 and 1).**
2	Run the Diagnostic Programs (MAINDEC-08-DHTDA). Refer to the diagnostic document for instructions necessary to run the diagnostic.

8.3 TD8-E INTERFACE

A 7008447 cable is used to interface with the TU56M Tape Transport (Table 8-1). M960 and M961 Connector Modules are used to connect to the TU56M. The M960 Module is used as connector P1 and the M961 Module as connector P2. The M960 Module has unit selection jumpers that must be installed to select the correct unit. Jumpers are installed between split lugs as indicated in Table 8-2 to select the proper unit code for the unit.

Table 8-1

TD8-E Signal Interface

J1 (P3) on TD8-E	Wire Color	Logic on M960 or M961	M960 Module Pin No.	M961 Module Pin No.	Description
NN	Black		M1		Time Mark Enable
MM	Brown		C2		Ground
TT	Red		E1		Reverse
			H1		Forward
SS	Orange		C2		Ground
JJ	Yellow		B1		Stop
			D1		Go
HH	Green		C2		Ground
RR	Blue		J1		Con All Halt
PP	Violet		C2		Ground
LL	Gray	0	V2		Unit 0
		1	E2		Unit 1
		2	H2		Unit 2
		3	K2		Unit 3
		4	M2		Unit 4
		5	P2		Unit 5
		6	S2		Unit 6
		7	T2		Unit 7
KK	White		C2		Ground
N	Black		P1		Select Echo
M	Brown		C2		Ground
T	Red		S1		Write Echo
S	Orange		C2		Ground
AA	Black		C2		Ground
BB	Brown			AA1	Write Time Track Pulses
				AB1	Write Time Track Pulses
EE	Red			AC2	Ground
FF	Orange			AC1	Word 0
				AD1	
H	Yellow			AC2	Ground
J	Green			AK1	Read Time Track
E	Blue			AC2	Ground
F	Violet			AM1	Read Mark Track
W	Gray			AC2	Ground
X	White			AR1	Word 2
				AS1	Word 2
CC	Black			AC2	Ground
DD	Brown			AT1	Word 1
				AV1	Word 1
Y	Red			AC2	Ground
Z	Orange			BA1	Word Enable
K	Yellow			AC2	Ground
L	Green			BB1	Read 1
C	Blue			AC2	Ground
D	Violet			BE1	Read 0
U	Gray			AC2	Ground
V	White			BK1	Read 2

Table 8-2
M960 Module Jumpers

Octal Code	Unit Numbers	Install Select Jumpers
677X	0 and 1	0 and 1
676X	2 and 3	2 and 3
675X	4 and 5	4 and 5
674X	6 and 7	6 and 7

SECTION 3 FUNCTIONAL DESCRIPTION

The TD8-E M868 Quad Module is inserted into the OMNIBUS and used to control either the TU56M or TU56MH Tape Drives. The PDP-8/E System can have as many as four TD8-E Modules on the OMNIBUS to control a maximum of 8 tape units (4 dual drive). For each TD8-E System purchased, the user also receives one H716 Power Supply to supply +5 Vdc and -15 Vdc to the TU56M DECtape. The TU56MH (tabletop model) does not receive the H716 Power Supply.

8.4 INSTRUCTION AND STATUS BITS

The TD8-E uses the following instructions:

Simple DECtape Skip on Single Line Flag (SDSS)
Octal Code: 67X1
Operation: Skip if Single Line flag is set.

Simple DECtape Skip on Time Error (SDST)
Octal Code: 67X2
Operation: Skip if Time Error flag is set.

Simple DECtape Skip on Quad Line Flag (SDSQ)
Octal Code: 67X3
Operation: Skip if Quad Line flag is set.

Simple DECtape Load Command Register (SDLC)
Octal Code: 67X4
Operation: Load Command Register from the AC, clear Time Error, and start UTS Delay if UNIT, DIRECTION or STOP/GO flip-flops are changed.

Simple DECtape Load Data Register (SDLD)
Octal Code: 67X5
Operation: Load Data Register from the AC, do not clear the AC, and clear Single Line and Quad Line flags.

Simple DECtape Read Command Register (SDRC)
Octal Code: 67X6
Operation: Load contents of Command Register, Mark Track Register, and Status bits into the AC. Clear Single Line and Quad Line flags.

Simple DECtape Read Data Register (SDRD)
Octal Code: 67X7
Operation: Load contents of Data Register into the AC, and clear Single Line and Quad Line Flags.

The X in the octal code of the instruction indicates one of four different I/O codes used so that four TD8-E modules can be used on the PDP-8/E OMNIBUS. The I/O codes used are 677X, 676X, 675X, and 674X. The first two TD8-Es ordered will have I/O codes 677X and 676X, respectively. If three or four TD8-Es are ordered, they will have codes 675X and 674X, respectively. The jumpers to be installed to select the correct device code and the unit number to select the correct unit on the TU56M are shown in Table 8-3.

Table 8-3
Device Code Jumpers

Octal Code	Install Select Jumpers	Unit Numbers
677X	W2 and W4	0 or 1
676X	W2 and W3	2 or 3
675X	W1 and W4	4 or 5
674X	W1 and W3	6 or 7

8.5 FUNCTIONAL OPERATION

Figure 8-2 is a functional block diagram of the TD8-E Simple DECtape Control. For discussion purposes the TD8-E is broken into functional groups of logic. Section 4 contains a detailed discussion of each logic group.

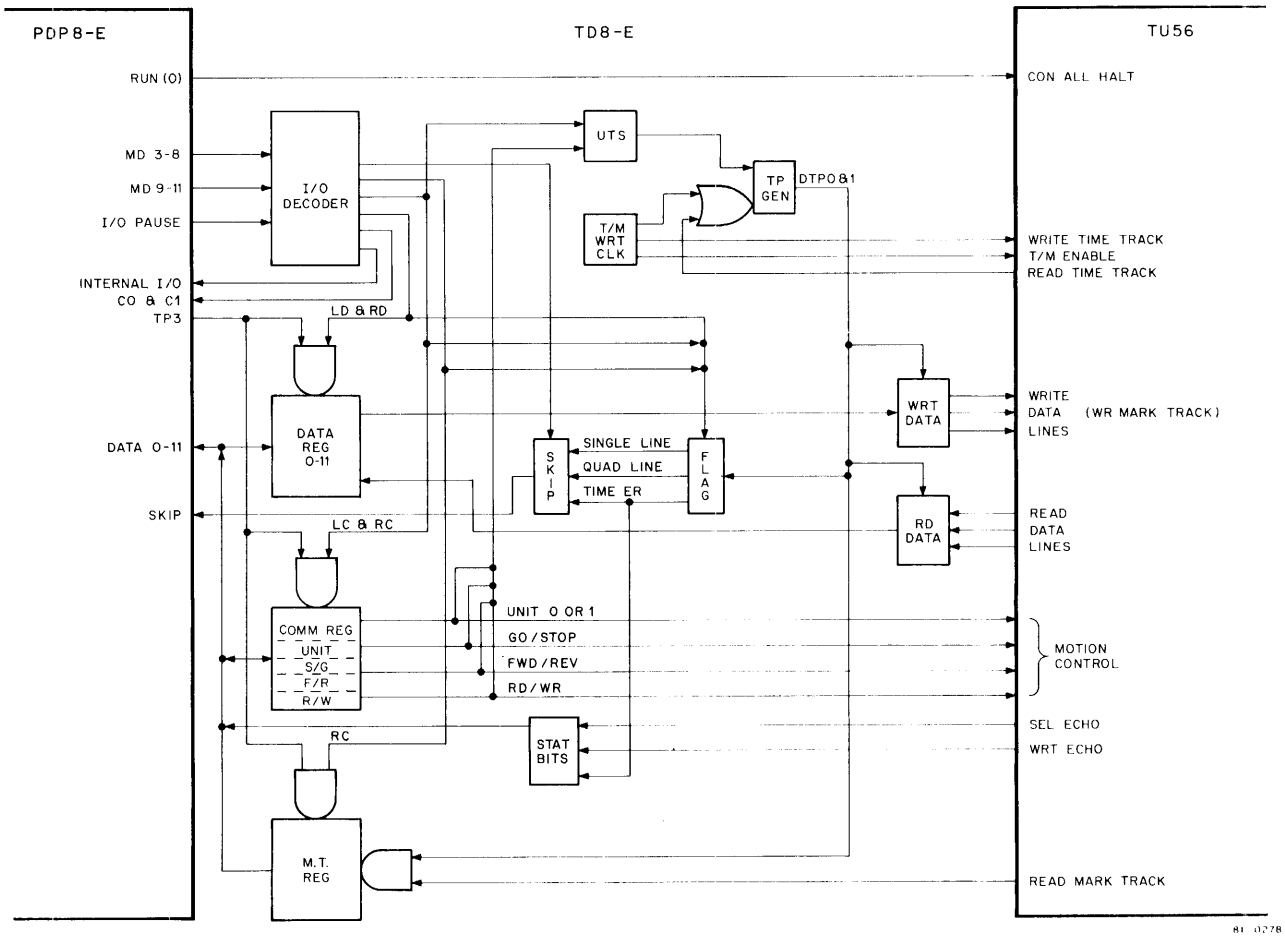


Figure 8-2 TD8-E Functional Block Diagram

8.5.1 I/O Decoder

As stated before, there are four sets of I/O codes that determine which of four possible TD8-Es is being addressed. The decoding is done by two jumpers connected to MD7 and MD8. When the correct code for the TD8-E goes to the I/O decoder and an I/O PAUSE is present an INTERNAL I/O is generated to allow decoding of bits MD 9–11 and generate an INTERNAL I/O L. The INTERNAL I/O L will prevent the positive I/O bus interface from generating IOTs while this operation is under way and will generate an enable signal (CC67X) to allow bits MD 9–11 to be decoded. MD 9–11 are decoded and control the transfer of data and commands to the Data Register, Command Register, and Mark Track Register. TP3 is used as a timing signal throughout the control logic. C0 and C1 determine the direction of data flow to and from the AC, and determine if the AC is cleared or not.

8.5.2 Command Register

The Command Register is made up of four flip-flops which are loaded from the DATA BUS by the SDLC instruction. 1s set the flip-flop and 0s clear it.

UNIT — Selects which drive on the TU56M is to be used. If UNIT is cleared, Unit 0 is selected.

F/R — Determines which direction the tape is to move. If F/R is cleared, direction is Forward (CW).

CAUTION

Because of circuit delays in the TU56M, the SDLC instruction to simultaneously change the F/R flip-flop and the S/G flip-flop should not be executed. If this instruction is executed, the brake signal in the TU56M will be applied to the wrong motor, causing the tape drive to drift much further down the tape (in the direction it was going) than it normally would if the brake were applied to stop tape movement.

S/G — Tells the selected unit to move tape or stop. If S/G is cleared, the selected tape will stop. The GO signal is delayed 200 ns after an SDLC instruction to ensure that the unit select line has had time to switch in the Tape Drive Unit before the tape starts to move.

R/W — Instructs the selected unit to read or write data. If R/W is cleared, a read operation will take place; if it is set, a write operation is executed.

The SDLC instruction also starts the UP TO SPEED (UTS) delay time and clears the TIME ERROR flip-flop. Figure 8-3 shows the format of data loaded into the Command Register when the SDLC instruction is executed.

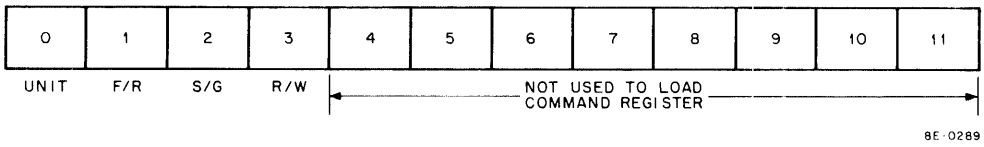


Figure 8-3 Format of Data Loaded into the Command Register

Any time an instruction is executed to change the Command Register, except when the R/W flip-flop is changed, it starts a new delay timeout of 120 ms; at the end of this time, the UTS will set again. UTS will not set when the S/G flip-flop is cleared.

The R/W flip-flop is cleared (set to a read condition) by any of the following:

a. SEL ERR
b. TIME ERROR
c. WRITE LOCKOUT
d. POWER NOT OK
e. INITIALIZE (Clears all logic)

8.5.3 Data Register

The Data Register contains the gating and register necessary to take data from the OMNIBUS and put data in the OMNIBUS. It also receives data from the tape during a read operation and places data on the tape during a write operation.

8.5.4 Mark Track Register

After UTS is set, the Mark Track (MT) Register constantly reads data from the mark track. The mark track data is read bit by bit, and tested by a Single Line Flag (SLF). Each time SLF is set, a new bit has been shifted into the MT Register. All decoding of mark track data must be done by the program.

The MT Register is cleared by the start of a UTS delay to ensure that no erroneous codes are left in from a previous operation. The program must be delayed at least six Single Line flags after UTS has timed out to ensure at least one complete mark track code has been shifted into the Mark Track Register. This delay ensures a valid code has been shifted into the register.

The contents of the MT Register are transferred to the AC using an SDRC instruction which also transfers the STATUS bits and the contents of Command Register at the same time. Figure 8-4 shows the format of the word used for this transfer.

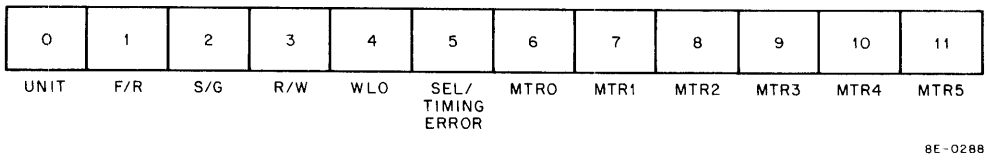


Figure 8-4 Format of Word Transferred to AC

8.5.5 Flags and Status Bits

The Single Line flag is set each time the DECtape reads one line of tape and is used to detect codes on the Mark Track as discussed in Paragraph 8.5.4. The Single Line flag is cleared by a not-up-to-speed condition and when an SDLD, SDRC, or SDRD instruction is executed.

A Quad Line flag is set once for each four lines of data read from the tape. Testing the Quad Line flag allows the program to read or write a full 12-bit word. The Quad Line flag is cleared by NOT UTS or by SDLD, SDRC, or SDRD instructions.

TIME ERROR is an indication that the program did not go back to the control in time to work on the Data Register before the next transfer of the DECtape took place or that the program was executing an SDLD, SDRD, or SDRC instruction when the DECtape requested another transfer. If the control has been writing data, TIME ERROR clears the R/W flip-flop to ensure that erroneous data is not written on the tape. TIME ERROR is ORed with SEL ERR and put onto the OMNIBUS during an SDRC instruction (Figure 8-4).

SEL ERR is sent to the TD8-E by the TU56M to indicate that no unit has been selected or more than one unit has been selected. SEL ERR has no effect on the TD8-E logic, but is transferred from the Command Register to allow the program to make decisions on what to do about the error.

WRITE LOCKOUT is sent to the TD8-E by the TU56M to indicate that the unit selected for writing was not write enabled. WRITE LOCKOUT clears the R/W flip-flop and has a status bit for transfer to the AC during an SDRC instruction (Figure 8-4).

8.5.6 Time Pulse Generator

The Time Pulse Generator and its logic reads a signal from the time track and produces full- and half-cycle pulses on the rising and falling edges of the time track signal. These pulses are required to read data from and write on the tape.

The time pulses are gated with and synchronized by the UTS flip-flop so that pulses will be produced when the tape is up to speed. There is a discriminating delay in the Time Pulse Generator to ensure that noise crosstalk picked up by the time track head during write operation is not converted into extra time pulses.

The Time Generator has a clock to produce the time pulses required to write the time and mark tracks. The time track is written directly from a complementing flip-flop in the Time Generator, and the mark track is written from DATA bit 0. The read time track line is gated off while writing the time and mark tracks to ensure that noise coming off the time track does not generate unwanted pulses.

8.6 TD8-E TIMING

The TD8-E timing discussed in this section does not indicate the correct way or the only way to program the TD8-E. The information presented here is meant only to show the interaction between groups of logic when various instructions are executed.

8.6.1 Timing for Writing Time and Mark Tracks

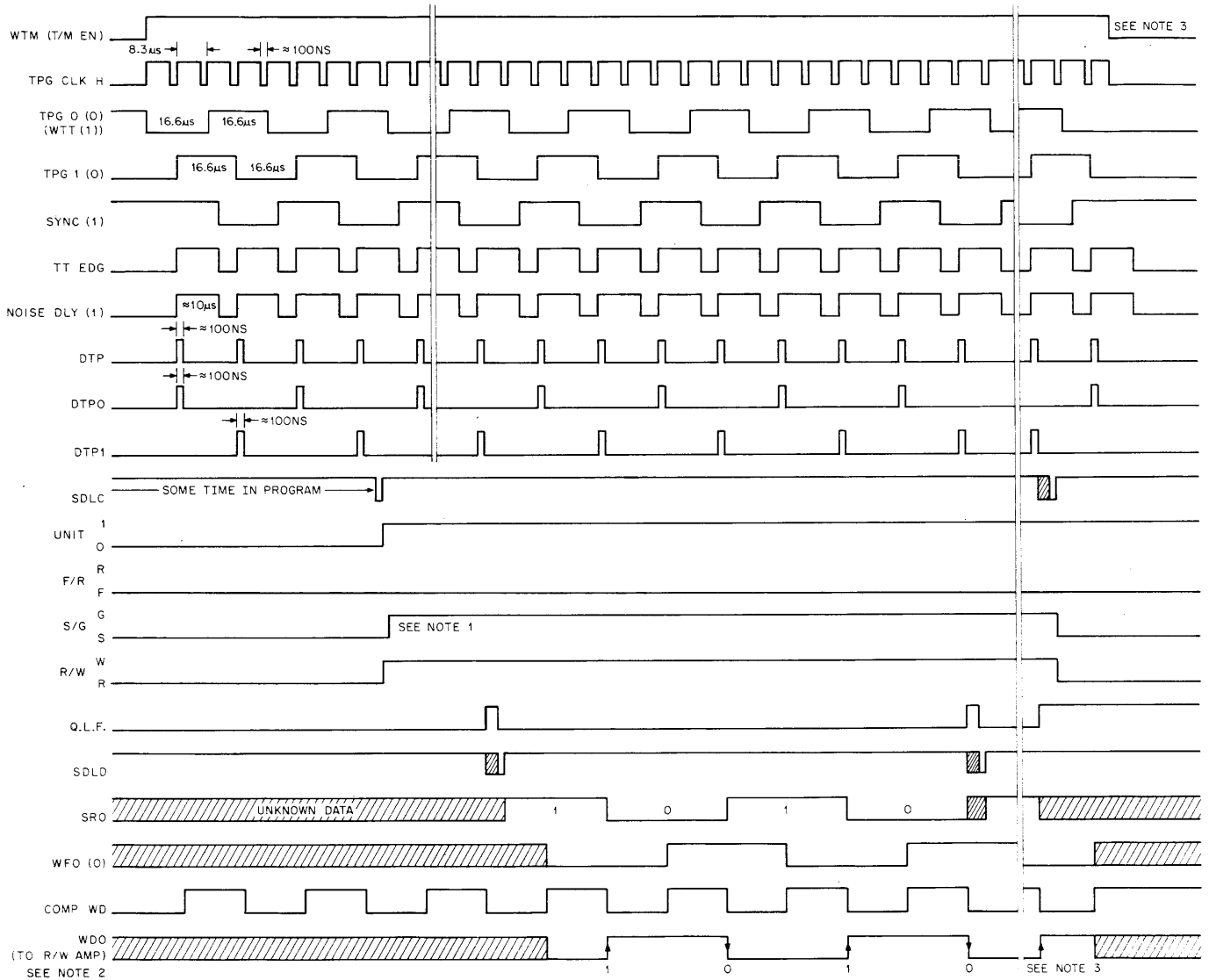
The time and mark tracks are written to format the DECtape for writing and reading data. Data to be written on the mark track is transferred from the AC to the DATA BUS in bit positions 00, 03, 06, and 09 (see the *PDP-8/E & PDP-8/M Small Computer Handbook* for the format of data on the tape). Figure 8-5 is a timing diagram for writing the mark and time tracks (formatting). Note that the T/M Enable switch, S1, must be set to WTM to enable writing the time and mark tracks (Table 8-4 for signal functions). DEC-8E-EUZC-D gives instructions for formatting DECtapes and the DEC-8E-EUZC-PD Tape Formatter should be used to format all tapes.

8.6.2 Write Data Timing

The timing diagram in Figure 8-6 shows the timing necessary to write data on the DECtape using the TD8-E. The data to be written is transferred to the TD8-E from the AC and written on the tape in four 3-bit bytes in the tape block determined by the programmed instructions. Note that the RTT time pulses must be written on tape using the Formatter prior to writing data.

8.6.3 Read Data Timing

Figure 8-7 shows the timing required to read data and the mark track from the TU56M DECtape (see Table 8-4 for signal functions).



NOTES

1. The GO signal is switched on by computer TP4 to allow setting of the Unit Select Lines.
2. During formatting the Mark Track is written from the Bit 0 Line.
3. At this time the last of the End Zone Codes has been written. The program stops the tape and the WTM switch is set to OFF.

Figure 8-5 Timing for Writing Mark and Time Tracks

Table 8-4
TD8-E Signals and Signal Functions

Signal	Function
CON ALL HALT	Signal sent to the TU56M to stop the tape drive if the computer program stops. The loss of the RUN signal from the processor will cause the TU56 to stop. CON ALL HLT stops an unselected drive that might be moving tape, clears the S/G command flip-flop to stop the selected drive, and clears the R/W command flip-flop to keep from writing while the drive comes to a stop.
F/R	F/R (Forward/Reverse) will control the direction of tape rotation. If F/R and S/G in the Command Register are set, the tape moves in reverse (CCW); if F/R is cleared and S/G is set, the tape will move forward (CW).
INITIALIZE	Signal generated by Clear key, Power Up, and CAF instruction used to clear all flags and control registers.
RD0 RD1 RD2	Four bits of serial data are taken from the three parallel tracks and assembled in the Data Register as a 12-bit word. The word is then transferred as 12 parallel bits to the DATA BUS as indicated below: RD0 Data, 00, 03, 06, 09 RD1 Data, 01, 04, 07, 10 RD2 Data, 02, 05, 08, 11
RMT	Read Mark Track is 6-bits of serial data from the mark track of the tape. The mark track codes and their functions are as follows (Figure 8-8): **Code** — **Name** — **Function** 55 REVERSE END ZONE MARK — This code identifies the code for end zone located at the beginning of the tape. When moving in the reverse direction, this code will be read as 22 meaning the end of tape is near and the program should HALT or change the direction of tape movement. 25 INTER BLOCK SYNC — Code 25 is another NO-OP code which lies between blocks and for several feet in the inside of the end zone. This code allows for turnaround time when reading the first and last block; it is used by the program to synchronize its timing logic between blocks. 26 FORWARD BLOCK MARK — The number assigned the block by the Formatter is stored on this cell. When the computer is searching for a block, it transfers this number into the AC and examines it. When code 26 is decoded by the program, it knows that the block number is in the Data Register and ready to be read into the AC and compared with the block wanted.

Table 8-4 (Cont)
TD8-E Signals and Signal Functions

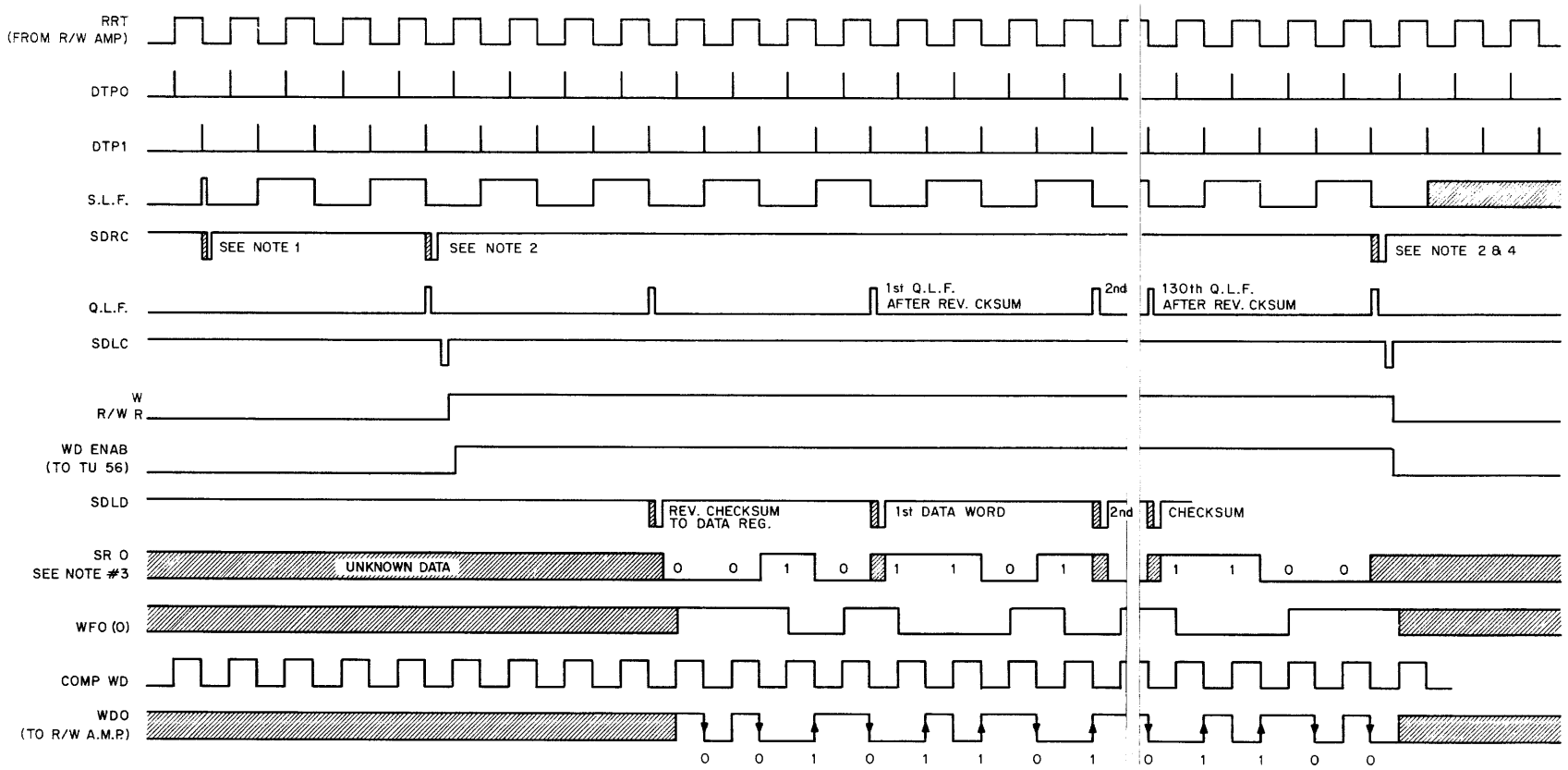
Signal	Function		
RMT (Cont)			
	Code	**Name**	**Function**
	32 10	REVERSE GUARD MARK LOCK MARK	These two cells are NO-OP conditions which give the program time to decide what to do with the block it has identified.
	10	REVERSE PCC MARK	This is the last cell before a data cell. It is used to initiate the parity checksum routine. If the computer is writing, the first 12-bit word to be written is transferred to the controller during this cell and every four lines thereafter.
	10 10	REVERSE FINAL MARK REVERSE PREFINAL MARK	These two codes indicate the first and second data words, respectively; otherwise, they have no special significance.
	70	DATA MARK	This code simply indicates that a data word is written on the data tracks. The program continuously checks to see that the mark track is coded.
	73 73	PREFINAL MARK FINAL MARK	These codes indicate that the last two words of data are being transferred.
	73	PCC MARK	The parity checksum which was being calculated by the program during the transfer is either written here during a write operation or compared by the program during a read operation.
	73 51	REVERSE LOCK MARK GUARD MARK	These are NO-OP spaces which become useful when the tape is traveling in the reverse direction.
	45	REVERSE BLOCK NUMBER	The block number is stored here to be picked up by the program when the tape is traveling in the reverse direction.
	25	INTER BLOCK SYNC	Has the same function as INTER BLOCK SYNC at the beginning of the tape.
	22	END ZONE MARK	When this code comes up, the program knows that it has just run out of tape (refer to REVERSE END ZONE) and that it had better do something about it. Note that this code is the complement of 55, the REVERSE END ZONE MARK.

Table 8-4 (Cont)
TD8-E Signals and Signal Functions

Signal	Function
RTT	Read Time Track is a 16.6-μs square wave signal coming from the time track. Pulses produced on the rising and falling edges of the time track signal are used to sync the TD8-E to read and write data.
SEL ERR	Select Error indicates no unit has been selected or that both units have been selected simultaneously. The software must decide what to do about the error.
SEL ECHO	Select Echo is sent to the TD8-E by the TU56M in response to command signals to indicate TU56M is on line.
S/G	Stop/Go is sent to the TU56 by the TD8-E to command the tape drive to move in the direction determined by F/R. This signal is generated by the S/G flip-flop in the Command Register.
TIME ERROR	Time Error is an indication that the program did not come back to the control in time to work on the Data Register before the next transfer occurred.
T/M ENABLE	Time Mark Enable allows tape to be formatted by writing on the time and mark tracks when S1 on the M868 Module is set to WTM.
WD0 WD1 WD2	Twelve bits of parallel data transferred from the DATA BUS to the Data Register and disassembled by the Data Register to form four 3-bit bytes of serial data. The four bytes of serial data are written by these three signals on parallel tracks on the DECtape as indicated below. WD0 Data, 00, 03, 06, 09 WD1 Data, 01, 04, 07, 10 WD2 Data, 02, 05, 08, 11
WTT	Write Time Track is a 16.6-μs square wave signal written on the time track when the tape is formatted.
WRITE LOCKOUT	Write Lockout is sent to the TD8-E by the TU56M to indicate that the unit to be written on is not write enabled. This signal will clear R/W in the Command Register and select the Read mode.
WD ENABLE	Word Enable is generated when R/W on the Command Register is set and UTS is set to allow writing data on tape.
UTS	Up To Speed is negated by any change in the Command Register except R/W. After a delay of 120 ms to allow tape to come up to speed, UTS is again asserted to allow reading or writing data. UTS is used to enable RTT or WTT time pulses.
TPG0 TPG1	Time pulses from the Time Pulses Generator which are produced by the rising and falling edges of the RTT signal (WTT signal while formatting).
QLF	The Quad Line flag is set each time four lines of data are transferred to or from the tape, so that by testing this line the program will know when a full 12-bit word has been read or written. QLF is cleared by NOT UTS, instructions SDLD, SDRC, SDRD or INITIALIZE.

Table 8-4 (Cont)
TD8-E Signals and Signal Functions

Signal	Function
SLF	The Single Line flag is set each time the DECtape transfers one line of data and is used to detect mark track codes. SLF is cleared by NOT UTS, instructions SDLD, SDRC, SDRD or INITIALIZE. SLF is ignored while reading or writing data.
NOISE DLY	Noise Delay is a 10-μs delay generated by the Time Pulse Generator to prevent the noise picked up by the time track head during a write operation from generating extra time pulses.
SYNC	The SYNC is used to generate and separate the TP0 and TP1 pulses required to read or write.

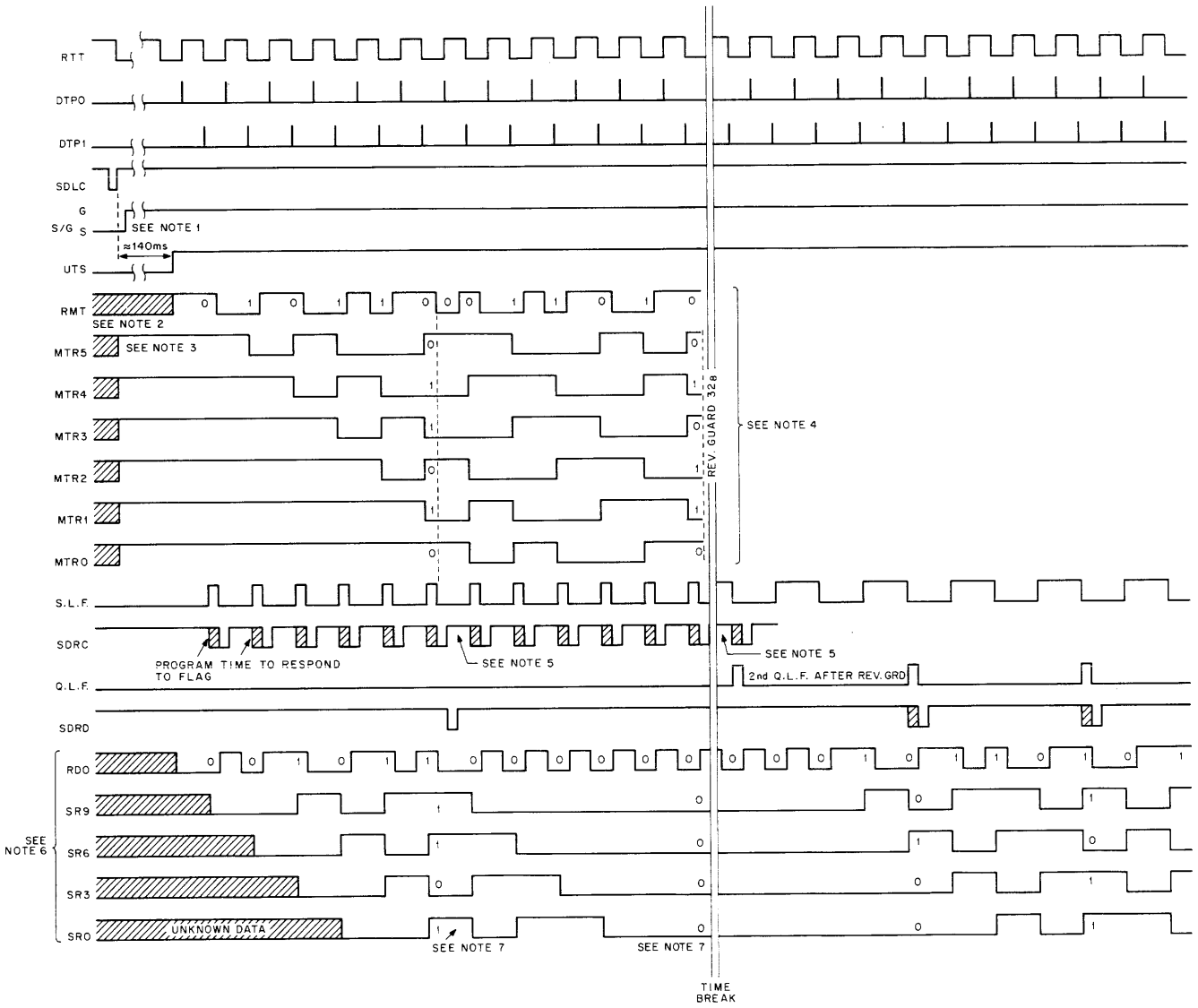


NOTES

1. At this point the COMMAND REGISTER is set for the correct UNIT, FWD, REV, GO, and READ. The correct block number has been found and at this SLF the REV ERSE GUARD is in the MT register.
2. This SDRC loads the status of the COM REG into the AC so that the write bit can be out, in, or removed without changing any other COM REG condition. This also clears the QLF which the SDLC does not.
3. The other two parallel write bits work identically to SR0, WF0, and WD0.
4. At this point if any COM REG function other than R/W is changed, UTS disappears and the TIME pulses stop until UTS DELAY times out and UTS is set.

8E-0342

Figure 8-6 Write Data Timing



NOTES

1. The GO signal is switched on by computer TP4 to allow settling time for the UNIT select lines. The UNIT, DIRECTION, and READ commands are set by this SDLC
2. The inputs to and outputs from the Mark Track Reg are redefined. A 1 is a low level
3. Any time the UTS delay is started, the MTR is set to all 0s (high output)
4. Once the correct block and it's REVERSE GUARD codes have been found, the Single Line Flag is ignored. The MTR is not looked at again until another search is started
5. At this point the complete Mark Track code is in the AC. If it is a Block Mark, an SDRD is issued to read the Block Number so that the program can test for the correct Block Number
6. The other two parallel Read lines work identically to RD0, SR9, SR6, SR3, and SR0
7. The first two bits of the Block Mark are lost because the Block Numbers is on the last four bits of the Block Mark. The Reverse Guard bits 2 data are the forward direction)

Figure 8-7 Read Data and Mark Track Timing

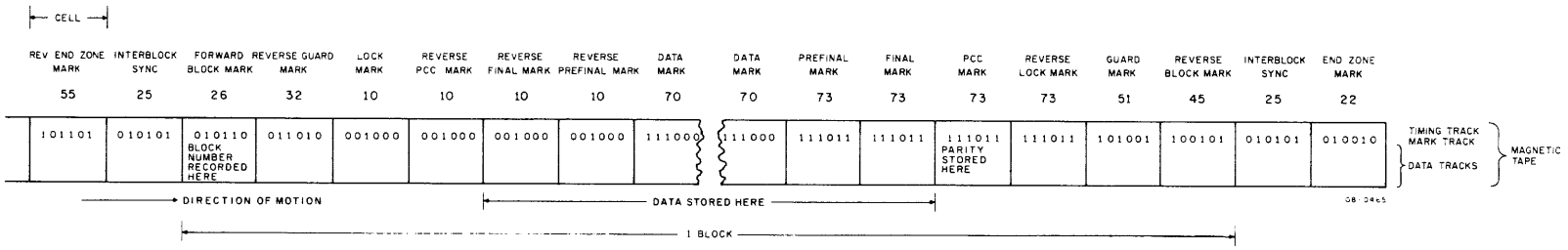


Figure 8-8 DECtape Data Format

SECTION 4 DETAILED LOGIC

The logic in the TD8-E will be broken into functional groups for discussion purposes. The block diagram, Figure 8-2, should be used to understand the interaction of the logic, the signal flow within the module, and the input or output signals.

8.7 INPUT/OUTPUT DECODER LOGIC

The I/O decoder decodes instructions from the Memory Data Bus and generates signals to control the operation of the TD8-E (Figure 8-9). Bits MD 3–11 are gated by the I/O PAUSE when an I/O instruction is generated. Bits MD 3 to MD 8 generate a signal CC67XH applying bits MD 9, MD 10, and MD 11 to the 8251 IC. The 8251 IC is a BCD-to-Decimal decoder (see Volume 1, Appendix A, for truth table logic and pin locations) which decodes MD 9–11 and produces a low on one output line. The low out of the 8251 IC indicates which instruction is to be executed. As an example MD 9 Low, MD 10 and MD11 High (100) produces a low on pin 4 which indicates an SDLC instruction was programmed. The jumpers for MD 7 and MD 8 will select the device code (see Table 8-3 for device codes) for multiple TD8-E Systems.

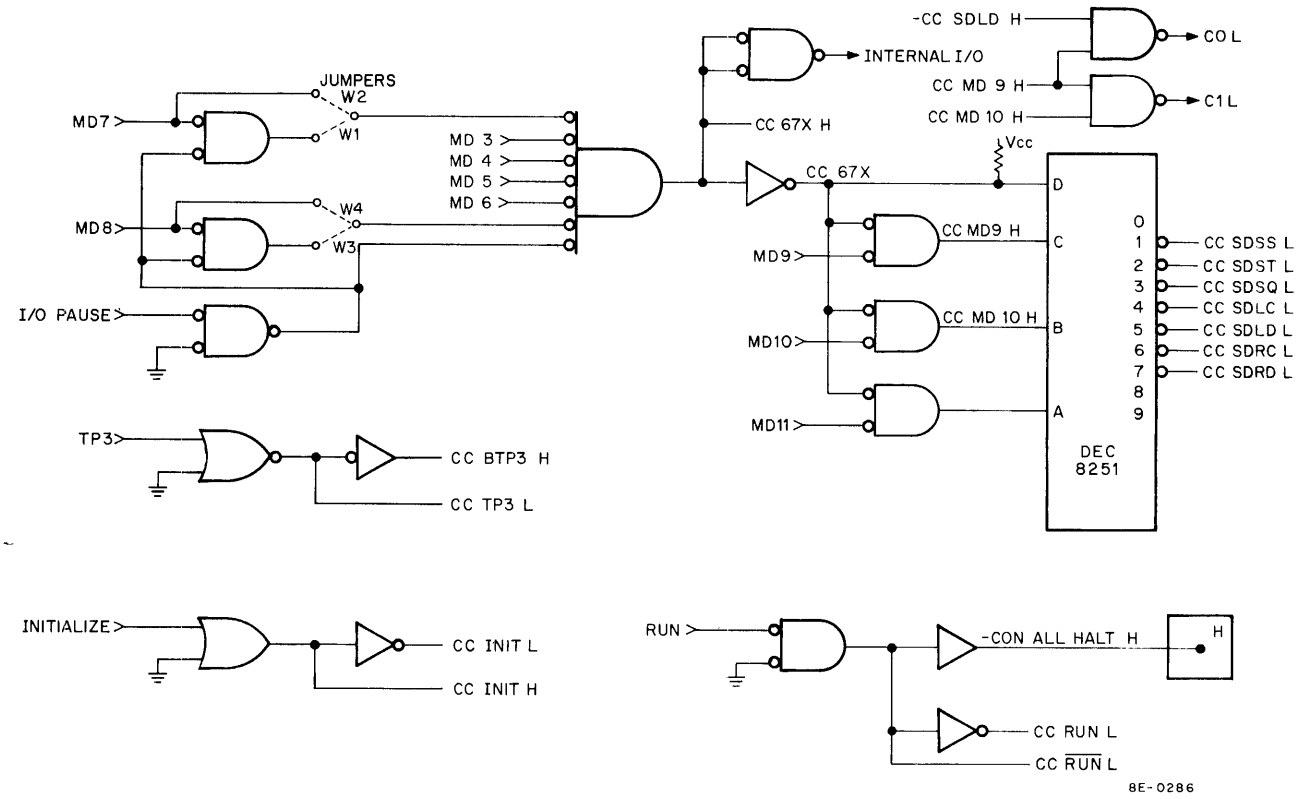


Figure 8-9 I/O Decoder Detailed Logic

8.7.1 Control Logic

8.7.1.1 C Line Select Logic – The C line logic (Figure 8-9) controls the direction of data flow between the DATA BUS and the AC and determines if the AC is clear or not. Table 8-5 shows the status of C0 and C1 to transfer data between the AC and the DATA BUS using the SDLC, SDLD, SDRC, and SDRD instructions.

Table 8-5
C-Line Select Levels and Transfer Operations

Instruction	C0	C1	Transfer Operation
SDLC	Low	High	AC → Data Bus then 0 → AC
SDLD	High	High	AC → Data Bus
SDRC	Low	Low	Data Bus → AC
SDRD	Low	Low	Data Bus → AC

8.7.1.2 Time Pulse 3 Logic – TP3 shown in Figure 8-9 is used throughout the module to enable gates for execution of instructions.

8.7.1.3 Initialize Logic – INITIALIZE clears all logic when the computer power is first turned on, when the CLEAR key on the console is operated, or when the CAF instruction is executed.

8.7.1.4 Run Signal and CON ALL HLT Logic – The loss of the RUN signal from the computer will generate CON ALL HLT, stopping the tape drive unit regardless of the status of the Command Register. RUN is negated any time the program stops.

8.8 COMMAND REGISTER

The Command Register (Figure 8-10) consists of the UNIT, Forward/Reverse (F/R), Stop/Go (S/G) and Read/Write (R/W) flip-flops. The flip-flops in the Command Register are set or cleared by AC 0–3 when the Command Register is loaded by the SDLC instruction (Paragraph 8.5.2).

8.8.1 Unit Select Logic

The UNIT SEL flip-flop determines which TU56M unit is selected. The UNIT flip-flop sets when bit 0 from the AC is a 1, and it is clocked into the flip-flop by TP3 during the execution of an SDLC instruction. If UNIT flip-flop is cleared, Unit 0 is selected. SDLC and TP3 clear the UNIT flip-flop if the data input is low (AC bit 0 is 0).

8.8.2 Forward/Reverse (F/R) Logic

The F/R flip-flop (Figure 8-10) determines the direction of tape movement. When an SDLC instruction is performed and bit 1 from the AC is a 1, the F/R flip-flop sets and directs the tape drive to move backward. If the data input is 0 (bit 1 from the AC is 0) F/R clears when the SDLC instruction and TP3 are applied to the clock (C) input, and the drive is directed to move forward.

8.8.3 Stop/Go Logic

The stop/go logic (S/G) flip-flop (Figure 8-9) enables the tape to move in a direction determined by the F/R flip-flop. If AC bit 2 is a 1 when the SDLC instruction is performed, the S/G flip-flop sets. The output of the flip-flop is applied to a latch which also has TP4 as an input. TP4 clocks the latch 300 ns after S/G is set and pulls latch output low. The 300-ns delay allows the unit select lines to settle before the S/G signal is applied to the TU56M. S/G is ANDed with POWER OK to remove the GO signal from the TU56M during a power down. Power in the TU56M does not drop as quickly as power on the PDP-8/E and the tape may continue to run and write erroneous data.

Loss of the RUN signal from the processor generates CON ALL HLT to the TU56M and clears the S/G flip-flop.

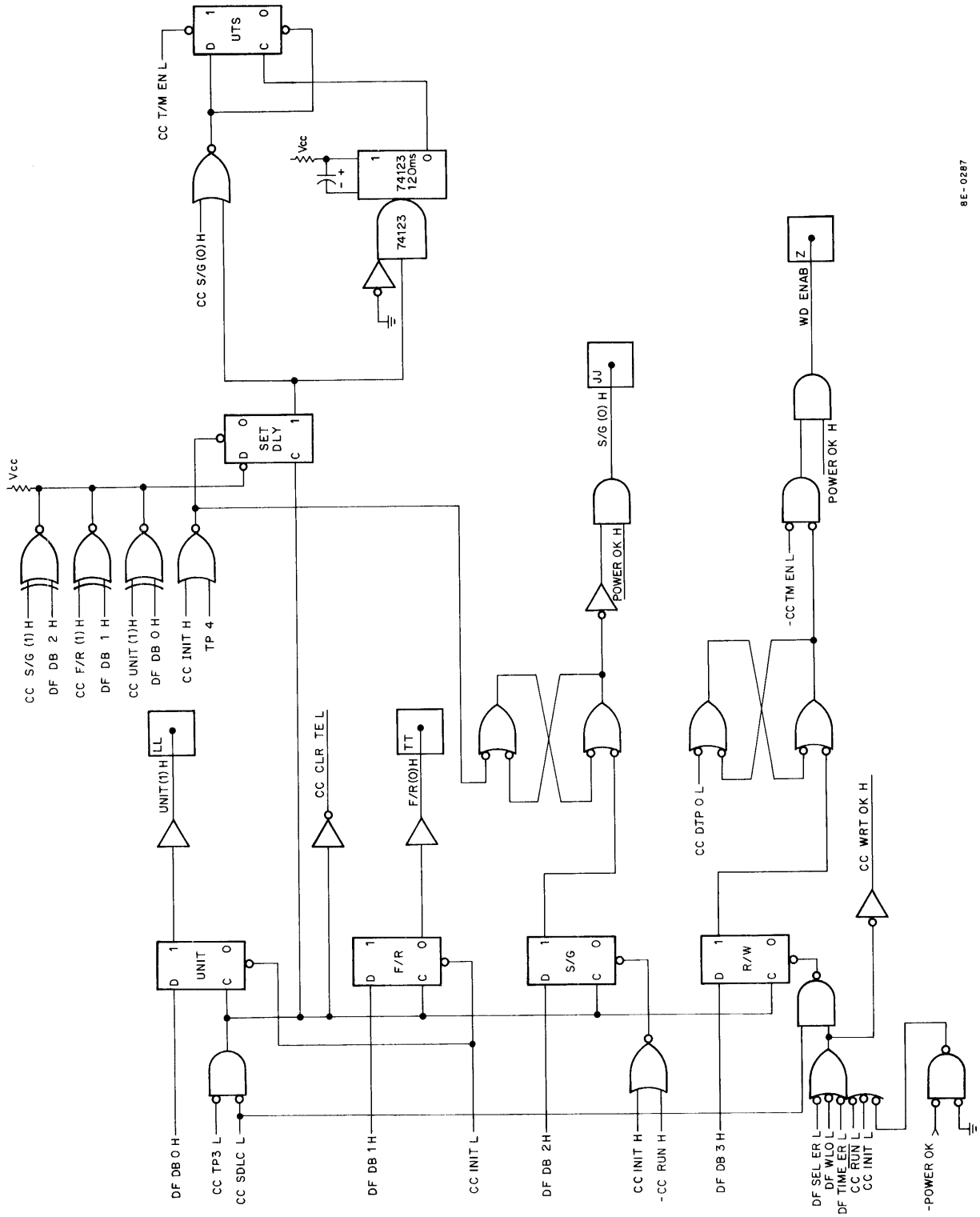


Figure 8-10 Command Register and UTS Logic

8.8.4 Read/Write Logic

The Read/Write flip-flop (R/W) (Figure 8-10) selects the read or write mode in the TU56M. If bit 3 from the AC is a 0 when the SDLC instruction is executed, R/W will clear and the TU56M will not write on the tape. If bit 3 is 1 when the SDLC instruction is executed, R/W sets, and its output is applied to the reset input of a latch. D TP0 is applied to the set input of the latch. When D TP0 is received from the Time Pulse Generator, the outputs of the latch will be low if R/W is set. The latch output is ANDed with NOT CC T/M EN, which enables the gate when S1 is set to OFF (Figure 8-11). The output of the first gate is ANDed with POWER OK H to generate WD ENAB, causing the TU56M to write on the DECtape. WD ENAB is ANDed with POWER OK to remove WD ENAB from the TU56M during a power down of the system. R/W is also cleared by any of the following conditions to select read mode and remove WD ENAB from the TU56M.

a. SEL ERR
b. TIME ERROR
c. WRITE LOCKOUT
d. POWER NOT OK
e. INITIALIZE
f. NOT RUN

The DECtape can read or write in both directions, but the program must take care of the obverse complement data.

8.9 UTS DELAY LOGIC

The UTS delay logic starts a 120-ms delay after S/G is set, to ensure the tape is up to speed before data is read from or written on the DECtape (Figure 8-10). Any change in the Command Register, except R/W, clears the UTS flip-flop and starts a new 120-ms timeout. The D input of SET DLY is enabled by the Exclusive-OR gates which cause SET DLY to set if the UNIT, S/G, or F/R flip-flops are changed, thus clearing UTS and starting another 120-ms delay. The following conditions set the SET DLY flip-flop clearing UTS:

a. S/G $\neq$ DF DB 2 (AC Bit 2)
b. F/R $\neq$ DF DB 1 (AC Bit 1)
c. UNIT $\neq$ DF DB 0 (AC Bit 0)

If SET DLY is set, the 74123 IC is triggered and starts a new 120-ms timeout. After 120 ms, if no new changes are made in the Command Register, the clock input of the UTS flip-flop goes high. This transition causes UTS to set if S/G is set supplying a true (high) to the D-input. UTS will not set if the S/G flip-flop is cleared. Any time UTS is cleared the TT ENABLE flip-flop (Figure 8-11) will clear and disable the Time Pulse Generator logic. The SET DLY flip-flop is cleared by TP4 of each CC SDLC instruction that changes the Command Register. This is to ensure that the 120 ms (74123) can trigger on each CC SDLC and the only timeout is 120 ms after the last SDLC.

When SET DLY clears it also clears the Mark Track Register (Figure 8-14, Paragraph 8.11).

8.10 TIME PULSE GENERATOR

The Time Pulse Generator (Figure 8-11) has two functions, one is to produce pulses to write the time and mark tracks (formatting) and the other is to produce timing pulses from the time track signal (RTT) to allow reading and writing of data. The WTT signal, a 33.2-μs square wave, is written on the time track of the DECtape when the tape is formatted. The Time Pulse Generator reads the RTT signal from the timing track of the tape when data is read from the tape or written on the tape. Full- and half-cycle pulses (Figure 8-5, signals DTP, DTP0, and DTP1) are produced on the rising and falling edges of the time track signal. The time pulses are synchronized with the UTS flip-flops so pulses will be produced only when the tape is up to speed.

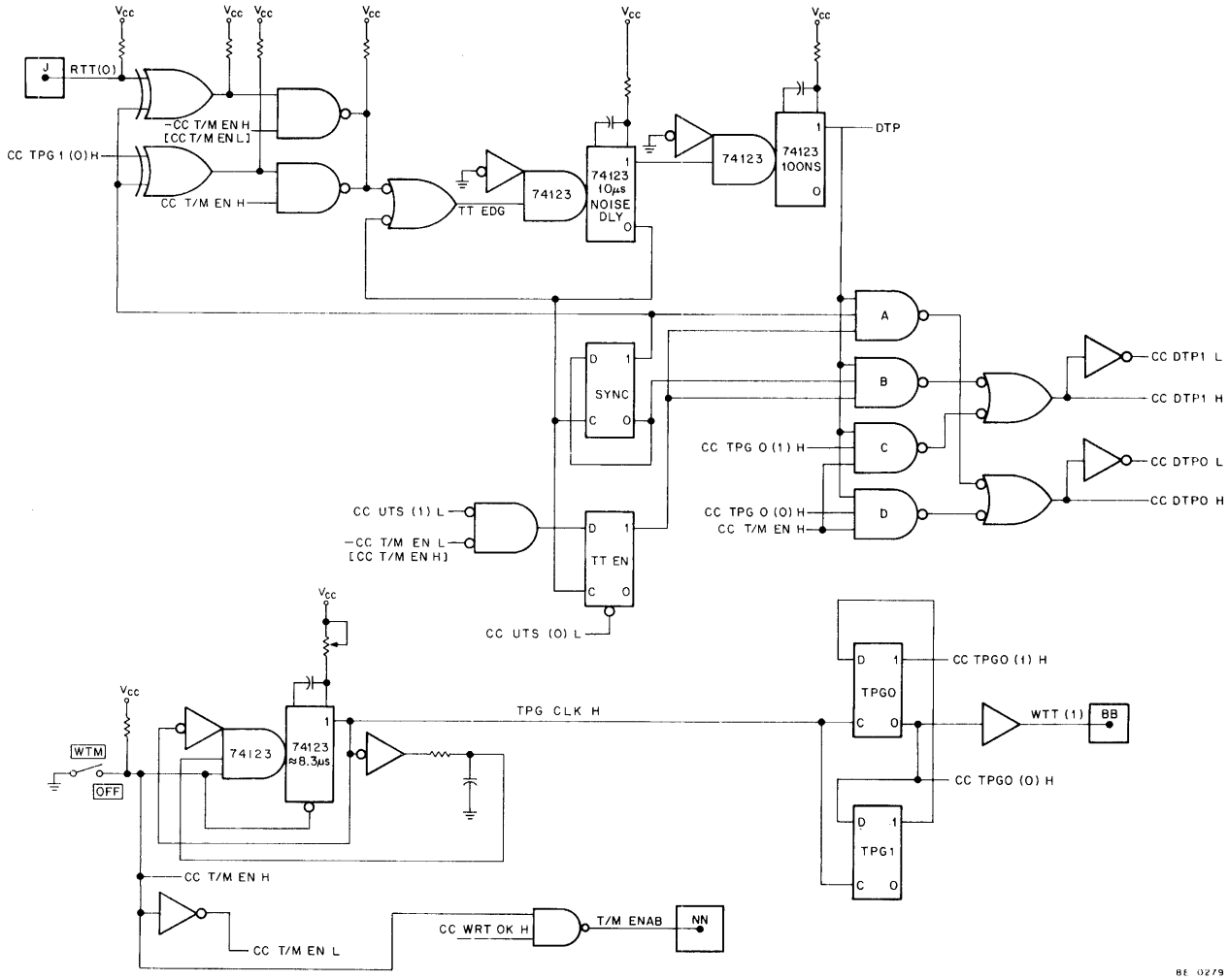


Figure 8-11 Time Pulse Generator Logic

8.10.1 Write Time Track Pulses

The Write Time Track (WTT) pulses are produced by a 74123 IC (Figures 8-5 and 8-11) and two flip-flops (TPG 0 and TPG 1) arranged in a conventional switch-tail ring counter. The 74123 IC outputs a pulse every 8.3 μs when S1 is set to WTM. S1 removes the low level from the clear input in the 74123 IC and enables the input gate, which allows the 74123 IC to be triggered. The T/M ENAB signal is also sent to the TU56M to allow writing on the time and mark tracks. CC T/M EN is ANDed with WRT OK to remove T/M ENAB from the TU56M during a power down of the PDP-8/E, and any other condition that clears the R/W flip-flop.

The 74123 used to generate TPG CLK H is a retriggerable monostable multivibrator (one shot) that is set for 8.3 μs. External circuitry causes this one shot to retrigger itself on its own trailing edge. An inverter and integrator on the output of the 74123 IC delays the triggering process for 100 ns, establishing a minimum width for TPG CLK H. TPG 0 and TPG 1 produce overlapping 33.2-μs square wave pulses (Figure 8-5). The leading edge of TPG 0 occurs 8.3 μs before the leading edge of TPG 1. The 0 output of TPG 0 is applied to the time track (WTT) signal. The outputs of TPG 0 and TPG 1 are also used to produce DTP0 and DTP1 when writing the time and mark tracks. Gates C and D (Figure 8-11) must be enabled to apply these signals to the control logic to allow writing on the time and mark track. CC T/M EN H is applied to C and D when S1 is set to WTM during a write operation and CC TPG 0 (1) H or CC TPG 0 (0) H are applied to the gates during a write. The source of the DTP signal is explained below.

CC TPG is combined in an Exclusive-OR gate with the output of SYNC. The output of the Exclusive-OR gate goes high when SYNC (1) H and CC TPG 1 (0) H are equal. The 74123 IC is triggered only on the rising edge of its input signal, and the SYNC flip-flop is complemented each time the 10-μs 74123 times out. Thus, the SYNC flip-flop changes state about 7 μs before CC TPG 1 changes state, this allows TT EDG to go low for about 7 μs. When CC TPG 1 switches to the same level as SYNC, then TT EDG again goes high retriggering the 10-μs 74123 (NOISE DLY). Once the NOISE DLY is triggered its output holds TT EDG high (through an OR gate) thus preventing any cross-talk noise coming from RTT (0) from retriggering the delay.

Note (Figure 8-5) the rising edge of NOISE DLY occurs in the center of CC TPG 0 (WTT). This produces a 90 degree phase shift between the writing of the time track and mark track. The phase shift is required so that when the time track (RTT) is read back during a normal data transfer, the time pulses used to strobe in the mark track occur in the center of the mark track signal.

The rising edge of the 10-μs 74123 IC (NOISE DLY) triggers the 100-ns 74123 and produces a 100-ns pulse (DTP). DTP is produced on every edge of CC TPG 1 and is applied to AND gates C and D. When CC TPG 0 (0) is high, D is enabled and CC DTP 0 H is produced; when CC TPG 0 (1) is high, C is enabled and CC DTP 1 L is produced. This separates the DTP pulses into two pulse trains, one has pulses on the rising edge of CC TPG 1 and the other has pulses on the falling edge of DTP 1.

Most signals in the Time Pulse Generator (Figure 8-11) are gated against CC TM EN. This is done to ensure the logic required for writing the time and mark tracks is enabled only for that operation and the logic to read and write data is gated off. The reverse is true when reading the time track and transferring data.

8.10.2 Read Time Track Pulses

The RTT signal read from the time track is used to produce time pulses (Figures 8-11 and 8-12) which allow data to be transferred to or from the DECtape. To supply time pulses (CC DTP0 and CC DTP1) AND gates A and B must be enabled by DTP, SYNC, and TT EN. TT EN is set by the first falling edge of NOISE DLY after UTS is set. This ensures that time pulses are not produced while the tape is getting up to speed. TT EN is cleared by the loss of the UTS signal.

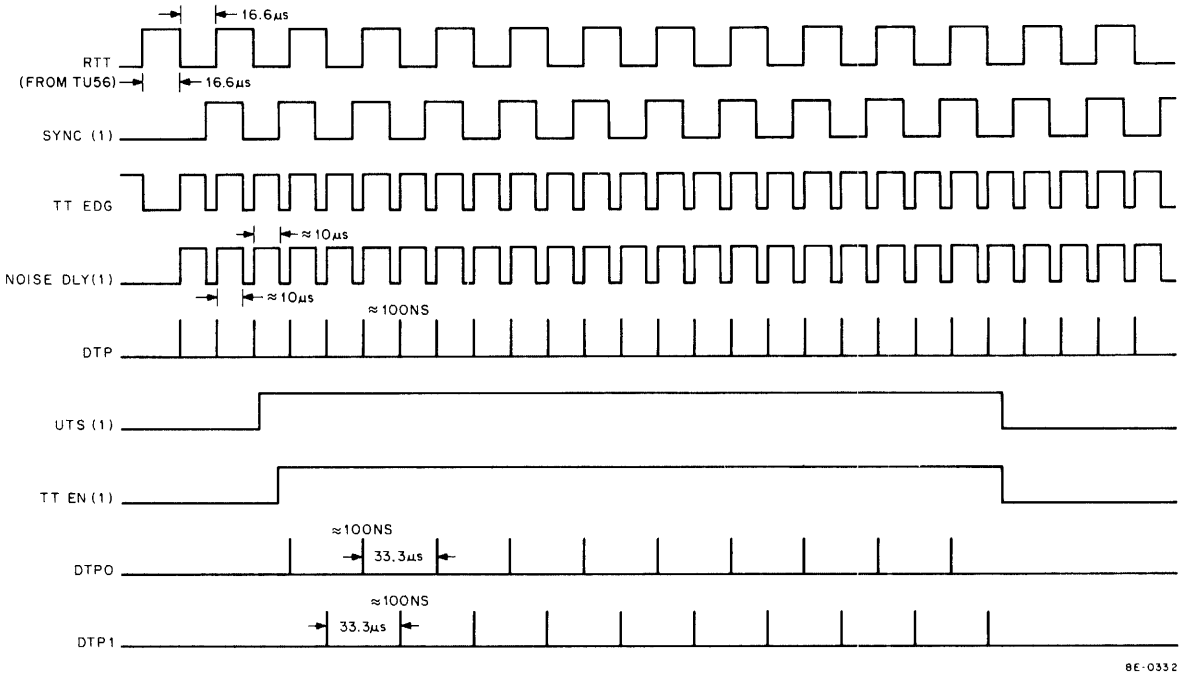


Figure 8-12 Read Time Track Pulse Timing

Note the WTM switch must be OFF when tapes are not being formatted. If it is in the WTM position and the tape moves (but it is not being formatted) the time and mark tracks will be destroyed and the tape must be formatted.

The third leg of gates A and B is enabled by DTP out of the 100-ns monostable multivibrator which is triggered by the rising edge of the 10-μs NOISE DLY.

The logic to produce CC DTP1 and CC DTP0 is the same as that for writing the time track. The only difference is that now the signal that generates these pulses is the time track (RTT) coming from the TU56M, rather than being generated on the M868. The SYNC flip-flop separates the DTP pulses through gates A and B, rather than CC TPG 0 and gates C and D.

As before SYNC is one input to the Exclusive-OR gate which triggers the NOISE DLY every time RTT and SYNC are at equal levels. The result is that DTP is produced on each edge of the RTT signal (Figure 8-12). When SYNC is set gate A is enabled and the DTP produced on the rising edge of RTT goes through gate A and comes out as CC DTP0. When SYNC is cleared, gate B is enabled and DTP produced on the falling edge of RTT goes through gate B and comes out as CC DTP1.

Thus, the time pulses are produced to shift in the data, set the flags, set WD ENAB (Figure 8-10) and shift the data out for writing, etc.

8.11 FLAGS AND SKIP LOGIC

The Single Line flag and Quad Line flag are used to count lines of data read from or written onto the tape and to enable skip logic when the CC SDSS or CC SDSQ instructions are performed (Figure 8-13). Time Error flag indicates the timing of a transfer was not correct and enables the skip logic when the SDST instruction is executed.

8.11.1 Single Line Flag

The Single Line flag (SLF) is used to detect codes on the mark track. SLF is set by CC DTP1 each time a line of data is read from the DECtape. If SLF is set and the SDSS instruction is executed, the SKIP line on the OMNIBUS is grounded, causing the program to skip to the next instruction. The SKIP could cause a subroutine to be performed to determine what code is in the Mark Track Register and take action accordingly; i.e., is the code a Block Mark? If so, read the Data Register, and check to see if it is the block number required. Is it an End Zone Mark? If it is, then you have run out of tape; stop, then reverse direction to continue. SLF is ignored by the program after the correct block of data has been found, as the program must keep track of the number of words being transferred and put the parity word at the end of the data.

8.11.2 Quad Line Flag and Counter Logic

The Quad Line Flag (QLF) (Figure 8-13) sets each time the counter made up of flip-flops B and C counts up to four, indicating four lines of data have been read from or written onto the DECtape. DTP1 is applied to the clock (C) input to cause the counter to increment each time a line of data is transferred. When QLF is set and the SDSQ instruction is performed, the SKIP line on the OMNIBUS is grounded causing the program to skip to the next instruction and call a routine to either load or read the Data Register. The 1 output of QLF is also applied to the logic to detect a TIME ERROR (Figure 8-13), as stated before SLF and QLF are cleared by instructions CC SDRC, CC SDRD, or CC SDLD, and the loss of UTS.

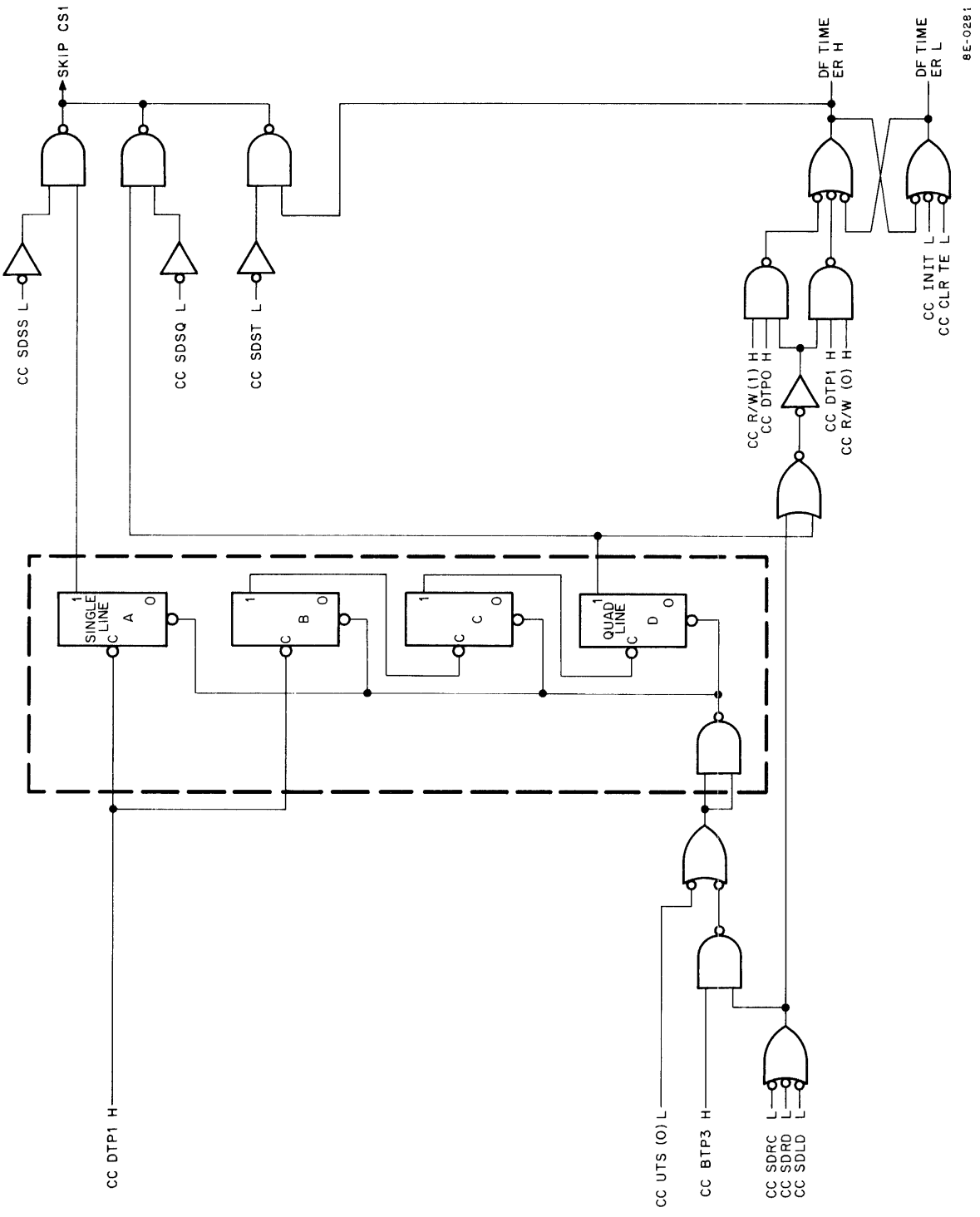


Figure 8-13 Single Line Flag, Quad-Line Flag, and Skip Logic

8.11.3 Time Error Flag

The Time Error flag (Figure 8-13) is a latch made from two 7410 gates which sets and generates a TIME ERROR to indicate the program did not transfer data to or from the Data Register before the next byte has transferred to or from the tape. Any of the following conditions will generate a TIME ERROR:

a. QLF (1), DTP0 H, and R/W Set (1) (Write Operation)

b. QLF (1), DTP1 H, and R/W Cleared (0) (Read Operation)

c. If SDRC, SDRD, or SDLD is executed just as the tape is ready to transfer another byte.

TIME ERROR is cleared by INITIALIZE or an SDLC instruction. When TIME ERROR is set and the SDST instruction is executed, the SKIP line is grounded, causing the program to skip the next instruction.

8.12 MARK TRACK REGISTER

The Mark Track (MT) Register (Figure 8-14) receives serial data from the mark track (RMT) containing the mark track codes and outputs 6 bits of parallel data for transfer to the AC. The MT Register is made up of two 8271 ICs. (See Appendix A.8, Volume 1, for timing diagram pin locator and truth table). The 8271 IC is a 4-bit shift register that receives a parallel serial input and provides a parallel output. The parallel output is applied to the Data Register (Figure 8-16) for the transfer to the AC during an SDRC instruction.

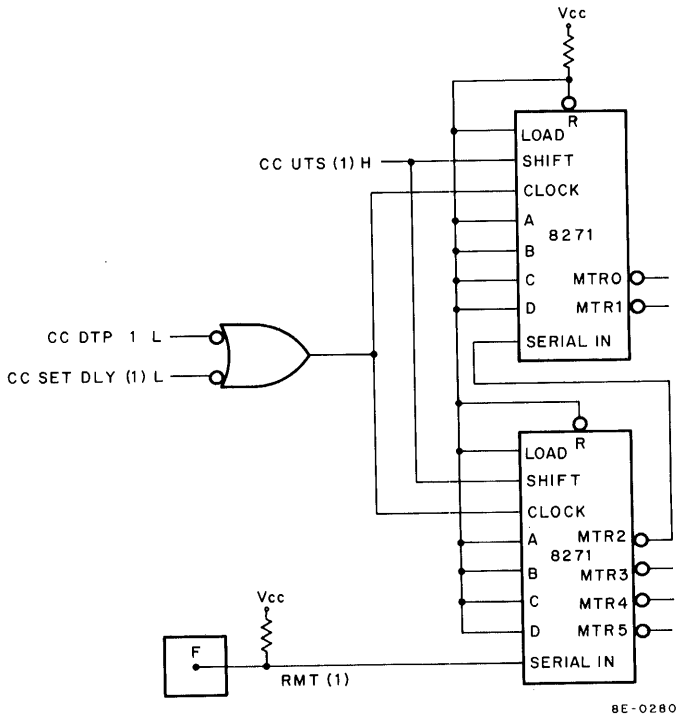


Figure 8-14 Mark Track Register

The output of the MT Register has been redefined; i.e., 1 is a low level and a 0 is a high level output.

The MT Register is cleared when SET DLY is cleared. When SET DLY is set UTS is cleared, so the CC UTS (1) signal on the shift input is low. When SET DLY is cleared it enables the clock input of the 8271, and as the parallel data output are held high the outputs all go high (redefined as 0 output). As stated before, the program must wait at least six SLFs before the MT Register holds a real mark track code.

8.13 DATA REGISTER AND GATING LOGIC

The Data Register (Figure 8-15) receives data from the DATA BUS and converts it to serial data to be written on the DECtape or takes serial data from the DECtape and converts it to parallel data to be gated to the DATA BUS for transfer to the AC. The Data Register consists of three 8271 ICs (see Volume 1, Paragraph A.8, for timing diagram, pin location, and logic diagram) and logic to select the input from the DATA BUS (parallel) or the input from the tape (serial). The output (the data being written on tape) is taken from SR0, SR1, and SR2.

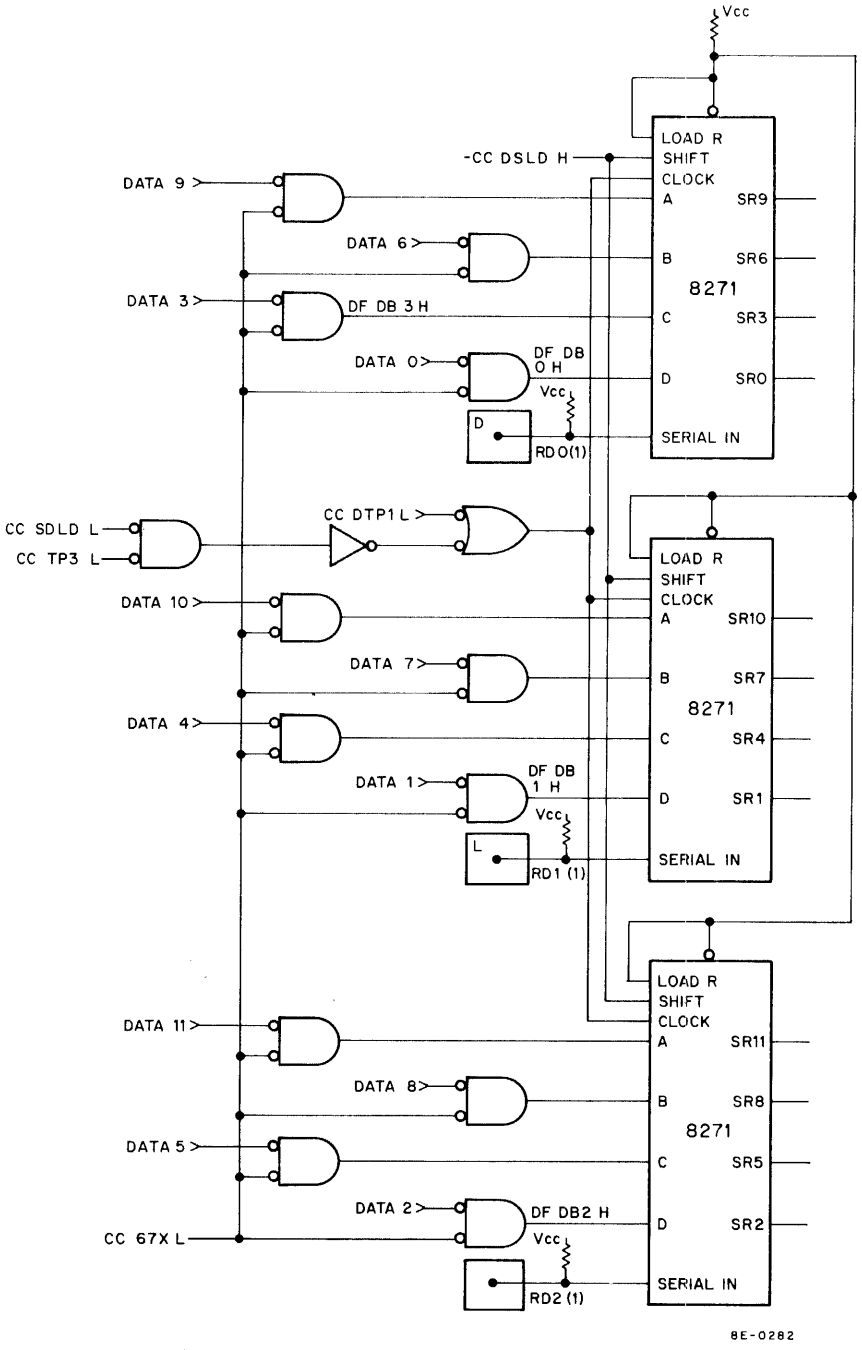


Figure 8-15 Data Register

Three outputs are shifted into the Write Register (Figure 8-17) to be written on tape. The serial input from the DECtape, RD0, RD1, or RD2 are shifted in by the CC DTP1 pulse and taken from the register as parallel data for transfer to the DATA BUS (Figure 8-16). The SDLD instruction is applied to the shift input to enable parallel transfer of data from the DATA BUS at TP3 time during a loading operation. At other times, the shift input is held high to enable serial shifting of data through the SR.

8.14 DATA GATING LOGIC

The data gating logic (Figure 8-16) will select the data to be applied to the DATA BUS for transfer to the AC by an SDRC or SDRD instruction. The SDRD instruction enables AND gates to transfer SR0–SR11 to the DATA BUS. SR0–SR11 are the 12 data bits read from the tape, applied to the Data Shift Register as serial data, and output to the data gating logic as 12 bits of parallel data. The SDRC instruction enables AND gates to transfer the contents of the Command Register, Status Bits, and MT Register to the DATA BUS.

8.15 WRITE FUNCTION REGISTER

The Write Function Register (WF0, WF1, WF2) receives data from SR0, SR1, and SR2 (Figures 8-17 and 8-6) and outputs the data to the TU56M at the correct timing pulse times.

At CC DTP0 (rising edge of RTT) the data from the Shift Register is loaded into the WF Register. At the same time, the Complement Word (COMP WD) output of the latch goes high. COMP WD is then compared to the complement of the data loaded into WF through the Exclusive-OR gates and if they are the same level, the Word (WD) lines go high. If a 1 had been loaded into WF0 at the CC DTP0, then its output would have been low. At CC DTP1 (falling edge of RTT) COMP WD goes low and WF0 will go high. The positive transition at CC DTP1 causes a 1 to be written on tape. If a 0 had been written into WF0, then between CC DTP0 and CC DTP1 the WD0 signal would be high. When COMP WD switches low at CC DTP1, there is a negative transition at WD0 and a 0 is written on tape. By examining the write timing diagram (Figure 8-6) you can see how alternating 1s and 0s always produce a negative transition for a 0 and a positive transition for a 1.

8.16 WRITE ECHO AND SELECT ECHO CIRCUITS

WRITE ECHO and SELECT ECHO (Figure 8-18) are supplied to the TD8-E by the TU56M. A SEL ERR condition exists if no unit has been selected or both units have been selected. Write Lockout exists if the selected drive unit is not Write Enabled. The voltage level for these signals and the resulting error condition are shown in Table 8-6.

The SEL ERR and WRITE LOCKOUT ERROR signals are applied to the data gates (Figure 8-16) as status bits to be transferred to the AC by an SDRC instruction. The software must decide what to do when these errors are detected. Both errors clear the R/W flip-flop to keep from writing under an error condition.

SECTION 5 MAINTENANCE

Recommended preventive maintenance should be scheduled on a regular basis to maintain the reliability and performance of the DECtape. Preventive maintenance schedules are found in the *TU56 DECtape Transport Maintenance Manual,* Chapter 6, Paragraph 6.2.

TD8-E DECtape Diagnostic (MAINDEC-08-DHTDA) and TD8-E Formatter (DEC-8E-EUZC-PB) were written to checkout and test the TD8-E DECtape Control with TU56M DECtape Transports. The diagnostic program and formatter check all logic, as well as the ability to read and write. The diagnostic also provides subroutines for monitoring TD8-E signals with an oscilloscope and display data in the AC. When a malfunction is suspected the TD8-E Diagnostic should be used to checkout and troubleshoot the TD8-E. Refer to the *TU56 Maintenance Manual* for test equipment, troubleshooting aids, and adjustments.

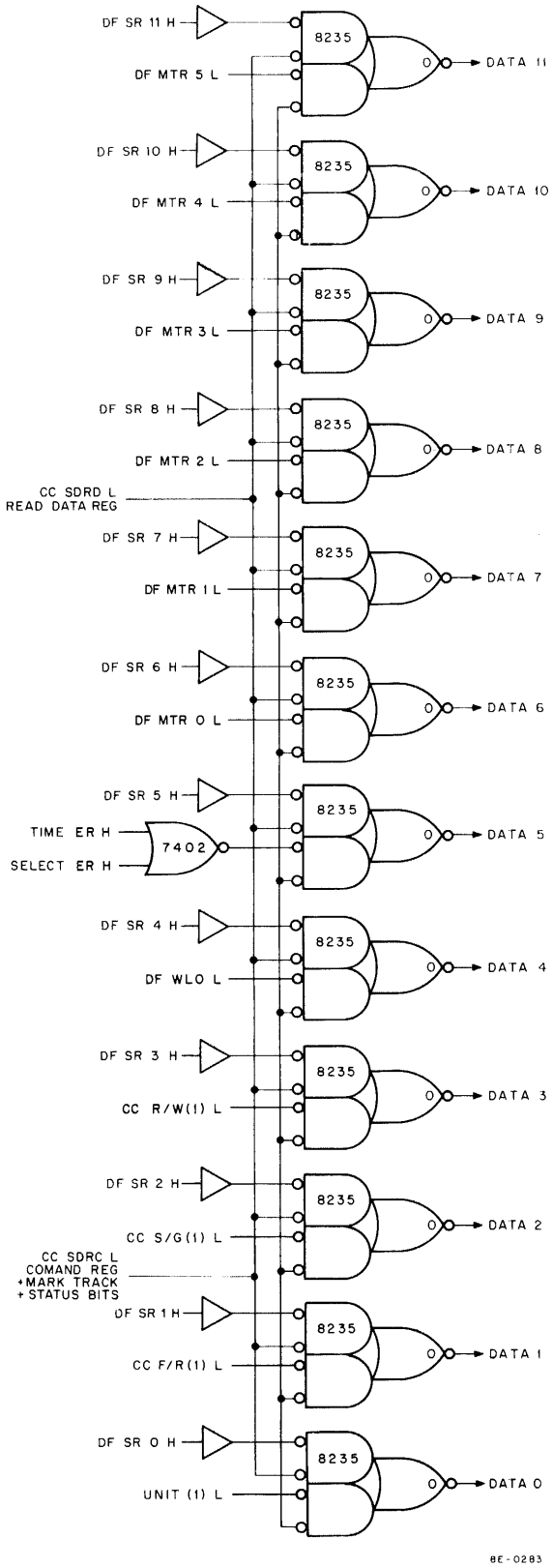


Figure 8-16 Data Gating Logic

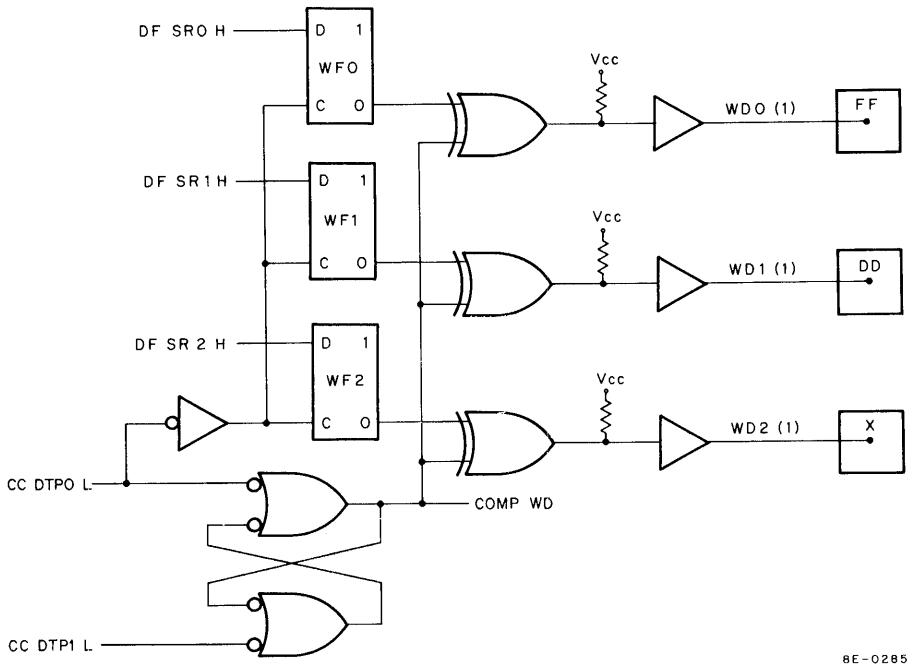


Figure 8-17 Write Function Register

Table 8-6

Write Echo and Select Echo Signal and Voltage Levels

Signal Voltage Level	Resulting Condition
WRITE ECHO 0V (Write Enable)	Write Lockout False
WRITE ECHO -3V (Write Lockout)	Write Lockout True
SELECT ECHO -3V (2 units selected)	Select Error (True)
SELECT ECHO -5V (1 unit selected)	Select Error (False)
SELECT ECHO -15V (No unit selected)	Select Error (True)

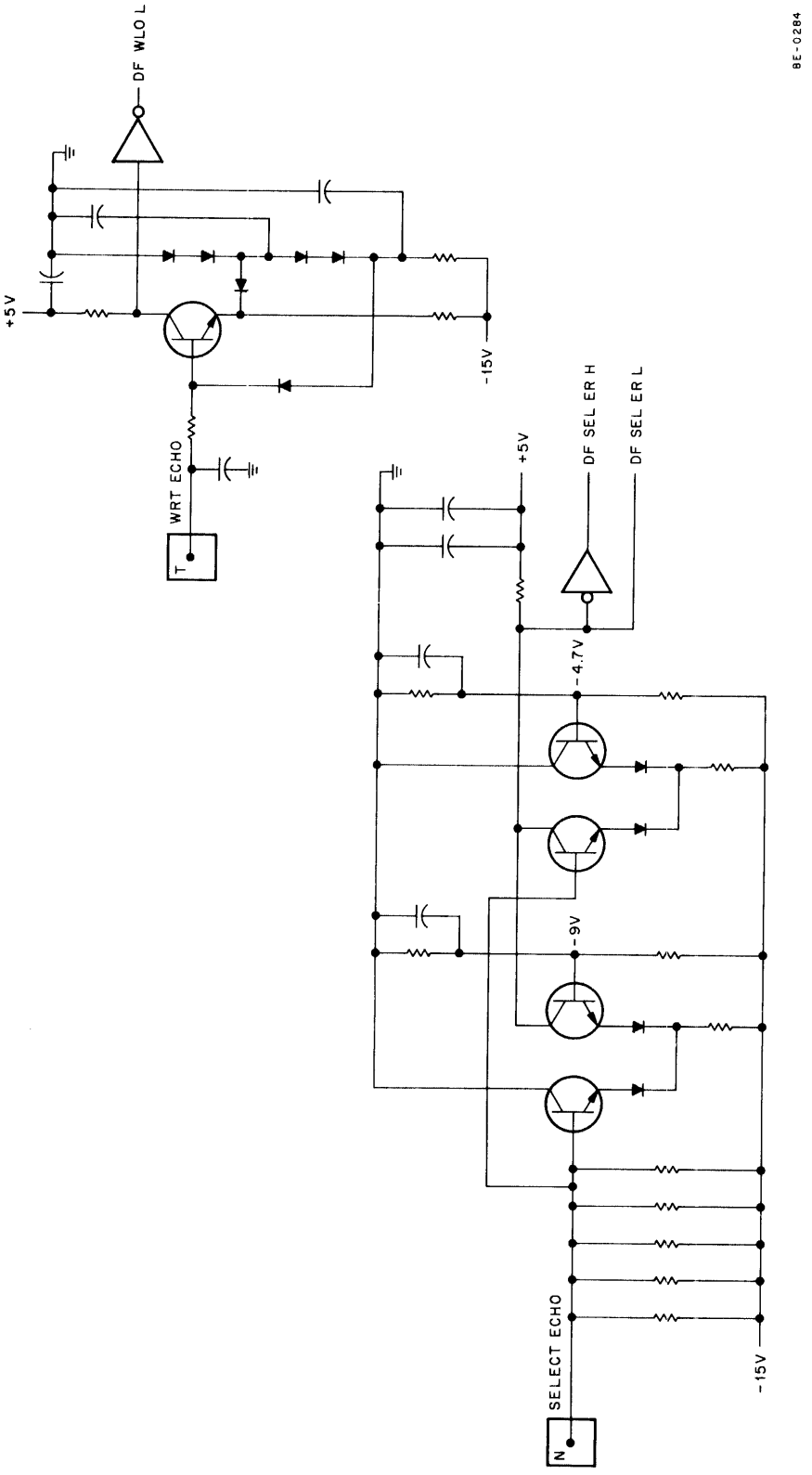


Figure 8-18 Write Echo and Select Error Circuits

SECTION 6 SPARE PARTS

Table 8-7 lists recommended spare parts for the TD8-E. These spare parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 8-7
TD8-E Recommended Spare Parts

DEC Part Number	Description	Quantity
19-10436	IC 74123	1
19-09935	IC 8235	1
19-09931	IC DEC 74H04	1
19-09929	IC DEC 7417	1
19-09712	IC DEC 8242	1
19-09705	IC DEC 8881	1
19-10391	IC DEC 5314	1
19-09686	IC DEC 7404	1
19-09615	IC DEC 8271	2
19-09594	IC DEC 8251	1
19-10394	IC DEC 5384	1
19-10392	IC DEC 5380	2
19-09054	IC DEC 7493	1
19-09050	IC DEC 7475	1
19-09004	IC DEC 7402	1
19-05590	IC DEC 7401	1
19-05578	IC DEC 7430	1
19-05576	IC DEC 7410	2
19-05575	IC DEC 7400	2
19-05547	IC DEC 7474	2
15-09338	Transistor DEC 6351	2
11-00114	Diode, D664	2
11-00113	Diode, D662	2

PART 9
DISPLAYS

CHAPTER 9
TM8-E DECMAGTAPE CONTROL

SECTION 1 INTRODUCTION

The TM8-E DECmagtape Control interfaces the PDP-8/E with the TU10 Master System (Figure 9-1).

To perform this function the TM8-E:

a. Decodes programmed instructions.

b. Accepts and stores word count, current address, command, and function words.

c. Selects a program-designated transport (eight maximum in the system) and starts the operation designated by the program.

d. Generates break requests to initiate a Single Cycle Data Break.

e. Generates interrupts and skips for flag checking .

f. Buffers the input/output data and assembles a 12-bit word into two 6-bit characters to be written on a 7-track transport; also controls the writing of the 8 LSBs of a 12-bit word on 9-track transports.

g. Performs housekeeping chores for Single Cycle Data Breaks, i.e., increments Word Count and Current Address Registers.

h. Provides ERROR and JOB DONE flags.

i. Provides IOTs for TM8-E maintenance.

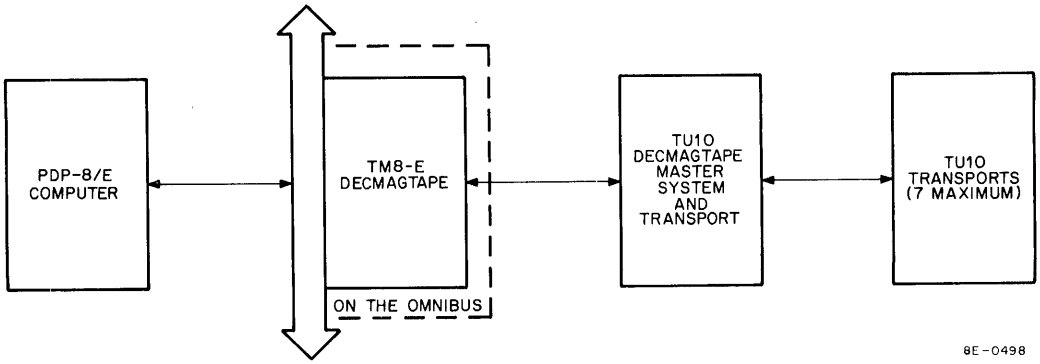


Figure 9-1 TM8-E DECmagtape Control and TU10 Master System, Block Diagram

The following quad modules comprise the TM8-E:

M8321 Output Control Module
M8322 Control and Data Break Module
M8323 Transport Status and Control Module
M8327 Registers Module

These quad modules must be inserted into the OMNIBUS and connected together via H851 Top Connectors. Two BC08-L cables are used to connect the TM8-E (input and output) to the TU10 Master System. The TM8-E receives +5V logic power from the PDP-8/E OMNIBUS. No power is supplied to or received from the TU10 Master System by the TM8-E or PDP-8/E.

The TU10 DECmagtape Transport operates at 45 ips and is available in the following formats:

a. 7-track version, with recording densities of 200, 556, or 800 bpi.

b. 9-track version, with recording density of 800 bpi.

9.1 RECORDING METHODS AND DECmagtape FORMATS

The DECmagtape system (TM8-E and TU10 Master/Slave System) is an on-line mass storage system for programs or data. Data is recorded on tape in vertical rows, termed characters. On a 7-track transport, each character consists of six data bits and one vertical parity bit; on a 9-track transport, each character consists of eight data bits and one vertical parity bit. The vertical parity bit is program selected as even or odd on 7- and 9-track transports. The odd parity bit guarantees that each character records at least one 1 bit, including an all zeroes character.

The parity bit is generated according to the rule that the number of 1s in a character (parity bit included) is odd or even; for example, when odd parity is used if the character contains an even number of 1 bits, a parity bit is generated to record an odd number of 1 bits. If an even number of bits is read from tape using odd parity, a vertical parity error is generated to notify the program that the data is in error.

The data characters are recorded in blocks of characters, termed records (Figure 9-2). Each record contains a specified number of characters determined by the word count and transport selected (7- or 9-track transport). The minimum record length is 4 characters, which is two 12-bit words for a 7-track transport or the eight LSB from 4 words on a 9-track transport. The minimum word count for a 7-track transport is the 2's complement of 2 or 7776_8; the minimum word count on a 9-track transport is the 2's complement of 4 or 7774_8. If a write operation is attempted for a record with less than 4 characters, there is no Cyclic Redundancy Check (CRC) or Longitudinal Redundancy Check (LRC) character and the tape transport runs away. When this occurs, an Initialize operation must be performed to stop the transport.

Records are separated by interrecord gaps (IRG). The IRG is approximately 0.5 inch at minimum, but may be extended to 3 inches by performing an Extended Gap operation. Tape IRGs (unrecorded areas) provide areas on the tape for the transport to start or stop and also separate data records.

9.1.1 NRZI Recording Method

The TU10 employs the NRZI (non-return-to-zero change on one) recording method. In the NRZI method, a 1 bit is represented by a reversal in the direction of tape magnetization on a track; a 0 bit is represented by no change in tape magnetization.

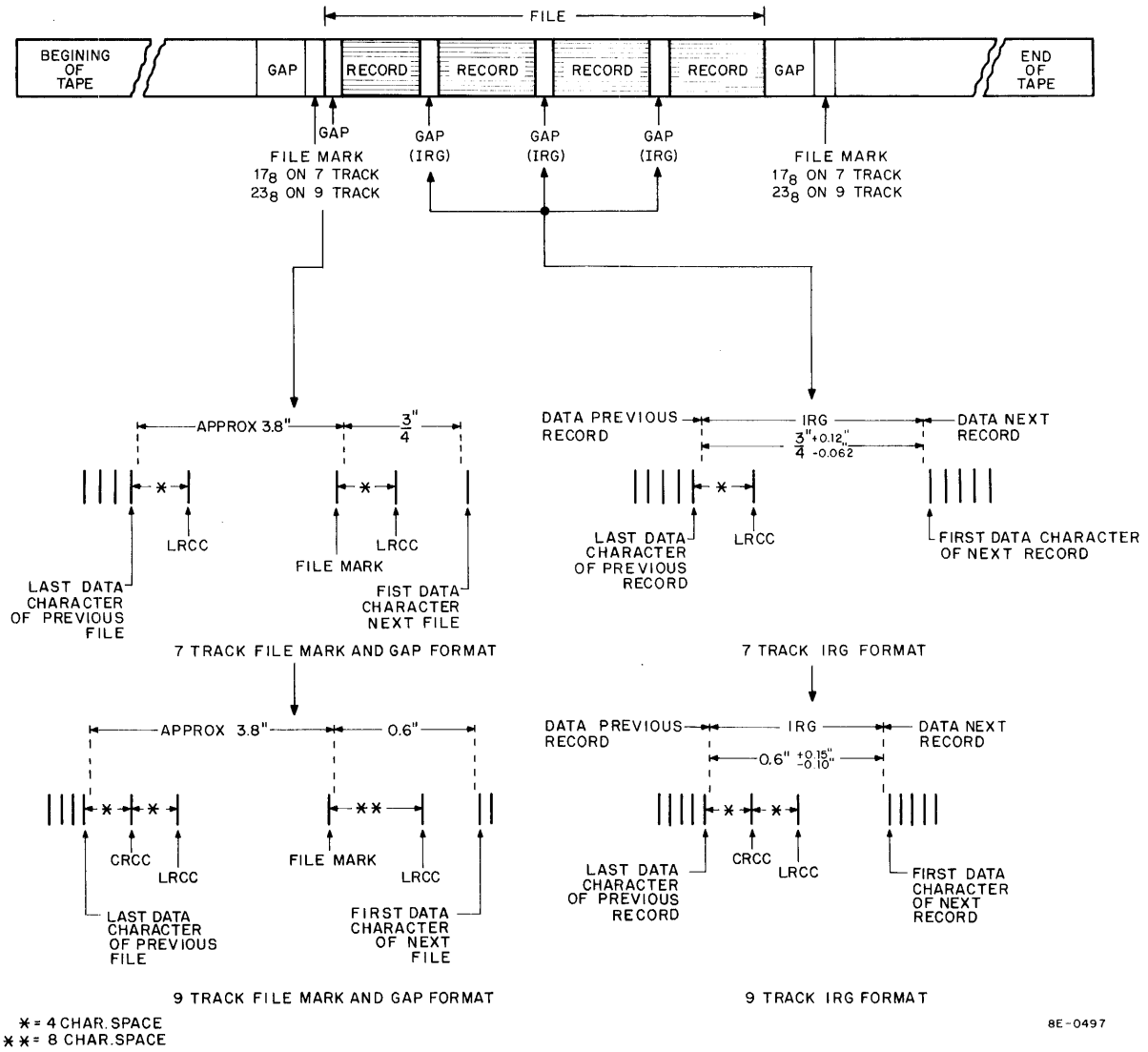


Figure 9-2 Data Recording Structure

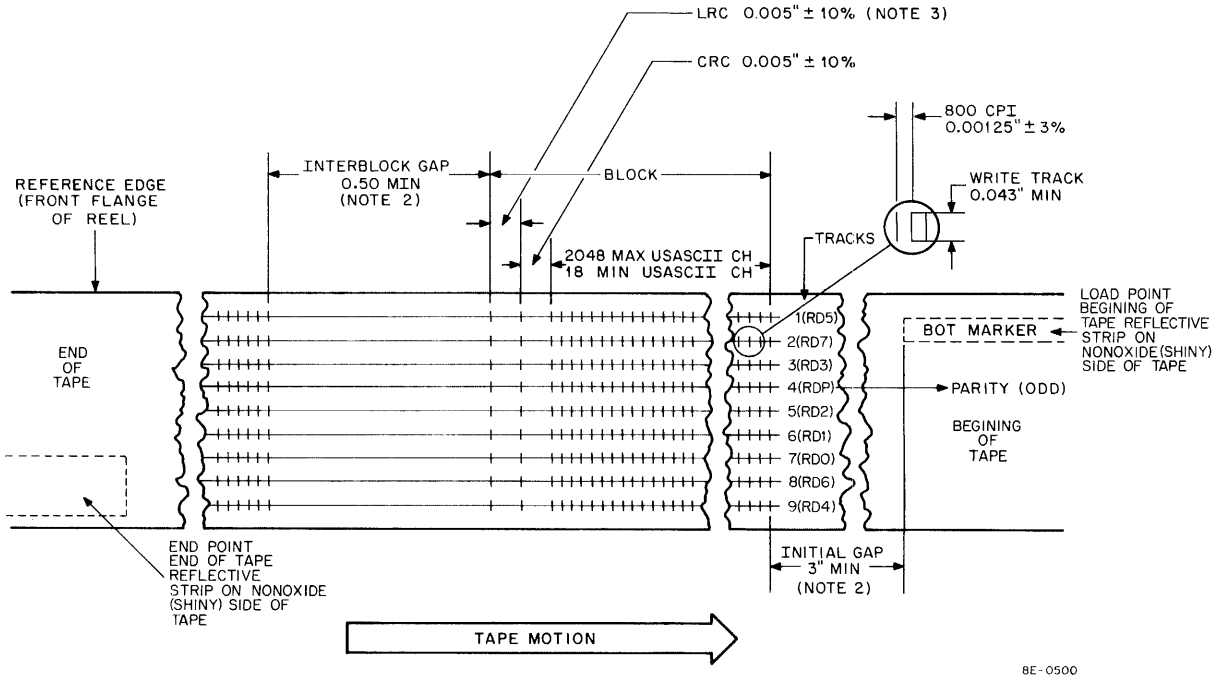
9.1.2 9-Track Tape Format

The 9-track format (Figure 9-3) is composed of from 18* to 2048 9-bit characters spaced 1/800th of an inch apart, followed by 4 character spaces, a CRC character, 4 more spaces, and an LRC character. This unit of data is called a record. At 800 characters per inch, the record is between 1/32 inch (minimum) and 5 inches (maximum). Between each record is a gap of at least 1/2 inch. The tape structure consists of a number of records followed by a File Mark (Figure 9-2). Since data is recorded and read at high speed, IRGs are used to provide space for starting and stopping the TU10 Transports. The TU10 Transport accelerates from standstill to full speed or vice versa in approximately 0.2 inch of tape; thus, the 0.5-inch IRG provides adequate space for starting and stopping the tape transport.

The CRC character (Paragraph 9.1.4) is generated in the TU10 Master System during a Write operation and written at the end of a record. The check character performs the same function to a record as the parity bit does to a character. A CRC character is not used on 7-track transports.

*UASCII program standards, not a hardware limit.

The LRC is the final character in the record and is generated so that for each track the sum of 1 bits (CRC character included) is even. The LRC character is written on tape by clearing the write buffer in the Master System after the CRC character is written. The LRC Register is gated to the write buffer and a 1 is written on each track containing an odd number of 1s; a 0 is written on each track containing an even number of 1s.



LEGEND

BPI	Tape Bits Per Inch
BOT	Beginning of Tape
LRC	Longitudinal Redundancy Check
CRC	Cyclic Redundancy Check

NOTES:

1. Tape is shown with oxide side up, Read/Write head on same side as oxide. Tape shown representing "1" bits in all NRZI recording; "1" bit produced by reversal of flux polarity, tape fully saturated in each direction.
2. Tape to be fully saturated in the erased direction in the inter-record gap and the initial gap.
3. An LRC bit is written in any track if the longitudinal count in that track is odd. Character parity is ignored in the LRC character.
4. CRC – Parity of CRC character is odd if an even number of data characters are written, and even if an odd number of characters are written.

Figure 9-3 9-Track Tape Format

9.1.3 7-Track Tape Format

In 7-track format (Figure 9-4), the CRC character is not written but the LRC character is written at the end of each record. Tape character density may be 200, 556, or 800 bpi, with even or odd parity selected by the program.

IRGs are approximately 0.75 inch instead of 0.5 inch (minimum). A record consists of 4* characters (minimum) to 8192 data characters (maximum) followed by 4 character spaces and an LRC character (Paragraph 9.1.5). A 0.75 inch IRG between each record allows the tape to be started and stopped (Paragraph 9.1.2).

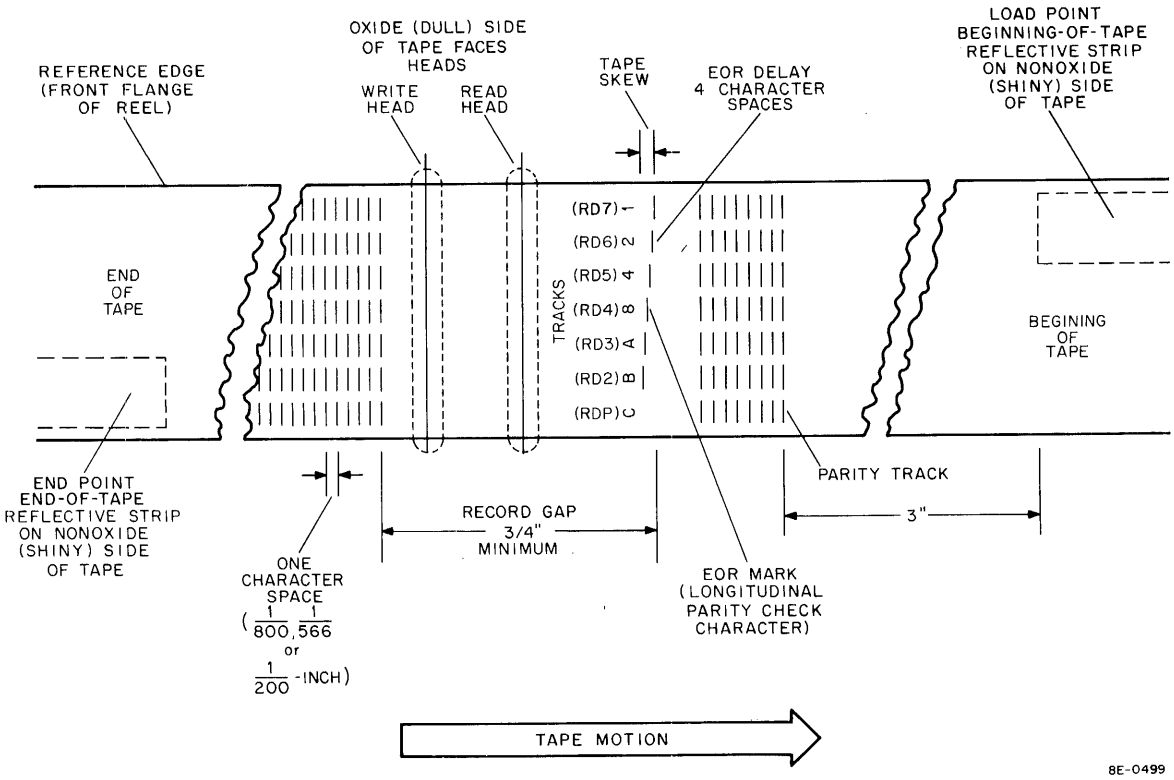


Figure 9-4 7-Track Tape Format

9.1.4 Cyclic Redundancy Check Characters (CRC)

The CRC character provides a method of error detection and correction on 9-track TU10 DECmagtape Transports only. The code has nine check bits that form a check character at the end of each record on 9-track TU10 DECmagtape Transports. To perform a correction, a record in which an error has been detected must be re-read into memory with the LRC and CRC characters for program evaluation. Errors involving more than one track can be detected but not corrected.

The CRC character is generated as follows:

a. The CRC Register, located in the Master System, is cleared at the beginning of each record. As each data bit is written on tape, it is Exclusively-ORed with its corresponding bit in the CRC Register.

b. The CRC Register is shifted one position to the right after the Exclusive-OR operation has taken place.

*Hardware limit.

c. The bits entering CRC 2, CRC 3, CRC 4, and CRC 5 of the CRC Register are inverted if the bit entering CRCP is a 1 (Tables 9-1 and 9-2). Data is shown in Table 9-1; the resultant CRC character is shown in Table 9-2.

d. Steps *a, b,* and *c* are repeated for each data character of record.

e. At CRC time, all positions of the CRC Register, except CRC 2 and CRC 4, are complemented and the resultant CRC character is written on tape.

f. The CRC Register is cleared for the next record.

Table 9-1
A Five-Character Record

Bit	Characters				
	Data Character 0	Data Character 2	Data Character 3	Data Character 4	Data Character 5
P	0	0	1	0	1
0	1	0	0	1	0
1	0	1	0	1	0
2	0	1	0	1	1
3	1	0	1	1	0
4	0	1	1	0	1
5	0	1	1	0	1
6	1	0	1	0	1
7	0	1	0	1	0

Table 9-2
CRCC In Register When Writing

CRC Bits	CRC Cleared	CRC Register				Final CRC	CRCC On Tape
		Character 1	Character 2	Character 3	Character 4		
(a) CRCP	0	0	0	0	1	1	0
(b) CRC0	0	0	0	1	0	0	1
(c) CRC1	0	1	0	0	0	0	1
(d) CRC2	0	0	0	0	0	1	1
(e) CRC3	0	0	1	0	0	0	1
(f) CRC4	0	1	0	0	0	1	1
(g) CRC5	0	0	0	1	1	0	1
(h) CRC6	0	0	1	1	1	0	1
(i) CRC7	0	1	0	0	1	0	1

9.1.5 Longitudinal Redundancy Check Character (LRC)

The LRC character is written four spaces after the last data character on a 7-track transport or four spaces after the CRC character on a 9-track transport. The vertical parity bit is always written on the LRC character; the vertical parity of LRC is never checked. The LRC character makes the longitudinal parity even for the entire record, including the CRC. The LRC is generated in the Master System by the LRC Register in the following manner:

a. The LRC Register is cleared at the beginning of a record.

b. As characters are written on tape, corresponding 1 bits complement the LRC Register at the time data is written on tape.

c. At LRC time, the LRC Register is cleared and 1s are written on tape in only those channels for which the LRC is 1 prior to clearing.

d. Following this method, the LRC character forces an even number of bits to be recorded on each track of the tape. The CRC character is included in determining the LRC character (CRC is used on 9-track transports only).

9.1.6 Data Files

As previously stated, a record is a group of characters preceded by an IRG and terminated by four spaces and an LRC character. A file is a group of records separated by IRGs and terminated by a 3-inch gap followed by a File Mark. The File Mark is a record consisting of a single data character [the end of file (EOF) character] followed by three blank characters and an LRC character. The CRC character is not written on an EOF record. The LRC character with a File Mark is a duplicate of the EOF character. On 7- and 9-track TU10 Transports, the EOF characters are 17_8 and 23_8, respectively.

9.1.7 Track Assignments

The track assignments for Read, Write, and Parity bits are shown in Table 9-3.

Table 9-3
TU10 Track Assignments for Data and Parity

9-Track Transport Track Number	Write Data Bits	Read Data Bits	7-Track Transport Track Number	Write Data Bits	Read Data Bits
1 (inside)	WD5	RD5	1	WD7	RD7
2	WD7	RD7	2	WD6	RD6
3	WD3	RD3	4	WD5	RD5
4	WDP	RDP	8	WD4	RD4
5	WD2	RD2	A	WD3	RD3
6	WD1	RD1	B	WD2	RD2
7	WD0	RD0	C	WDP	RDP
8	WD6	RD6			
9 (outside)	WD4	RD4			

9.2 COMPANION DOCUMENTS

The following documents and publications are necessary for the operation, installation, and maintenance of the TM8-E:

a. *PDP-8/E & PDP-8/M Small Computer Handbook,* 1972
b. *PDP-8/E Maintenance Manual,* — Volumes 1 and 2
c. *Introduction to Programming,* DEC 1972
d. *DEC Engineering Drawing, Magnetic Tape* (DEC-00-TM8-E-0-0)
e. *TU10 DECmagtape Master System Manual* (DEC-00-TU10M-D)
f. *TU10 DECmagtape Maintenance Manual* (DEC-00-TU10S-DC)

9.3 SOFTWARE DOCUMENTS

The following diagnostics and programs are available for the TM8-E:

a. TM8-E Control Test Part 1, MAINDEC-08-DHTMA-A
b. TM8-E Control Test Part 2, MAINDEC-08-DHTMB-A
c. Drive Function Timer, MAINDEC-08-DHTMC-A
d. TM8-E Data Reliability Test — 9-Track, MAINDEC-08-DHTME-A
e. TM8-E Data Reliability Test — 7-Track, MAINDEC-08-DHTME-A
f. TM8-E Random Exerciser, MAINDEC-08-DHTMF-A
g. TM8-E DECmagtape System Module for DEC/8X, MAINDEC-8X-DHTMA-A

The diagnostics have instructions for loading and running to check the TM8-E.

SECTION 2 SITE PREPARATION, INSTALLATION, AND ACCEPTANCE TEST

The TM8-E is installed on site by DEC Field Service personnel. No attempt should be made by the customer to unpack, inspect, install, test, or service the TM8-E until a DEC Field Service representative is present.

9.4 SITE PLANNING AND CONSIDERATIONS

Adequate site planning and preparation can simplify the installation process and result in a more efficient and reliable TM8-E installation. DEC Sales Engineers or Field Service Engineers are available for consultation with user personnel regarding installation. The customer should refer to the *TU10 DECmagtape Master System Manual* and *TU10 DECmagtape Maintenance Manual* for TU10 space requirements, environmental requirements, and installation procedures to ensure that the installation site has adequate space, cooling, and power.

Primary planning considerations for TM8-E installation are:

a. Adequate power on the OMNIBUS for the TM8-E modules (Table 9-4).

b. A 33 ASR Teletype and programmer's console to run diagnostic and MAINDEC programs.

c. Space for the TU10 Tape Transports.

d. TM8-E software for acceptance test and system operation.

Table 9-4
TM8-E Module Power Requirements

Module	Power Requirements
M8321	+5V, 1,000 mA
M8322	+5V, 775 mA
M8323	+5V, 900 mA
M8327	+5V, 1,500 mA
	Total 4,175 mA

9.5 INSTALLATION

Perform the following procedure to install TM8-E modules:

Step	Procedure
1	Ensure that power is removed from the PDP-8/E and the TU10.
2	Ensure that the PDP-8/E and the TU10 cabinets are tied to the same ground or install a ground wire between the cabinets.
3	Unpack the TM8-E modules and visually inspect each module for shipping damage.
4	Ensure that the jumpers are installed correctly to select the priority assigned to the TM8-E (Paragraph 9.14.3).
5	Insert the TM8-E modules into the OMNIBUS in the order shown in Figure 9-5. (Refer to Figure 2-3 of *PDP-8/E Maintenance Manual*, Volume 1, for module priorities.) **WARNING** **The modules must not be installed upside down. The +5V, 0.01 μF capacitors should be at the bottom (next to the OMNIBUS) on all modules installed on the OMNIBUS.**
6	Install two H851 Top Connectors between the following modules (Figure 9-5): *a.* M8321 and M8327 *b.* M8327 and M8322 *c.* M8322 and M8323
7	Insert an M989 Terminator Module in slot A06 of the TU10 Master System.
8	Connect one BC08-L cable as follows: *a.* P1 to J1 on the M8321 Output Control Module. *b.* P2 to J2 on the M8321 Output Control Module. *c.* Insert the M954 Connector Module into slot A07 of the TU10 Master System.

9 Connect the other BC08-L cable as follows:

a. P1 to J1 on the M8323 Status and Control Module.
b. P2 to J2 on the M8323 Status and Control Module.
c. Insert the M954 Connector Module into slot B07 of the TU10 Master System.

NOTE

Route cables between the PDP-8/E and TU10 so that they are protected and out of the way.

10 Check TU10 slave terminators (refer to TU10 Print Set).

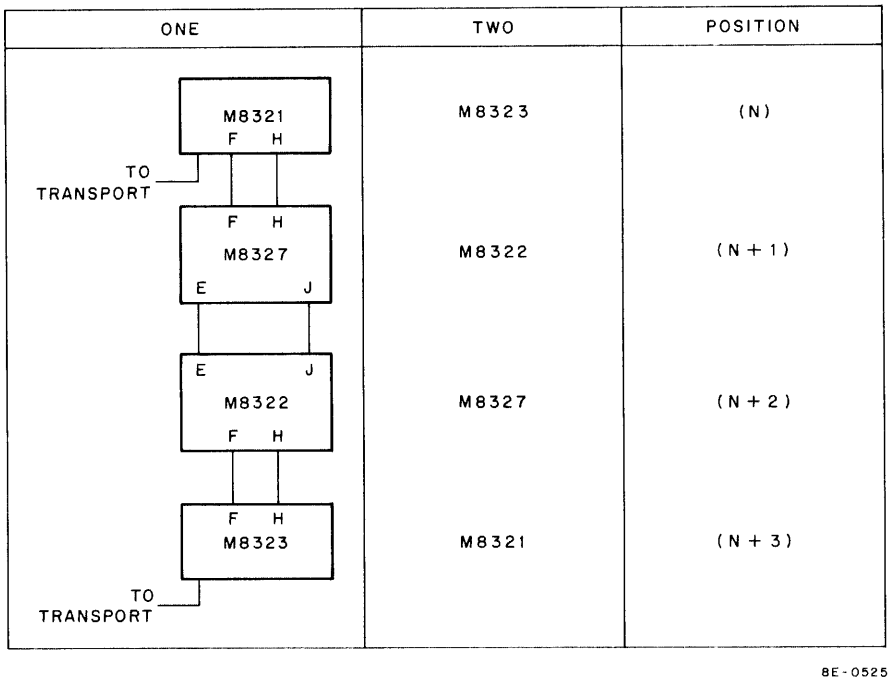


Figure 9-5 TM8-E Module Installation

9.6 ACCEPTANCE TEST

Run the Acceptance Test specified in the TM8-E Print Set (D-TD-TM8-E-1).

9.7 TM8-E INTERFACE

Two BC08-L cables are used to connect the TM8-E to the TU10 Master System. One BC08-L cable is connected between the M8321 Output Control Module and slot A07 of the TU10 Master System to provide control signals to the tape drive and data to be written on the TU10 DECmagtape (Table 9-5). The other BC08-L (Table 9-6) cable connects the M8323 Status and Control Module and slot B07 of the Master System to provide status information and data read from the TU10 DECmagtape to the TM8-E Control. An M989 Terminator Card must be installed in slot A06. The signals on the H851 Top Connectors are shown in Tables 9-7 through 9-10. The signal prefix indicates the origin of the signal, i.e., all signals prefixed by C originate at the TU10. The following is a list of prefixes and their origin.

	Prefix	Origin
a.	C	TU10
b.	OC	M8321 Module
c.	CB	M8322 Module
d.	SC	M8323 Module
e.	RE	Registers Module

The numeral following the prefix indicates the sheet of the module print where the signal originates, i.e., RE-1 indicates the signal originates on the M8327 Module, sheet 2.

Table 9-5
M8321 Output Control Module Signals and Interface

On TU10 M954 (Slot A07) Pin No.	J1 M8321 Pin No.	J2 M8321 Pin No.	Signal	Description
A1	D		C SEL 0 H	*Buffered SELECT 0
B1	F		C SEL 1 H	*Buffered SELECT 1
C1	J		C SEL 2 H	*Buffered SELECT 2
D1	L		C SEL 16 H	Not used
E1	R		C DEN 5 H	*Density 5
F1	N		C DEN 8 H	*Density 8
S1	LL		C FMK L	File Mark
J1	V		C WXG H	Extended gap
K1	X		C FWD H	Move tape forward
L1	Z		C RWD H	Move tape reverse
M1	BB		C WRE H	Write Enable with CFWD H, go off line with C REW H
D2		L	C WD0 H	Write bit 0
E2		N	C WD1 H	Write bit 1
F2		R	C WD2 H	Write bit 2
H2		T	C WD3 H	Write bit 3
J2		V	C WD4 H	Write bit 4
K2		X	C WD5 H	Write bit 5
L2		Z	C WD6 H	Write bit 6
M2		BB	C WD7 H	Write bit 7
N2		DD	C REW H	Rewind
P2		FF	C INIT H	Initialize
R2		JJ	C SET H	Begin tape operation
S2		LL	C WDR H	Write Data Ready
T2		NN	C PEV W H	Generate or check for even parity when asserted
U2		RR	C WFMK H	Write File Mark

*Refer to Table 9-11. Some pins not used are tied to ground.

Table 9-6
TM8-E M8323 Transport Status Control Module Signals and Interface

On TU10 M954 (Slot B07) Pin No.	J1 M8323 Pin No.	J2 M8323 Pin No.	Signal	Description
A1	D		C RDS L	Read Data strobe
B1	F		C SDWN L	Tape motion is stopping
C1	J		C TUR L	Tape Unit Ready
F1	R		C RD0 L	Read bit 0 from tape unit
H1	T		C RD1 L	Read bit 1 from tape unit
J1	V		C RD2 L	Read bit 2 from tape unit
K1	X		C RD3 L	Read bit 3 from tape unit
L1	Z		C RD4 L	Read bit 4 from tape unit
M1	BB		C RD5 L	Read bit 5 from tape unit
N1	DD		C RD6 L	Read bit 6 from tape unit
P1	FF		C RD7 L	Read bit 7 from tape unit
R1	JJ		C RDP L	Read Parity bit
S1	LL		C FMK L	File Mark (end of file)
D2		L	C WRS L	Write Strobe indicates data on CWD lines has been written on tape
E2		N	C CRCS L	CRC strobe, appears with CRC character
F2		R	C RWS L	Tape Rewinding
K2		X	C BOT L	Beginning of Tape
L2		Z	C WRL L	Write Lock prevents writing on tape
M2		BB	C VPE L	Vertical Parity Error
N2		DD	C SELR L	Existing transport is on line
P2		FF	C 7CH L	7 channel asserted when 7 channel tape unit is selected
R2		JJ	C EOT L	End of Tape
S2		LL	C CRCE L	CRC Error
T2		NN	C LRCE L	LRC Error
U2		RR	C LRCS L	LRC strobe appears with the LRC character

Table 9-7
TM8-E M8321 Output Control Module Top Connector Signals

To M8327 Connector F		To M8327 Connector H	
Signal	Pin No.	Signal	Pin No.
Not used	A1	CB-2 MAC 2 H	A1
OC-2 RWCR L	B1	RE-1 SEL 16 H	B1
RE-1 DB7 H	C1	RE-1 PEVN H	C1
RE-1 FR0 H	D1	SC-1 SET H	D1
RE-1 DB5 H	E1	Not used	E1
CB-1 WR 1st 7 H	F1	RE-1 DB8 H	F1
Not used	H1	Not used	H1
RE-1 DB3 H	J1	RE-1 DB9 H	J1
RE-1 DB2 H	K1	Not used	K1
Not used	L1	RE-1 DB10 H	L1
CB-3 MTTF L	M1	Not used	M1
SC-2 ERROR L	N1	CB-1 WR 2nd 7 H	N1
OC-2 LCAR L	P1	RE-1 DEN 8 H	P1
SC-1 TUR L	R1	RE-1 FR1 H	R1
OC-2 LCMR L	S1	RE-1 FR2 H	S1
CB-3 CLR ALL L	T1	OC-2 CWCR L	T1
OC-2 LCM/F/DB H	U1	OC-2 RMSR L	U1
OC-2 LFGR L	V1	OC-2 RCAR L	V1
Not used	A2	Not used	A2
Not used	B2	Not used	B2
RE-1 DB6 H	C2	CB-1 WDR H	C2
Not used	D2	Not used	D2
OC-1 R/C ERROR L	E2	CB-3 INIT H	E2
RE-1 CB1 H	F2	RE-1 BSEL2 H	F2
OC-2 LWCR L	H2	RE-1 BSEL1 H	H2
OC-1 RDB L	J2	RE-1 BSEL0 H	J2
RE-1 DB0 H	K2	CB-1 WR9 H	K2
OC-2 CCAR L	L2	RE-1 DB11 H	L2
RE-1 FR3 L	M2	RE-1 DEN5 H	M2
OC-2 IBCM L	N2	OC-2 AC ENABLE L	N2
OC-2 CLF L	P2	OC-2 B TP3 H	P2
SC-1 CONTROL BSY L	R2	OC-2 RFSR L	R2
OC-2 SBRM L	S2	OC-2 RCMR L	S2
OC-2 LDBR L	T2	RE-1 DB4 H	T2
Not used	U2	Not used	U2
Not used	V2	Not used	V2

Table 9-8
TM8-E M8322 Control Module, Top Connector Signals

To M8327 Connector E		To M8323 Connector F		To M8323 Connector H		To M8327 Connector J	
Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.
SC-2 RD3 H	T1	SC-1 PRESET H	T1	CB-1 SP REV L	T1	CB-1 WR 2nd 7 H	T1
SC-2 RDP H	U1	SC-1 TUR L	U1	CB-1 REWIND L	U1	CB-3 CLR ALL L	U1
SC-2 RD5 H	V1	SC-1 FM L	V1	CB-1 BRK RQST H	V1	CB-1 WR 1st 7 H	V1
Not used	A2	SC-1 Test	A2	Not Used	A2	Not used	A2
Not used	B2	Not used	B2	Not used	B2	Not used	B2
SC-1 CONTROL BSY L	C2	SC-1 SDWN L	C2	RE-1 DEN 8 H	C2	RE-1 EMA INC ENABLE L	C2
OC-2 IBCM L	D2	CB-2 CHG DIR L	D2	OC-2 RMSR L	D2	CB-2 DBC 1 L	D2
SC-1 TUR L	E2	SC-2 RDP H	E2	OC-1 RC ERROR L	E2	RE-1 DEN 5 L	E2
SC-1 EMA INC L	F2	SC-2 RD5 H	F2	OC-2 LCM/F/DB H	F2	OC-2 RFSR L	F2
SC-2 RD0 H	H2	SC-2 RD3 H	H2	RE-2 EMA 7	H2	SC-2 RD4 H	H2
Not used	J2	SC-2 RD2 H	J2	SC-1 COUNT CA L	J2	CB-3 MTTF L	J2
SC-1 7 CHANNEL H + DEN 5 L	K2	RE-2 CA0 L	K2	RE-2 GO H	K2	RE-1 GO H	K2
SC-2 RD7 H	L2	SC-1 RD7 H	L2	SC-2 RD4 H	L2	RE-2 EMA 7 H	L2
RE-1 B SEL1 H	M2	SC-2 RD1 H	M2	OC-2 RFSR L	M2	CB-2 MAC 2 H	M2
RE-1 B SEL0 H	N2	Not used	N2	RE-1 DEN 5 H	N2	RE-1 F2 H	N2
CB-2 DBC 2 L	P2	SC-2 RD0 H	P2	RE-1 EMA INC ENABLE L	P2	RE-1 FR0 H	P2
RE-2 WCO L	R2	SC-1 EMA INC L	R2	RD6 H	R2	RE-1 FR1 H	R2
OC-2 LDBR L	A1	SC-2 ERROR L	A1	CB-1 R/RC H	A1	SC-2 RD6 H	A1
OC-2 SBRM L	B1	SC-1 DATA LATE L	B1	RE-1 WR/WFM	B1	CB-1 CONT WC L	B1
CB-1 WDR L	C1	CB-3 CLR STATUS L	C1	CB-2 R/RCAFT WR	C1	CB-2 MAC1 H	C1
OC-2 CLF L	D1	CB-1 OFF LINE	D1	Not used	D1	OC-2 LCMR L	D1
SC-1 SET H	E1	CB-2 BTP3 H	E1	Not used	E1	RE-1 SEL 16 H	E1
RE-1 ENABLE CHECK CHAR L	F1	CB-1 SPACE H	F1	SC-1 RDS · R + RCH	F1	RE-1 IEEF	F1
SC-2 RD1 H	H1	CHG TRANS L	H1	SC-1 WRS H	H1	RE-1 IEMF	H1
SC-2 ERROR L	J1	SC-2 EOT L	J1	CB-1 WCOV H	J1	SC-1 COUNT CA L	J1
RE-1 SEL0 H	K1	CB-3 MTTF L	K1	SC-1 SET H	K1	Not used	K1
RE-1 SEL1 H	L1	Not used	L1	SC-2 B LRCS L	L1	Not used	L1
CB-3 LBC M L	M1	SC-2 REWINDING L	M1	CB-2 MAC ACC L	M1	CB-1 WR9 H	M1
RE-1 B SEL 0 H	N1	SC-2 BOT L	N1	SC-1 7 CHANNEL + DEN 5 L	N1	OC-2 LCM/F/DB H	N1
RE-2 CA 0 L	P1	CB-3 SEL ERROR L	P1	CB-3 BTP4 H	P1		P1
SC-2 RD2 H	R1	SC-1 WRS L	R1	CB-3 CLR ALL	R1	OC-1 RC ERROR L	R1
CB-2 DB MPX B H	S1	SC-1 SELR L	S1	SC-1 RECORD LENGTH INCORRECT H	S1	OC-2 RMSR L	S1
RE-1 DBC 1 H	S2	OC-2 IBCM L	S2	Not used	S2	CB-3 INIT H	S2
CB-2 CB MPX A H	T2	CONTROL BSY H	T2	SC-2 SP REV · BOT H	T2	RE-1 DEN 8 H	T2
Not used	U2	Not used	U2	Not used	U2	Not used	U2
Not used	V2	Not used	V2	Not used	V2	Not used	V2

Table 9-9
TM8-E M8327 Register Module, Top Connector Signals

To M8322 Connector E		To M8321 Connector F		To M8321 Connector H		To M8322 Connector J	
Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.
OC-2 LDBR L	A1	Not used	A1	CB-2 MAC 2 H	A1	SC-2 RD 6 H	A1
OC-2 SBRM L	B1	OC-2 RWCR L	B1	RE-1 SEL16 H	B1	CB-1 COUNT WC L	B1
CB-1 WDR H	C1	RE-1 DB7	C1	RE-1 PEVN H	C1	CB-2 MAC 1 H	C1
OC-2 CLF L	D1	RE-1 FR0 H	D1	SC-1 SET H	D1	OC-2 LCMR L	D1
SC-1 SET H	E1	RE-1 DB5	E1	Not used	E1	RE-1 SEL16 H	E1
RE-1 ENABLE CHECK CHAR L	F1	CB-1 WR 1st 7 H	F1	RE-1 DB8 H	F1	IEEF L	F1
SC-2 RD1 H	H1	Not used	H1	Not used	H1	RE-1 IEEF L	H1
SC-2 ERROR L	J1	RE-1 DB3	J1	RE-1 DB9 H	J1	SC-1 COUNT CA L	J1
RE-1 SEL2 H	K1	RE-1 DB2	K1	Not used	K1	Not used	K1
RE-1 SEL1 H	L1	Not used	L1	RE-1 DB10 H	L1	Not used	L1
CB-3 LBCM L	M1	CB-3 MTTF L	M1	Not used	M1	CB-1 WR 9 H	M1
RE-1 B SEL0 H	N1	SC-2 ERROR L	N1	CB-1 WR 2nd 7 H	N1	OC-2 LCM/F/DB H	N1
RE-2 CAO H	P1	OC-2 LCAR L	P1	RE-1 DEN 8 H	P1	Not used	P1
SC-2 RD 2 H	R1	SC-1 TUR L	R1	RE-1 FR1 H	R1	OC-1 RC ERROR L	R1
CB-2 DB MPXB H	S1	OC-2 LCMR L	S1	RE-1 FR2 H	S1	OC-2 RMSR L	S1
SC-2 RD3 H	T1	CB-3 CLR ALL L	T1	OC-2 CWCR L	T1	CB-2 WR 2nd 7 H	T1
SC-2 RDP H	U1	OC-2 LCM/F/DB H	U1	OC-2 RMSR L	U1	CB-3 CLR ALL L	U1
SC-2 RD5 H	V1	OC-2 LFGR L	V1	OC-2 RCAR L	V1	CB-1 WR 1st 7 H	V1
Not used	A2	Not used	A2	Not used	A2	Not used	A2
Not used	B2	Not used	B2	Not used	B2	Not used	B2
SC-1 CONTROL BSY L	C2	RE-1 DB6	C2	CB-1 WR 7 H	C2	RE-1 EMA INC ENABLE L	C2
OC-2 IBCM L	D2	Not used	D2	Not used	D2	CB-2 DBC1 L	D2
SC-1 TUR L	E2	OC-1 RC ERROR L	E2	CB-3 INIT H	E2	RE-1 DEN 5 H	E2
SC-1 EMA INC L	F2	RE-1 DB1	F2	RE-1 B SEL 2 H	F2	OC-2 RFSR L	F2
SC-2 RD 0 H	H2	OC-2 LWCR L	H2	RE-1 B SEL 1 H	H2	SC-2 RD 4 H	H2
Not used	J2	OC-1 RD B L	J2	RE-1 B SEL 0 H	J2	CB-3 MTTF L	J2
SC-1 7 CHANNEL H + DEN 5 H	K2	RE-1 DB0	K2	CB-1 WR 9 H	K2	RE-1 GO H	K2
SC-2 RD 7 H	L2	OC-2 CCAR	L2	RE-1 DB11 H	L2	RE-2 EMA 7 H	L2
RE-1 B SEL 0 H	M2	RE-1 FR3 H	M2	RE-1 DEN 5 H	M2	CB-2 MAC 2 H	M2
RE-1 SEL H	N2	OC-2 IBCM	N2	OC-2 AC ENABLE L	N2	RE-1 FR2 H	N2
CB-2 DBC 2 L	P2	OC-2 CLF	P2	OC-2 BTP 3 H	P2	RE-1 FR0 H	P2
RE-2 WCO H	R2	SC-1 CONTROL BSY	R2	OC-2 RFSR L	R2	RE-1 FR1 H	R2
RE-1 DBC 1 H	S2	OC-2 SBRM	S2	OC-2 RCMR L	S2	CB-3 INIT H	S2
CB-2 DB MPX A H	T2	OC-2 LDBR	T2	RE-1 DB4 H	T2	RE-1 DEN 8 H	T2
Not used	U2	Not used	U2	Not used	U2	Not used	U2
Not used	V2	Not used	V2	Not used	V2	Not used	V2

Table 9-10
TM8-E M8323 Transport Status and Control Module, Top Connector Signals

To M8322 Connector F		To M8322 Connector H	
Signal	Pin No.	Signal	Pin No.
CB-1 R/RC H	A1	SC-2 ERROR L	A1
RE-1 WR/WFM	B1	SC-1 DATA LATE L	B1
R/RC AFT WR	C1	CB-3 CLR STATUS L	C1
Not used	D1	CB-1 OFF LINE L	D1
Not used	E1	CB-2 B TP 3 H	E1
SC-1 RDS · R + RCH	F1	CB-1 SPACE H	F1
SC-1 WRS H	H1	CB-3 CHG TRANS L	H1
CB-1 WCOV H	J1	SC-2 EOT L	J1
SC-1 SET H	K1	CB-3 MTTF L	K1
SC-2 B LRCS L	L1	Not used	L1
CB-2 MAC ACC L	M1	SC-2 REWINDING L	M1
SC-1 7 CHANNEL + DEN 5 L	N1	SC-2 BOT L	N1
CB-3 BTP4 H	P1	CB-3 SEL ERROR L	P1
CB-3 CLR ALL	R1	SC-1 WRS L	R1
SC-1 RECORD LENGTH INCORRECT H	S1	SC-1 SELR L	S1
CB-1 SP REV L	T1	SC-1 PRESET H	T1
CB-1 REWIND L	U1	SC-1 TUR L	U1
CB-1 BRK RQST H	V1	SC-1 FM L	V1
Not used	A2	SC-1 Test	A2
Not used	B2	Not used	B2
RE-1 DEN 8 H	C2	SDWN L	C2
OC-2 RMSR L	D2	CB-2 CHG DIR L	D2
OC-1 RC ERROR	E2		
OC-2 LCM/F/DB H	F2	SC-2 RDP H	E2
RE-2 EMA 7 L	H2	SC-2 RD 5 H	F2
SC-1 COUNT CA L	J2	SC-2 RD 3 H	H2
RE-2 GO H	K2	SC-2 RD 2 H	J2
SC-2 RD 4 H	L2	SC-1 RD 7 H	L2
OC-2 RFSR L	M2	SC-2 RD 1 H	M2
RE-1 DEN 5 H	N2	Not used	N2
RE-1 EMA INC ENABLE L	P2	SC-1 RD 0 H	P2
SC-2 RD 6 H	R2		
Not used	S2	SC-1 EMA INC L	R2
SC-2 SP REV BOT H	T2	OC-2 LBCM L	S2
Not used	U2	SC-1 CONTROL BSY H	T2
Not used	V2	Not used	U2
		Not used	V2

9.8 BLOCK DIAGRAM DESCRIPTION

Figure 9-6, a block diagram of the TM8-E DECmagtape Control, depicts the flow of signals between the modules, OMNIBUS, and the TU10 DECmagtape Master System and slaves. The modules are inserted into the OMNIBUS and signals are carried between the modules by H851 Top Connectors. The TM8-E is connected to the TU10 DECmagtape System by two BC08-L cables. The TM8-E modules are described in the following paragraphs.

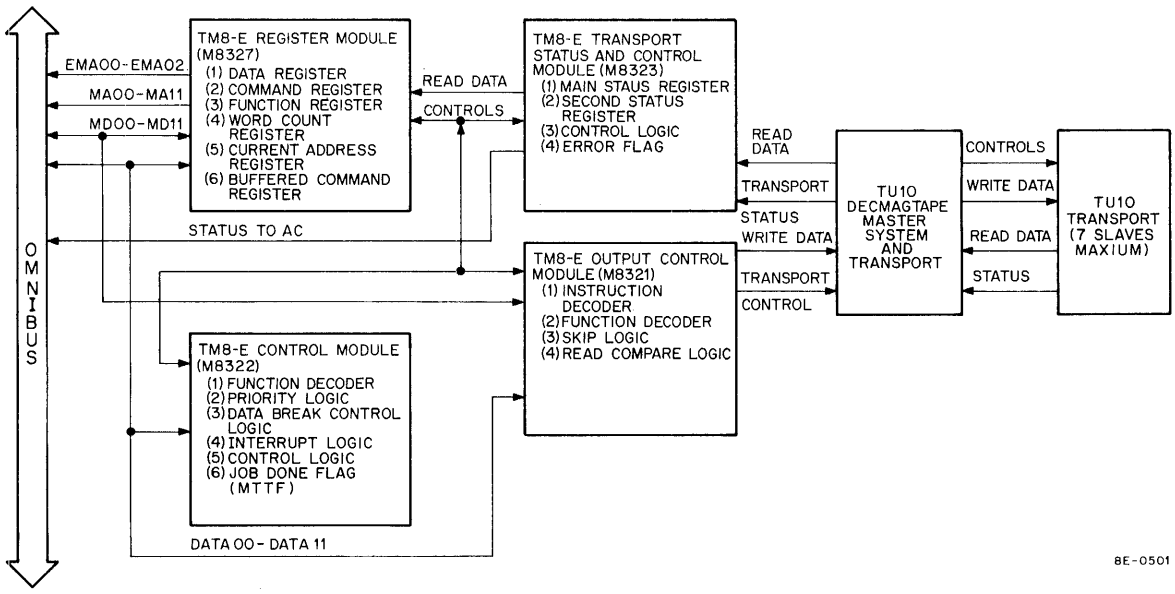


Figure 9-6 TM8-E Block Diagram

9.8.1 M8321 Output Control Module

The M8321 Output Control Module comprises three IOT instruction decoders, a Function Decoder, Read/Compare Error detection logic, buffers, gating logic to multiplex data to be written on DECmagtape during a Write operation, and Skip logic.

9.8.1.1 IOT Instruction Decoder – The three decoders (device codes 70, 71, and 72) provide control signals in response to the IOT instructions listed in Paragraph 9.9. The IOT decoders generate control signals that are distributed to the logic of the other TM8-E modules to control data transfer between the TU10 DECmagtape and core memory. The control signals also control the loading and reading of TM8-E Registers and enable the error detection logic to monitor data transfer operations.

9.8.1.2 Function Decoder – The Function Decoder receives three function bits from the Function Register and decodes them to select one of the following DECmagtape functions (Paragraph 9.8.2.3).

a.	Offline	*e.*	Write
b.	Rewind	*f.*	Write End of File
c.	Read	*g.*	Space Forward
d.	Read/Compare	*h.*	Space Reverse

The function signals generated by the Function Decoder are sent to the TU10 DECmagtape Master System to control the selected TU10 DECmagtape.

9.8.1.3 Gating Logic – The WD bits are gated to the Write Data Buffers in response to control signals from the TM8-E control module and transferred to the TU10 DECmagtape. On a 7-track transport, data is written on tape in two 7-bit characters (6 data bits plus parity); on a 9-track transport, data is written in 9-bit characters (8 data bits plus parity). Parity for each character is generated in the TU10 by the Master System.

9.8.1.4 Read/Compare Error Detection Logic – The Read/Compare error detection logic compares data read from the DECmagtape with data in memory during the Break cycle and generates a Read/Compare error if the data is different. This operation is accomplished by Exclusively-ORing the memory data with the data read from the DECmagtape. Note the parity bit is not checked by Read/Compare.

9.8.1.5 Skip Logic – The Skip logic grounds the Skip line and causes the program to skip the next instruction when the following conditions exist:

a. Tape Unit Ready (TUR) and an SKTR instruction is executed by the program.
b. ERROR flag is set and an SKEF instruction is executed by the program.
c. Control not busy and an SKCB instruction is executed by the program.
d. JOB DONE (MTTF) is set and an SKJD instruction is executed by the program.

This logic is used by the programmer for flag and error checking operations.

9.8.2 M8327 Registers Module

The M8327 Registers Module contains all of the TM8-E registers except the Main Status Register and Second Status Register. Each of the registers on the M8327 module is described in the following paragraphs.

9.8.2.1 Multiplexer and Data Register – The Multiplexer and Data Register stores information to be multiplexed to or from the transport or OMNIBUS. It accomplishes this task in the following manner:

a. It receives data to be written on tape from the MD lines during a Write Break cycle.
b. It receives data from the AC via IOT instructions.
c. The OMNIBUS receives data from the tape transport during a Read operation via the Data Bus.
d. The Data Register receives data from the tape transport.
e. The Master System receives data from Data Buffers during a Write Break cycle.

9.8.2.2 Command Register – The Command Register (Figure 9-7) is loaded with a 12-bit word from the AC by an LCMR instruction. The Command Register is used to select a tape transport (0–7), enable or disable interrupts, select parity mode (odd or even), select memory field, and select DECmagtape recording densities. The contents of the Command Register are transferred to the AC for program evaluation by an RCMR instruction.

9.8.2.2.1 Buffered Command Register (BCM) – The Buffered Command Register is loaded with SEL 0 through SEL 2 when LBCM is asserted by the control logic. The output of BCM (B SEL 0 through B SEL 2) is compared with SEL 0 through SEL 2 to determine when a new transport has been selected by the program. If the program selects a new transport, CHG TRANS is asserted to inform the controller that a new transport has been selected. LBCM is asserted when the following conditions exist:

a. The CHG TRANS flip-flop is set and the Rewind status from the selected transport is asserted.
b. CLR ALL is asserted.
c. At TP4 time, if any one of the following conditions exist.
    1. C TUR L asserted.
    2. C SDWN L asserted.
    3. C SELR L negated.

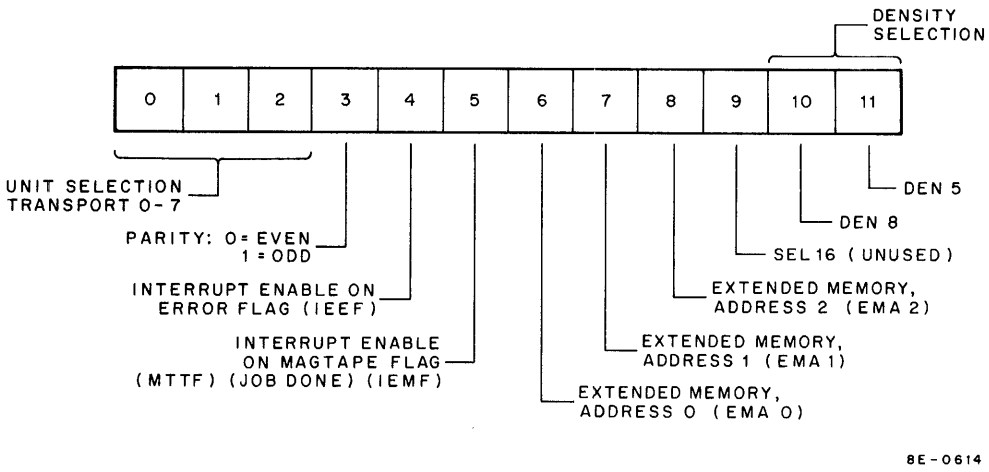


Figure 9-7 Contents of Command Register

9.8.2.3 Function Register – The Function Register (Figure 9-8) is loaded from the AC by an LFGR instruction. The three most significant bits (F0–2) are decoded by Function Decoders in the M8321 Output Control Module and the TM8-E M8322 Control Module to select the following DECmagtape functions.

Offline	Selected transport is taken OFFLINE and rewound to beginning of tape (BOT).
Rewind	The selected transport rewinds to BOT and stops.
Read	Data is transferred from tape to memory in the forward direction only.
Read/Compare	Data read from the tape is compared to data in core memory; if there is a comparison error, the Current Address (CA) Register stops incrementing and the CA Register holds the memory address in error at the end of the operation.
Write	Data is written on tape in the forward direction only.
Write End of File	The transport leaves a 3-inch gap and writes a File Mark that consists of one character followed by three character spaces and an LRC character.
Space Forward	The transport moves forward, at 45 ips, the number of records specified by the Word Count (WC) Register (Paragraph 9.8.2). If File Mark is encountered, the transport stops at IRG; if EOT is encountered, the transport stops at the next IRG.
Space Reverse	The transport spaces in reverse, at 45 ips, the number of blocks specified by the WC Register (Paragraph 9.8.2). If at the beginning of tape (BOT) a File Mark is encountered, the tape stops.

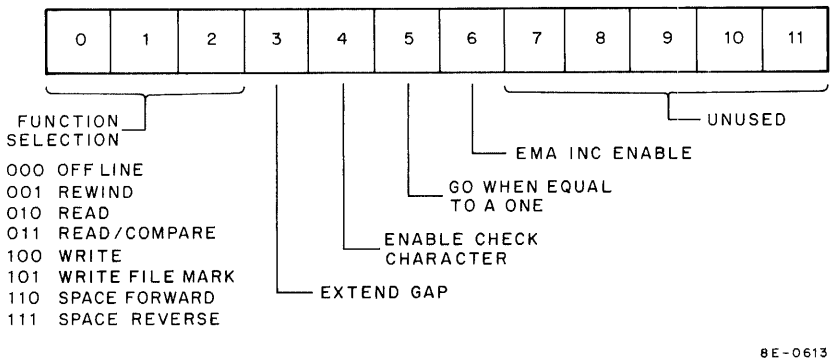


Figure 9-8 Contents of Function Register

The remaining bits of the Function Register enable the following operations if they are set by a 1 from the AC.

Extended Gap	If bit 3 is a 1, there is a 3-inch gap between records. This bit is used only during Write functions.
Enable Check Character	If bit 4 is a 1 and a 9-track transport is selected, the LRC and CRC are transferred to memory at the end of a record during Read operations. This operation is accomplished by executing two more Data Breaks after the WC Register overflows. Record Length Incorrect is disabled at this time.
Go	When bit 5 is a 1, the controller asserts GO, sets CNTL BSY (Control Busy), generates PRESET, and if no Illegal Functions exist, SET is asserted to start an operation. A GO command is issued to the transport if it is ready (TUR is true, and SELECT REMOTE is low).
EMA INC Enable	If bit 6 is a 1, the EMA bits in the Command Register and the CA Register are used as a 15-bit register to address all PDP-8/E core memory as a block instead of in 4K segments.
Continuous Operation	The MTTF (JOB DONE) signifies the end of a specified operation. If an LFGR instruction is desired immediately, prior to TUR, this instruction may be executed by the program.

9.8.2.4 Current Address Register – The CA Register is loaded from the AC by an LCAR instruction with a memory address that is one location less than the desired starting memory location. The CA Register is incremented before each data transfer to sequentially address a block of memory during a data transfer operation. The contents of the CA Register are placed on the MA lines during a Single Cycle Data Break to address memory.

9.8.2.5 Word Count Register – The WC Register counts the number of words in a block of data transferred to or from memory by the TM8-E. The 2's complement of the number of words to be transferred is loaded into the WC Register by an LWCR instruction at the beginning of a data transfer. The WC Register is incremented before each data character is transferred until the WC Register contains all 0s, causing an OVERFLOW. When the WC Register overflows, data transfer is stopped. This register is also used in spacing operations to count records to be spaced over.

9.8.3 M8323 Transport Status and Control Module

The TM8-E transport status and control logic contains the majority of the Main Status Register, the second Status Register, the Error detection logic (ERROR flag), an illegal Function detection logic, and receives Read data (RD0–RD7) from the DECmagtape before it is applied to the Data Register.

9.8.3.1 Main Status Register – The Main Status Register (Figure 9-9) retains transport status information that is transferred to the AC by an RMSR instruction for evaluation by the program.

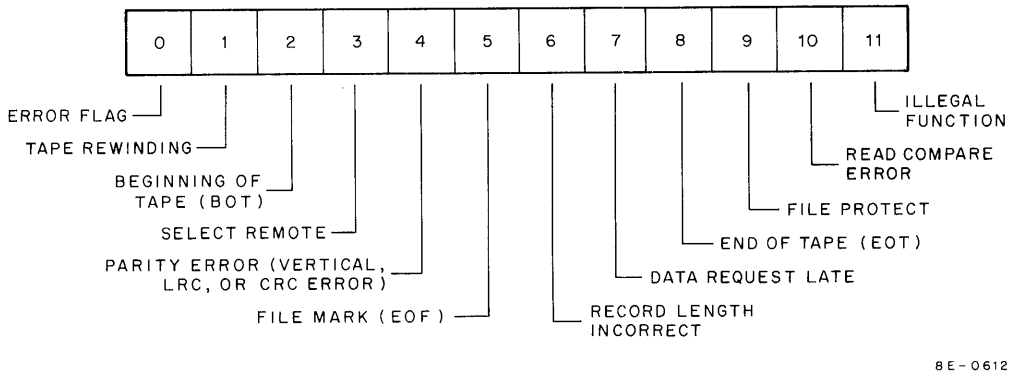


Figure 9-9 Contents of Main Status Register

9.8.3.2 Second Status Register – The Second Status Register (Figure 9-10) retains additional transport status information that is transferred to the AC by an RFSR instruction for evaluation by the program.

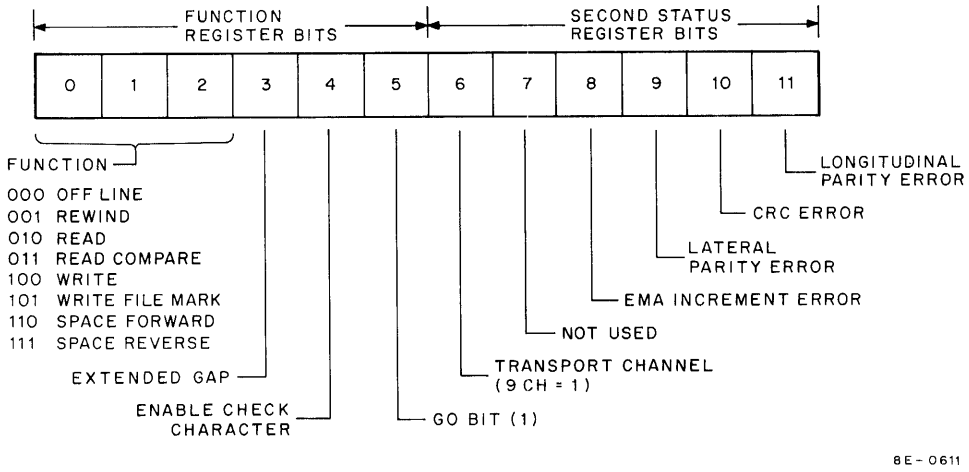


Figure 9-10 Contents of Function and Second Status Register

9.8.3.3 ERROR Flag – The ERROR flag is set by any one of the following error conditions:

a. End of Tape (EOT)
b. Read/Compare (R/C) ERROR
c. Parity Error
d. Beginning of Tape (BOT)
e. EMA 7 INC ERR
f. RECORD LENGTH INCORRECT
g. DATA LATE
h. ILLEGAL FUNCTION
i. FILE MARK

9.8.3.4 Illegal Function Detection – The ILLEGAL FUNCTION flag sets, setting the ERROR flag, if any of the following are attempted:

a. A Rewind is attempted when tape is at BOT.

b. A Space Reverse is attempted when tape is at BOT.

c. An attempt is made to select other than 800 bpi density on 9-track transports.

d. An attempt is made to Read after Write on the same transport.

e. IOTs are executed to load the Data Buffer Register, Command Register, or Function Register while the Control is busy.

f. Issue a Write or Write File Mark to a tape transport with the Write Ring removed.

g. An attempt is made to start an operation when the following conditions exist:

1. CHG TRANSPORT L is true.
2. TUR H is true.
3. PRESET is true.

9.8.3.5 PRESET and SET Pulse Generator – PRESET is a fixed delay that is generated to allow adequate time for interrogation of the control in order to check for errors and illegal functions prior to asserting the SET pulse. If there are no illegal functions or errors, the SET pulse is asserted, thus asserting the C SET H signal to the tape transport and starting tape motion.

9.8.3.6 Control Busy (CNTL BSY) – CNTL BSY is set when the GO bit is issued to indicate that an operation is pending.

9.8.4 M8322 Control and Data Break Module

The M8322 Control and Data Break Module comprises the Data Break Control logic, a Control Function Decoder, and the Interrupt logic.

9.8.4.1 Data Break Control Logic – The Data Break Control logic allows the TM8-E to transfer large blocks of data between the TU10 DECmagtape and memory. When the TM8-E asserts BRK RQST, a priority check is made by the controller. A priority network on the M8322 module is compared with priorities of other peripherals requesting a data break and, if the TM8-E has the highest priority, the Break Control allows the TM8-E to assert the Break Control lines. This action enables the TM8-E to assume control of the CP Major Register gating and to address memory using the Current Address logic and Data Break Control logic. When BRK RQST is granted by the TM8-E,

data is transferred from the TM8-E Data Register to the Data Bus (read) or from the MD lines to the M8321 Output Control Module (Write or Read/Compare). The TM8-E is is capable of one Single Cycle Data Break approximately every 28 μs until a complete record is transferred to or from memory. The CRC and LRC characters are also transferred to memory during a Read operation if the ENABLE CHECK CHARACTER bit in the Function Register is set.

9.8.4.2 Function Decoder – The Control Function Decoder decodes FR0–FR2 from the Function Register and generates the same function as the Output Control Function Decoder on the M8321 Output Control Module (Paragraph 9.8.1.2). The outputs of this Function Decoder are applied to the control logic on the control module. The FR0–FR2 function bits are applied to the Control Function Decoder from the Function Register.

9.8.4.3 Interrupt Logic – The Interrupt logic on the TM8-E control module generates an interrupt request (INT RQST) when the following conditions exist (Table 9-11):

a. Bit 4 in the Command Register (IEEF) is set (1) and the ERROR flag is set.
b. Bit 5 in the Command Register (IEMF) is set (1) and the JOB DONE flag (MTTF) is set.

Table 9-11
Command Register Contents and Function

Bit No.			Function
Bits 0, 1, and 2			
SEL 0 (Bit 0)	SEL 1 (Bit 1)	SEL 2 (Bit 2)	
0	0	0	Transport 0
0	0	1	Transport 1
0	1	0	Transport 2
0	1	1	Transport 3
1	0	0	Transport 4
1	0	1	Transport 5
1	1	0	Transport 6
1	1	1	Transport 7
Bit 3			0 = Even Parity; 1 = Odd Parity
Bit 4			If bit 4 is a 1, enable interrupt ERROR flag.
Bit 5			Enable interrupt on JOB DONE (MTTF) if bit 5 is a 1.
Bits 6, 7, and 8			Extended Memory Address (EMA), these bits determine which memory field the controller uses for data transfer operations during a Data Break. Function Register bit 6 (Table 9-12) determines if the EMA address is to be incremented or used in the wrap-around mode.

Table 9-11 (Cont)
Command Register Contents and Function

Bit No.			Function
Bit 6 (EMA 0)	Bit 7 (EMA 1)	Bit 8 (EMA 2)	
0	0	0	Field 0
0	0	1	Field 1
0	1	0	Field 2
0	1	1	Field 3
1	0	0	Field 4
1	0	1	Field 5
1	1	0	Field 6
1	1	1	Field 7
Bit 9			Reserved for future use.
Bits 10 and 11			Density bits, these bits select the density for tape transport operation and are referred to as Den 8 (bit 10) and Den 5 (bit 11).
Bit 10 Den 8	Bit 11 Den 5		
0	0		200 bpi, 7 track
0	1		556 bpi, 7 channel
1	0		800 bpi, 7 channel*
1	1		800 bpi, 9 channel

*This mode is also referred to as Core Dump Mode. When this command is issued to a 9-track transport, zeroes are written on tracks 0 and 1 of the DECmagtape and the 9-track transport operates as a 7-track transport.

9.9 INSTRUCTIONS AND STATUS BITS

The following instructions are used to program the TM8-E. Refer to the appropriate table for the status bits associated with each instruction.

Load Word Count Register (LWCR)

Octal Code: 6701

Operation: Loads the WC Register with the contents of the AC (Figure 9-11) and clears the AC. The WC Register should not be loaded when the control is busy. If the register is loaded during CNTL BSY, data reliability and tape compatibility are not ensured. The WC Register is loaded with the 2's complement of the number of words to be transferred or number of blocks to be spaced. The WC Register is incremented at TP1 of a Data Break cycle during data transfers, at LRCS during a Space Forward, or at the first word of a record during a Space Reverse operation.

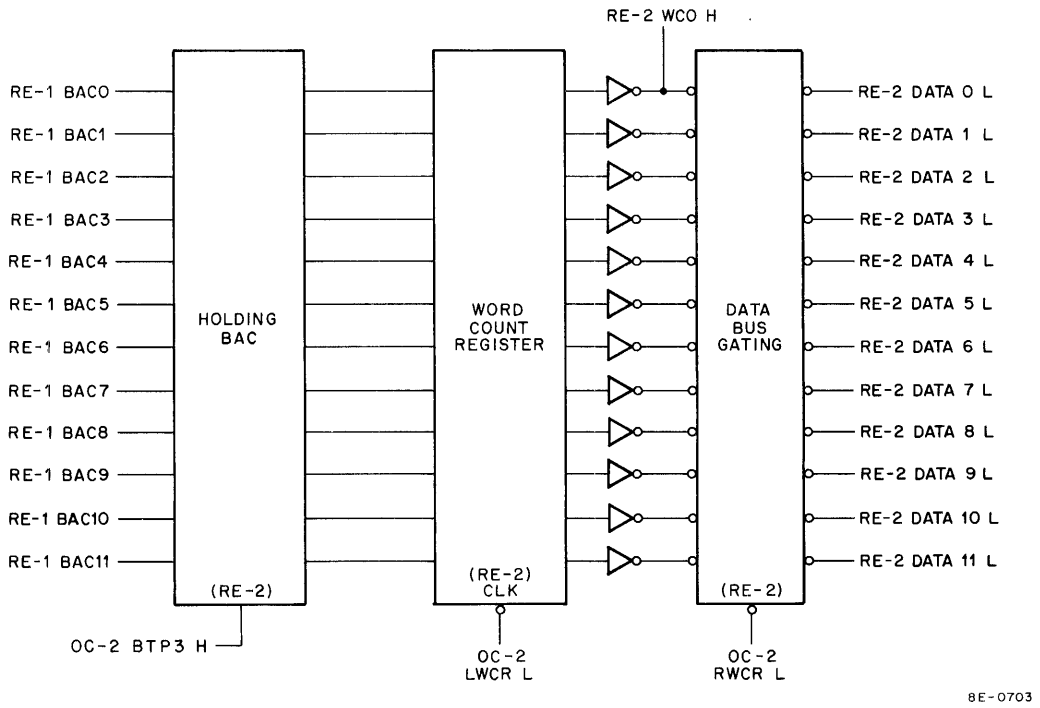


Figure 9-11 LWCR and RWCR Instruction Data Flow

Clear Word Count Register (CWCR)

Octal Code: 6702

Operation: Clears the WC Register. This instruction is used primarily in maintenance operations and should never be used during CNTL BSY.

Load Current Address Register (LCAR)

Octal Code: 6703

Operation: Loads the CA Register with the contents of the AC (Figure 9-12) and clears the AC. The CA Register is loaded to one less than the memory address of the first word to be transferred. If this instruction is executed during CNTL BSY, one of the following occurs:

1. In the wrap-around modes (Function bit 6 = 0), the location of the data transfer cannot be ensured within the selected memory field.

2. In the EMA INC ENABLE mode (Function bit 6 = 1), the location of the data transfer cannot be ensured within memory.

The CA Register is incremented at each BRK RQST.

Clear Current Address Register (CCAR)

Octal Code: 6704

Operation: Clears the CA Register. This instruction is used primarily for maintenance and should never be used during CNTL BSY.

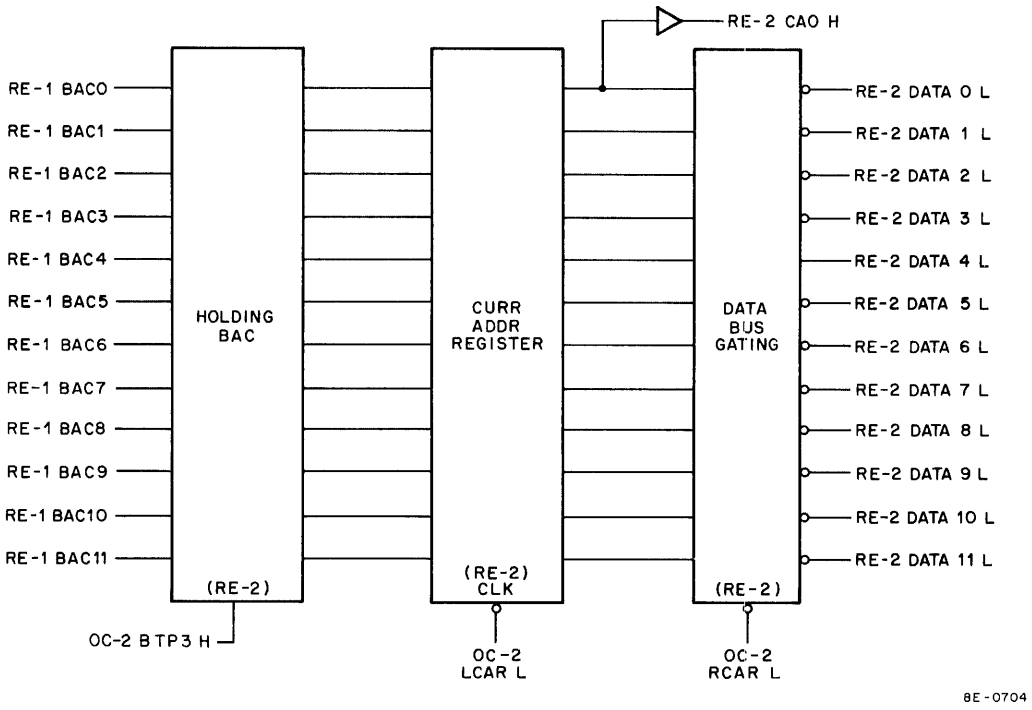


Figure 9-12 LCAR and RCAR Instruction Data Flow

Load Command Register (LCMR)

Octal Code: 6705

Operation: Loads the Command Register with the contents of the AC and clears the AC (Figure 9-13). This instruction must not be issued during CNTL BSY. The LCMR instruction selects tape transport, Parity mode, memory field, recording densities, and enables or disables interrupts (Table 9-11 and Figure 9-7).

Load Function Register (LFGR)

Octal Code: 6706

Operation: Loads the Function Register with the contents of the AC and clears the AC (Figure 9-14). The Function Register is the last register loaded because it contains the GO bit. This instruction determines the function the transport is to perform (Table 9-12 and Figure 9-8).

Load Data Buffer Register (LDBR)

Octal Code: 6707

Operation: Loads the Data Buffer Register with the contents of the AC, clears the AC, and sets the MTTF flag (Figure 9-15). This instruction is used for maintenance purposes.

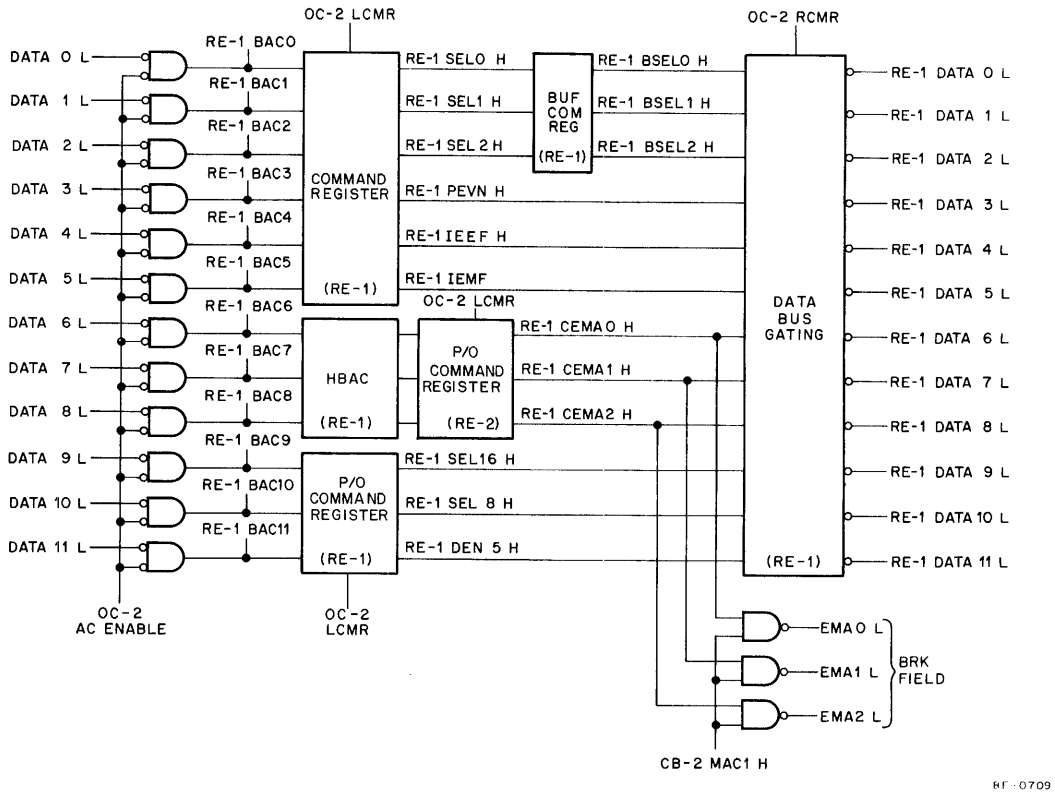


Figure 9-13 LCMR and RCMR Instruction Data Flow

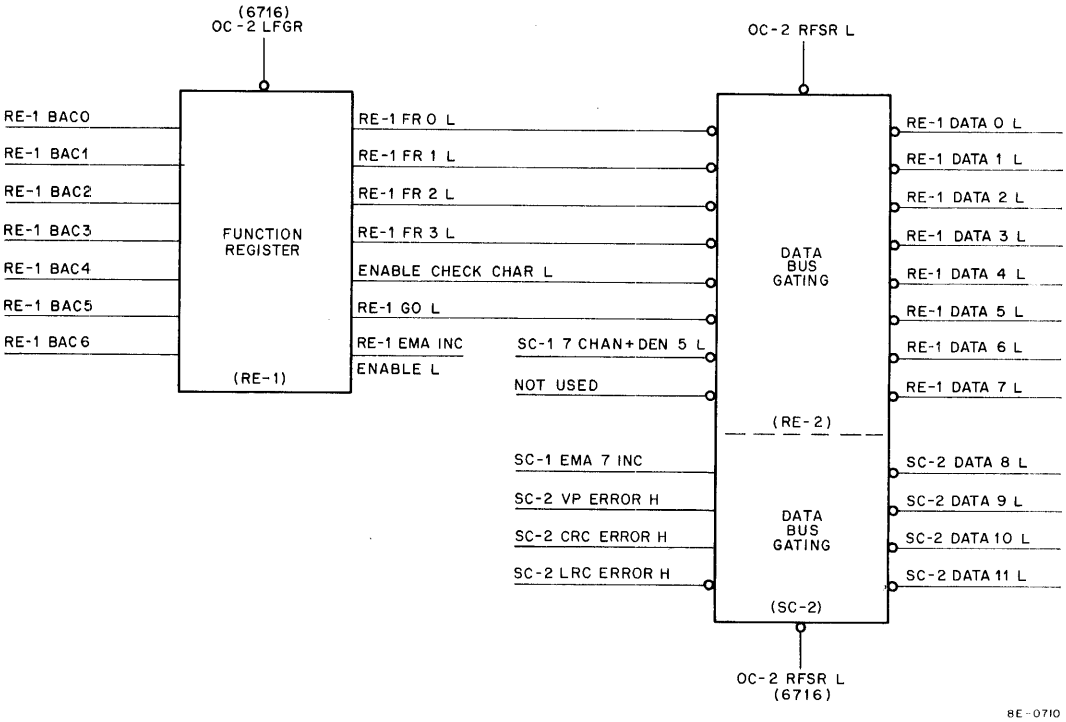


Figure 9-14 LFGR and RFSR Instruction Data Flow

Table 9-12
Function Register Contents and Functions

Bit No.			Function
Bit 0, 1, and 2			Function Selection: These bits determine the function the transport is to perform.
Bit 0	Bit 1	Bit 2	
0	0	0	Offline: The selected transport is taken Offline and rewound to BOT. The MTTF is set when the transport responds to this function and the controller can select and use another transport. The transport must be manually reset to the on-line state. The WC and CA Registers need not be loaded.
0	0	1	Rewind: The transport rewinds at high speed (150 ips) to BOT and stops. The MTTF is set when the transport responds to the Rewind function. The controller can select and use another transport. The WC and CA Registers need not be loaded.
0	1	0	Read: Data is transferred from the tape to memory in the forward direction only. All registers must be loaded.
0	1	1	Read/Compare: Tape data is compared to data in core memory. All registers must be loaded. If there is a comparison error, CA incrementation ceases, the R/C ERROR bit is set, and tape motion continues to the end of the record. The CA Register contains the address of the word that produced the error.
1	0	0	Write: Data is written on the tape in the forward direction only. All registers must be loaded. The Write function is controlled by WC OVERFLOW (which disables the Write); the transport writes the appropriate check characters to end the block.
1	0	1	Write End of File (File Mark): The transport writes the File Mark, which consists of a one word record. The CA and WC Registers need not be loaded.
1	1	0	Space Forward: The tape moves forward at 45 ips the number of records specified by the WC Register, or until a File Mark is read. If EOT is read, Space Forward stops at the first interrecord gap. The CA Register need not be loaded for Space Forward to occur.

Table 9-12 (Cont)
Function Register Contents and Functions

Bit No.			Function
Bit 0, 1, and 2 (Cont)			
Bit 0	Bit 1	Bit 2	
1	1	1	Space Reverse: The tape moves in the reverse direction at 45 ips the number of blocks specified by the WC Register, or until a File Mark or BOT marker is read. The CA Register need not be read during a Space Reverse.
Bit 3			Extended Gap: When bit 3 is a 1, the transport writes with an additional 3-inch gap between records.
Bit 4			Enable Check Character: When this bit is set (1) and a 9-track transport is selected, it allows the check characters to be read into the computer during a Read function. When the Word Count overflows, this bit allows two breaks during 9-track operation for the CRC and LRC to be transferred to memory. If a Record Length Incorrect error occurs, the check character is considered bad and is not used. This bit is used primarily for 9-track error correction.
Bit 5			Go: This bit causes the controller to issue a Set command to the transport when the transport is capable of accepting it. The Set command is not issued if the specified function is illegal.
Bit 6			EMA INC Enable: If this bit is not set (0), the TM8-E (like all other PDP-8 data break options) treats the extended memory the same way, i.e., each 4K block is used in a wrap-around mode. If this bit is set (1), the extended memory is treated as a continuous memory rather than 4K blocks. When the last location in one field is reached, the EMA bits are incremented and the transfer continues in the next field; i.e., if a word is placed in Field 2, location 7777, the following word is placed in Field 3, location 0000 if the EMA increment bit is set. If bit 6 is not set, the word is placed in Field 2, location 0000.

Table 9-12 (Cont)
Function Register Contents and Functions

Bit No.	Function
Bit 6 (Cont)	In both modes of operation, the Current Address is set to one less than the first location to be accessed. In EMA increment mode, the 12-bit CA Register and the three EMA bits are treated as one 15-bit register with the EMA bits most significant. For example, to access Field 2, location 20, load EMA = 2 and CA = 0017; to access Field 2, location 0, load EMA = 1 and CA = 7777. If Field 7 is selected, the EMA cannot increment, but wraps around in Field 7 and an EMA 7 INCREMENT ERROR occurs.

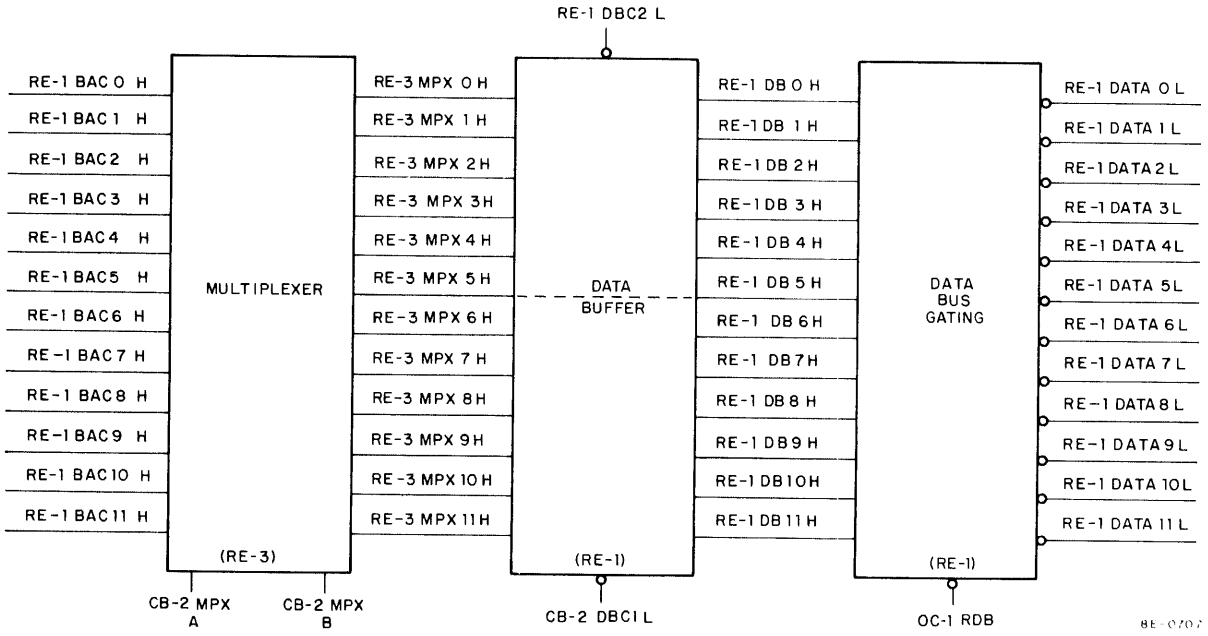


Figure 9-15 LDBR and RDBR Instruction Data Flow

Read Word Count Register (RWCR)

Octal Code: 6711

Operation: Clears the AC and transfers the contents of the WC Register into the AC (Figure 9-11). This instruction is used primarily for maintenance, but it can also be used during error check routines.

Clear Transport (CLT)

Octal Code: 6712

Operation: Clears the transport master registers and all TM8-E registers and flags.

Read Current Address Register (RCAR)

Octal Code: 6713

Operation: Clears the AC and transfers the contents of the CA Register to the AC (Figure 9-12). This instruction is used primarily for maintenance, but it can be used for error check routines.

Read Main Status Register (RMSR)

Octal Code: 6714

Operation: Clears the AC and transfers the contents of the Main Status Register to the AC (Figure 9-16). The 12-bit Status Register contains the status of the transport and control logic (Table 9-13 and Figure 9-9).

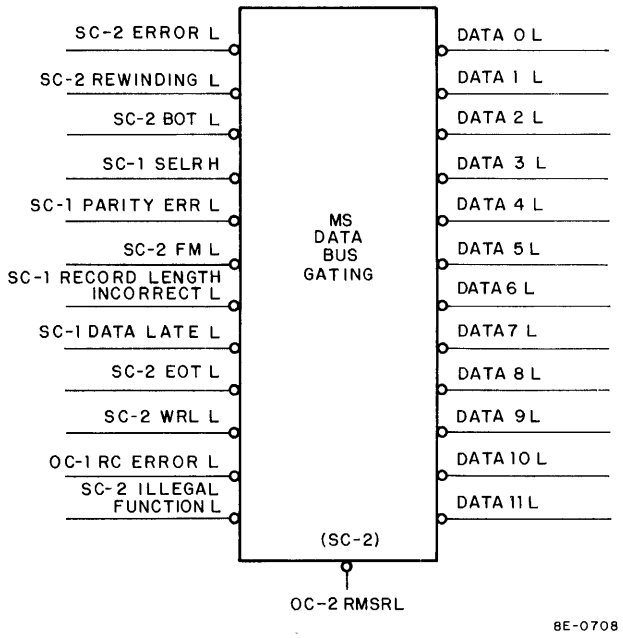


Figure 9-16 RMSR Instruction Data Flow

Read Command Register (RCMR)

Octal Code: 6715

Operation: Clears the AC and transfers the contents of the Command Register to the AC. The contents of the Command Register for this instruction are the same as that for the Load Command Register instruction shown in Table 9-11 and Figure 9-7.

Table 9-13
Main Status Register Contents and Indications

Bit No.	Status Indication
0	Error: The ERROR flag interrupts the processor if bit 4 in the Command Register is set (1). An ILLEGAL FUNCTION or SELECT ERROR sets the MTTF flag immediately and stops Data Break operations. The following errors, if they occur during any operation, set the ERROR flag after the MTTF flag is set. a. BOT b. EOT c. READ/COMPARE ERROR d. Parity Error (VPE, CRCE, or LRCE) e. RECORD LENGTH INCORRECT f. File Mark (EOF) g. DATA LATE h. EMA 7 INCREMENT ERROR
1	Rewind Status (RWS): A 1 indicates the selected transport is rewinding.
2	Beginning of Tape (BOT): A 1 indicates the BOT reflective strip is sensed by the selected transport.
3	Select Remote: A 1 indicates the selected transport is not on-line.
4	Parity Error: A 1 indicates a longitudinal parity error, vertical parity error, or CRC error has been detected.
5	File Mark (FMK): A 1 indicates the selected transport has detected a File Mark during a Write FMK, Space, Read, or Read/Compare operation.
6	Record Length Incorrect: A 1 indicates that during a Read or Read/Compare operation, the record length was different from the contents of the WC Register. The WC Register is read to determine whether the record was long or short.
7	Data Request Late: A 1 indicates the computer failed to service the BRK RQST before the next data transfer to or from the transport.
8	End of Tape (EOT): A 1 indicates the EOT reflective strip has been sensed by the selected transport.
9	File Protect: A 1 indicates the selected transport has a write lockout ring removed, and no write functions are accepted.
10	R/C ERROR: A 1 indicates a comparison failure occurred during the Read/Compare function. The CA Register contains the address of the word that produced the error.

Table 9-13 (Cont)
Main Status Register Contents and Indications

Bit No.	Status Indication
11	A 1 indicates one of the following Illegal Functions has been programmed. 1. Execution of LCMR, LFGR, or LDBR while the control is busy. 2. Specifying any density but 800 bpi for a 9-track transport. 3. A Space Reverse function when the transport is at BOT. 4. Read, Read/Compare, or Space Forward after a Write or Write End of File (WEOF) command on same transport. 5. Changing to transports that are not ready (TUR is false). 6. Attempting to rewind when tape is at BOT.

Read Function Register and Second Status Register (RFSR)

Octal Code: 6716

Operation: Clears the AC and transfers the contents of the Function Register and Second Status Register to the AC (Figure 9-14). The contents of the Second Status Register and Function Register are shown in Table 9-14.

Table 9-14
Second Status Register Contents and Functions

Bit No.	Function
7	Not used.
8	EMA 7 INC ERROR: EMA 7 INC ERROR occurs if an attempt is made to increment the EMA from Field 7 to Field 0. The data wraps around in Field 7.
9	Vertical Parity Error (VPE): A 1 indicates that a VPE error has been detected. This bit is set only on the character that is bad and cleared by the next good character.
10	CRC Error (CRCE): A 1 indicates a CRC error has been detected.
11	Longitudinal Parity Error (LPCE): A 1 indicates an LPCE has been detected.

Read Data Buffer Register (RDBR)

Octal Code: 6717

Operation: Clears the AC and transfers the contents of the Data Buffer Register to the AC (Figure 4-15). This instruction can be used in an error check routine to read the contents of the LRC Register.

Skip If ERROR Flag Is Set (SKEF)

Octal Code: 6721

Operation: Skip the next instruction if the ERROR flag is set.

Skip Control Not Busy (SKCB)

Octal Code: 6722

Operation: Skip the next instruction if the control is not busy. Control is busy when the transport is in a GO condition, control is not busy when MTTF is set at the End of Job (data transfer completed).

Skip Job Done (SKJD)

Octal Code: 6723

Operation: Skip the next instruction under following conditions.

a. When JOB DONE (MTTF) is set at LRCS time of a Read, Read/Compare, Write, or Write File Mark operation.

b. At the IRG following EOT, FMK, or WCOV during space operations.

c. MTTF is set by OFFLINE function, SELECT ERROR, or REWINDING status.

d. MTTF is set by an LDBR (Load Data Buffer Register) instruction.

Skip if Tape Unit Ready (SKTR)

Octal Code: 6724

Operation: Skip the next instruction if TUR is true.

Clear All Registers and Flags (CLF)

Octal Code: 6725

Operation: Clear all TM8-E registers and flags if TUR is true. If TUR is false clear MTTF, ERROR flag, and status registers.

Check for Data Late Error (CKDL)

Octal Code: 6726

Operation: Force a DATA LATE error condition during a data transfer. This instruction is used only for maintenance (Paragraph 9.13.6).

Set Break Request (SBRM)

Octal Code: 6727

Operation: Set BRK RQST for one Data Break. This instruction is used for maintenance only.

9.10 OPERATION AND PROGRAMMING

TM8-E operation and programming for each of the DECmagtape functions is described in the following paragraphs. The timing necessary to perform each function and an example of the method used to program the TM8-E are illustrated for each DECmagtape function. A flow diagram of TM8-E functions is illustrated in Figure 9-20. The logic used to accomplish these operations is discussed in Chapter 4; the signals on the timing diagrams are defined in Table 9-15.

Table 9-15
TM8-E Signals and Signal Functions

Signal	Origin	Function
BAC 0-BAC 11	Processor AC	A 12-bit data word transferred from the Processor AC to load TM8-E registers.
OC-2 AC ENABLE	M8321	AC ENABLE is asserted any time a 670X instruction is executed to enable bits on the Data Bus to be applied to the TM8-E registers.
C BOT	TU10	BOT indicates the reflective strip at the beginning of the tape is being sensed by the tape transport. If the transport is REWINDING or doing a SPACE REVERSE operation when C BOT is asserted, the transport stops.
*BREAK CYCLE L	M8322	**
* BRK IN PROG L	M8322	**
* BRK RQST	M8322	The BRK RQST flip-flop is set by an SBRM instruction or during the Write, Read, and Read/Compare operations to initiate the Single Cycle Data Break and transfer data.
RE-1 B SEL 0 RE-1 B SEL 1 RE-1 B SEL 2	M8327	RE-1 B SEL 0 through RE-1 B SEL 2 are outputs of the Buffered Command Register applied to the TU10. They are compared with RE-1 SEL 0 through RE-1 SEL 2 on the M8323 module; if they are different, the CB-2 CHG TRANS L signal is asserted.
*BUS STROBE	Processor M8323	***
OC-2 CCAR	M8321	OC-2 CCAR is asserted when a 6702 instruction is executed to clear the CA Register.
*C0 and C1	M8321	**
OC-2 CLF	M8321	Clear all Flags (CLF) is asserted when the 6725 instruction is executed to clear the TM8-E and the Transport Master System Register if tape unit is ready (TUR). If tape unit is not ready, clear status register, MTTF, and ERROR flag.

*OMNIBUS signals.
**Refer to Table 9-3, *PDP-8/E & PDP-8/M Small Computer Handbook*.
***Refer to Table 9-2, *PDP-8/E & PDP-8/M Small Computer Handbook*.

Table 9-15 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
CB-3 CLR ALL L	Processor M8322 M8321	Signal asserted by INIT from processor, SC-1 TUR AND OC-2 CLF, OC-2 CLT, and the INITIALIZE instruction to clear all TM8-E and TU10 Master System registers.
CB-3 CLR STATUS	M8322	CB-3 CLR STATUS is asserted to clear the status registers, ERROR flag, and MTTF if a CLF instruction is executed and C TUR is not asserted by the transport.
SC-1 CONTROL BSY	M8323	The Control Busy flip-flop is set by an RE-1 GO command at the Command Register (bit 5 = 1) on the next TP4 time and cleared by MTTF.
SC-1 COUNT CA L	M8323	SC-1 COUNT CA L is asserted at Break Request time. If the Read/Compare (R/C) ERROR flag is set to stop incrementing the CA Register, the address of the data that produced a Read/Compare error is left in the CA Register.
C REV H	M8321	C REV H is asserted by the Space Reverse function.
CB-2 CHG DIR L	M8322	The Change Direction flip-flop is set any time a change in direction is sensed.
C SDWN L	TU10	Tape Settling Down (C SDWN L) is asserted 2.3 ms after the MTTF flag sets for 10 ms.
C LRCS L	TU10	LRC Strobe (C LRCS) is asserted by the TU10 when a LRC character is read from the tape.
C CRCS L	TU10	CRC Strobe (C CRCS) is asserted when a CRC character is read from tape.
C VPE L	TU10	Vertical Parity Error (C VPE L) is asserted when the TU10 detects a vertical parity error to set the VPE flip-flop.
C CRCE L	TU10	Cyclic Redundancy Check Error (C CRCE L) is asserted when the TU10 detects a CRC error.
C LRCE L	TU10	Longitudinal Redundancy Check Error (C LRCE L) is asserted when the TU10 detects an LRC error.
C SELR L	TU10	Select Remote (C SELR L) is asserted when the transport is selected and on-line. Other status signals are not valid until C SELR L is asserted.
C SEL 16 H	M8327	For future use.
C FWD H	M8321	C FWD H is asserted by Read, Read/Compare, Write, Write File Mark, and Space Forward functions.

Table 9-15 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
C RWS L	TU10	Rewind Status (C RWS L) is asserted any time the selected transport is rewinding.
C CRCE	TU10	The CRC Error (CRCE) is set when the TU10 detects a CRC error.
CB-3 T INIT L	M8322	T INIT (tape initialize) is asserted by Space Reverse at BOT, Select Error, and CLR ALL L.
C INIT L	M8321	C INIT L (initialize transport) is asserted by INIT from processor.
C SET H		SET (C SET H) is generated by the TM8-E to initiate transport operation.
C REW H	M8321	C REW H is asserted when 1XXX is loaded into the Function Register and initiates the Rewind operation. The three bits are decoded by the Output Control Function Decoder and applied to the tape transport. The transport rewinds to BOT and stops.
C WDR H	M8322	Write Data Ready (C WDR H) is asserted by SC-1 SET during a Write operation and is negated when Word Count goes to zero by Word Count Overflow (CB-1 WCOV).
C WFMK H	M8321	Write File Mark (C WFMK) is asserted when 5XXX is loaded into the Function Register. The 3 bits (FR0–FR2) are decoded by the Output Function Decoder, and C WFMK is asserted to cause the TU10 to write the End of File Mark (EOF).
C WRE H	M8321	Write Enable (C WRE H) is asserted to inform the TU10 that the TM8-E is ready to Write, Write File Mark, or Rewind.
C WD0 H C WD1 H C WD2 H C WD3 H C WD4 H C WD5 H C WD6 H C WD7 H	M8321	C WD0 H through C WD7 H are data bits to be written on tape during a Write operation. C WD0 H and C WD1 H are not written on 7-track transports, and they are zero values when core dump mode is called for on a 9-track transport.
C WXG H	M8321	Extended Gap (C WXG H) is asserted when bit 3 in the Function Register is a 1 to cause the transport to leave a 3-inch gap between records.

Table 9-15 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
SC-1 DATA LATE L	M8323	SC-1 DATA LATE L is asserted when the computer fails to service a BRK RQST before the next data transfer to or from tape.
C RD0 L C RD1 L C RD2 L C RD3 L C RD4 L C RD5 L C RD6 L C RD7 L	TU10	C RD0 L through C RD7 L are data bits read from the tape during a Read or Read/Compare operation. C RD0 and C RD1 are not read from 7-track transports; they are zero values when the core dump mode is called for on a 9-track transport.
C PEVN L	M8321	C PEVN L is asserted when bit 3 in the Command Register is a 1 to select odd parity. The 7-track transports can use even or odd parity, but bit 3 must always be 0 when writing on a 9-track tape. Even parity operation on 9-track tapes causes a 1 to be written on channel 3 (on the Parity track) if Data is all 0s.
C RDS L	TU10	Read Strobe (C RDS L) is a 100-ns pulse asserted by the TU10 each time a data character is read from DECmagtape.
C TUR L	TU10	Tape Unit Ready (C TUR L) is asserted by the TU10 when the selected tape unit is ready.
C 7 CH L	TU10	Seven channel (C 7 CH L) is asserted by the selected transport if it is a 7-track transport. When C 7 CH L is not asserted a 9-track transport has been selected and eight data bits are transferred.
CB-3 CHG TRANS L	M8322	The CB-3 CHG TRANS flip-flop sets and asserts CB-3 CHG TRANS L when RE-1 BSEL 0 through RE-1 BSEL 2 from the Buffered Command Register and RE-1 SEL 0 through RE-1 SEL 2 are different. CB-3 CHG TRANS is cleared by the next SC-1 SET Pulse.
CPMA DISABLE	M8322	*
OC-1 R/C ERROR L	M8321	The OC-1 R/C ERROR flag is set to assert OC-1 R/C ERROR if an error occurs during a Read/Compare operation (data read from DECmagtape is different from data in memory).

*Refer to Table 9-3, *PDP-8/E & PDP-8/M Small Computer Handbook*.

Table 9-15 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
RE-1 DB00–RE-1 DB11	M8327	RE-1 DB 00 through RE-1 DB 11 is a 12-bit word from the Data Register which could be data read from tape, data from the AC, or data from the Memory Data lines. The input to the Data Register is controlled by a Data Multiplexer on the input of the Data Register. These bits are applied to the Read/Compare Error detection logic to compare them with memory data during a Read/Compare operation.
CB-2 DB MPX A L	M8322	Selects data for input to the Data Register (Table 9-17).
CB-2 DB MPX B L	M8322	Selects data for input to the Data Register (Table 9-17).
RE-1 DEN 5 H (bit 10)	M8321	See Table 9-12 for these function bits.
RE-1 DEN 8 H		
RE-1 IEEF	M8327	Enable Interrupt when ERROR flag (RE-1 IEEF) is asserted if bit 4 in the Command Register is a 1.
RE-1 IEJF	M8327	Enable Interrupt when JOB DONE (RE-1 IEJF) is asserted if bit 5 in the Command Register is a 1.
RE-1 EMA 0 RE-1 EMA 1 RE-1 EMA 2	M8327	RE-1 EMA 0 through RE-2 EMA 2 are used to address extended memory (Table 9-11). Bit 6 in the Function Register must be a 1 to use Extended Memory Addressing.
RE-2 EMA 7 INC ERR L	M8327	RE-2 EMA 7 INC ERR L is asserted when the program tries to increment beyond memory fields 7 and sets bit 8 in the Second Status Register.
RE-1 EMA INC EN L	M8327	Extended Memory Address Increment (RE-1 EMA INC EN L) is asserted when bit 6 in the Function Register is a 1 to allow memory to be treated as a continuous memory rather than 4K blocks.
RE-1 ENAB CHK CHAR L	M8327	Enable Check Character (RE-1 ENAB CHK CHAR L) is asserted and sets bit 4 of the Second Status Register if bit 4 of the Function Register is a 1 to read the CRC and LRC character from 9-track transports.

Table 9-15 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
SC-2 EOT L	TU10	End of Tape (SC-2 EOT) is asserted if the EOT reflective strip is sensed by the selected transport. C EOT sets bit 8 of the Main Status Register.
SC-2 ERROR L	M8323	The SC-2 ERROR flag is set by any one of the following conditions: *a.* EOT *b.* R/C ERROR *c.* PARITY ERROR *d.* BOT *e.* EMA 7 INC ERR *f.* REC LENGTH INCORRECT *g.* DATA LATE *h.* EOF *i.* ILLEGAL FUNCTION *j.* SELECT ERROR The ERROR flag allows the SKIP line to be grounded if the SKEF instruction is executed by the program.
RE-1 FR0–FR2	M8327	Function bits FR0 through FR2 are decoded by Function decoders in the TM8-E output control module and TM8-E control module to determine TU10 DECmagtape functions and generate TM8-E control signals (Table 9-12).
RE-1 GO	M8327	RE-1 GO is asserted when bit 5 in the Function Register is a 1. RE-1 GO must be a 1 to allow tape operation to start.
SC-2 ILLEGAL FUNCTION	M8323	SC-2 ILLEGAL FUNCTION is asserted by any of the conditions listed in Table 9-13 to set bit 11 in the Main Status Register.
INT STROBE H	Processor	*
INT I/O L	M8321	**
INIT	Processor	*Clears all flags in the TM8-E and TU10 Master System. It is asserted by pressing the CLEAR key on the front panel or by a 6007 IOT instruction.

*Refer to Table 9-3, *PDP-8/E & PDP-8/M Small Computer Handbook.*
**Refer to Table 9-1, *PDP-8/E & PDP-8/M Small Computer Handbook.*
} OMNIBUS SIGNALS

Table 9-15 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
*CB-3 INT RQST L	M8322	CB-3 INT RQST L is asserted by one of the following conditions: *a.* Bit error in the Command Register is a 1 and the SC-2 ERROR flag is set. *b.* Bit 5 in the Command Register is a 1 and the JOB DONE (CB-3 MTTF) flag is set.
I/O PAUSE L*	M8321	*
C LRCE L	TU10	LRC ERROR (C LRCE L) is set by the TU10 when a LPE is detected by the Master System.
OC-2 LWCR L	M8321	OC-2 LWCR is asserted to load the WC Register when a 6701 instruction is executed by the program.
OC-2 LDBR	M8321	Load Data Buffer Register (OC-2 LDBR) is asserted when a 6707 instruction is executed by the program to transfer the contents of the AC to the Data Buffer Register. This instruction also sets CB-3 MTTF (JOB DONE).
MA0--MA11	OMNIBUS **	MA0 through MA11 are used to address 4096 possible memory locations. During a data break, the CA Register controls the MA lines to select a memory location for a data transfer between memory and the DECmagtape.
CB-2 MAC ACC L	M8322	CB-2 MAC ACC is asserted when a BRK RQST is granted to enable the data transfer and clear BRK RQST.
SC-2 NOT LAST XFER L	M8322	**
MD0--MD11	Processor	***
MSIR DISABL	M8322	****
CB-1 OFFLINE L	M8322 and M8321	CB-1 OFFLINE is asserted when 0XXX is loaded into the Function Register by a LFGR instruction and the selected transport rewinds to beginning of tape and stops. The transport must be manually reset to on-line condition.
SC-1 PARITY ERROR L	M8323	The SC-1 PARITY ERROR flip-flop is set when an LRC, CRC, or VPE error is detected by the selected TU10 Tape Transport.

*Refer to Table 9-1, *PDP-8/E & PDP-8/M Small Computer Handbook*.
**Refer to Table 9-2, *PDP-8/E & PDP-8/M Small Computer Handbook*.
***Refer to Table 9-4, *PDP-8/E & PDP-8/M Small Computer Handbook*.
****Refer to Table 9-3, *PDP-8/E & PDP-8/M Small Computer Handbook*.

Table 9-15 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
RE-1 PEVN H	M8327	If RE-1 PEVN is high, the TU10 generates and checks for even parity; if it is low, the TU10 generates and checks for odd parity. The level of RE-1 PEVN is controlled by bit 3 of the Command Register (when bit 3 is a 1, RE-1 PEVN is low).
POWER OK H*	Processor	POWER OK goes high when a PDP-8/E power failure occurs and generates a CB-3 CLR ALL to stop all transports and end any operation occurring at the time of a power failure.
SC-1 PRESET H	M8323	SC-1 PRESET H is a 2.5-μs pulse that is triggered by setting the RE-1 GO bit in the Function Register to a 1 if the selected transport is ready (C TUR is true). RE-1 PRESET H triggers the RE-1 SET pulse.
RE-1 RCAR L	M8321	Read CA Register (RE-1 RCAR) is asserted when the 6713 instruction is executed by the program to transfer the contents of the CA Register to the AC.
OC-1 RDB L	M8321	Read Data Buffer (OC-1 RDB) is asserted by an RDBR instruction or by CB-2 MAC 1 H during a read data break to transfer the contents of the Data Buffer Register to the Data lines.
RE-1 RDBR L	M8321	Read Data Buffer Register (RE-1 RDBR) is asserted when a 6717 instruction is executed by the program to ground OC-1 RDB L and transfer the contents of the Data Buffer Register to the AC.
SC-1 RECORD LENGTH INCORRECT H	M8323	SC-1 RECORD LENGTH INCORRECT is asserted and sets bit 6 in the Main Status Register if the record length differs from the WC Register. The WC Register must be read by the program to determine if the record was too short or too long.
RE-1 REWIND	M8321	RE-1 REWIND is asserted by the Function Decoders if a 1XXX is loaded into the three most significant bits of the Function Register.
RE-1 RFSR L	M8321	RE-1 RFSR is asserted when a 6716 instruction is executed to transfer the contents of the Second Status Register and Function Register to the AC.
OC-2 RMSR L	M8321	OC-2 RMSR is asserted when a 6714 instruction is executed by the program to transfer the contents of the Main Status Register to the AC.

*OMNIBUS signals.

Table 9-15 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
OC-2 RWCR L	M8321	OC-2 RWCR is asserted when a 6711 instruction is executed by the program to transfer the contents of the WC Register to the AC.
RE-1 SEL 0 H RE-1 SEL 1 H RE-1 SEL 2 H	M8327	RE-1 SEL 0 through RE-1 SEL 2 are loaded into the three most significant bit positions of the Command Register by an LCMR instruction. These bits are used to select one of the eight (maximum) transports for a data transfer operation (Table 9-11).
SC-1 SET H	M8323	SC-1 SET H is approximately a 5-μs pulse that is triggered by setting the GO bit in the Function Register to 1. SC-1 SET H is applied to the selected TU10 transports to start tape movement if TUR is true (Tape Unit Ready).
OC-2 SKIP L	M8321	The OC-2 SKIP line is grounded when one of the following conditions exist: *a.* SKEF instruction is executed and the SC-2 ERROR flag is set. *b.* SKCB instruction is executed and SC-1 CONTROL BSY is not set. *c.* SKTR instruction is executed and C TUR is asserted. *d.* SKJD instruction is executed and the JOB DONE (CB-3 MTTF) flag is set.
CB-1 SPACE H	M8322	CB-1 SPACE H is asserted during Space Reverse or Space Forward operation and continued until EOT, FMK, or WCOV, is encountered. File Mark is read from the tape.
CB-1 SP FWD L	M8322	CB-1 SP FWD is asserted when 6XXX is loaded into the three most significant bit positions of the Function Register. The transport spaces forward the number of records specified by the WC Register.
CB-1 SP REV L	M8322	CB-1 SP REV is asserted when 7XXX is loaded into the three most significant bit positions of the Function Register. The transport spaces in reverse the number of records specified by the WC Register.

Table 9-15 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
SC-1 SELR L	M8323	Select Remote (SC-1 SELR L) indicates to the control that the selected transport is on-line.
OC-2 SBRM L	M8321	Set BRK RQST Maintenance (OC-2 SBRM) is asserted when a 6727 instruction is executed by the program to initiate one Single Cycle Data Break.
SC-1 TUR L	TU10 and M8322	Tape Unit Ready (SC-1 TUR L) is asserted when the selected tape transport is ready.
RE-2 WCOL	M8327	Word Count 0 (WC0) is asserted when the WC Registers read all 0s to indicate the data transfer is complete. RE-2 WC0 is used to generate CB-1 WCOV (Word Count Overflow).
CB-1 WCOV L	M8322	Word Count Overflow (RE-2 WCOV) is asserted when the WC Register contains all 0s to negate C WDR and end a Data Transfer operation.
CB-1 WR 9 L	M8322	Enables logic to apply 8 bits of data to the selected 9-track transport during a Write operation.
CB-1 WR 1st 7 L	M8322	Enables the logic to apply the six most significant bits of a 12-bit data word from memory to the selected 7- or 9-track transport during a Write operation. Tracks 0 and 1 of a 9-track transport are 0s if it is used as a 7-track format.
CB-1 WR 2nd 7 L	M8322	Enables logic to apply the six least significant bits of a 12-bit data word to the selected 7- or 9-track transport during a Write operation. Tracks 0 and 1 of a 9-track transport are 0s if it is used to record a 7-track format.
SC-1 WRS L	TU10	Write Strobe (SC-1 WRS) is asserted by C WRS from the TU10 when the selected transport is ready to write new data: C WRS is a 100-ns pulse that is asserted once for each character written on tape.

9.10.1 Single Cycle Data Break

The Single Cycle Data Break is used for data transfers between PDP-8/E core memory and the TU10 DECmagtape Transports (Figure 9-17). The concept of data transfers and the interrelationship of the Data Break Interface are explained in Chapter 6 of the *PDP-8/E & PDP-8/M Small Computer Handbook*, 1972. A detailed description of the Data Break Interface is explained in Chapter 10, Volume 2. Figure 9-18 is a timing diagram of the Single Cycle Data Break Interface; reference this diagram during the discussion of the TM8-E functions and programming that follows. Data flow for the core dump mode of operation is shown in Figure 9-18.

NOTE

The programs and timing diagrams presented here are not necessarily the best or only way to program the TM8-E. They are shown to illustrate TM8-E functional operation and the interaction of functional groups of logic. The timing diagram referred to in the description of TM8-E functions is part of the TM8-E Print Set (Drawing D-TD-TM8-E-1).

9.10.1.1 Signal Conventions – The following signal conventions are used in the TM8-E.

a. Interface signals. All signals that are used to interface the TM8-E with the TU10 are preceded by C, e.g., C SET L. All signals applied to the TU10 are asserted when they are low (0.0V); all signals from the TU10 are asserted when they are high (+3.0V).

b. All signals on the TM8-E modules followed by L, e.g., SBRM L, are asserted (true) when they are 0.0V. All signals followed by H, e.g., SEL 1 H, are asserted (true) when they are 3.0V.

c. All signals on the TM8-E preceded by B, e.g., BTP3 L, are inverted signals or the outputs of holding registers, e.g., B SEL 0 H.

d. All signals on the TM8-E have a prefix to indicate their origin as shown in Paragraph 9.7.

9.10.1.2 Write Data – Data can be written on a 7- or 9-track DECmagtape only in the forward direction (see D-TD-TM8-E-1, sheets 7 and 8 for timing diagram). The CA Register must be loaded with the starting memory address minus one; the WC Register must be loaded with the 2's complement of the number of words to be transferred. The density and parity bits in the Command Register (Table 9-11) must be set to select tape density, parity mode, and tape unit. The Write function is controlled by the WC Register such that when WCOV occurs the data transfer stops. CB-3 MTTF is set when the LRC character passes under the read heads. Note that the WC, CA, and Command Registers must be loaded prior to the Function Register because the Function Register contains the GO bit, which initiates tape movement and sets SC-1 CNTL BSY (control busy). If any errors other than illegal functions or select errors occur during a write operation, the ERROR flag is set after MTTF is set. Operation may be continued on the same transport in the same direction immediately if the registers are reloaded following MTTF. A continuous operation may still be achieved when a change direction or change transport is encountered; however C TUR from the selected transport must be asserted.

9.10.1.3 Read Data – Records are read from a 7- or 9-track DECmagtape transport and transferred to memory only in the forward direction (D-TD-TM8-E-1, sheets 1 and 6 for timing diagrams). The WC, CA, and Command Registers must be loaded because they are for a Write operation. Density tape unit, and parity must be selected; density and parity must be the same as they were when the data was written on tape. During a Read operation, the number of words loaded into the WC Register (in 2's complement) is transferred to memory. If the WC Register is set to less than the actual record length, only the number of words in the WC are transferred. If the WC Register is greater than or equal to the actual record length, the entire record is transferred to memory. In either case, a Record Length Incorrect Error (SC-1 REC LNG INCORRECT) is generated for evaluation by the program. The WC and CA Registers contain the number of words read from tape and the address where the last word was stored. The contents of the WC Register can be checked by the program to determine the cause of error (record too long or too short).

Parity checks are made by the TU10 as data is read from tape. If any parity errors are detected, the SC-2 ERROR flag is set at the same time as CB-3 MTTF. The Second Status Register must be read and evaluated by the program to determine what caused the error. CB-3 MTTF (JOB DONE flag) is set when the LRCS character is read from tape. Note that if a 9-track transport is used, a BRK RQST is made for each character read from tape; a 7-track transport reads two characters before a BRK RQST is made. Core dump mode causes a 9-track transport to operate the same as a 7-track transport. Continuous operation may be obtained under the same conditions as a write operation. Read after Write operations set the Illegal Function flag. To read the CRC and LRC characters, bit 4 in the Function Register must be 1.

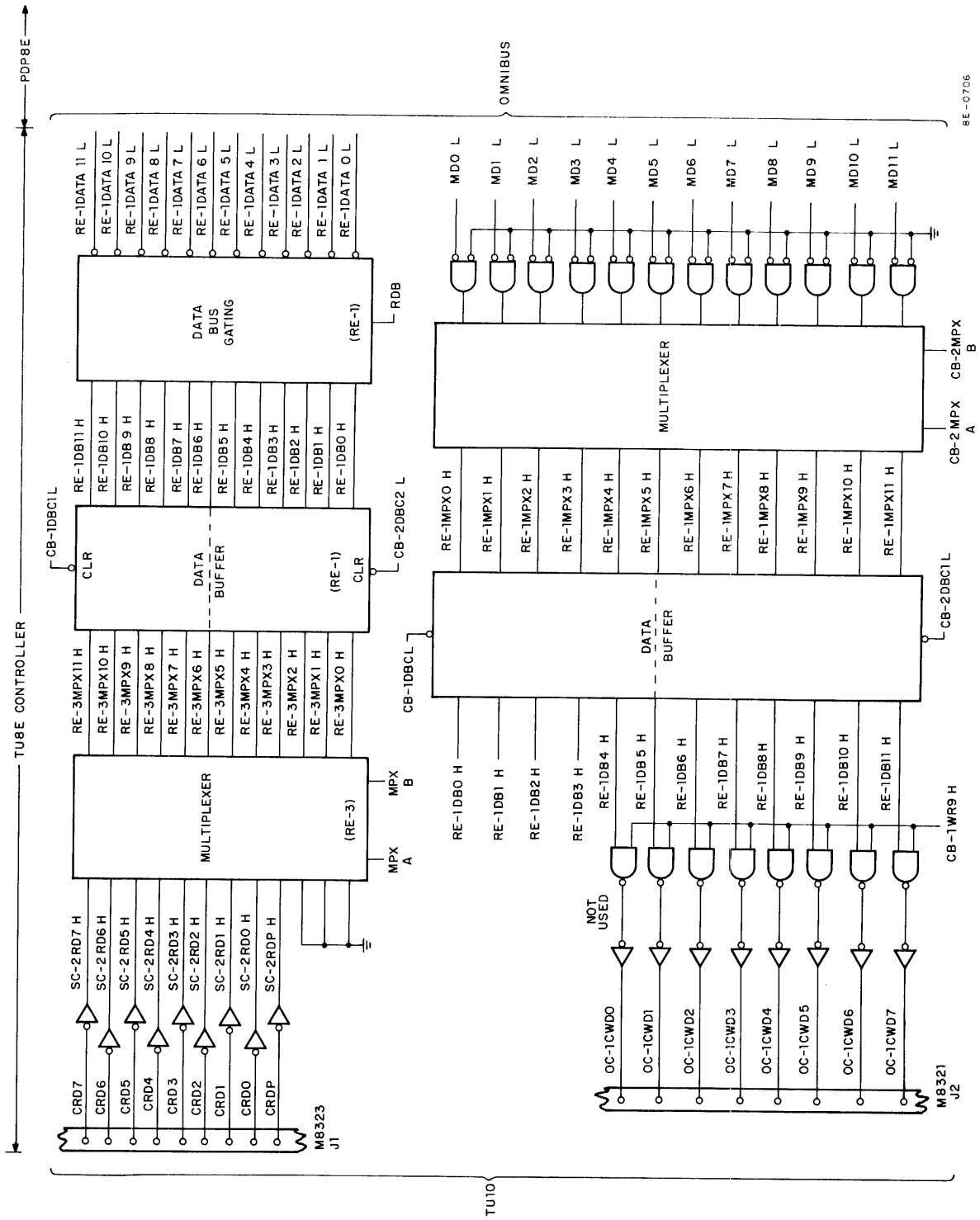


Figure 9-17 Single Cycle Data Break Data Transfer Data Flow

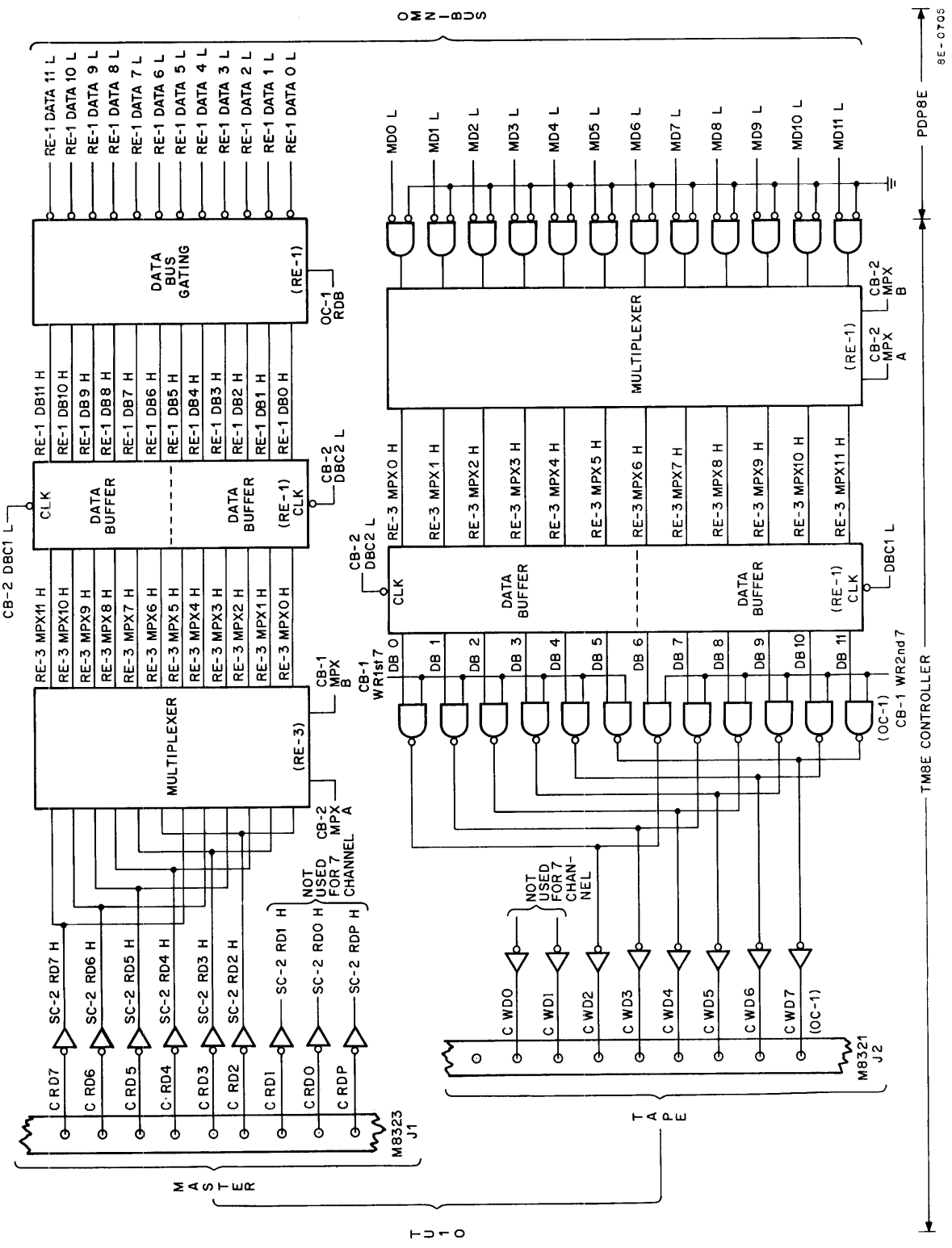


Figure 9-18 Core Dump Data Flow

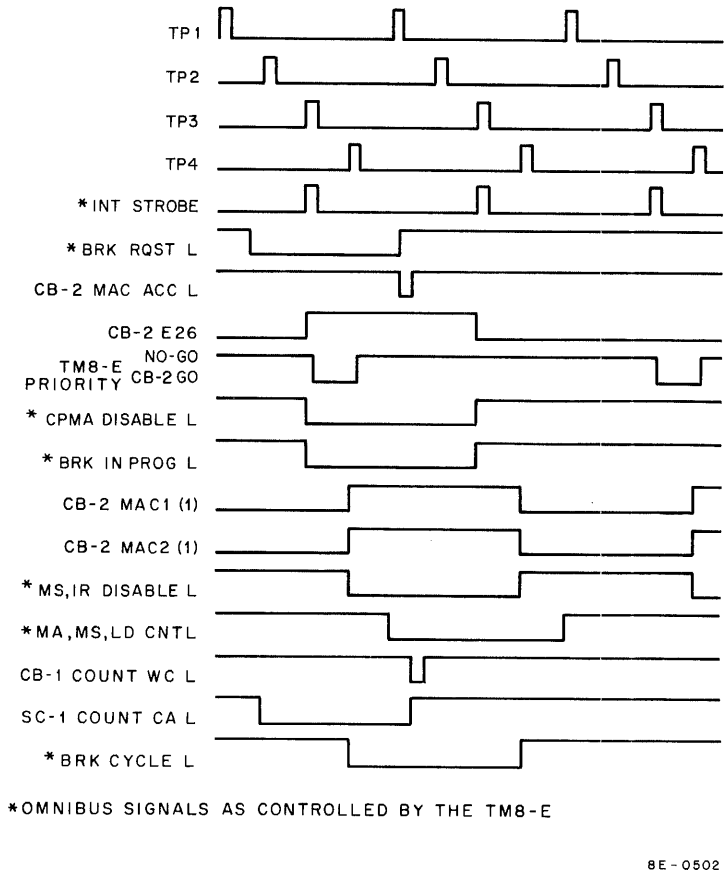


Figure 9-19 Single Cycle Data Break Timing Diagram

9.10.1.4 Read/Compare – The Read/Compare operation (see D-TD-TM8-E-1 sheet 2 for timing diagram) compares data read from tape with data from memory that is addressed by the CA Register. The WC and CA Registers must be loaded and density and parity modes must be set. If an OC-1 R/C ERROR occurs, the incrementation of the CA Register stops and the CA Register contains the address of the data that produced the error. An OC-1 R/C ERROR also sets bit 10 in the Main Status Register (Figure 9-9). Tape motion continues to the end of record and MTTF is set. If interrupt is enabled (Figure 9-7), the program is interrupted by an OC-1 R/C ERROR and the Main Status Register is read to determine if the error was a OC-1 R/C ERROR. The CA Register must be read by the program to determine the memory location where data was stored that caused the error. Note a Read/Compare operation cannot follow a Write operation, the tape must be backspaced before starting a Read/Compare operation.

9.10.1.5 Extended Gap – Extended Gap is used with Write operation (bit 3 in the Command Register must be set) to cause the transport to leave a 3-inch blank space (gap) at the beginning of a record (Drawing No. TD-TM8-E-1, sheets 1 through 9). This feature is used to leave spaces to separate records or groups of records and to space over bad spots on tape. Note that the only difference between this operation and a normal Write operation is the time required to obtain the first write strobe pulse from the TU10 (Table 9-15 for definition).

9.10.1.6 Write End of File – The Write End of File operation (D-TD-TM8-E-1, sheet 4) writes a single character on tape to designate the end of a record or group of records. A 17_8 is written on 7-track transports and 23_8 is written on 9-track transports. On 7- and 9-track transports, the EOF character is followed by an LRC character that is identical to the EOF character. The WC and CA Registers do not have to be loaded for this operation.

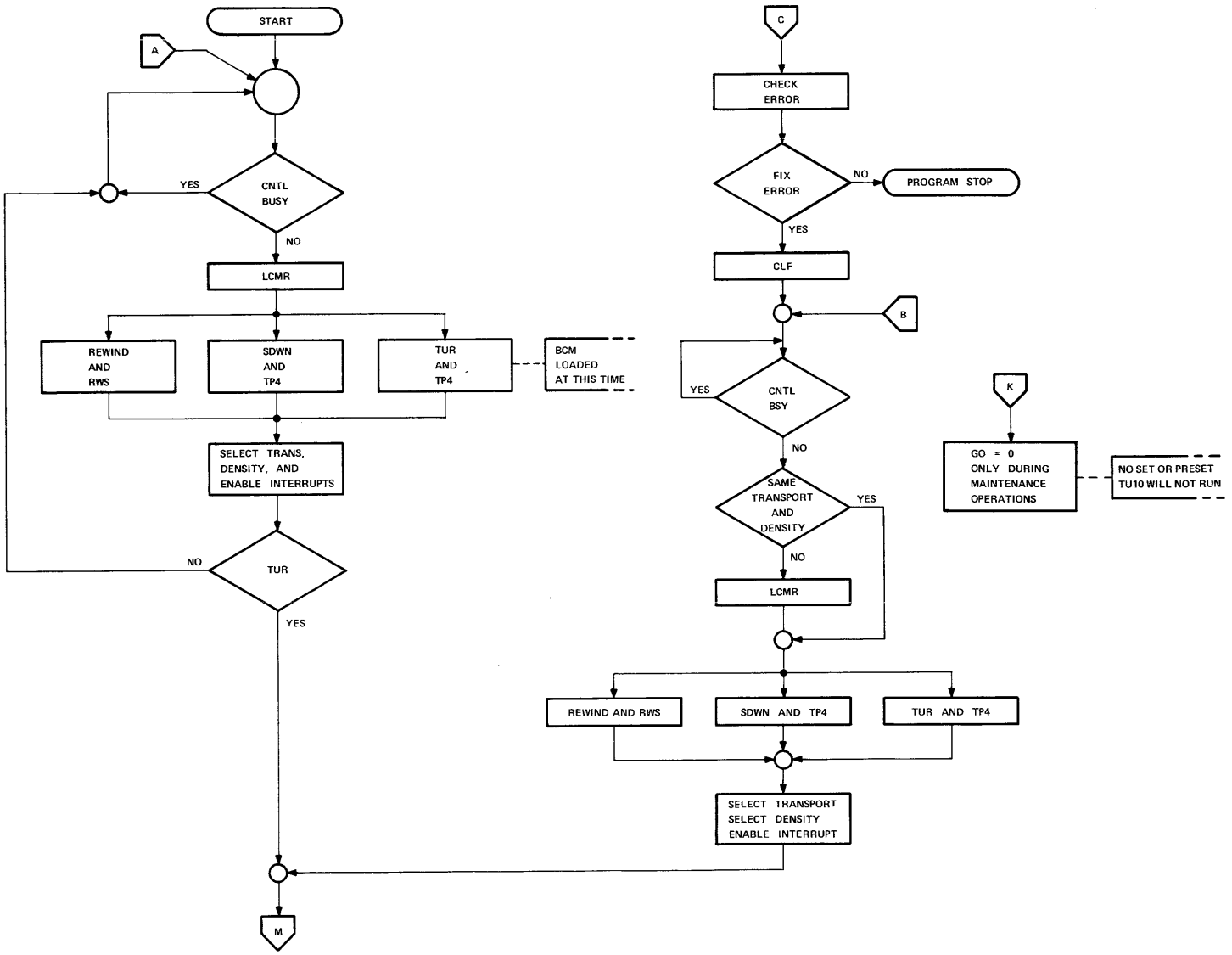


Figure 9-20 TM8-E Flow Diagram (Sheet 1 of 10)

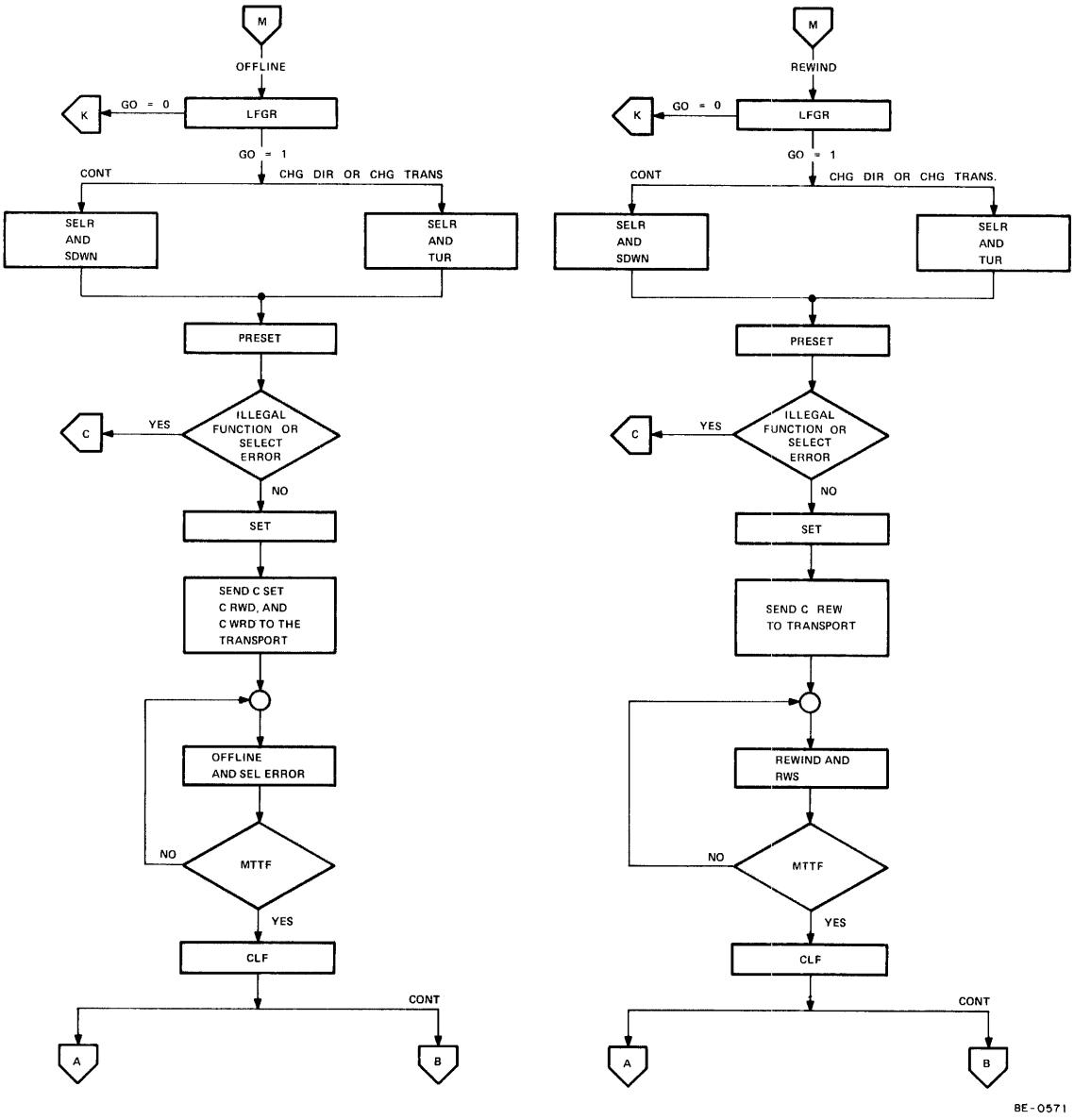


Figure 9-20 TM8-E Flow Diagram (Sheet 2 of 10)

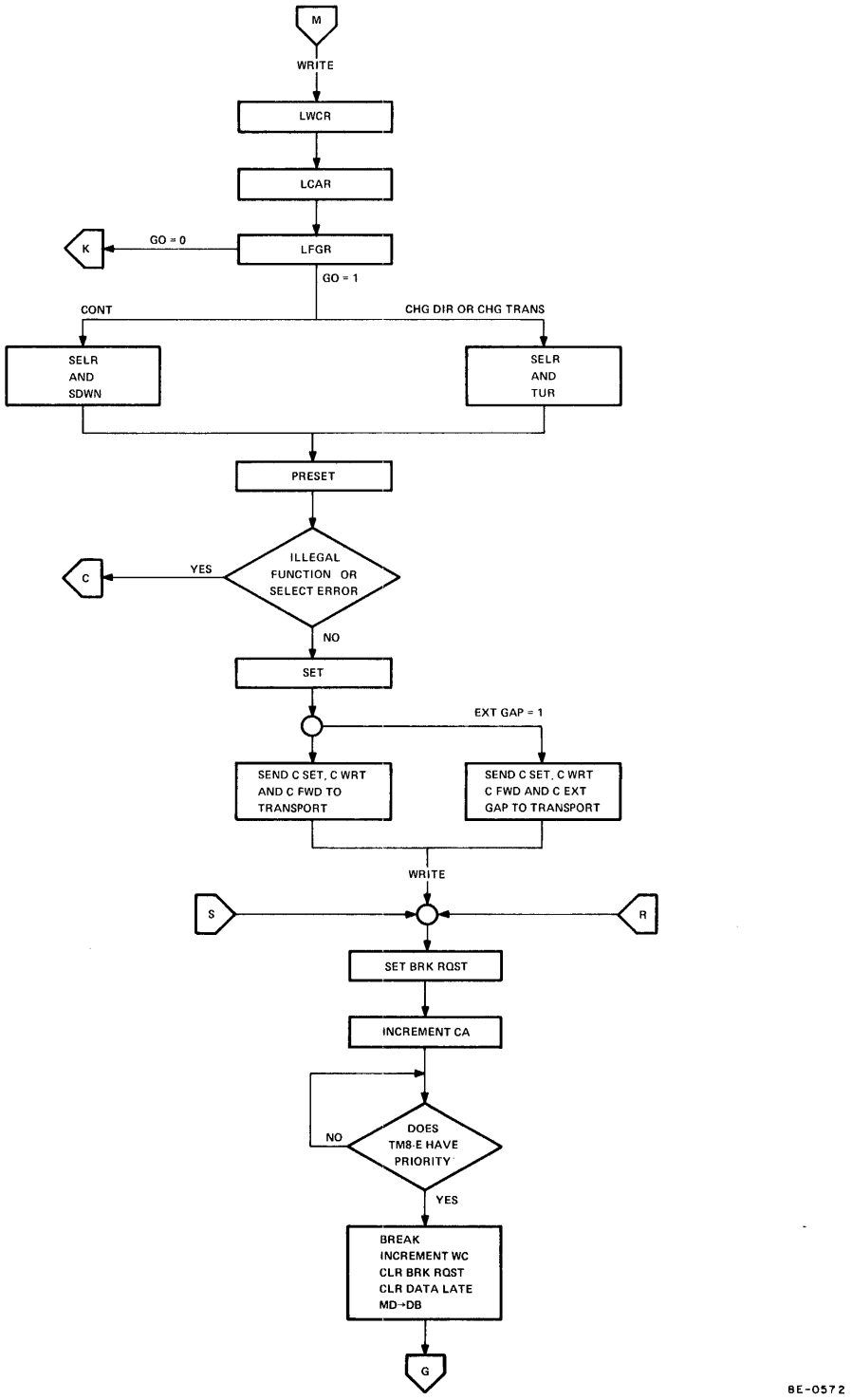


Figure 9-20 TM8-E Flow Diagram (Sheet 3 of 10)

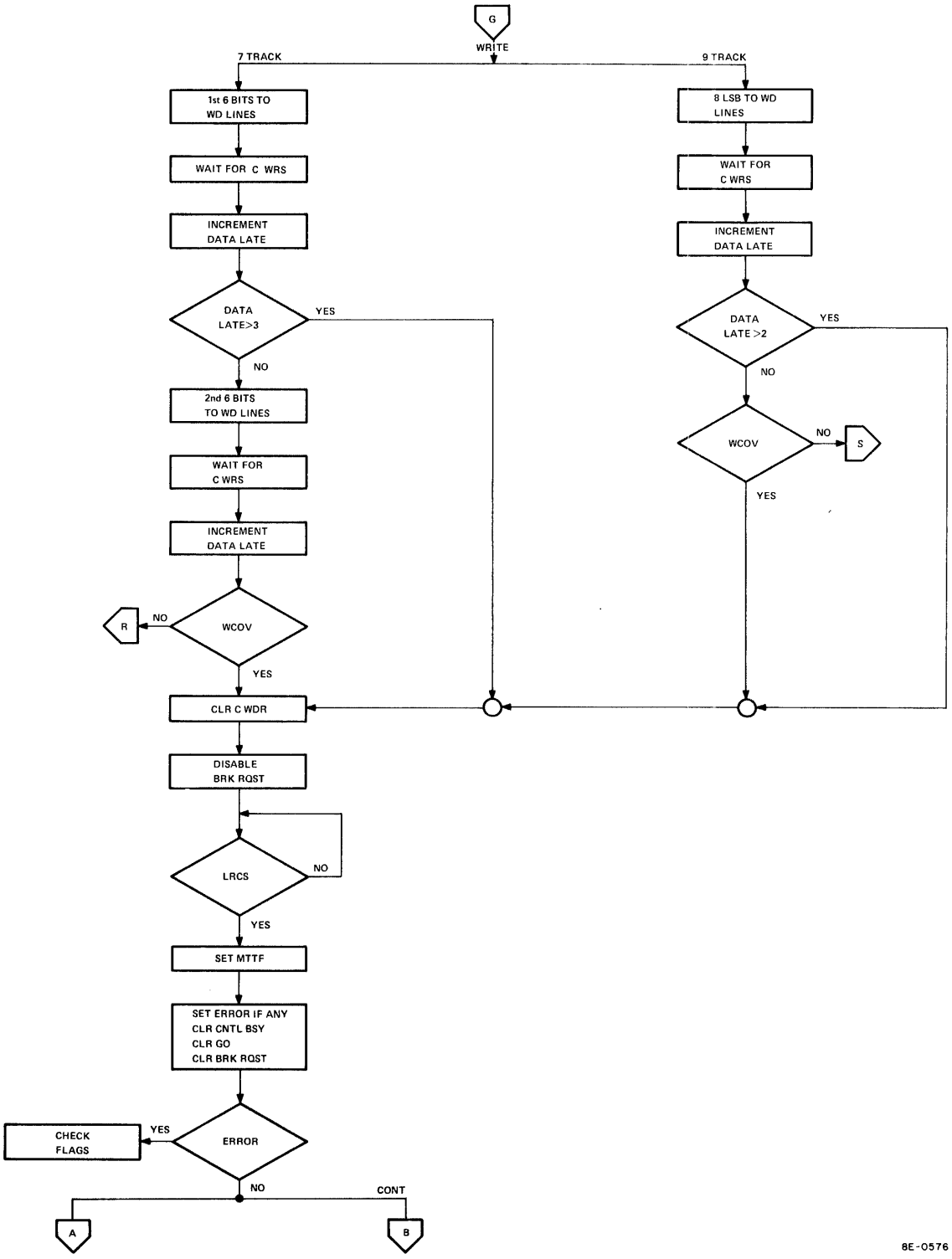


Figure 9-20 TM8-E Flow Diagram (Sheet 4 of 10)

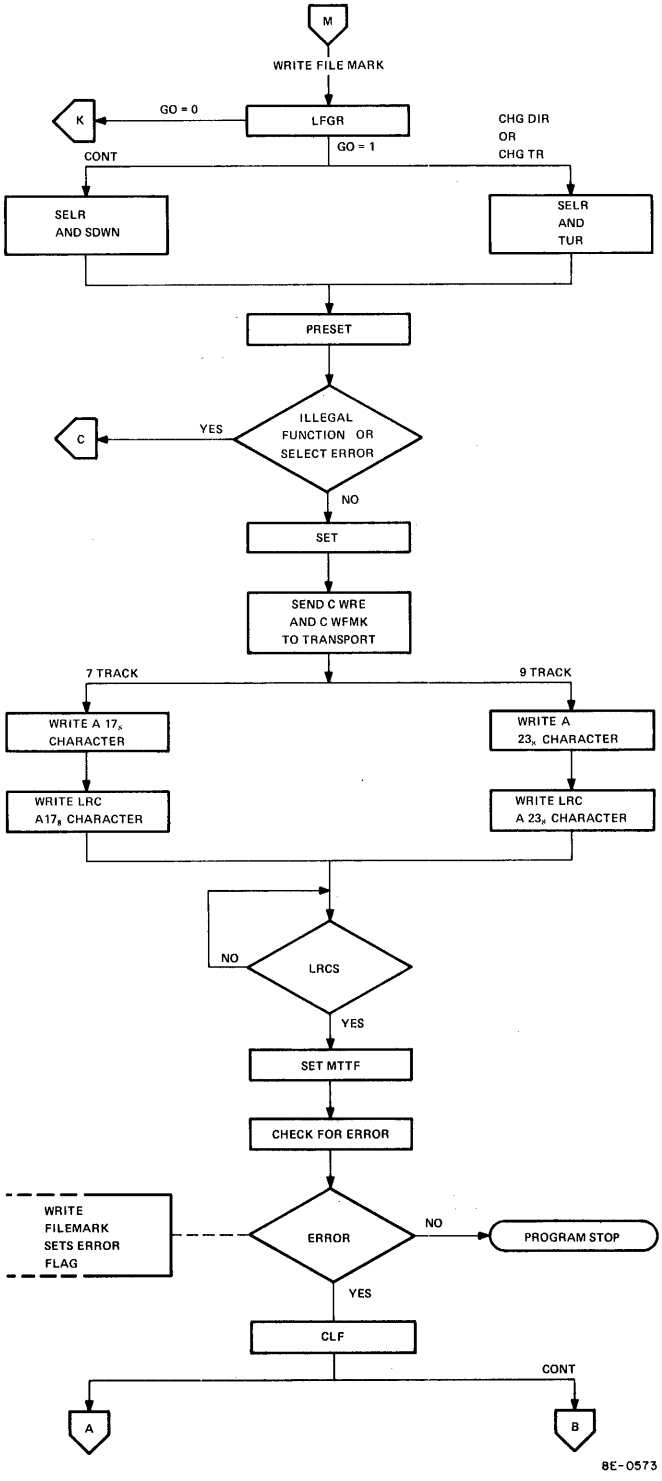


Figure 9-20 TM8-E Flow Diagram (Sheet 5 of 10)

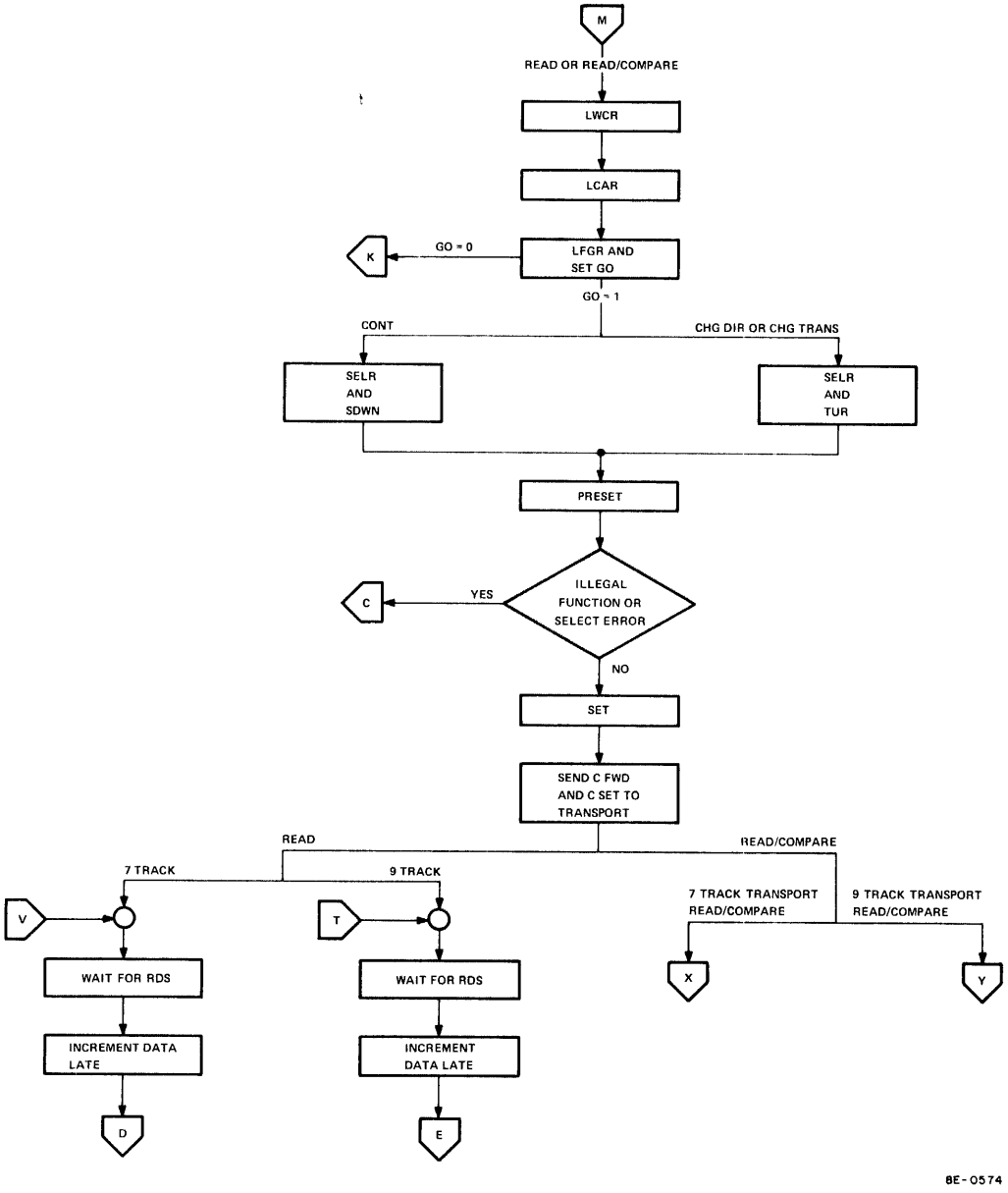


Figure 9-20 TM8-E Flow Diagram (Sheet 6 of 10)

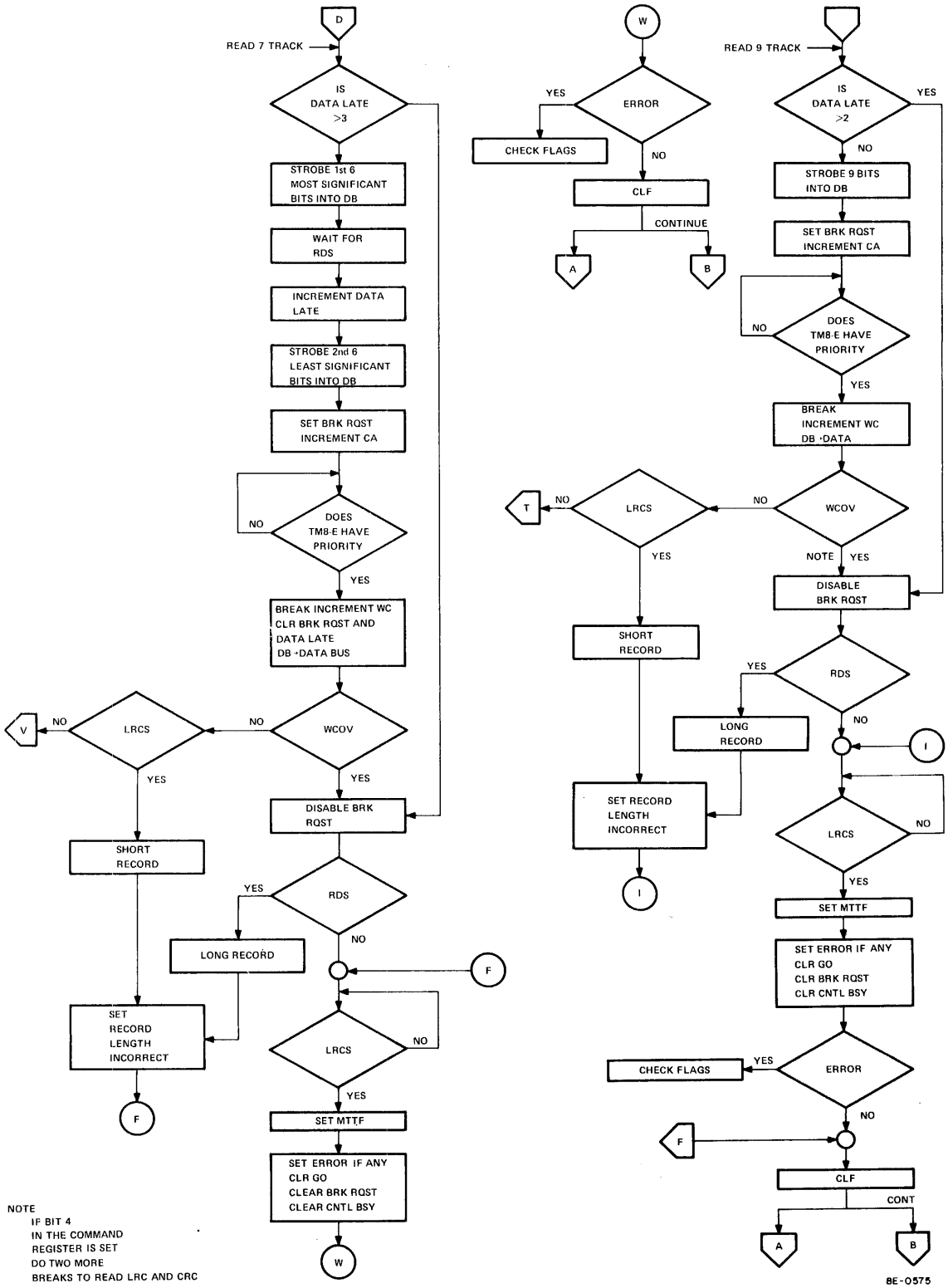


Figure 9-20 TM8-E Flow Diagram (Sheet 7 of 10)

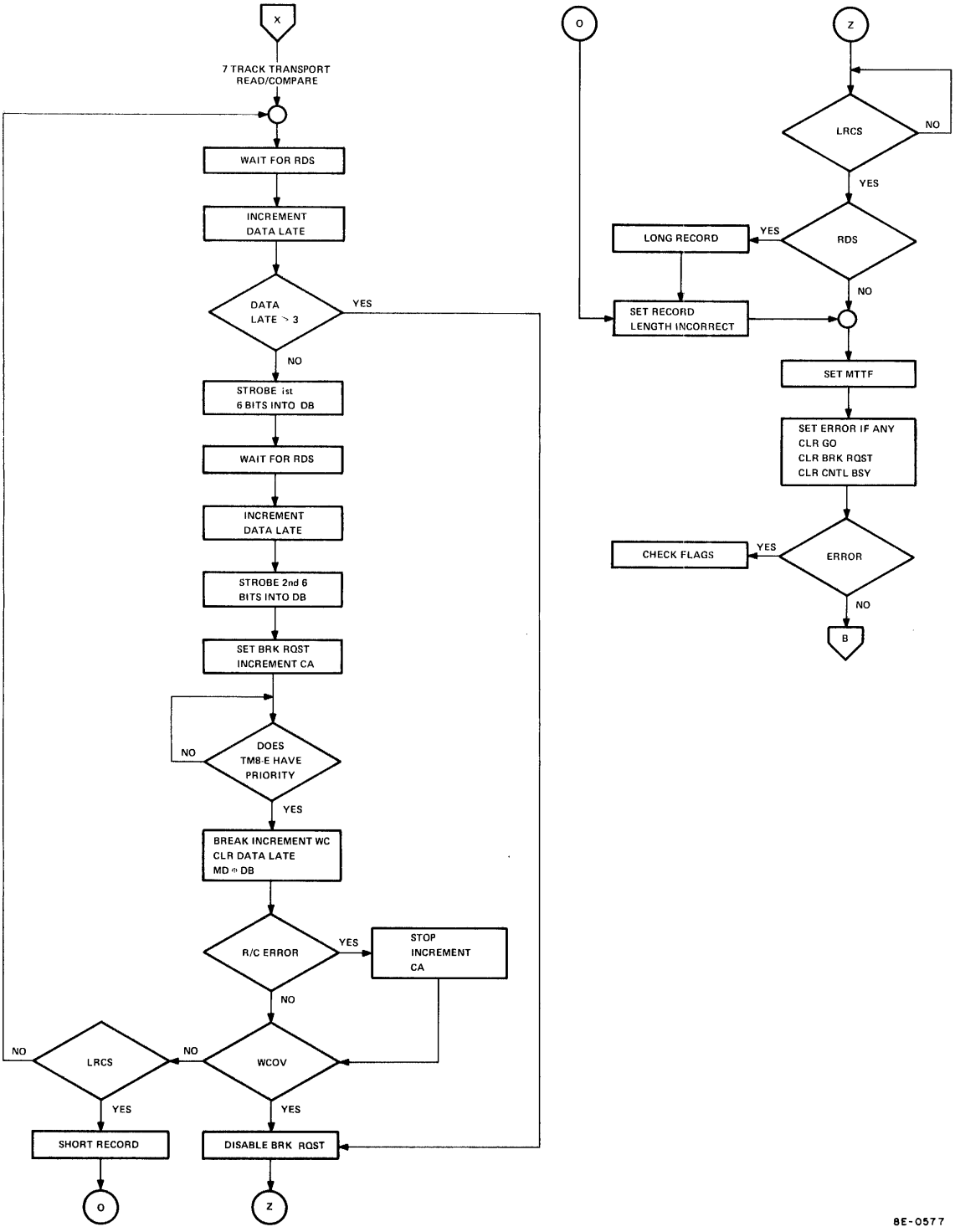


Figure 9-20 TM8-E Flow Diagram (Sheet 8 of 10)

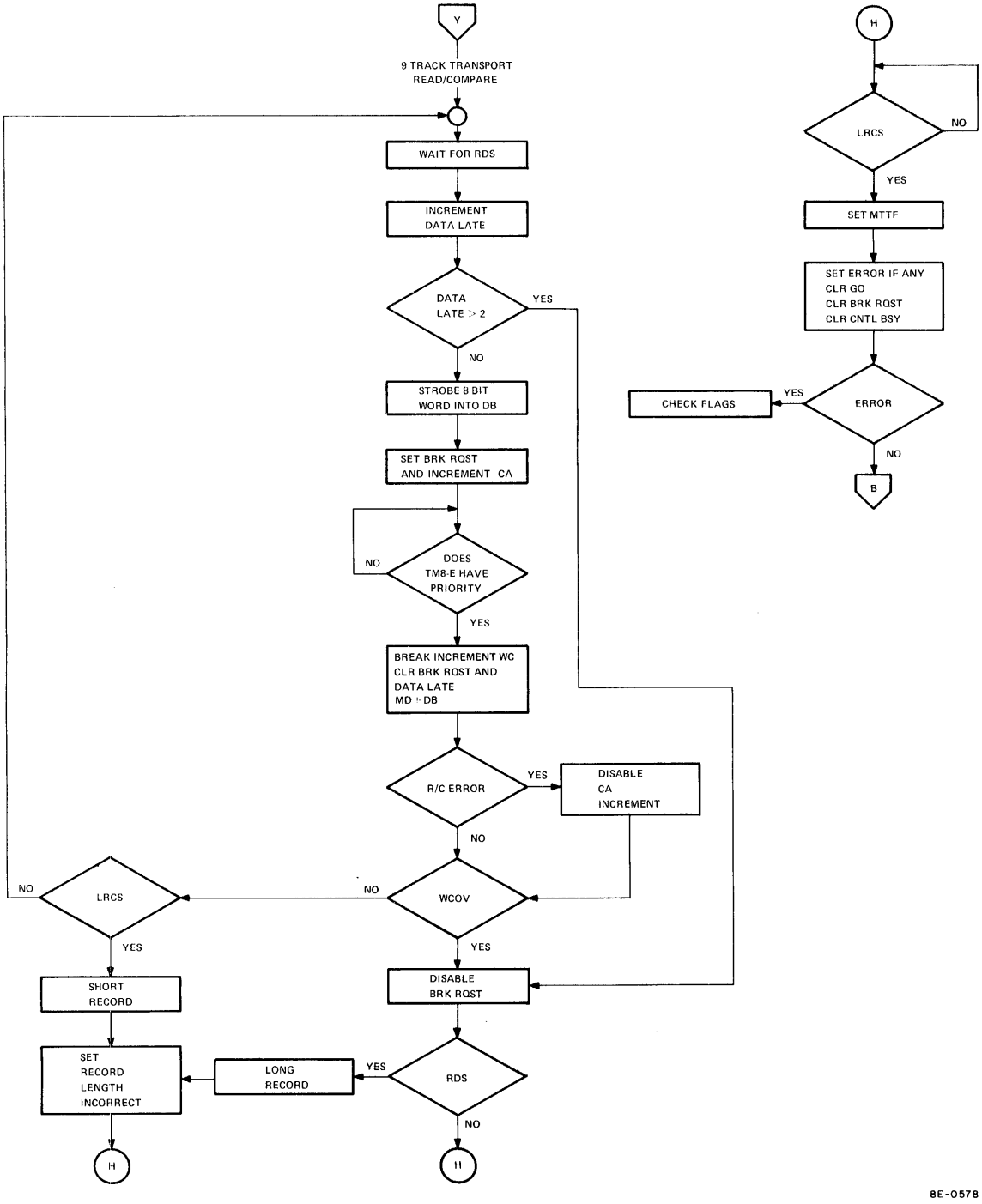


Figure 9-20 TM8-E Flow Diagram (Sheet 9 of 10)

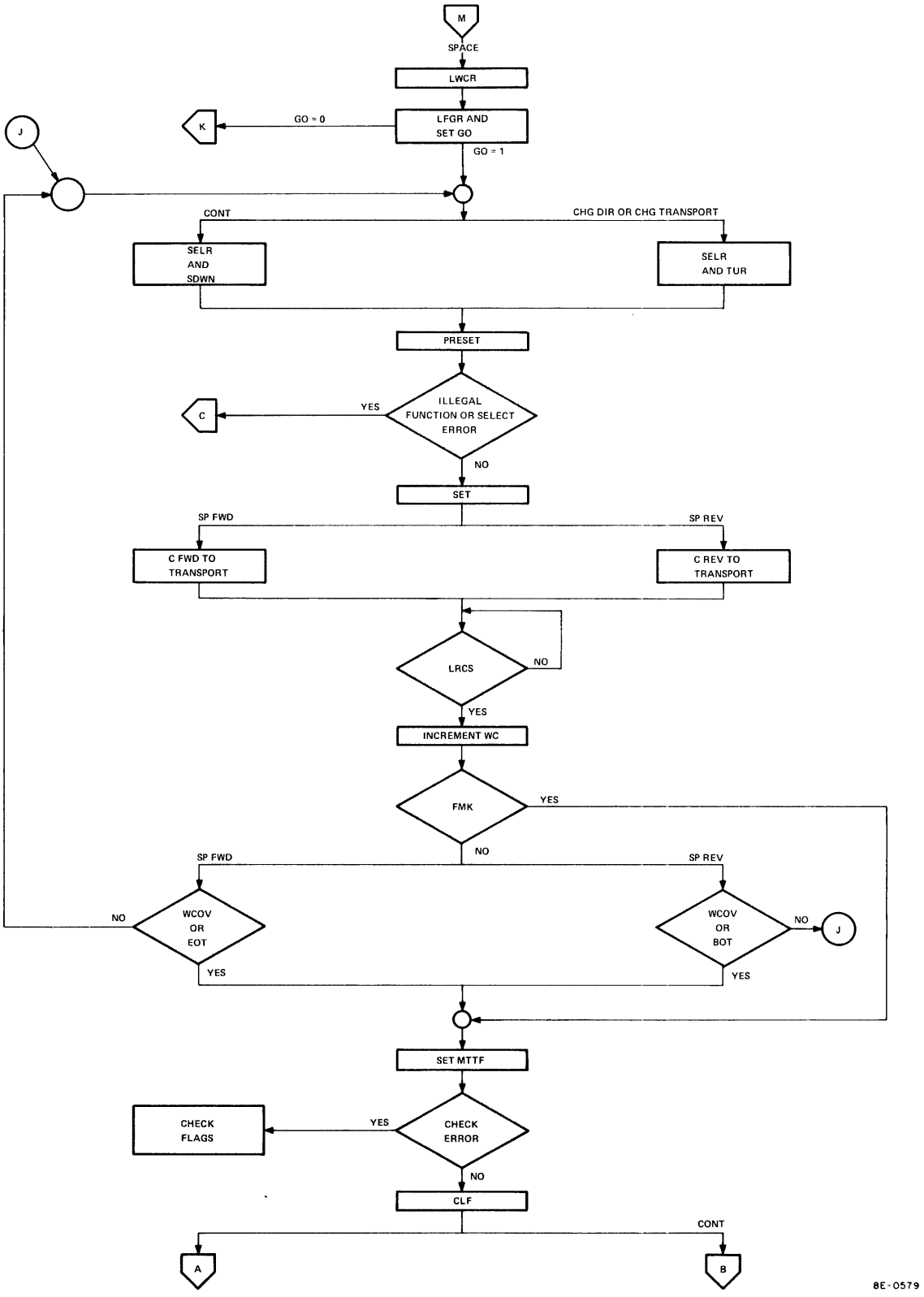


Figure 9-20 TM8-E Flow Diagram (Sheet 10 of 10)

9.10.1.7 Space Forward – The Space Forward operation (see D-TD-TM8-E-1, sheet 5 for timing diagram) causes the tape to space forward a number of records specified by the WC Register. The WC Register must be loaded with the 2's complement of the number of records to be spaced over. The WC Register is incremented by the C LRCS pulse at the end of each record. CB-3 MTTF sets when the WC Register overflows and the last record has been passed over. Note that an attempt to Space Forward when the tape is at EOT is an error that sets the SC-2 ERROR flip-flop after CB-3 MTTF is set. Space Forward is terminated if a File Mark is encountered. SC-2 ILLEGAL FUNCTION is set if Space Forward is initiated after a Write or Write File Mark function.

9.10.1.8 Space Reverse – The Space Reverse operation (see D-TD-TM8-E-1, sheet 3 for timing diagram) causes the tape to space reverse a number of records specified by the WC Register. The WC Register must be loaded with the 2's complement of the number of records to be spaced over. CB-3 MTTF sets when the WC Register overflows and the last record has been passed over. Note that an attempt to do a Space Reverse operation when tape is at BOT is an illegal function that sets the SC-2 ILLEGAL FUNCTION flip-flop and ends the operation. A Space Reverse operation is terminated if a File Mark, BOT, or WCOV is encountered.

9.10.1.9 Rewind – The Rewind operation causes the tape to rewind at high speed (150 ips) to BOT. The WC and CA Registers need not be loaded for this operation. CB-3 MTTF is set when the selected transport asserts Rewind Status. After one transport is given the command to rewind another transport can be selected for other operations. If the selected unit is rewinding, C TUR is false (not ready) and no operations can be performed on that transport.

9.10.1.10 Continuous Operation – As previously stated, an operation ends when the CB-3 MTTF (JOB DONE) flag is set. To continue an operation after CB-3 MTTF sets, the program must execute the LFGR instruction before SDWN (tape settling down time) to restart the transport and continue the operation. Note that the WC and CA Registers may have to be loaded to select new Word Count and Memory Address parameters. The operation continues until the WC Registers overflow and the operation is terminated.

9.10.2 Programming Notes and Examples

This section is not designed to teach programming but to give some programming notes and examples to be used in programming the TM8-E. For programming information, refer to the following PDP-8/E handbooks:

a. *Introduction to Programming,* 1970
b. *PDP-8/E & PDP-8/M Small Computer Handbook,* 1972

9.10.2.1 Programming Notes – The only programming restrictions to be considered are those that generate SC-2 ILLEGAL FUNCTIONS (Table 9-13), which includes attempting to perform Read operations after Write operations. To read after writing a record, the program must do at least one tape move operation, i.e., Space Reverse or Rewind.

9.10.2.2 Programming Examples – The following routine is an example of the method to be used to program the TM8-E. Note that in this particular example program interrupts are not used.

The general method of calling this TM8-E routine is as follows:

a. Set locations "COMMAND" (Figure 9-8), "CUR ADR," "WRD CNT," and "FUNCTN" (Figure 9-9) as indicated at the end of the TM8-E routine.

b. Execute "JMS TM8-E."

The routine returns to the next location if and only if the CB-3 ERROR flag is set with the final contents of the Function/Status Register in the MQ and the final contents of the Main Status Register in the AC. Refer to Table 9-13 for conditions to set the CB-3 ERROR flag. The routine returns to the second location following "JMS TM8" if the ERROR flag is cleared (the AC is all 0s and the MQ is unchanged).

```
TM8E,     0                    Enter here.
          CLA                  Ensure AC = 0000
          CLF                  Clear TM8-E flags.
          TAD       COMMAND    Get drive, parity, field, and density.
          LCMR                 Load Command Register.
          CLA CMA              Get starting address minus one.
          TAD       CURADR
          LCAR                 Load CA Register.
          TAD       WRDCNT     Get 2's complement of the number of words to be transferred
                               or records to be spaced.
          LWCR                 Load WC Register.
          TAD       FUNCTION   Get Function, Gap, GO bit, and EMA Increment.
          LFGR                 Load Function Register and GO.
          SKEF                 Wait for ERROR flag or MTTF flag.
          SKP
          JMP       TM8ENO     ERROR flag set.
          SKTD
          JMP       .-4
          SKEF                 MTTF set? ERROR flag set?
          JMP       TM8EOK     No. No errors reported for this operation.
TM8ENO,   RFSR                 ERROR flag set. Read Function/Status.
          MQL                  Register and load into MQ.
          RMSR                 Read Main Status Register and leave in AC.
          SKP                  Bypass return address update if in error.
TM8EOK,   ISZ       TM8E       No error reported then update return address.
          CLF                  Clear TM8-E flags.
          JMP 1     TM8E       Exit.
COMMAND,  0         This location must contain all information to be loaded into the TM8-E Command
                    Register.
FUNCTION, 0         This location must contain all information to be loaded into the TM8-E Function
                    Register.
CURADR,   0         This location must contain the first memory address minus one to be used in
                    Write, Read, or Read/Compare operations.
WRDCNT,   0         This location must contain the 2's complement of absolute value of the number
                    of words to be transferred in Write, Read or Read/Compare operations, or the
                    absolute number of records to be spaced in Space Forward or Space Reverse
                    operations.
```

The following is an example of a TM8-E routine using the Program Interrupt System.

```
TM8-E     0                    Enter here.
          CLA                  Clear AC (AC = 0000).
          CLF                  Clear TM8-E flags.
          TAD       COMMAND    Get drive, parity, field, and density (Table 9-12).
          IOF                  Turn PDP-8/E Interrupt System off.
          LCMR                 Load Command Register (Table 9-11).
          CLA CMA              Get starting address minus one.
          TAD                  CURADR.
          LCAR                 Load CA Register.
          TAD       WRDCNT     Get 2's complement of number of words to be transferred or
                               records to be spaced.
          LWCR                 Load WC Register.
```

```
TM8-E (Cont)    TAD          FUNCTN    Get Function, Gap, GO bit, and EMA Increment (Table 9-13).
                LFGR                   Load Function Register and GO (Table 9-13).
                ION                    Turn on program interrupt system.
                INT SET,               ERROR flag set.
Poll another    TM8-EOK                Service another device if Interrupt Request is made.
Device
TM8-E No,       RFSR                   If ERROR flag is set then Read Function/Status Register and
                                       load into MQ.
                MQL
                RMSR                   Read Main Status Register and leave in AC.
TM8EOK,         ISZ          TM8-E     No error reported then update return address.
                CLF                    Clear TM8-E flags.
                JMP 1        2
                INT SER                Continue servicing other devices.
```

SECTION 4 DETAILED LOGIC

The logic in the TM8-E is broken into functional groups for discussion purposes. Figure 9-21 should be used to understand the interaction of the logic, signal flow between groups of logic, and the input or output signals. The purpose of each group of logic is discussed in Paragraph 9.8.

NOTE

The signals on the TM8-E print set are preceded by two letters and a number to indicate the origin of the signal, i.e., a signal with SC1 in front of it originates on sheet 1 of the status and control module prints. Signals without prefixes are OMNIBUS signals.

9.11 M8321 OUTPUT CONTROL MODULE

9.11.1 Input/Output Instruction Decoder

The I/O Instruction Decoders (Figure 9-21) decode instructions from the Memory Data Bus and generate signals to control the operation of the TM8-E. Bits MD 3 through MD 11 are gated by I/O PAUSE when an I/O instruction is executed by the processor. Bits MD 3 to MD 6 generate a signal, 67XX, which partially enables the gates to the I/O Decoders. MD 7 and MD 8 generate a signal (670X, 671X, or 672X) to apply bits MD 9, MD 10, and MD 11 to the I/O Decoder. Each I/O Decoder is an 8251 IC; the 8251 IC is a Binary-to-Decimal Decoder (see Appendix A of Volume 1 for a truth table, logic diagram, and pin locations), which decodes MD 9 through MD 11 and produces a low on one output line. The low out of the 8251 IC indicates which instruction is to be executed. As an example, a 670X instruction with MD 9 low and MD 10 and 11 high (100) produces a low on pin 4 of the 670X Decoder to indicate that a LFGR instruction (6706) was executed by the program. INT I/O L is grounded to prevent execution of IOT instructions by the processor while TM8-E instructions are underway.

9.11.2 C Line Select Logic

The C Line Select logic (Figure 9-21) controls the direction of data flow between the Data Bus and AC and determines if the AC is to be cleared or not. Table 9-16 shows the status of C0 and C1 to transfer data between the AC and Data Bus using the TM8-E IOT instructions.

9.11.3 TP3 Logic

TP3 is used to enable the selection of the 670X I/O Decoder and is used throughout the TM8-E to enable the execution of instructions (Figure 9-21) and to enable data transfers using the Single Cycle Data Break Interface.

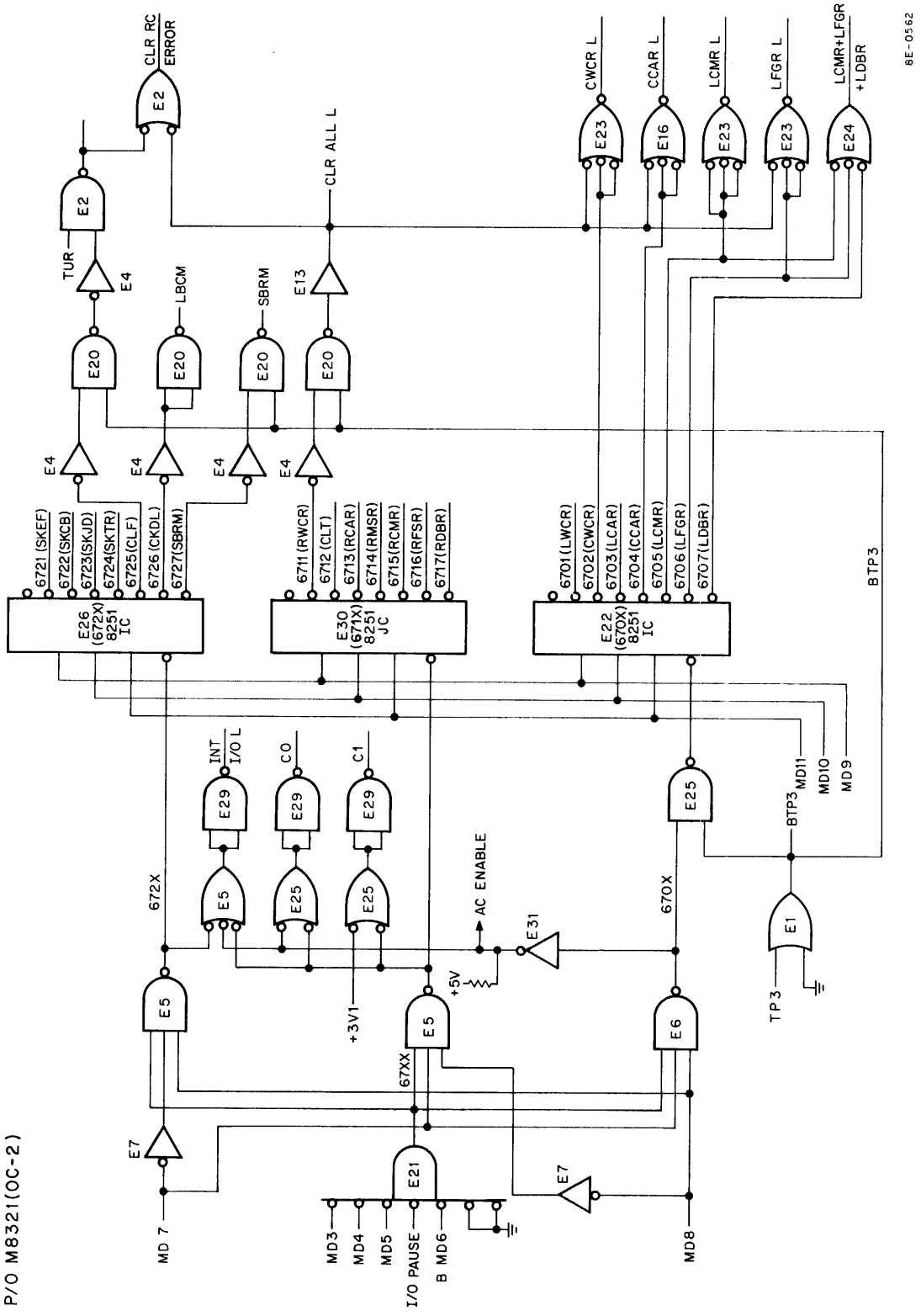


Figure 9-21 IOT Decoder Logic

Table 9-16
C Line Select Levels for TM8-E Transfer Operations

Instruction	C0	C1	Transfer of Operation
LWCR	Low	High	AC → Data Bus 0 → AC
LCAR	Low	High	AC → Data Bus 0 → AC
LCMR	Low	High	AC → Data Bus 0 → AC
LFGR	Low	High	AC → Data Bus 0 → AC
LDBR	Low	High	AC → Data Bus 0 → AC
RWCR	Low	Low	Data Bus → AC
RCAR	Low	Low	Data Bus → AC
RMSR	Low	Low	Data Bus → AC
RCMR	Low	Low	Data Bus → AC
RFSR	Low	Low	Data Bus → AC
RDBR	Low	Low	Data Bus → AC

9.11.4 CLR ALL Logic

CLR ALL L (Figure 9-21) is asserted to clear TM8-E logic under the following conditions:

a. At TP3 time, if a CLT (6712) instruction is executed by the program.

b. When a CLF (6725) instruction is executed by the program if C TUR is true.

c. When PWR OK H from the processor is lost due to a power failure.

d. When the processor asserts INIT H. This occurs during power up or when the CLEAR key is depressed on the PDP-8/E console.

9.11.5 AC ENABLE Logic

OC-2 AC ENABLE (Figure 9-21) is asserted when a 670X instruction is executed by the program to enable gates to apply the Data Bus information to the TM8-E registers that are loaded from the AC (Figure 9-27) and Control C0 and C1 levels (Paragraph 9.11.1).

9.11.6 Skip Logic

The Skip logic (Figure 9-22) asserts OC-2 SKIP BUS L and causes the processor to skip an instruction when the following conditions exist.

a. The 6721 (SKEF) instruction is executed and the SC-2 ERROR flag is set.
b. The 6722 (SKCB) instruction is executed and SC-1 CNTL BSY flag is set.
c. The 6723 (SKJD) instruction is executed and CB-3 MTTF flag is set.
d. The 6724 (SKTR) instruction is executed and C TUR L is true.

9.11.7 Output Control Function Decoder

The Output Control Function Decoder (Figure 9-23) is an 8251 IC, which decodes the three most significant bits of the Function Register and determines what function the TU10 Transport performs (Table 9-12). The 8251 IC is a BCD-to-Decimal Decoder (see Appendix A, Volume 1, for truth table, logic, and pin locations) which decodes FR0, FR1, and FR2 and produces a low on one output line. The low out of the 8251 IC indicates the function to be performed. As an example, if FR0 is low, and FR1 and FR2 are high, pin 9 is low indicating a Write operation is to be performed. The outputs of the Function Decoder, applied to the TU10, are defined in Table 9-15 and Figure 9-7.

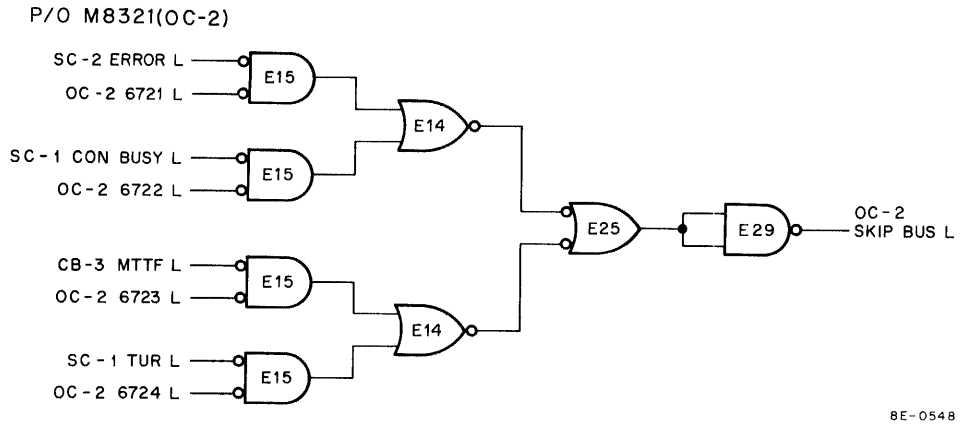


Figure 9-22 Skip Logic

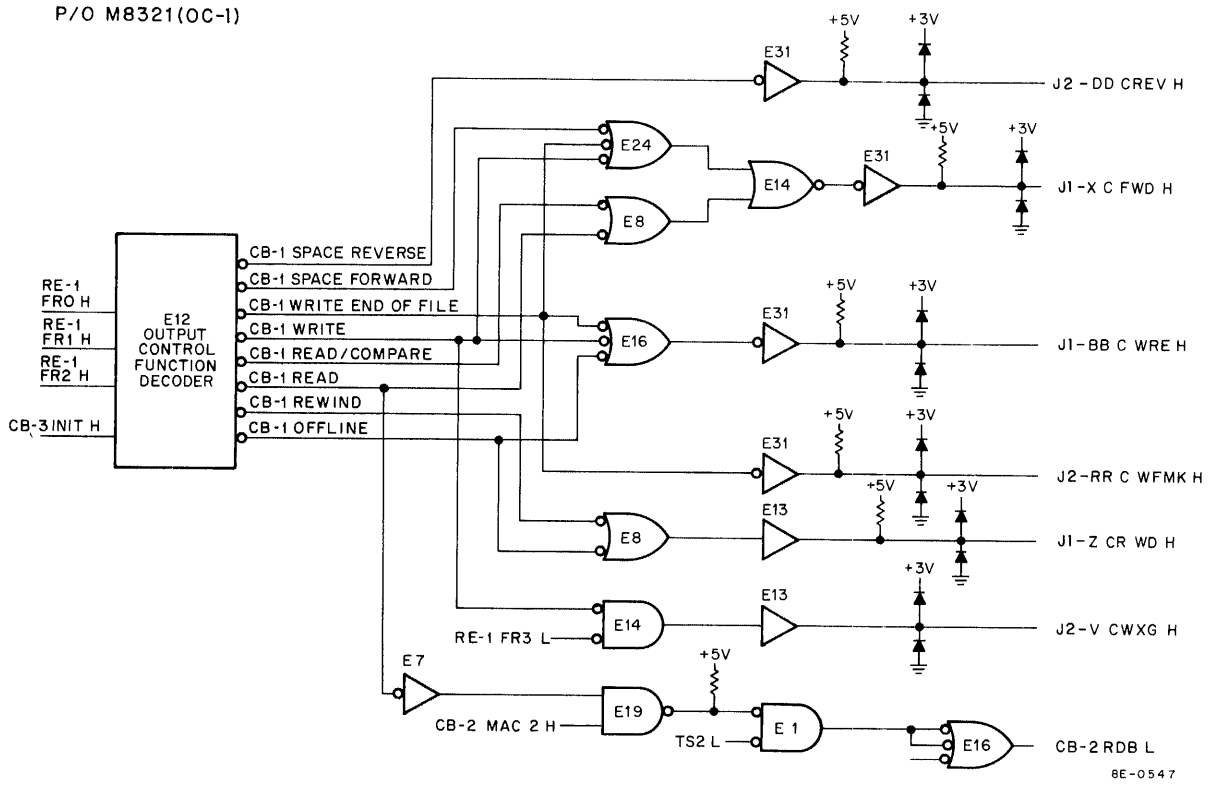


Figure 9-23 Output Control Function Decoder

9.11.8 Read/Compare Logic

The Read/Compare logic consists of 12 Exclusive-OR gates and the OC-1 R/C ERROR flag (flip-flop). The 12 bits of data from the Memory Data Bus (data read from memory) are Exclusively-ORed with 12 bits of data from the Data Register (data read from tape). During the data break, at TP3 time, if the data from memory is different from data read from DECmagtape the SC-1 R/C ERROR flag is set and CA incrementation stops. Tape motion continues until an LRC strobe is obtained at End of Record. RE-1 DEN 5 H and RE-1 DEN 8 H are used to enable a gate on the outputs of the Exclusive-OR gates for the four most significant bits to prevent them from causing a Read/Compare Error when a 9-track transport is selected. RE-1 R/C ENABLE is always high when a Read/Compare function is selected by the program. Refer to D-TD-TM8-E-1, sheet 2, for the timing during a Read/Compare operation.

9.11.9 Write Data Select Logic

The Write Data Select logic selects 6 or 8 bits of data from memory to be written on DECmagtape (Figure 9-24). To write on a 9-track transport, the gates labeled C on Figure 9-24 are enabled by CB-1 WR 9 H to apply 8 bits of data from the Data Buffer Register to the selected transport (see D-TD-TM8-E-1, sheet 8, for timing).

When writing on a 7-track transport, CB-1 WR 1st 7 H enables the gates (labeled B in Figure 9-24) for the six most significant bits and then the gates (labeled A in Figure 9-24) are enabled by CB-1 WR 2nd 7 H for the six least significant bits. The control signals for the gates originate in the control logic shown in Figure 9-46. The outputs to the transport are limited to 0.0V and +3V levels by the diode and resistor networks tied to the output lines.

9.12 TM8-E REGISTERS (M8327)

The TM8-E Registers are used to address memory, count the words in a data transfer, select DECmagtape operations, and generate command signals for the TM8-E control logic and the TU10 Tape Transports. Each of the registers used in the TM8-E are discussed in the following paragraphs; the Status Register is discussed with the Transport Status and Control logic in Paragraph 9.13.1.

9.12.1 Data Buffer Register and Multiplexer

The Data Buffer Register and Multiplexer (Figure 9-25) provides temporary storage for data manipulation (transfers and Read/Compares). Inputs to the Data Multiplexer come from memory (MD 0 through MD 11), from the AC (DATA 0 – DATA 11), or from the tape (CRD 0 through CRD 7). The Data Multiplexer is a 74153 IC (refer to Section 7 for logic diagram, truth table and pin locations) which selects one of the four data inputs to be applied to the Data Buffer Register. CB-2 DB MPX A and CB-2 DB MPX B controls the selection of data that is supplied to the Data Buffer Register. Table 9-17 shows the levels required to load the Data Buffer Register for each operation. CB-1 DBC 1 and CB-1 DBC 2 are used to clock the output of the multiplexer into the Data Buffer Register. The Data Buffer Register is two 74174 ICs (refer to Section 7 for truth table, logic diagram, and pin locations) each containing six flip-flops that are set or cleared by the input from the Multiplexer. The contents of the Data Buffer Register are applied to the Read/Compare logic, to output control logic, and to an 8235 IC (refer to Appendix A, Volume 1, for truth table, logic diagram and pin locations) as shown in Figure 9-26. During a Read operation or when a RDBR instruction is executed, the data is transferred to the Data Bus. During a Read operation, data is transferred to a memory location selected by the Current Address Register during Single Cycle Data Break. If the RDBR (6717) instruction is executed, the data is transferred to the AC via Data Bus. Refer to the flow diagram (Figure 9-20 and Figure 9-15) for an illustration of this operation. The timing diagrams for these operations are shown in Drawing No. D-TD-TM8-E-1, sheets 1 through 9.

9.12.2 AC Input Gating

The AC Input Gating (Figure 9-27) is used as a buffer between the Data Bus (inputs from the AC) and the TM8-E Registers. OC-2 AC ENABLE L is asserted (low) any time a 670X instruction is executed by the program to transfer data from the AC to the TM8-E Registers. The outputs of the NAND gates enabled by OC-2 AC ENABLE are applied to the Command, Data, and Function Registers, and to two 74174 ICs, which provide a Holding Buffer for inputs from the AC. The 74174 ICs (refer to Section 7 for truth table, logic diagram, and pin locations) are 6-bit buffer registers for inputs to the WC and CA Registers and bits 6 through 8 of the Command Register. SC-1 B TP3 is used to clock the outputs of the NAND gates into the AC Holding Buffer Register. The outputs of the AC Holding Buffer Register are applied to the WC and CA Registers (Figure 9-28).

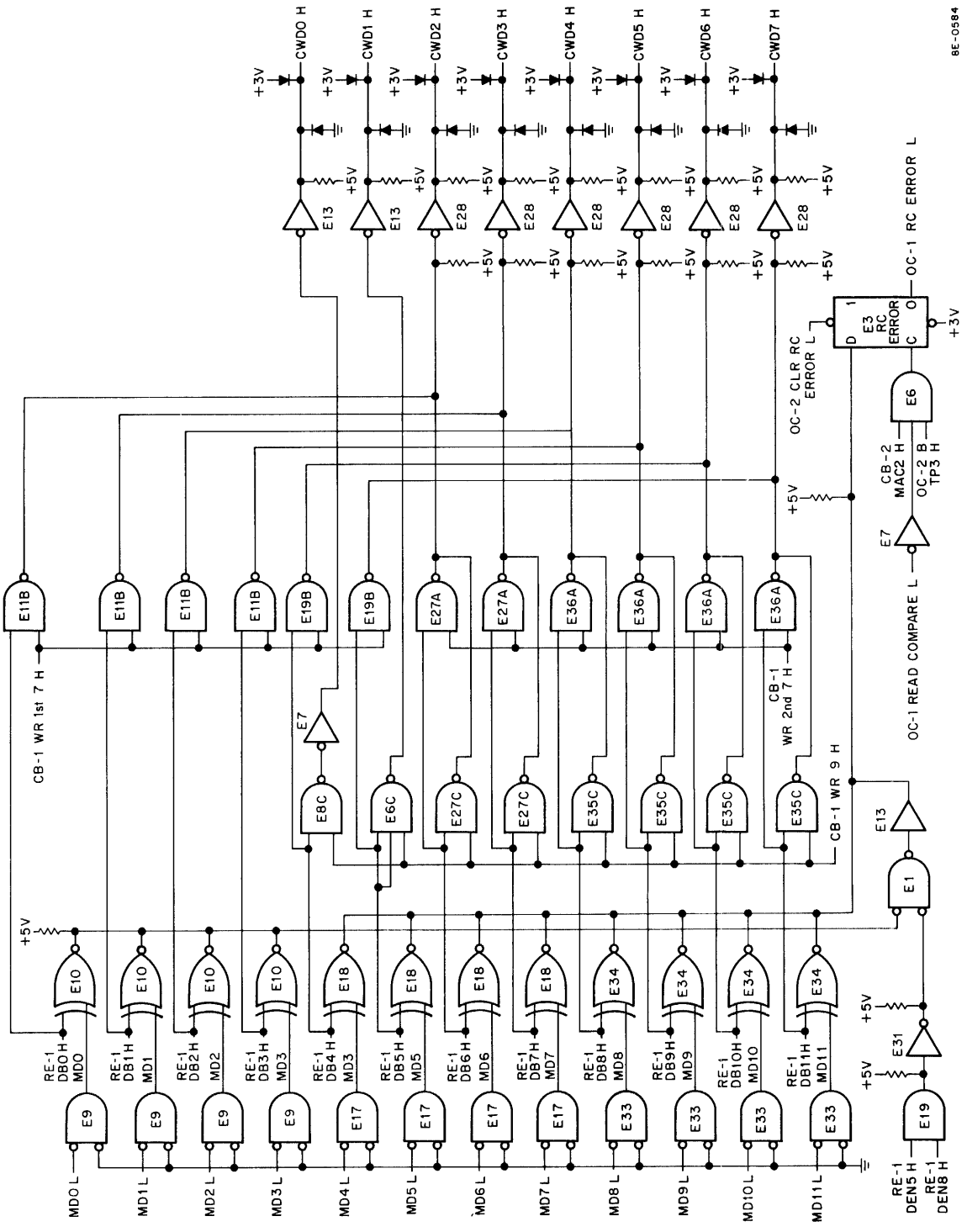


Figure 9-24 Read/Compare and Write Data Select Logic

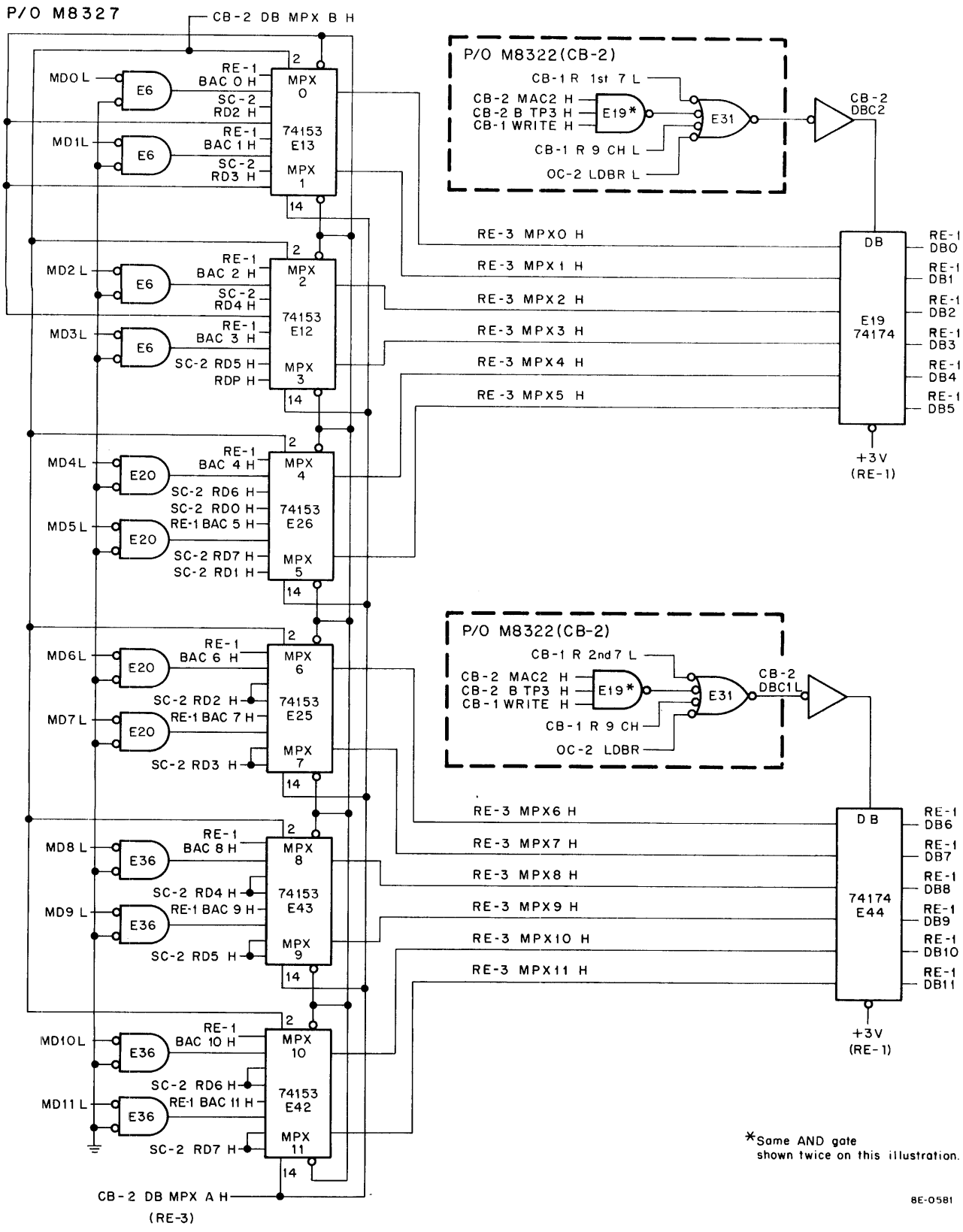


Figure 9-25 Input Data Multiplexer and Data Register

Table 9-17
Data Multiplexer Selection Levels

Operation	CB-2 DB MPXA H (pin 14)	CB-2 DB MPXB H (pin 2)
Load Data Buffer	low	low
Write	high	low
Read 7 Channels	low	high
Read 9 Channels	high	high

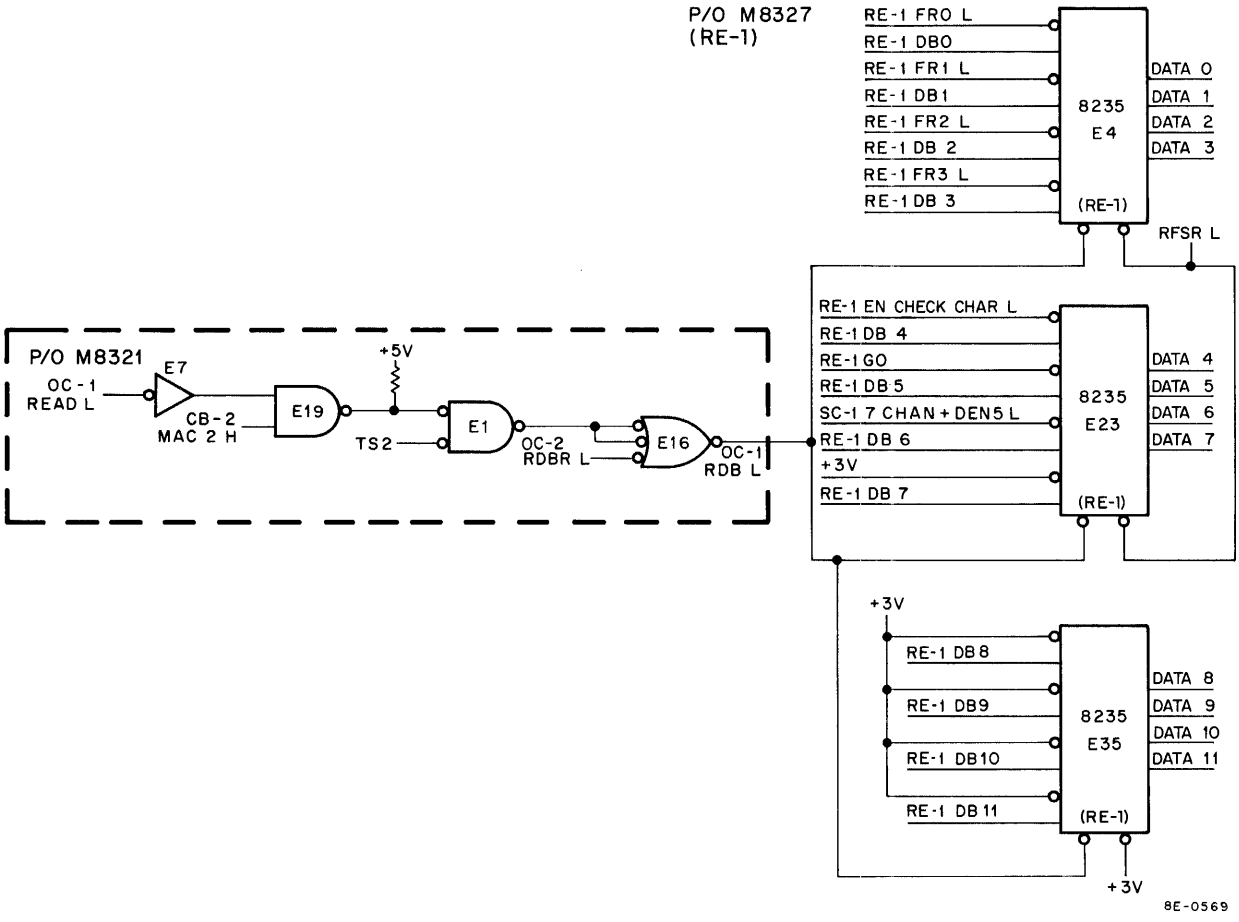


Figure 9-26 Data Register and Function Register Output Multiplexer

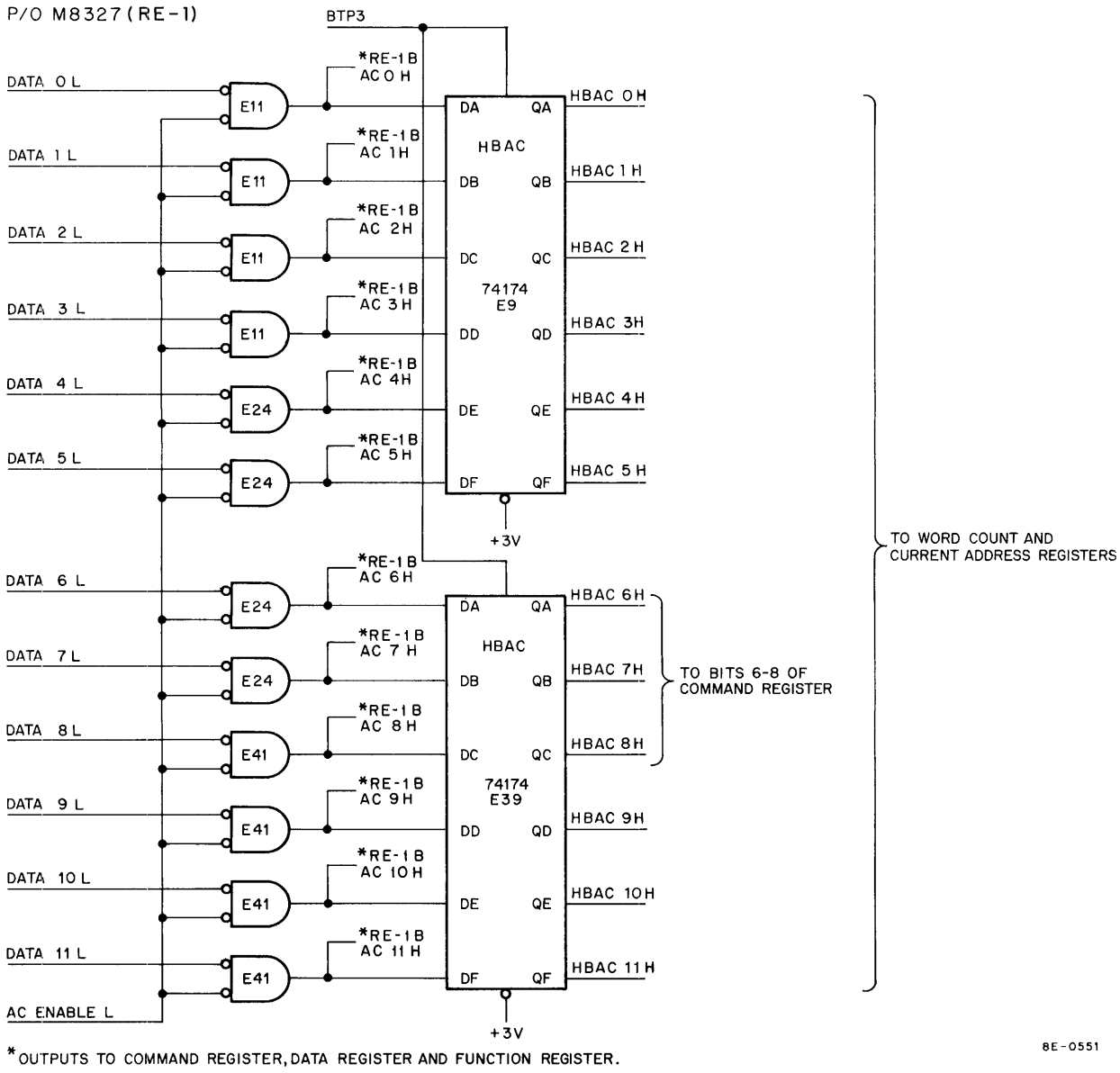


Figure 9-27 AC Input Gating and Holding Buffer Register

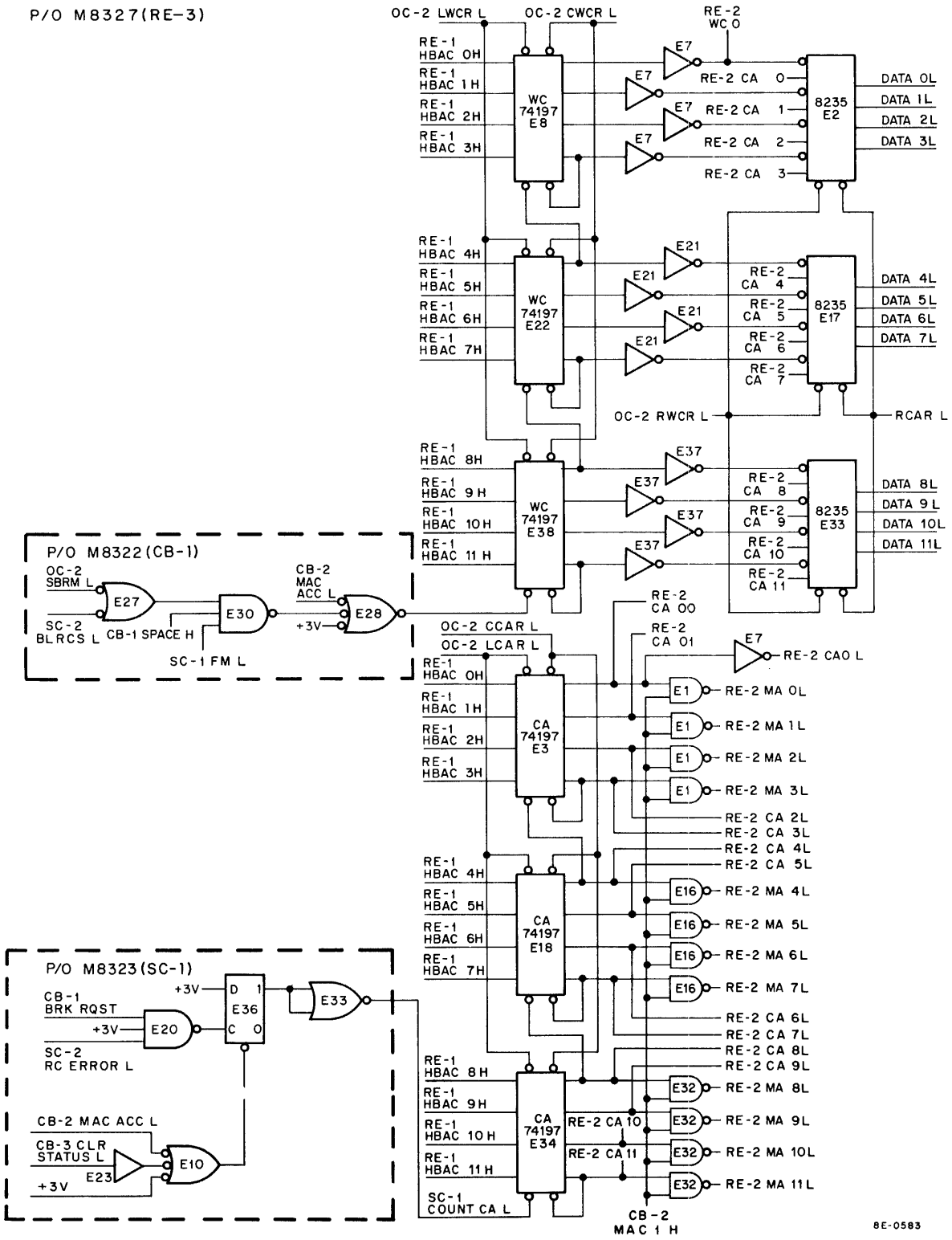


Figure 9-28 Current Address and Word Count Registers

9.12.3 Current Address (CA) Register

The Current Address Register (Figure 9-28) is a ripple counter that sequentially addresses locations in memory by incrementing before each data transfer. The CA Register is loaded with a 12-bit address that is one less than the desired starting address. The CA Register is incremented by the leading edge of SC-1 COUNT CA L (Figure 9-28) each time a BRK RQST is made by the TM8-E. CB-2 MAC ACC is asserted after a BRK RQST is granted to the TM8-E and removes the SC-1 COUNT CA L signal from the CA Register. The CA Register is not incremented when SC-1 COUNT CA L goes high because the counter increments only a high-to-low transition of the signal. The CA Register is loaded by the LCAR instruction before each DECmagtape operation and must not be loaded during CNTL BSY.

The output of the CA Register is applied to the MA lines when CB-2 MAC 1 H enables the NAND gates (Figure 9-28) to select a location in memory which contains data to be read or a location to store data from the DECmagtape. The contents of the CA Register are also applied to an 8235 IC (refer to Appendix A of Volume 1 for truth table, logic diagram, and pin locations) for transfer to the AC when an RCAR instruction is executed by the program. The CA Register is read by the program during error check routines and maintenance operations to determine what address in memory generated an error. The CA Register is cleared by an CCAR instruction.

9.12.4 Word Count (WC) Register

The Word Count Register is a ripple counter that (Figure 9-28) counts the data words transferred to or from the DECmagtape during data transfers and counts the records during space operations. The WC Register is loaded from the AC with the 2's complement of the number of words to be transferred or number of records to be spaced when a LWCR instruction is executed by the program.

The output of the WC Register is applied to an 8235 IC (see Appendix A, Volume 1, for truth table, logic diagram, and pin locations) and is transferred to the AC when an RWCR instruction is executed by the program. When bit 0 makes the transition from the high to low state. RE-2 WC 0 is applied to the CB-1 WCOV flip-flop (Figure 9-21). CB-1 WCOV indicates to the control logic that the data transfer is complete (the specified number of words have been transferred). Word Count is incremented during the Break cycle when SC-1 COUNT WC makes a high to low transition by asserting one of the following:

a. CB-2 MAC ACC L during a Read or Write operation.
b. C LRCS L during a CB-1 SPACE operation if a File Mark is not detected.

9.12.5 Function Register

The Function Register (Figure 9-29) is loaded with 6 bits of data from the AC by an LFGR instruction. The 6 bits determine the function (Table 9-12) the TU10 Transport is to perform and provide control signals to initiate DECmagtape operations. The Function Register consists of two 74175 ICs (refer to Section 7 for truth table, logic diagram, and pin locations) which contain the flip-flops that are set or cleared by bits from the AC. The three most significant bits of the Function Register (FR0 through FR2) are applied to the output control Function Decoder (Figure 9-23) and the control Function Decoder (Figure 9-39). FR3 through FR6 are applied to the control logic to accomplish the functions shown in Table 9-12. The CB-3 MTTF input to the 74175 IC clears the three least significant bits FR4 through FR6 when the CB-3 MTTF (JOB DONE) flag is set at LRCS time (Figure 9-42).

The outputs of the Function Register are also applied to an output multiplexer (Figure 9-28) for transfer to the AC when an RFSR instruction is executed by the program. The 8235 IC (refer to Appendix A, Volume 1, for truth table, logic diagram, and pin locations) transfers the Function and Status to the Data Bus for display in the AC or evaluation by the program when RE-1 RFSR L is asserted. RE-1 RFSR L is asserted when an RFSR instruction is executed by the program.

NOTE

The Function Register must be the last register loaded because it contains the GO bit, which initiates CNTL BSY, PRESET, and SET to start the tape transport.

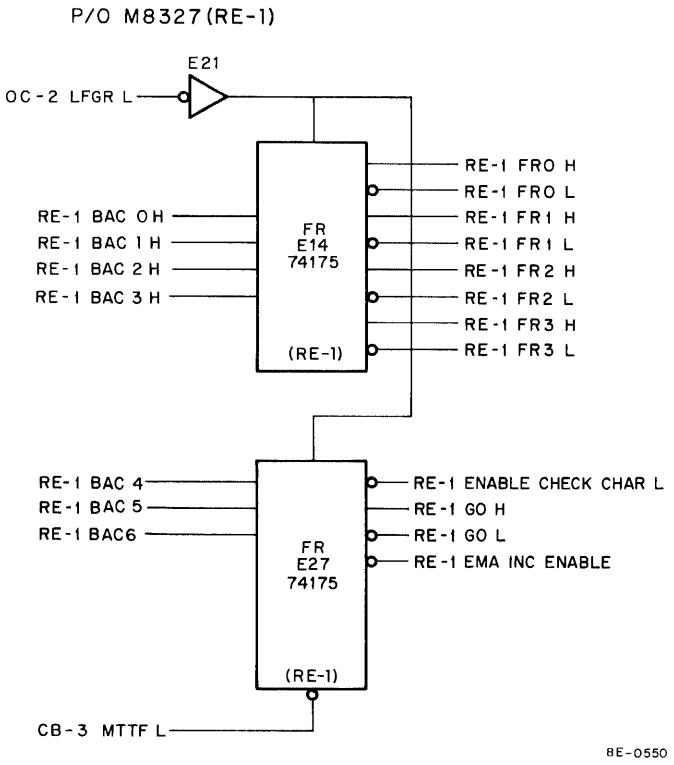


Figure 9-29 Function Register

9.12.6 Command Register

The Command Register (Figure 9-30) consists of nine flip-flops and a 3-bit ripple counter that are loaded from the AC when an LCMR instruction is executed by the program (Table 9-11).

The four flip-flops that receive RE-1 BAC 0 through RE-1 BAC 3 (Table 9-11) as inputs are on a 74175 IC (refer to Section 7, for truth table, logic diagram, and pin locations). Three of the flip-flops on this IC generate SEL 0 through SEL 2 for indication of selection of one of the TU10 Transports and provide an input to the Buffered Command Register for TU10 Transport selection (Paragraph 9.12.7). AC 03 is used to select odd or even parity mode for the TU10 Transport. If this flip-flop is in a 0 state, even parity is selected and C PEVN L to the TU10 Master System is asserted.

RE-1 BAC 4, RE-1 BAC 5, and RE-1 BAC 9 through RE-1 BAC 11 are applied to a 74174 IC (refer to Section 7 for truth table, logic diagram, and pin locations), containing six flip-flops that are loaded by the inputs from the AC (Table 9-11).

The remainder of the bits from the AC (AC 6 through AC 8) are applied to a 74197 I (refer to Appendix A, Volume 1, for truth table, logic diagram, and pin locations containing three flip-flops to select a memory field during data transfer. The 74197 IC is a 3-bit ripple counter that is incremented by SC-1 EMA INC L if bit 6 in the Function Register is set (1). The output of the 74197 IC (RE-1 EMA 0 – RE-1EMA 2) is applied to the OMNIBUS when CB-2 MAC 1 H enables the three AND gates (Figure 9-0) during a Single Cycle Data Break. Refer to Paragraph 9.13.3 for a discussion of the SC-1 EMA INC L signal generation.

The contents of the Command Register are transferred to the Data Bus when the progam executes an RCMR instruction to assert the control input of the 8235 ICs (Figure 9-30). The Command Register is cleared by CB-3 CLR ALL L (Paragraph 9.11.4).

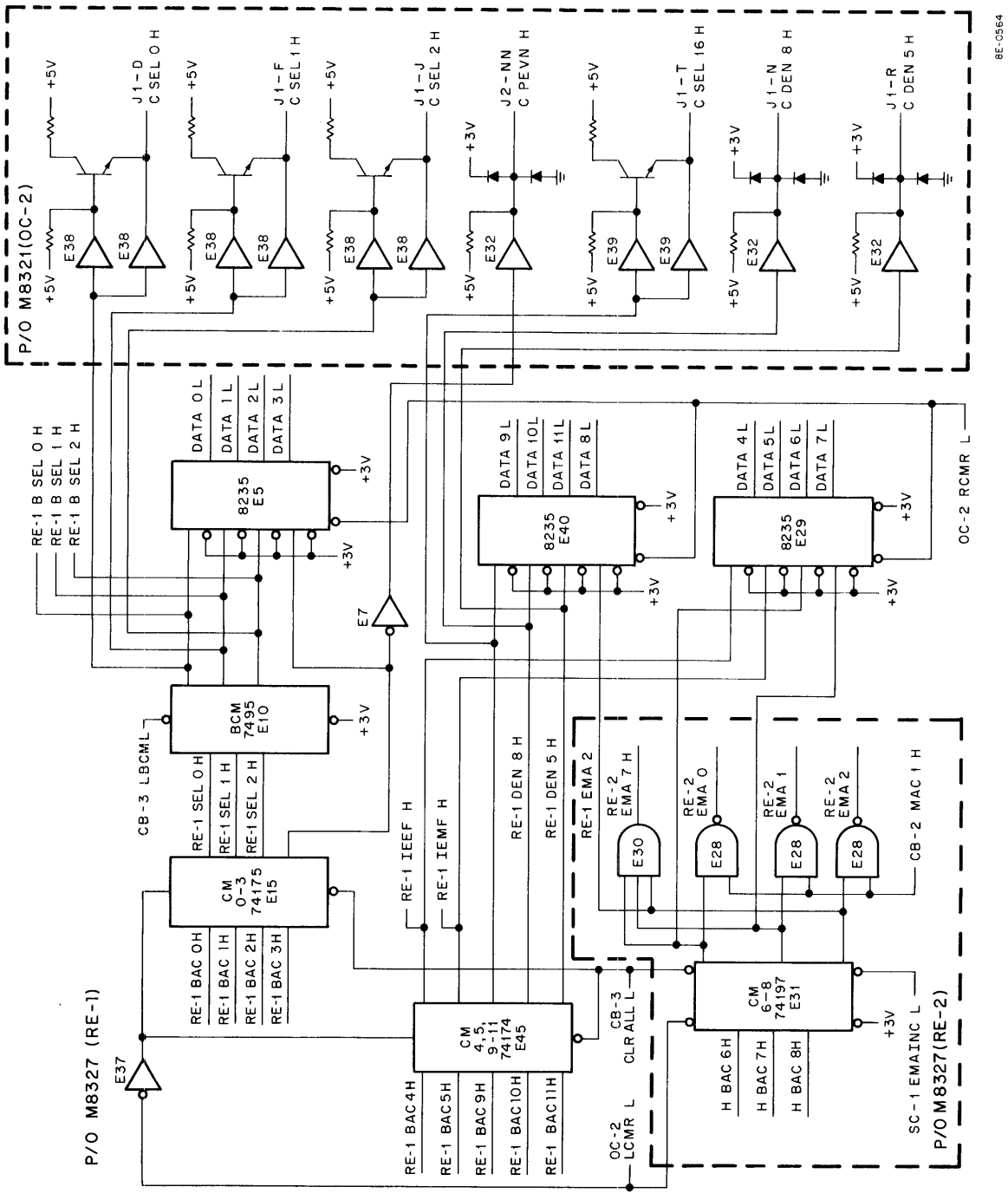


Figure 9-30 Command Register and Multiplexer

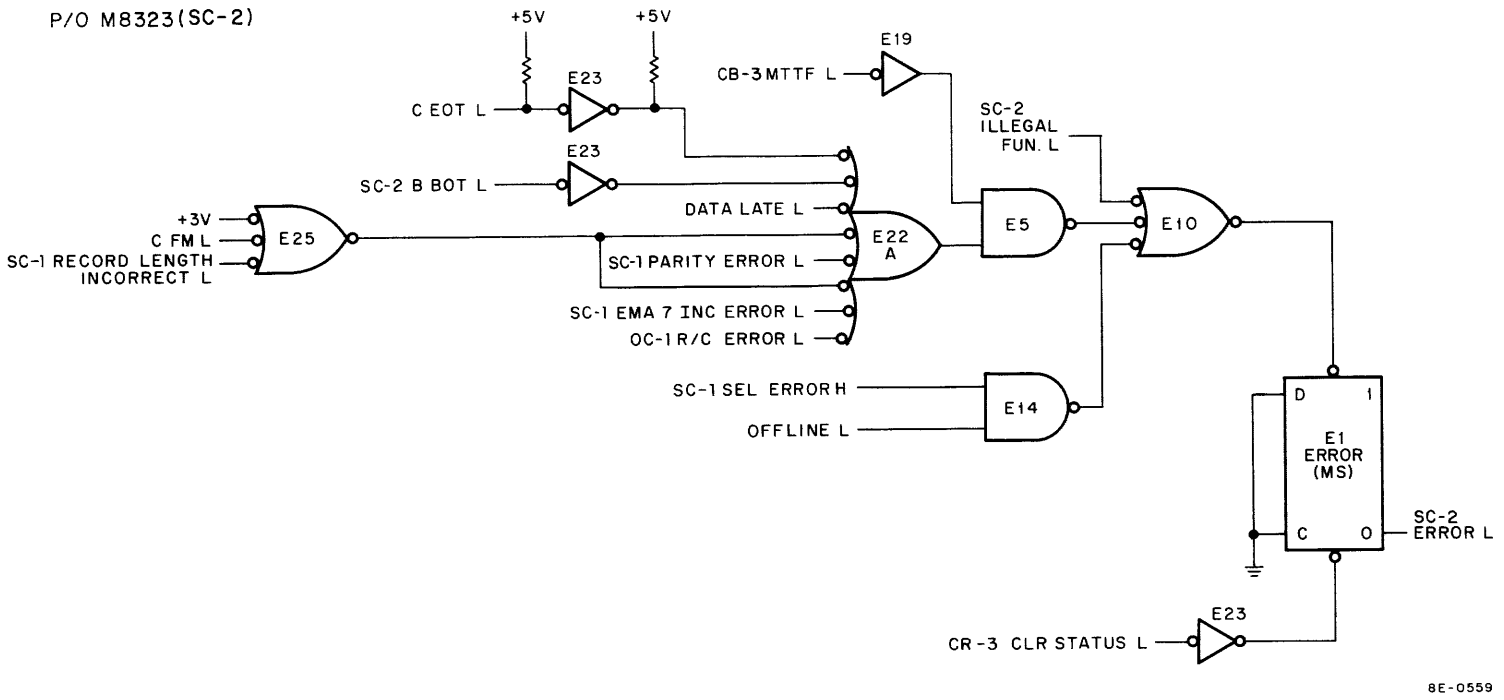


Figure 9-31 Error Flags

9.12.7 Buffered Command Register (BCM)

The Buffered Command Register (Figure 9-30) receives RE-1 SEL 0 through RE-1 SEL 2 as inputs from the command register. RE-1 B SEL 1 through RE-1 B SEL 2 out of the BCM are applied to the TU10 Master System to select a transport and provides an input to a comparison circuit to determine when a new transport has been selected (Figure 9-43). CB-2 CHG TRANS L is asserted if RE-1 SEL 0 through RE-1 SEL 2 from the command register and RE-1 B SEL 0 through RE-1 B SEL 2 from the Buffered Command Register are different; thus CB-2 CHG TRANS L is asserted if a new transport is selected by the program. The output of the BCM holds the select lines to the previously selected transport in the same state until C SDWN L (settled down) is obtained from the transport. Then the BCM is loaded by RE-2 LBCM L to select a new transport. Thus the BCM allows the program to load the command and select a new transport without deselecting the previously selected transport before it stops.

9.13 M8323 TRANSPORT STATUS AND CONTROL MODULE

The M8323 Transport Status and Control Module consists of the Main Status Register (Table 9-13), Second Status Register (Table 9-14), logic for generation of timing and control signals, and a Data Multiplexer to transfer the contents of the Status Registers to the Data Bus.

9.13.1 Main Status Register

The logic elements that make up the Main Status Register perform as follows.

9.13.1.1 SC-2 ERROR Flag Logic – The SC-2 ERROR flag (Figure 9-31) is set immediately if the program attempts an illegal function or if SC-2 SEL ERROR is asserted by the selected transport. The SC-2 ERROR flag is set after CB-3 MTTF is set if any of the following errors are detected.

a. EOT
b. BOT
c. DATA LATE
d. PARITY ERROR (LRCE, CRCE, or VPE in Second Status Register)
e. REC LNG INCORRECT
f. EMA 7 INC ERROR (Second Status Register)
g. R/C ERROR
h. File Mark (FM)

9.13.1.2 Illegal Function Logic – The SC-2 ILLEGAL FUNCTION flip-flop (Figure 9-32) is set if the program attempts any of the following SC-2 ILLEGAL FUNCTIONS:

a. The program executes an LCMR, LFGR, or LDBR instruction when the SC-1 CNTL BSY flip-flop is set (Paragraph 9.13.5).

b. Selection of any density other than 800 bpi if a 9-track transport is selected.

c. Selection of a Space Reverse operation when the selected TU10 Transport is at BOT.

d. Selection of Read, Read/Compare, or Space Forward after a Write or Write End of File operation if the same transport is used.

e. Changing to a transport that is not ready (C TUR is false) and SC-1 PRESET is issued.

f. Attempting a Rewind when tape is at BOT.

g. Any Write command issued to a transport with write lockout set.

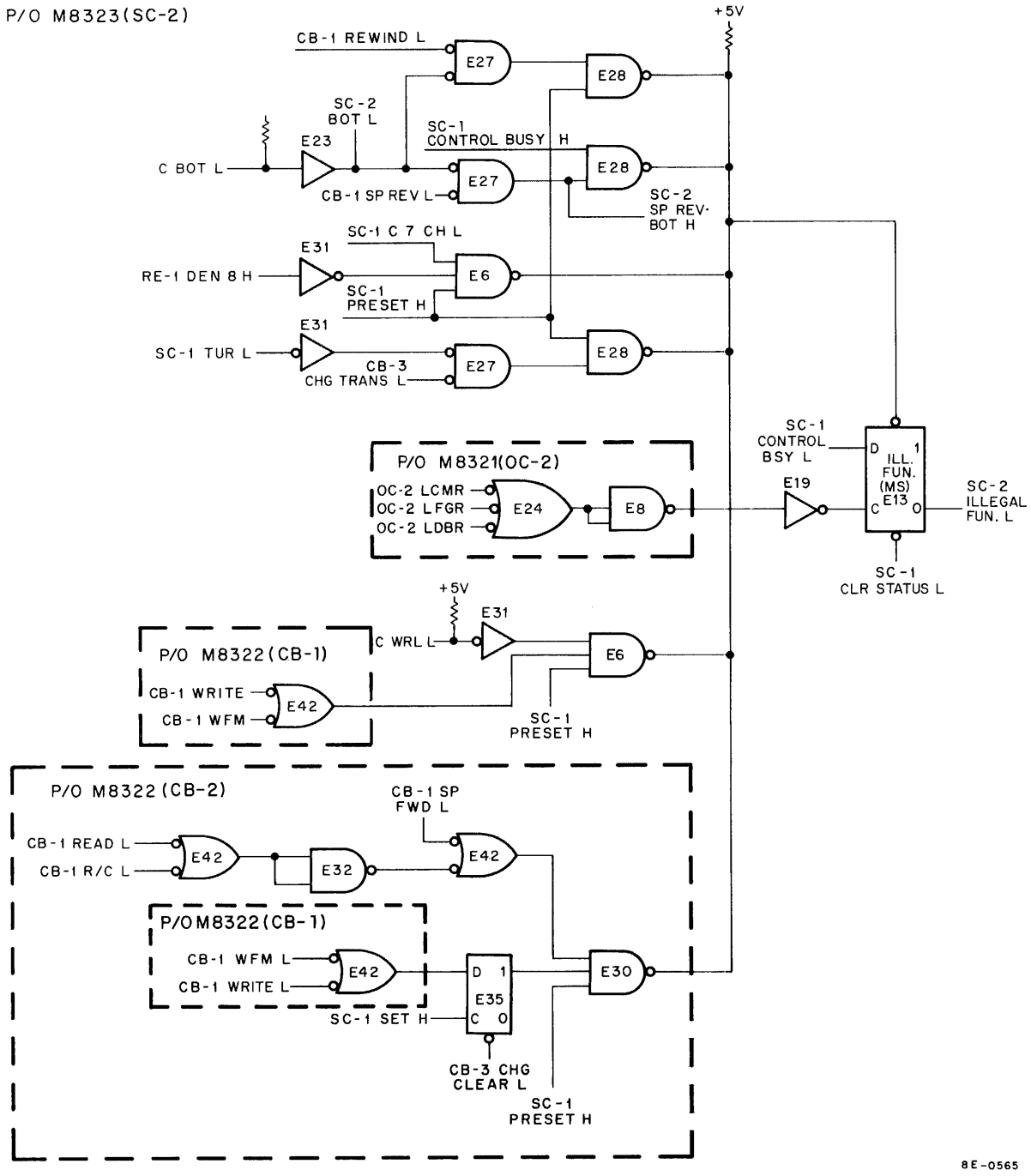


Figure 9-32 Illegal Function Flag and Control Logic

9.13.1.3 Data Late Logic – The SC-1 Data Late (Figure 9-33) flip-flop is set if the computer fails to service a BRK RQST before the next word is transferred to or from tape. A counter made up of flip-flops A, B, and C (Figure 9-33) counts the Read Strobe or Write Strobe pulses generated by the TU10 each time a character is read from or written on tape. SC-1 WRS L or SC-1 B RDS L clocks the three flip-flops (A, B, and C). CB-2 MAC ACC L (Figure 9-33) is asserted after a BRK RQST is granted to the TM8-E by the processor to clear the counter and prevent the SC-1 DATA LATE flip-flop from setting when the next SC-1 WRS or SC-1 B RDS pulse occurs. If a 9-track transport is selected and CB-2 MAC ACC is not asserted by the time the next SC-1 WRS or SC-1 B RDS pulse occurs, the set side of the B flip-flop causes SC-1 DATA LATE to set. The set output of the B flip-flop is applied to the clock input of SC-1 DATA LATE if the NAND gate tied to the set output is not disabled by C 7 CH L or RE-1 DEN 5 H. When a 7-track transport is selected, SC-1 DATA LATE sets after three SC-1 WRS L or SC-1 B RDS L pulses if the counter has not been cleared by CB-2 MAC ACC L. Note that a 7-track transport requires only one Data Break cycle to transfer two data characters to or from tape. The SC-1 DATA LATE flip-flop is always cleared during a Space operation since no data is transferred. SC-1 DATA LATE is also cleared when a File Mark (C FMK) is detected during a Read operation or by CB-3 CLR STATUS L.

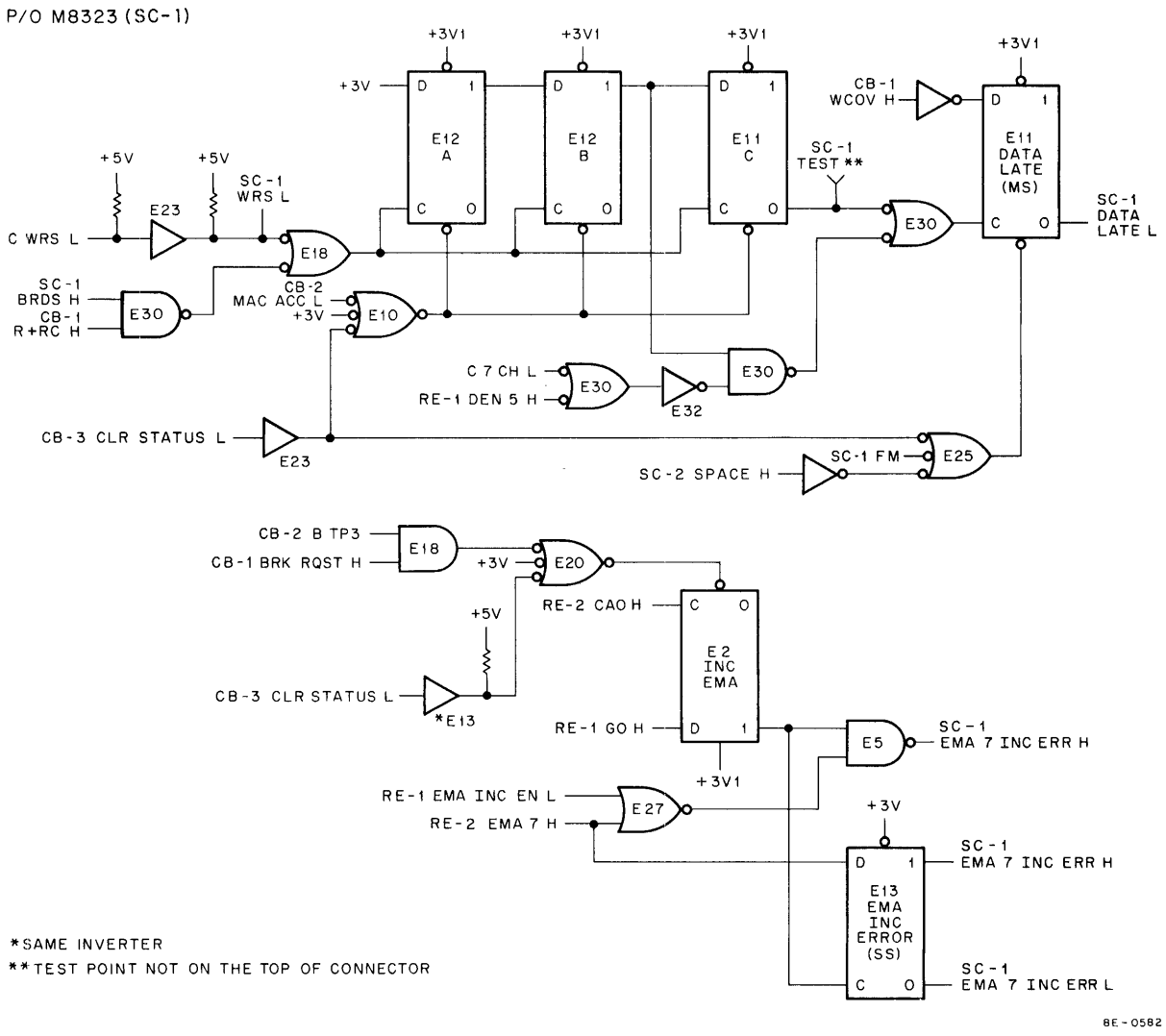


Figure 9-33 Data Late and EMA Increment Error Flags

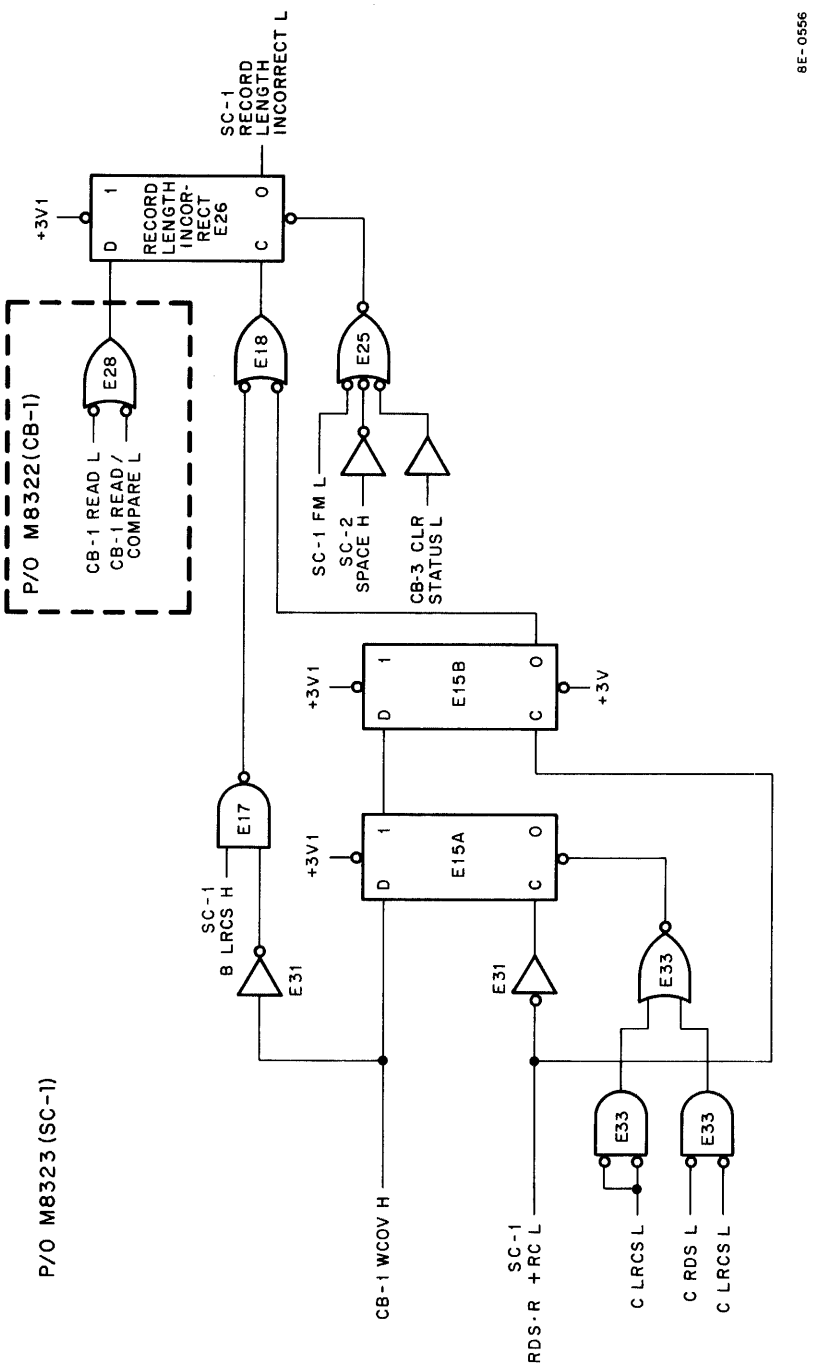


Figure 9-34 Record Length Incorrect Error Detection Logic

9.13.1.4 Record Length Incorrect Logic – The SC-1 RECORD LENGTH INCORRECT flip-flop (Figure 9-34) is set when the number of data words read from the tape and the contents of the WC Register are different (record too long or too short). As previously stated, the WC Register is loaded with the 2's complement of the number of words to be transferred. Word Count is incremented during the data transfer. The WC Register should contain all 0s and generate CB-1 WCOV L before the LRC character is read from tape. If C LRCS H occurs before CB-1 WCOV, gate E33 (Figure 9-34) is enabled, and the SC-1 RECORD LENGTH INCORRECT flip-flop sets. This condition occurs if the WC Register has been loaded with a Word Count greater than the number of words in the record (record is short). To detect a record that is too long, a counter made up of flip-flops A and B (Figure 9-34) counts the RDS pulses that occur after CB-1 WCOV H. If two or more C RDS L pulses occur after CB-1 WCOV and there are no C LRCS L or C CRCS L pulses, the SC-1 RECORD LENGTH INCORRECT flip-flop sets. This condition occurs if the Word Count Register is loaded with a Word Count less than the number of words transferred (record is long). Note that flip-flop A is cleared by C CRCS L or C LRCS L so that SC-1 RECORD LENGTH INCORRECT is not set during the termination of a normal operation.

CB-1 SPACE H and C FILE MARK L keep the SC-1 RECORD LENGTH INCORRECT flip-flop cleared during a Space or Write File Mark operation. CB-3 CLR STATUS L clears the SC-1 RECORD LENGTH INCORRECT flip-flop when the Status Register is cleared by a CLF instruction.

9.13.1.5 Tape Rewinding – Tape Rewinding (C RWS L) is asserted (Figure 9-36) if the selected transport is rewinding.

9.13.1.6 End of Tape – End of Tape (C EOT) is asserted if the End of Tape reflective strip has been detected by the TU10 (Figure 9-31). If C EOT is detected before CB-3 MTTF (JOB DONE) is set, the SC-2 ERROR flip-flop sets and the Main Status Register must be read by the program to determine the cause of the error.

9.13.1.7 Beginning of Tape – Beginning of Tape (C BOT) is asserted when the BOT reflective strip is detected by the TU10. If BOT is detected before CB-3 MTTF (JOB DONE) is set, the SC-2 ERROR flip-flop (Figure 9-31) sets. The Main Status Register must be read by the program to determine the cause of the error.

9.13.1.8 Read/Compare Error – The Read/Compare operation is discussed in Paragraph 9.1.8.

9.13.1.9 Parity Error – The SC-1 PARITY ERROR flip-flop (Figure 9-35) is set if the TU10 detects any of the following errors.

a. C LRCE (Longitudinal Parity Error)
b. C CRCE (Cyclic Redundancy Check Error)
c. C VPE (Vertical Parity Error)

If SC-1 PARITY ERROR is set, the SC-2 ERROR flip-flop (Figure 9-31) sets when MTTF (JOB DONE) sets. SC-1 PARITY ERROR is cleared any time a File Mark is read from tape. During space operations, CB-1 SPACE H keeps SC-1 PARITY ERROR cleared (Figure 9-35) to prevent generation of erroneous parity errors. Note that the C VPE is cleared by the next good word read from tape and will not be seen unless it occurs as the last word read from tape.

9.13.1.10 File Mark (EOF) – The FILE MARK flip-flop (Figure 9-35) is set any time the TU10 detects a File Mark during a Space, Read, or Read/Compare operation (Paragraph 9.1).

9.13.1.11 Select Remote – SC-1 SELR L (Select Remote) (Figure 9-37) is true when the selected transport is OFFLINE (not ready). SC-1 SEL ERROR is set if SC-1 SELR L is lost during data transfer operation.

9.13.1.12 File Protect – File Protect is a 1 when Write Lockout (C WRL L) is asserted by the TU10, indicating that the selected transport has the Write Lockout ring removed. Transports without a Write Lockout ring will set the ILLEGAL FUNCTION flag during SC-1 PRESET time (Figure 9-32) if they are selected for a Write or Write File Mark operation.

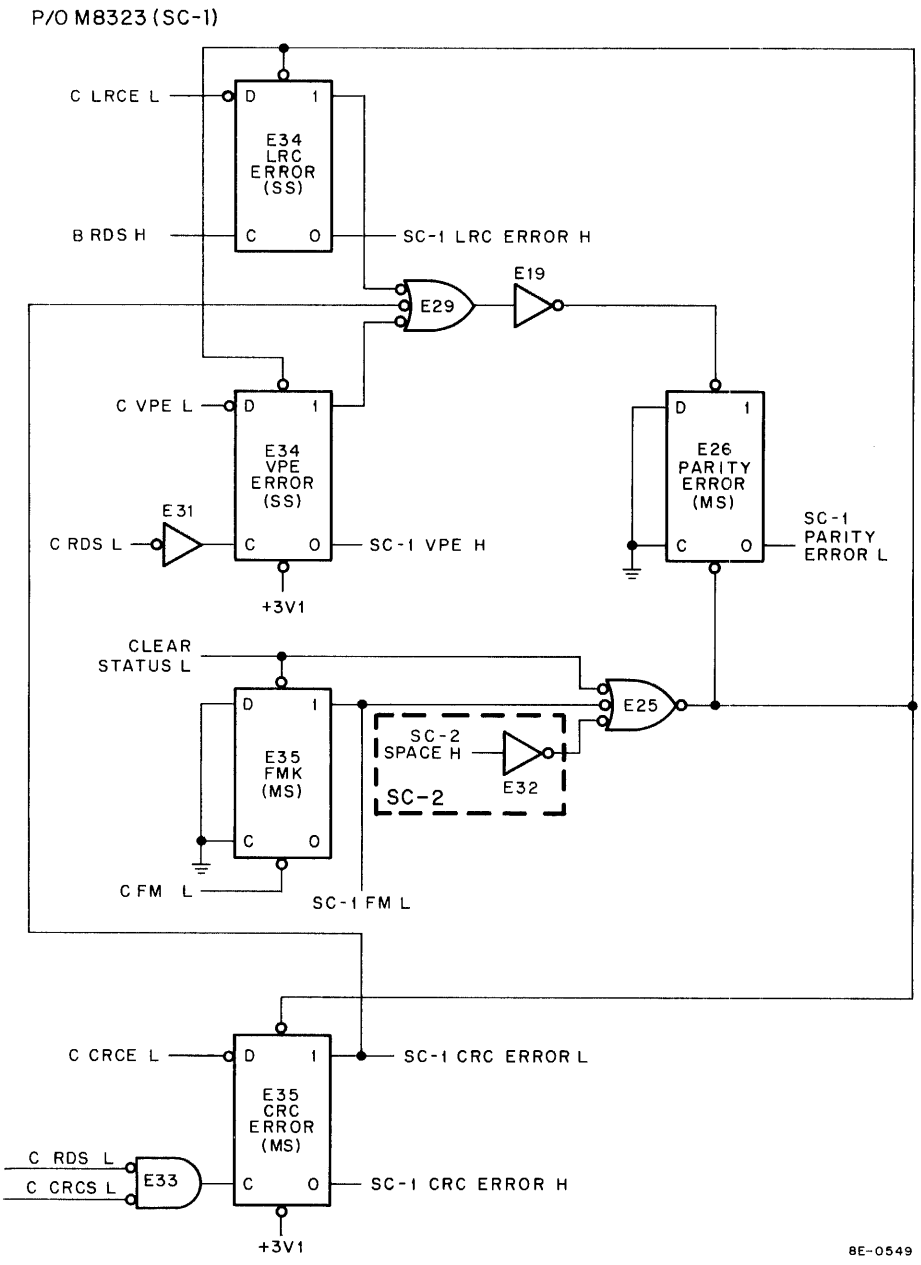


Figure 9-35 Parity Error Flags

9.13.2 Second Status Register

The Second Status Register is read using the RFSR IOT (Figure 9-14). This IOT transfers the condition of the Second Status Register to the AC for evaluation by the program. The logic elements in the Second Status Register perform as follows.

9.13.2.1 EMA 7 Increment Error – RE-2 EMA 7 flip-flop (Figure 9-33) is set if the program tries to increment from Field 7 to Field 0 (RE-1 EMA INCREMENT bit must be set). If RE-2 EMA 7 H (Figure 9-30) is applied to the data input and RE-1 EMA INC L is asserted, the RE-2 EMA 7 flip-flop sets, which in turn sets the SC-2 ERROR flag when CB-3 MTTF is set (Figure 9-31). Refer to Paragraph 9.13.3 for a discussion of the EMA INC logic. The Second Status Register must be read by the program after CB-3 MTTF is set to determine the cause of the error.

9.13.2.2 Vertical Parity Error (C VPE) – The SC-1 VPE flip-flop (Figure 9-35) is set during a Read or Read/Compare operation if the TU10 Master System detects a Vertical Parity Error and asserts C VPE L. SC-1 VPE is cleared when the next good word is read from tape. If SC-1 VPE is set at the end of an operation, the last word in the record was the one that set SC-1 VPE.

9.13.2.3 LRC ERROR – The SC-1 LRC ERROR flip-flop (Figure 9-35) sets if the selected TU10 detects an LRC error when the LRC character is read. The TU10 asserts C LRCE L when an error is detected and sets SC-1 PARITY ERROR and SC-1 LRC ERROR.

9.13.2.4 CRC ERROR – The SC-1 CRC ERROR flip-flop (Figure 9-35) sets if the TU10 detects a CRC error when it reads the CRC character from tape. The TU10 Master System asserts C CRCE L when a CRC error is detected to set the SC-1 CRC ERROR flip-flop and the SC-1 PARITY ERROR flip-flop.

9.13.3 Main and Second Status Register Multiplexer

The contents of the Main Status Register and Second Status Register (Figure 9-36) are applied to three 8235 ICs (refer to Appendix A, Volume 1, for truth table, logic diagram, and pin locations). The 12 bits (Figures 9-9 and 9-16) from the Main Status Register are applied to the Data Bus if an RMSR instruction is executed by the program and the 4 bits from the Second Status Register (Figures 9-10 and 9-14) are transferred to the Data Bus if an RFSR instruction is executed by the program. Note that 8 bits of the Function Register (Figure 9-29) are also applied to the Data Bus when the RFSR instruction is executed by the program.

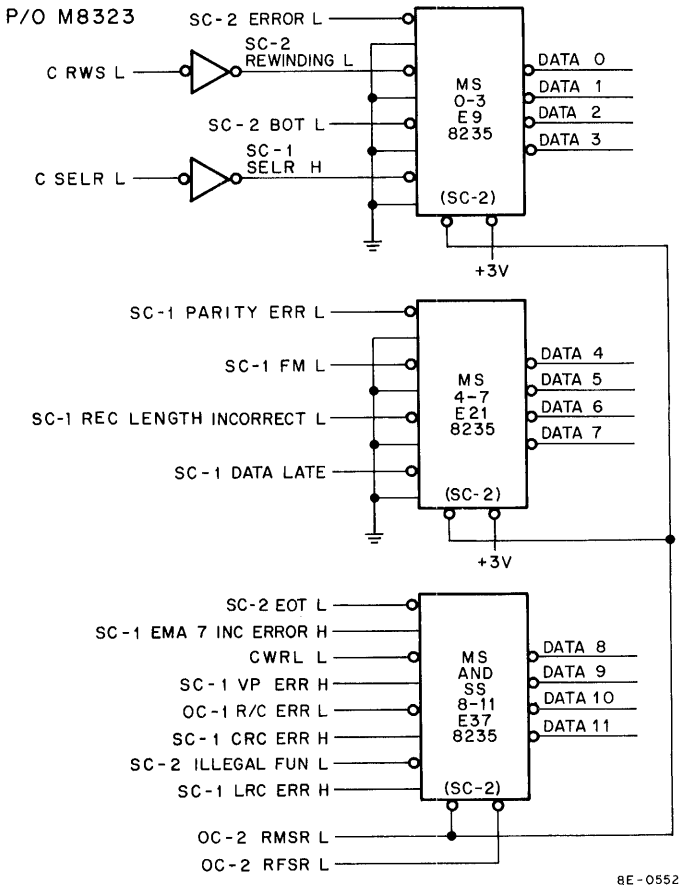


Figure 9-36 Main Status Register and Second Status Register Multiplexer

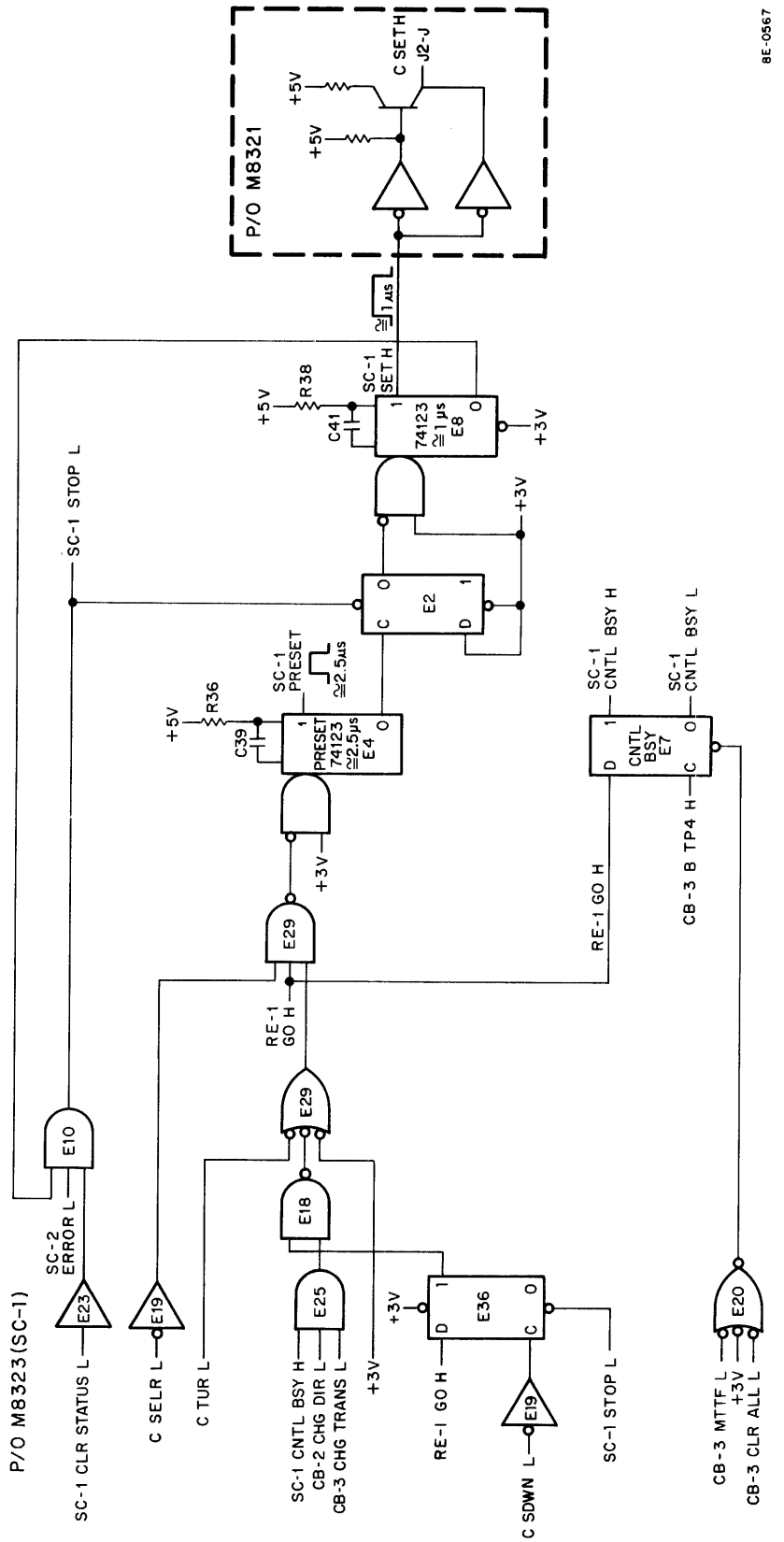


Figure 9-37 PRESET and SET Pulse Generation Logic

9.13.4 Extended Memory Address Increment Logic

The EMA bits (6, 7, and 8) in the Command Register (Figure 9-30) are used to select one of the memory fields during a Data Break operation if bit 6 in the Function Register is a 1. When bit 6 is set, the PDP-8/E memory is treated as continuous memory instead of 4K blocks (Table 9-12). To accomplish this the EMA bits must be incremented when the last memory location (7777) in each field is addressed and SC-1 COUNT CA L is asserted. The RE-1 EMA INC flip-flop (Figure 9-33) is set when the Current Address Register goes to all 0s and RE-1 EMA INC EN L is asserted (bit 6 in the Function Register is 1). The EMA bits in the Command Register are incremented each time bit 0 in the CA Register makes a 1 to 0 transition until the EMA bits are all 1s (RE-2 EMA 7). When RE-2 EMA 7 H is asserted, the NAND gate on the output of RE-1 EMA INC is disabled. If an attempt is made to increment beyond Field 7, the RE-1 EMA INC ERROR flip-flop is set by RE-2 EMA 7 H and the set side of RE-1 EMA INC. The RE-1 EMA INC flip-flop is cleared at TP3 time of BRK RQST and remains cleared until RE-2 CA 0 L makes a high-to-low transition at the end of a memory field.

9.13.5 Control Busy (CNTL BSY)

The SC-1 CNTL BSY flip-flop (Figure 9-37) is set by RE-1 GO and OC-2 B TP4 when bit 5 in the Function Register is loaded with a 1. SC-1 CNTL BSY is cleared when MTTF (JOB DONE) sets at the end of an operation or by CB-3 CLR ALL.

9.13.6 PRESET and SET Pulse Generator

Figure 9-37 shows the SC-1 PRESET and SC-1 SET pulse generation logic. The 74123 ICs are monostable multivibrators that generate a pulse on the output when the input signal makes a high-to-low transition. The duration of the output pulse is determined by an external resistor and capacitor, i.e., C39 and R36.

SC-1 PRESET is a 2.5-μs pulse (approximate time) that is triggered when the RE-1 GO bit (bit 5) in the Function Register is set. Note that C SELR L and C TUR L must be asserted to enable the gate when starting from a standstill condition. In a continuous mode of operation, C SDWN L allows the RE-1 GO signal to trigger the 74123 IC if CB-2 CHG DIR or CB-2 CHG TRANS are both high (false). If CB-3 CHG DIR or CB-3 CHG TRANS are asserted the TM8-E must wait for C SELR L and C TUR L. When SC-1 PRESET returns to the clear state, E2 is clocked, and if the SC-2 ERROR flag is not set the second 74123 IC is triggered. When the second 74123 IC is triggered, it outputs a 1.0-μs pulse (approximate time) that is applied to the selected TU10 to initiate tape motion. The E2 flip-flop is cleared by CB-3 CLR STATUS L, the SC-1 SET pulse, or the SC-2 ERROR flag.

9.13.7 Data Late Error Check Logic

The logic shown in Figure 9-38 is used to check the Data Late Error logic (Figure 9-33). The processor timing is stopped at TP3 time by the assertion of SC-1 NOT LAST XFER and restarted by asserting SC-1 BUS STROBE.

The 74123 ICs are monostable multivibrators that are triggered on a high-to-low transition of the input signal to generate an output pulse. The duration of the output pulse is determined by an external capacitor and resistor, i.e., C40 and R37. When the CKDL instruction is executed by the program, OC-2 IBCM L is asserted to trigger the first 74123 IC and generate a long timing pulse, which is ANDed with E1 flip-flop and applied to the OMNIBUS as SC-1 NOT LAST XFER to stop processor timing. E1 is cleared at TP3 time and the trailing edge of the first 74123 causes the second 74123 IC to output a pulse. This pulse asserts SC-1 BUS STROBE L and restarts processor timing. During the time processor timing was stopped, an attempt was made by the TM8-E to transfer data. The SC-1 DATA LATE ERROR flip-flop (Figure 9-33) should be set, because the TM8-E would normally transfer several words in a time period this long. If the SC-1 DATA LATE ERROR flip-flop does not set, this group of logic is not working properly.

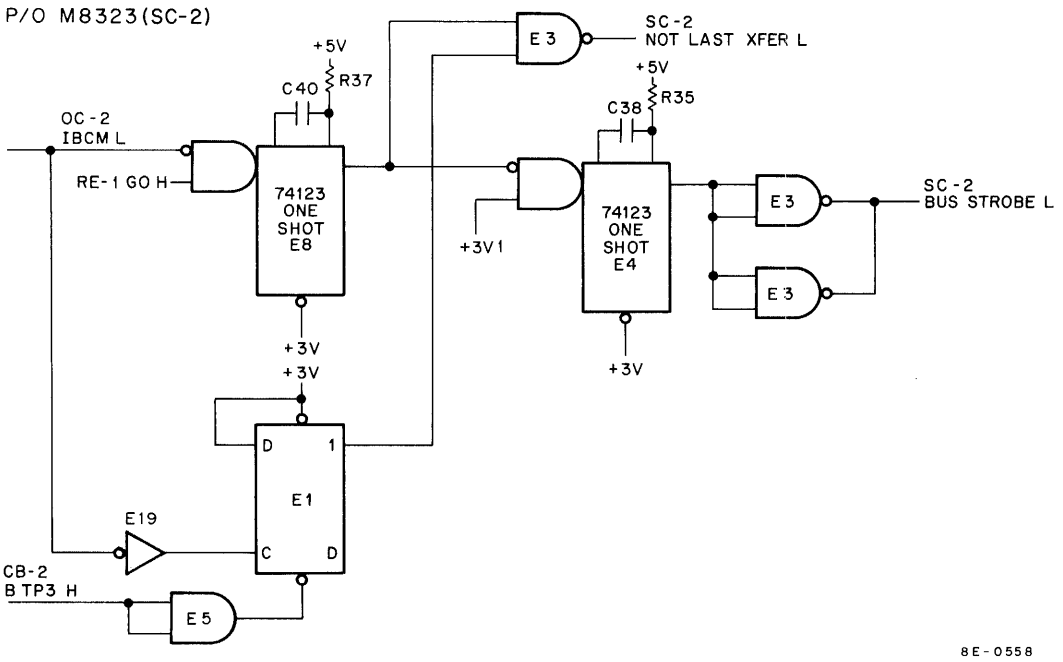


Figure 9-38 Data Late Error Check Logic

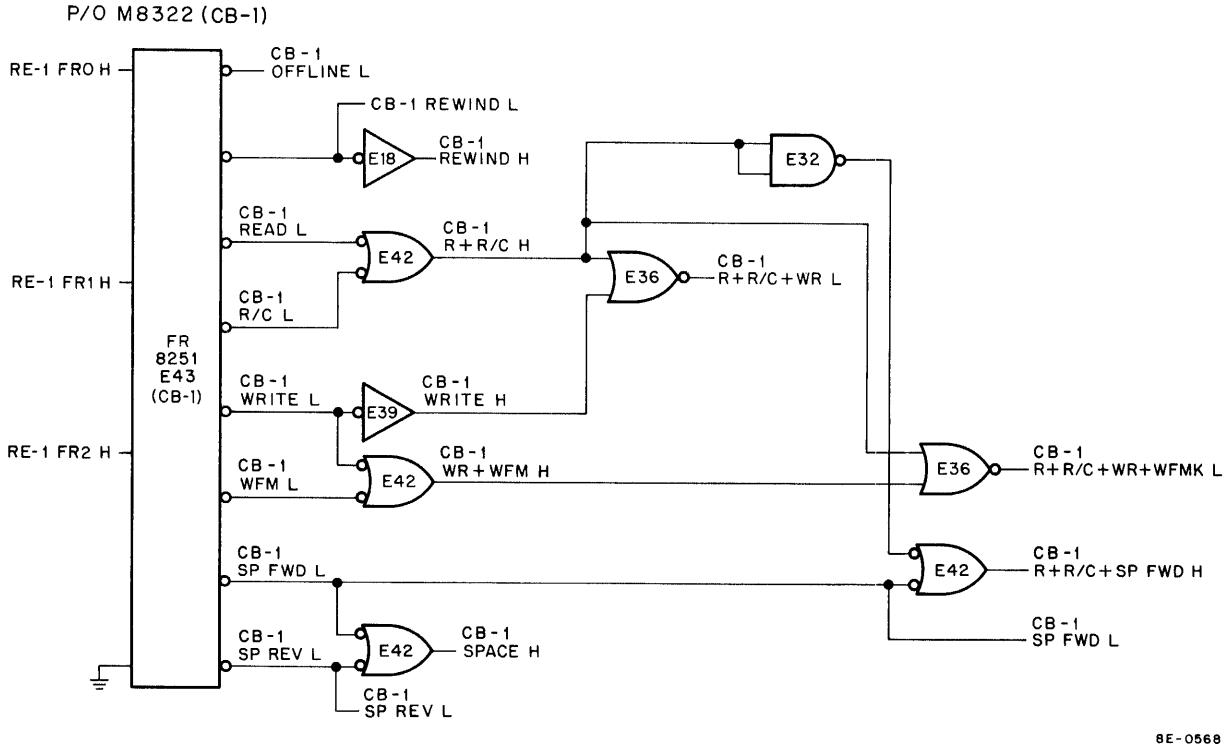


Figure 9-39 Control Function Decoder

9.14 M8322 CONTROL MODULE

The logic elements of the M8322 Control Module are described in the following paragraphs.

9.14.1 Control Function Decoder

The Control Function Decoder (Figure 9-39) is an 8251 IC that decodes the three most significant bits (FR0–FR2) of the Function Register (Table 9-12) to set up the control logic for a TU10 Transport operation.

NOTE

This decoder is identical to the output Control Function Decoder (Paragraph 9.11.7).

The 8251 IC is a BCD-to-Decimal Decoder (refer to Volume 1, Appendix A, for truth table, logic diagram, and pin numbers) that decodes bits FR0 through FR2 and produces a low on one output line of the IC for each 3-bit combination, i.e., 100_2 causes pin 9 to be low and indicates a Write operation. The outputs of the IC are NORed to generate one signal to represent a combination of operations, i.e., CB-1 SP REV L and CB-1 SP FWD L are NORed to generate CB-1 SPACE H, to reduce the number of signals that are applied to elements of the control logic.

9.14.2 Data Break Request Logic

Figure 9-30 shows the logic used to make a BRK RQST during data transfer operations. The CB-1 BRK RQST flip-flop is cleared and CB-1 BRK RQST H is asserted when the following conditions exist during Read, Write, and Read/Compare operations.

a. Write operation and SC-1 SET H are asserted for the first CB-1 BRK RQST at the beginning of a Write operation.

b. If CB-1 WRITE 1st 7 H is low and SC-1 WRS L (write strobe) is asserted during a Write operation. Refer to Paragraph 9.14.10 for origin and discussion of these signals.

c. If CB-1 READ 9 or SC-2 READ 2nd 7 is asserted (Figure 9-35) during a Read operation.

d. If an SBRM instruction (for maintenance only) is executed by the program.

Note that the CB-1 BRK RQST flip-flop is set for only Write, Read, or Read/Compare operations, which are the only operations requiring data transfers. CB-1 BRK RQST is set and CB-1 BRK RQST H is negated by CB-1 MAC ACC L at TP1 time when the BRK RQST is accepted by the processor. The BRK RQST flip-flop is negated by SC-1 DATA LATE, CB-3 CLR ALL, RECORD LENGTH INCORRECT, or CB-1 WCOV if RE-1 ENAB CHK CHAR is not asserted. E24 is cleared at the beginning of each data transfer operation by SC-1 PRESET H so that SC-1 RECORD LENGTH INCORRECT, CB-1 WCOV, or SC-2 ERROR can be reported during the operation and stop data transfers if these errors occur.

9.14.2.1 Word Count Overflow Logic – The CB-1 WCOV flip-flop (Figure 9-41) is set by RE-2 WC0 L when bit 0 in the WC Register makes a high-to-low transition (Figure 9-29). The set side of CB-1 WCOV is applied to NAND gate E32, which has as its other input RE-1 ENAB CHK CHAR L. If bit 4 in the Function Register (Table 9-12) is 0, RE-1 ENAB CHK CHAR is high and CB-1 WCOV (Figure 9-40) sets E24 flip-flop which causes CB-1 BRK RQST to negate and stop data transfers. If bit 4 in the Function Register is a 1, RE-1 ENAB CHK CHAR L is asserted and CB-1 WCOV does not set E24. This allows two more data breaks to transfer the CRC and the LRC character on a Read from a 9-track transport to memory. CB-1 WCOV is cleared by CB-3 CLR STATUS when a CLF instruction is executed by the program.

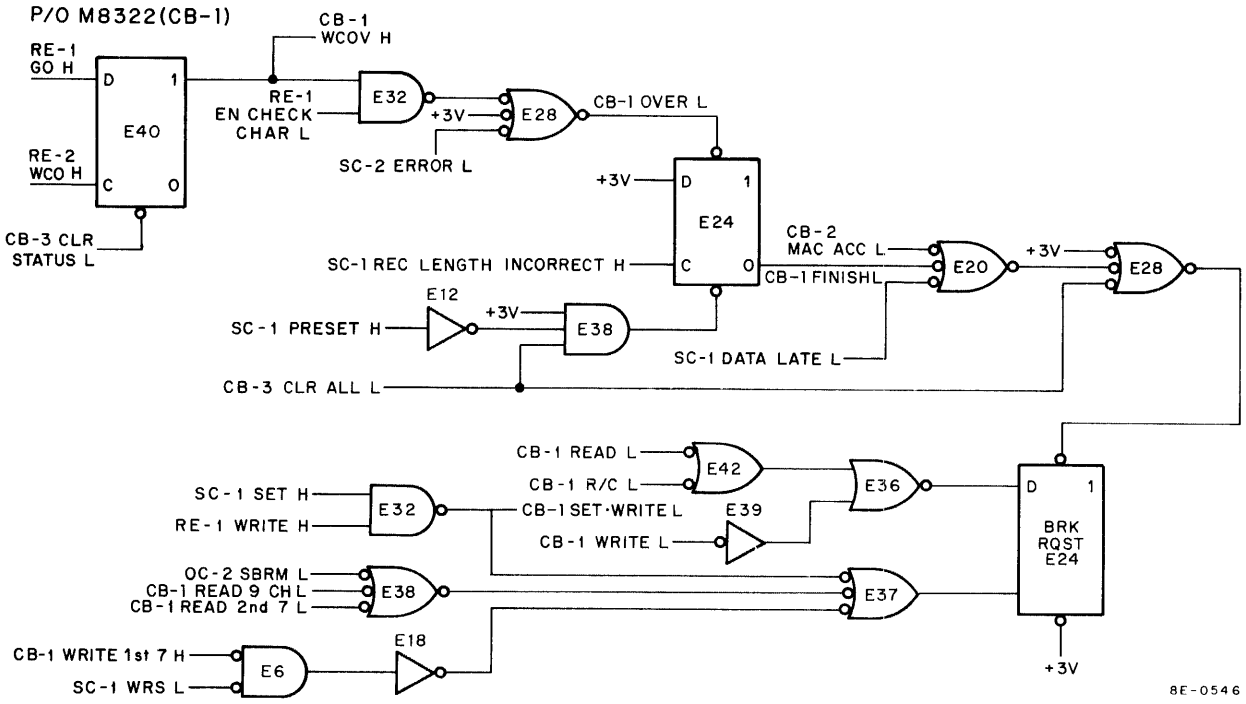


Figure 9-40 Data Break Control Logic

9.14.3 Data Break Priority Logic

The priority of the TM8-E (Figure 9-41) is established by removing one of the A jumpers (A0—A5) and installing one of the B jumpers (B0—B5); thus to establish a 0 priority (the highest priority) for the TM8-E, remove A0 and install B0. By this action all five NAND gates are disabled and the output of E9 is high, which enables E21. This enables the set side of E26 to be applied to the CB-2 MAC 1 and CB-2 MAC 2 flip-flops and allows the TM8-E to begin a Data Break operation at TP4, because the TM8-E has been assigned the highest priority. No other peripheral using the Data Break Interface can have its A0 jumper removed and its B0 jumper installed. Note that when NAND gate E34 is enabled at TS4 time, DATA 0 line is low (the TM8-E B0 line is in place). Since all of the other peripherals are monitoring the Data Bus, one of the NAND gates in their priority logic is enabled and their BRK RQST is not accepted.

As a further example, consider what happens if the TM8-E ranks third in the priority structure. This priority is established by removing jumper A2 and installing jumper B2. Because jumpers A0 and A1 are left in place, two other peripherals can keep the TM8-E from making a BRK RQST. If the second highest priority peripheral has a BRK RQST at the same time as the TM8-E, its interface brings the DATA 1 line low during TS4 and NAND gate E5B is enabled. The output of E5B causes the output of E9 to go low and disable AND gate E21. This prevents the set side of E26 from setting CB-2 MAC 1 and CB-2 MAC 2 until the other peripheral completes its Data Break operation. As implied, priority decreases from 0 through 11, and the TM8-E is assigned any priority between 0 and 5 by removing the correct A jumper and installing the correct B jumper.

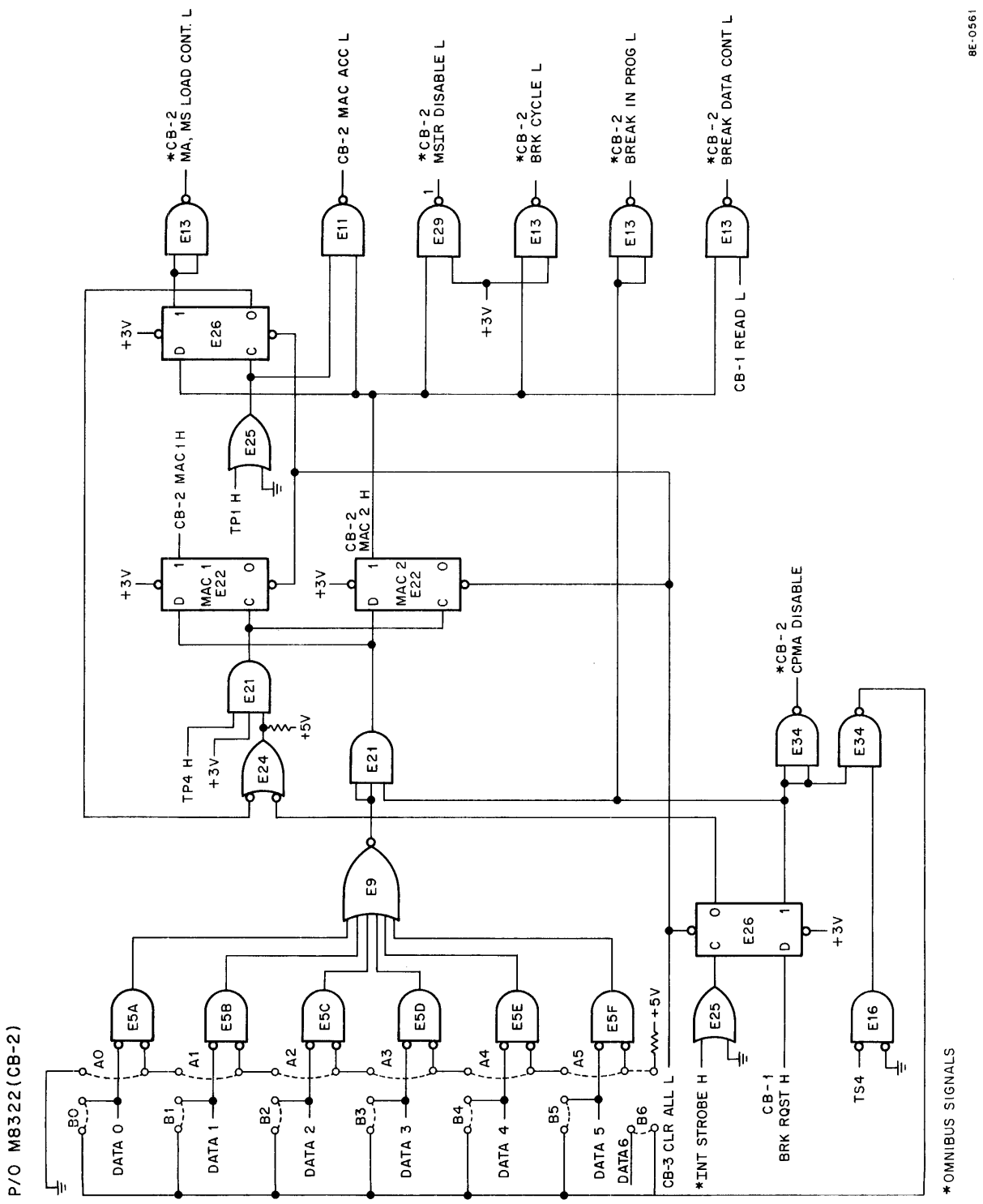


Figure 9-41 Priority and Processor Control Logic

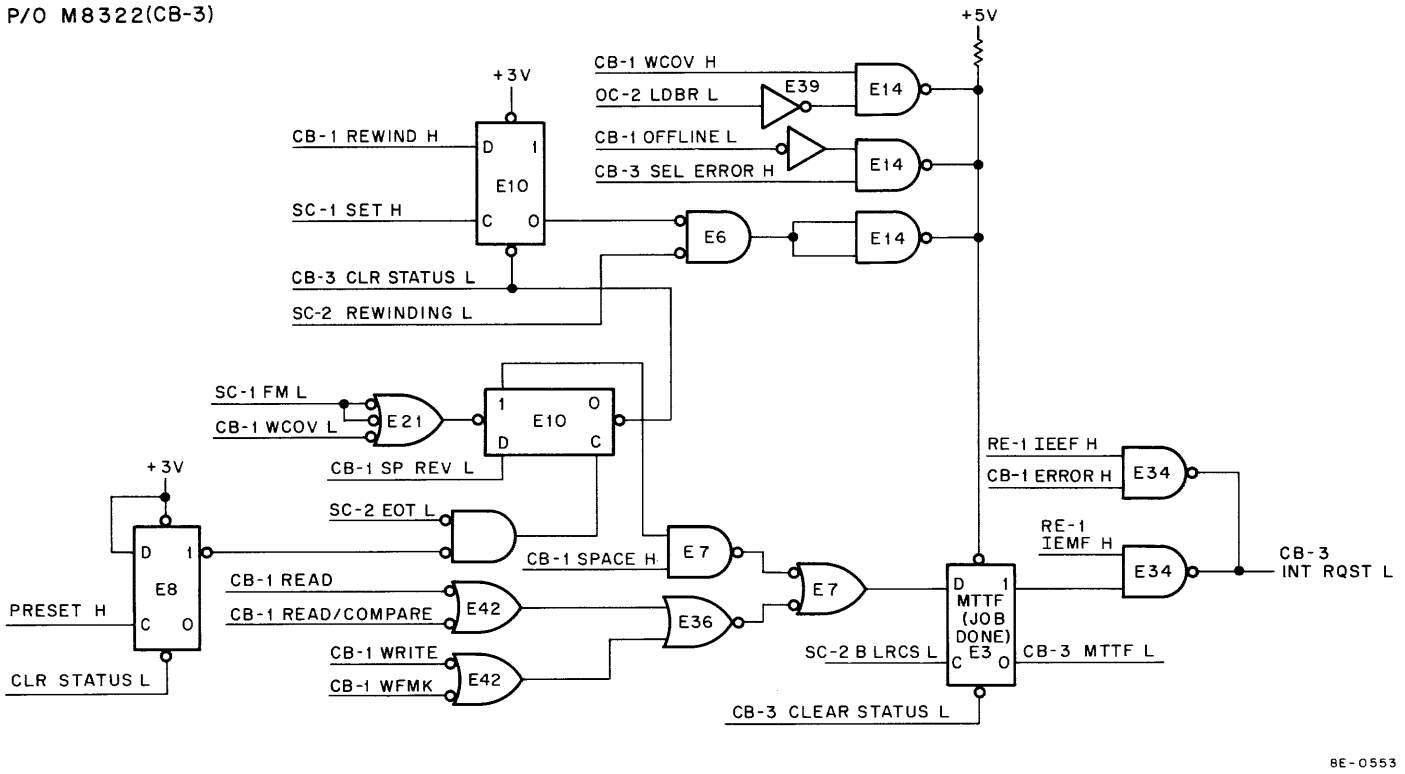


Figure 9-42 MTTF (JOB DONE Flag) and Interrupt Request Logic

9.14.4 Processor Control Logic

The logic shown in Figure 9-41 is used to control the PDP-8/E processor during a Single Cycle Data Break operation. If E21 is enabled by the priority logic and the set side of E26, CB-2 MAC 1 and CB-2 MAC 2 are set to assert the OMNIBUS signals (the OMNIBUS signals are explained in Chapter 9 of the *PDP-8/E & PDP-8/M Small Computer Handbook*) and take control of the processor for a Single Cycle Data Break operation. Note that MA, MS is not asserted until TP1 time. CB-2 BREAK DATA CONT L, which controls direction of data flow on the Data Bus, is controlled by READ L. During a Read operation, CB-1 READ L is asserted and data is transferred from tape to memory. During Write and Read/Compare operations, CB-1 READ L is high to transfer data from memory to the TM8-E. CB-2 MAC 1 and CB-2 MAC 2 are cleared by the output of AND gate E21 at TP4 time if BRK RQST is removed. CB-1 BRK RQST (Figure 9-40) is cleared by CB-2 MAC ACC L at the same time CB-2 MAC 1 and CB-2 MAC 2 are set to start a Single Cycle Data Break. The TM8-E continues to make break requests and to transfer data to or from memory until the WC Register reads all 0s (WCOV).

9.14.5 MTTF (JOB DONE) Logic

MTTF (JOB DONE flag shown in Figure 9-42) is set by one of the following conditions to indicate that a specified function is complete or cannot be performed.

a. C LRCS (LRC character read from tape at the end of a record) during a Read, Read/Compare, Write, or Write File Mark operation.

b. The C LRCS is read from tape during a Space operation.

c. If File Mark, EOT, or WCOV are encountered during a Space operation.

d. The selected transport is given a command to rewind and C RWS is asserted by the selected transport to indicate Rewind has started.

e. The selected transport is given the CB-1 OFFLINE command and C SEL ERR L is asserted by the selected TU10.

f. If IOT LDBR is executed by the program and CB-1 WCOV L is asserted.

9.14.6 Interrupt Logic

The Interrupt logic (Figure 9-42) asserts INT RQST L, which is serviced by the processor (i.e., perform a flag check routine) when one of the following conditions exist.

a. Bit 6 in the Command Register (Interrupt Enable on SC-2 ERROR flag) is a 1 and the SC-2 ERROR flag is set (Figure 9-32). Note that the SC-2 ERROR flag does not set until after CB-3 MTTF is set unless CB-3 SEL ERR or SC-2 ILLEGAL FUN is set at the beginning of an operation.

b. Bit 5 in the Command Register (Interrupt Enable on JOB DONE flag) is a 1 and the CB-3 MTTF flag is set.

9.14.7 Change Transport Control Logic

Figure 9-43 shows the logic used to generate the CB-3 CHG TRANS L signal when a new transport is selected by the program. If an LCMR instruction is executed by the program, flip-flop E3 clears (Figure 9-43) and enables NAND gate E7. At TP4 time, the output of E7 supplies a clock input to E8 and if any of the inputs (RE-1 SEL 0—RE-1 SEL 2 and RE-1 B SEL 0—RE-1 B SEL 2) to the E4 Exclusive-OR gates are different, E8 zeroes and asserts CB-3 CHG TRANS L. The output of E7 also clocks the E3 flip-flop, causing it to set and disable E7. If C TUR L and C SDWN L are asserted or SEL REM L is negated, NAND gate E11 is enabled at TP4 time. LBCM L is asserted to load the Buffered Command Register with bits RE-1 SEL 0 through RE-1 SEL 2 from the Command Register (Figure 9-30). If CB-3 CHG TRANS is set and C RWS L is asserted, RE-1 LBCM L is asserted to load the BCM (Figure 9-43). CB-3 CLR STATUS resets the CB-3 CHG TRANS flip-flop. The Buffered Command Register is also loaded with RE-1 SEL 0 through RE-1 SEL 2 when CB-3 CLR ALL is asserted (CLF instruction executed by the program).

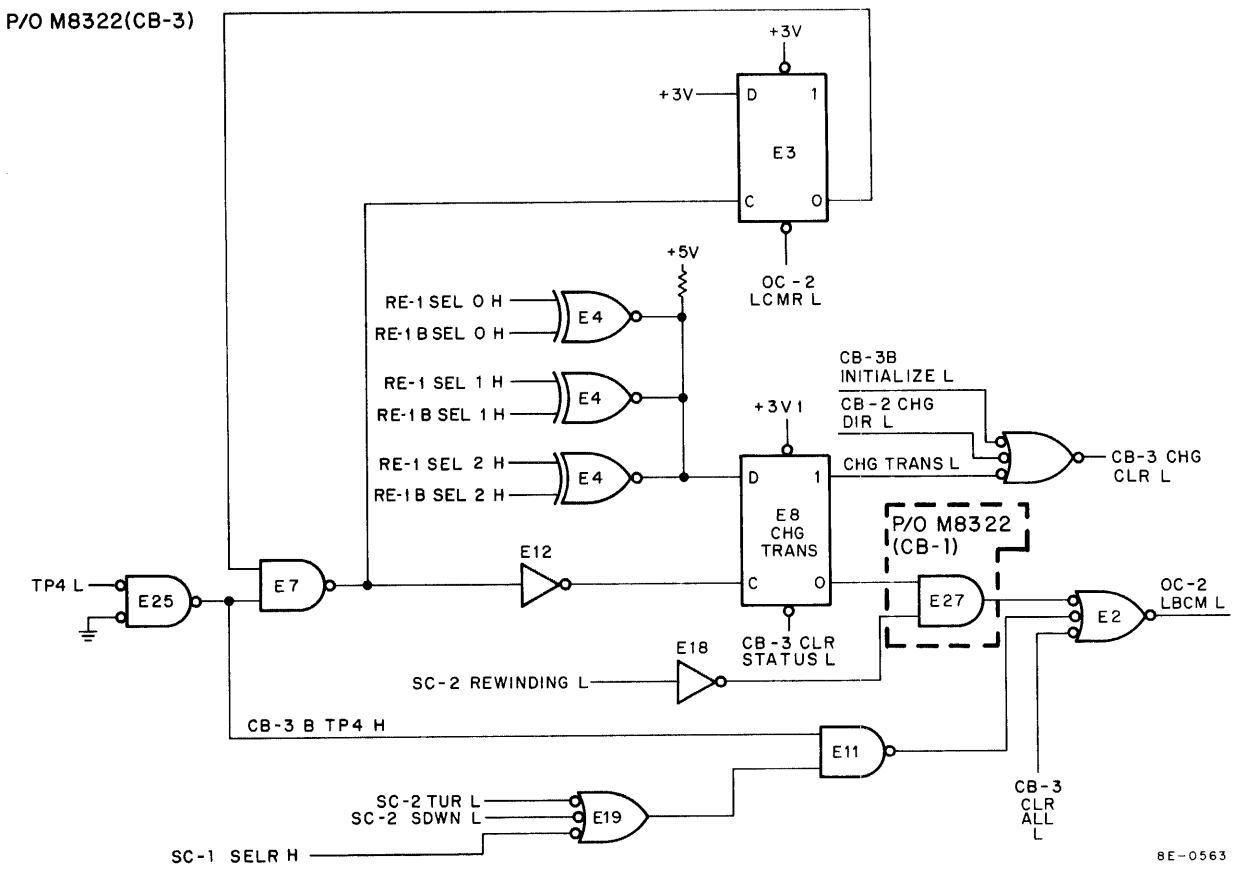


Figure 9-43 Change Transport and Buffered Command Register Control Logic

9.14.8 Change Direction Control Logic

Figure 9-44 shows the logic used to detect a change in direction of tape movement. E35 flip-flop is cleared by SC-1 SET H at the beginning of all operations except Space Reverse, Rewind, or Offline. This applies a high to the input of E4, which is the same as the high out of E19. E4 has a high output if both inputs are equal and a low output if the inputs are unequal. If CB-1 SP REV L, CB-1 REWIND L, or CB-1 OFFLINE L are asserted, the output of E19 goes low and the output of E4 (CB-3 CHG DIR L) is asserted. CB-3 CHG DIR L forces the control to wait for C TUR L and C SELR L before starting a new operation.

9.14.9 Write Data Ready Logic

Figure 9-45 shows the Write Data Ready logic. C WDR H is applied to the selected transport when the TM8-E is ready to start a Write operation. SC-1 SET H and CB-1 WRITE H enable NAND gate E32 to set flip-flops E23A and E23B. This enables E27A if a 7-track transport is selected and E27B if a 9-track transport is selected to assert CB-1 WDR H. If a 9-track transport is selected, E23A is cleared when CB-1 WCOV L is asserted, which in turn disables NAND gate E27B and CB-1 WDR H goes low. If a 7-track transport is selected, E23A is cleared by the first SC-1 WRS L pulse after CB-1 WCOV L is asserted and E23B is cleared by the second SC-1 WRS L pulse. This operation disables NAND gate E27A and C WDR H goes low. SC-1 DATA LATE L and SC-2 ERROR L clear both E23 flip-flops if these errors occur during a Write operation. If a CLF instruction is executed by the program, CB-3 CLR STATUS sets E23A and E23B to cause CB-1 WDR H to go low, which terminates a Write operation.

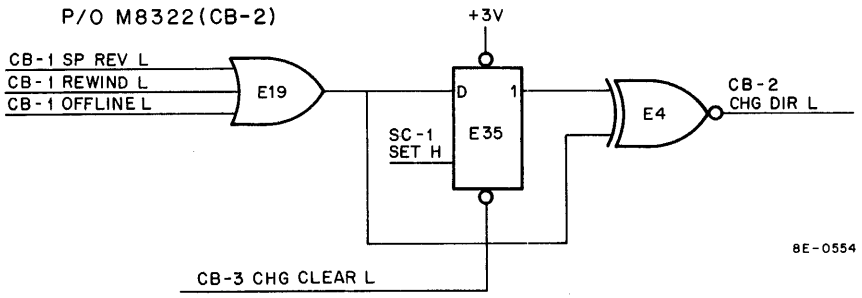


Figure 9-44 Change Direction Detection Logic

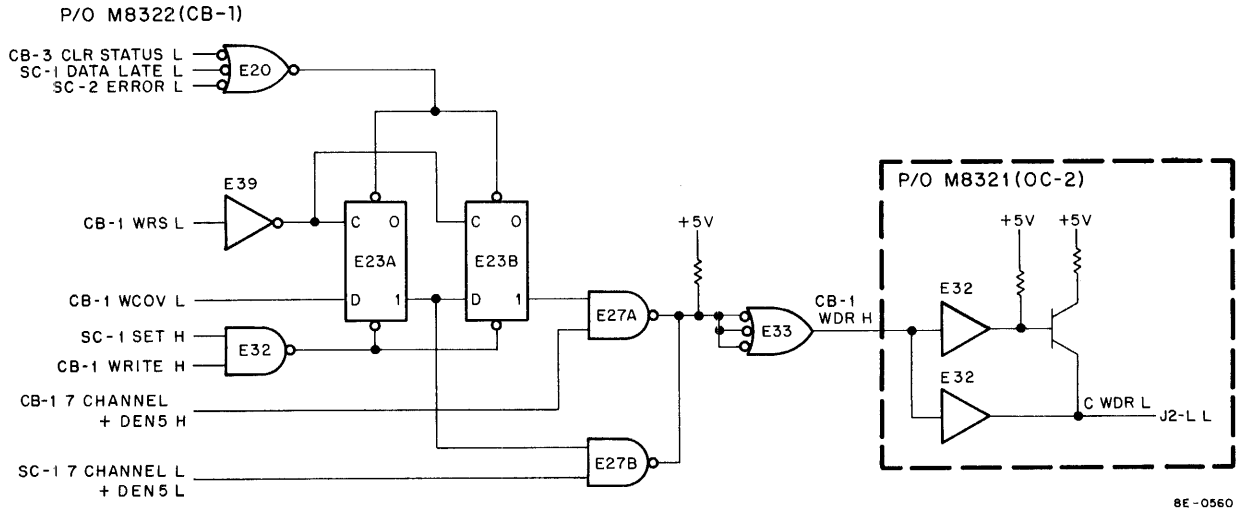


Figure 9-45 Write Data Ready Logic

9.14.10 Read and Write Control Logic

The logic shown in Figure 9-46 is used to generate control signals during Read and Write operations. Table 9-18 shows the levels of the control signals and the logic used to assert each signal for each Read and Write operation on 7- and 9-track transports. E40 is used only if a 7-track transport is selected. E40 is clocked on the rising edge of the SC-1 RDS or SC-1 WRS pulses.

The Read and Write control signals are applied to the CB-1 BRK RQST control logic to determine when a BRK RQST is to be made by the TM8-E (Figure 9-40). CB-1 BRK RQST is clocked on the falling edge of the SC-1 RDS or SC-1 WRS pulses. Refer to Drawing D-TD-TM8-E-1, sheets 1 through 8, for the timing diagrams that illustrate these operations.

9.14.11 Data Multiplexer Control Logic

Figure 9-47 shows the Data Multiplexer Control logic used to select data read from tape, from memory, or from the AC as input to the Data Register (Figure 9-25). Table 9-17 shows the level of CB-2 DB MPXA H and CB-2 DB MPXB H for all TM8-E operations.

Table 9-18
Read and Write Control Logic Signal Levels

Operation	SC-1 RDS L	SC-1 WRS L	CB-1 READ 9 L	CB-1 READ 1st 7 L	CB-1 READ 2nd 7 L	CB-1 WRITE 9 L	CB-1 WRITE 1st 7 L	CB-1 WRITE 2nd 7 L	Enabled Gate	Condition of E40
Read a Character From 9-Track Transport	low pulse	high level	low pulse	high level	high level	high level	high level	high level	E32	*
Read 1st 7 Character From 7-Track Transport	low pulse	high level	high level	low pulse	high level	high level	high level	high level	E37A	Set to 1 state on rising edge of C RDS
Read 2nd 7 Character From 7-Track Transport	low pulse	high level	high level	high level	low pulse	high level	high level	high level	E37B	Reset to 0 state on the rising edge of RDS
Write Character on a 9-Track Transport	high level	low pulse	high level	high level	high level	low pulse	high level	high level	E41C	*
Write 1st Character on 7-Track Transport	high level	low pulse	high level	high level	high level	high level	high level	low pulse	E41A	Set to 1 state on rising edge of C WRS
Write 2nd Character on 7-Track Transport	high level	low pulse	high level	high level	high level	high level	low level	high level	E41B	Reset to 0 state on rising edge of C WRS

*Condition of E40 does not matter on 9-track transports.

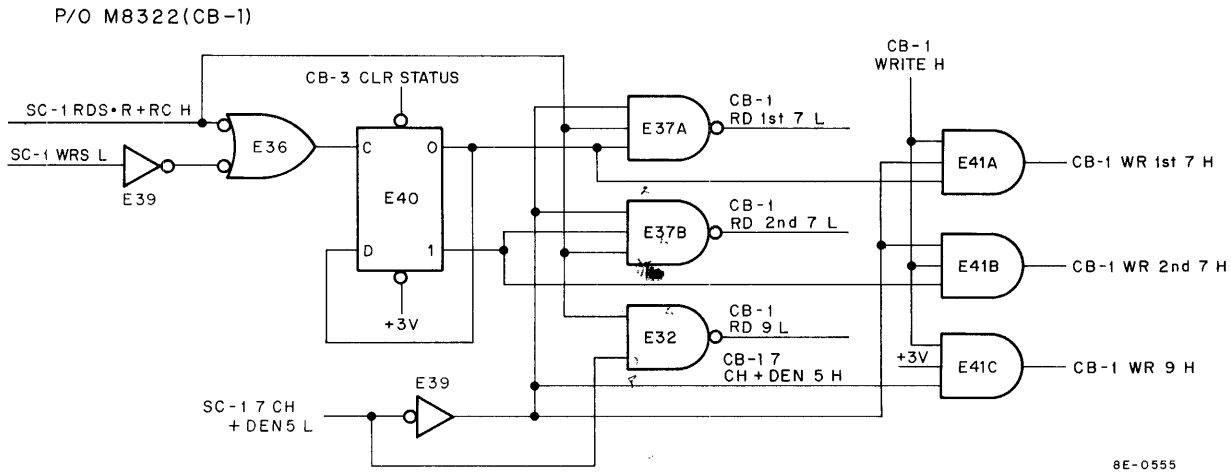


Figure 9-46 Read and Write Control Logic

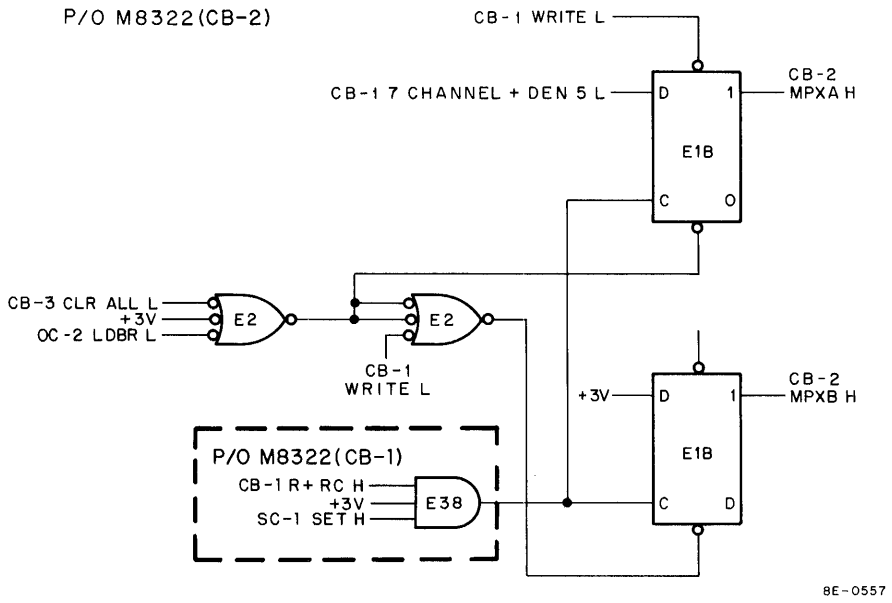


Figure 9-47 Data Multiplexer Control Logic

9.14.12 POWER OK Logic

The POWER OK logic shown in Figure 9-48 is used to assert CB-3 CLR ALL if PDP-8/E power falls below a certain level. If PWR OK H goes low, NAND gate E16 is enabled to assert CB-3 CLR ALL. This initializes all TM8-E logic and the selected transport.

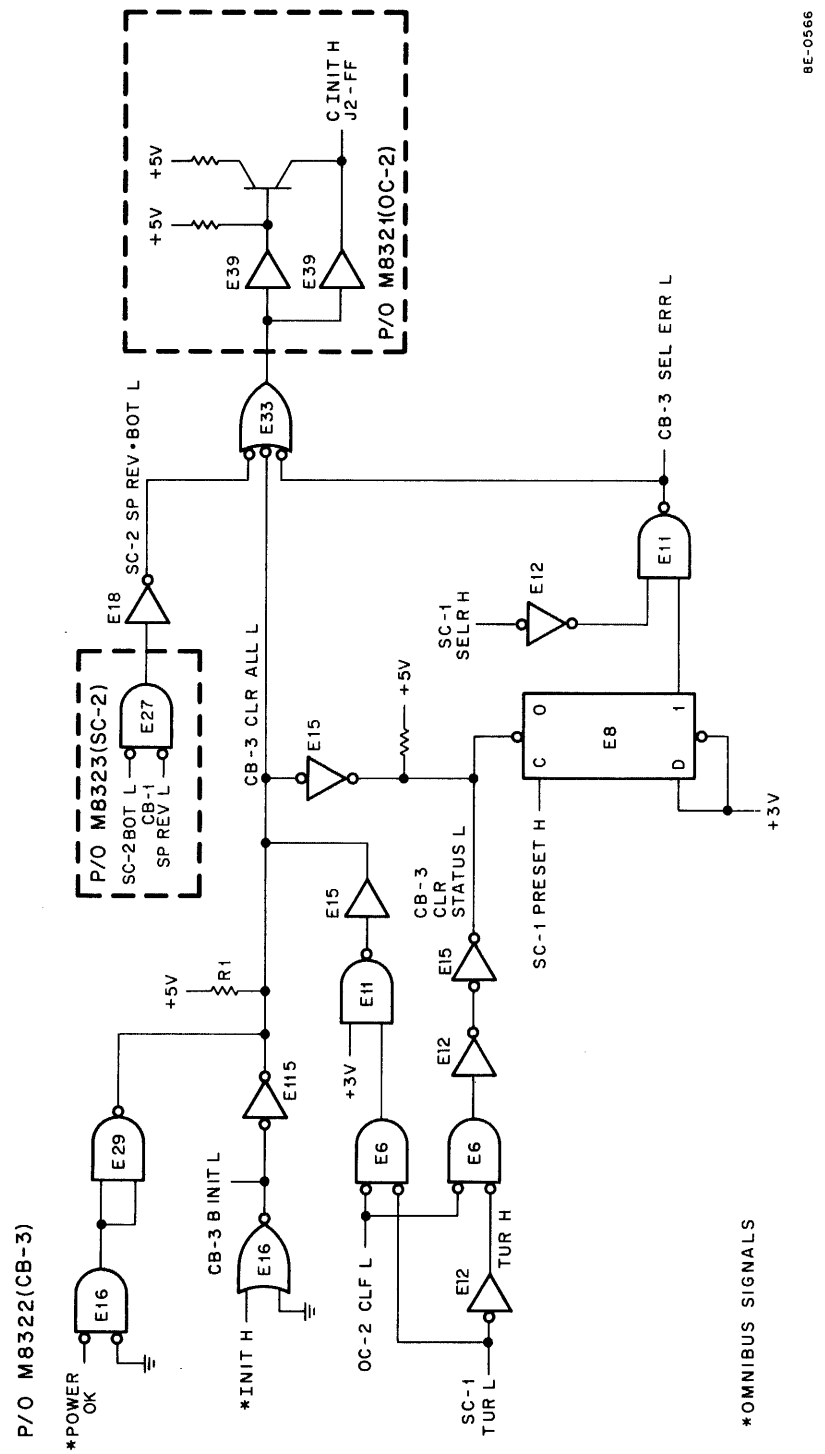


Figure 9-48 Initialize and Clear Logic

9.14.13 Initialize Logic

INIT H (Figure 9-48) is asserted when the PDP-8/E is powered up or by depressing the CLEAR key on the PDP-8/E power control console. Note that INIT H is not the same signal as C INIT H; C INIT H is used to clear all logic on the selected transport when the following conditions exist.

a. INIT H is asserted by the processor.

b. If the tape unit is ready (C TUR L true) when a CLF instruction is executed by the program (CB-3 CLR ALL is asserted).

c. If a Space Reverse operation is attempted and transport is at BOT.

d. If the CLT instruction is executed to assert CB-3 CLR ALL.

SECTION 5 MAINTENANCE

Recommended preventive maintenance should be scheduled on a regular basis to maintain the performance and reliability of the DECmagtape system. Preventive maintenance schedules are included in the *TU10 DECmagtape Maintenance Manual*, Chapter 5, Paragraph 5.1.1. TM8-E DECmagtape diagnostics (Paragraph 9.3) are provided to test and troubleshoot the TM8-E controller and the TU10 DECmagtape Transports. Preventive maintenance on the TM8-E modules consists of running the TM8-E diagnostics periodically to check system operation.

SECTION 6 SPARE PARTS

Table 9-19 lists the recommended spare parts for the TM8-E.

SECTION 7 IC DESCRIPTIONS

Only those ICs not included in Appendix A of Volume 1 are discussed in this section.

Table 9-19
TM8-E Spare Parts

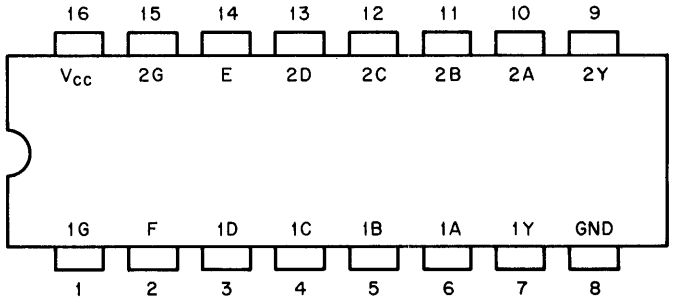
DEC Part Number	Description	Quantity
10-00007	Capacitor, 15 pF, 100V	1
10-00042	Capacitor, 1000 pF, 100V	1
10-00067	Capacitor, 618 pF, 35V	2
10-01610	Capacitor, 0.01 μF, 100V	2
12-09941	Connector, 40 pins	1
13-00204	Resistor, 47Ω, ¼W	1
13-00229	Resistor, 100Ω, ¼W	1
13-00275	Resistor, 220Ω, ¼W	2
13-00286	Resistor, 270Ω, ¼W	2
13-00293	Resistor, 330Ω, ¼W	3
13-00317	Resistor, 470Ω, ¼W	3
13-00443	Resistor, 417Ω, ¼W	1
13-00498	Resistor, 18 KΩ, ¼W	1
13-00534	Resistor, 100 KΩ, ¼W	1
13-01316	Resistor, 8.2 KΩ, ¼W	1
13-01401	Resistor, 750Ω, ¼W	3
13-01420	Resistor, 27Ω, ¼W	1
15-10015	IC, DEC 4008	2
19-05547	IC, DEC 7474	2
19-05575	IC, DEC 7400	2
19-05576	IC, DEC 7410	2
19-05578	IC, DEC 7430	1
19-05570	IC, DEC 7401	2
19-09004	IC, DEC 7402	2
19-09055	IC, DEC 7495	1
19-09056	IC, DEC 74H00	1
19-09057	IC, DEC 74H10	1
19-09058	IC, DEC 74H21	1
19-09267	IC, DEC 74H11	3
19-09485	IC, DEC 380	3
19-09486	IC, DEC 384	2
19-09584	IC, DEC 8251	1
19-09667	IC, DEC 74H74	1
19-09686	IC, DEC 7404	2
19-09704	IC, DEC 314	1
19-09705	IC, DEC 8881	3
19-09712	IC, DEC 8242	1
19-09928	IC, DEC 7416	1
19-09929	IC, DEC 7414	2
19-09935	IC, DEC 8235	2
19-09937	IC, DEC 74153	1
19-09955	IC, DEC 7412	1
19-10035	IC, DEC 74197	1
19-10435	IC, DEC 74123	1
19-10651	IC, DEC 74175	1
19-10652	IC, DEC 74174	1

DEC 74153 IC

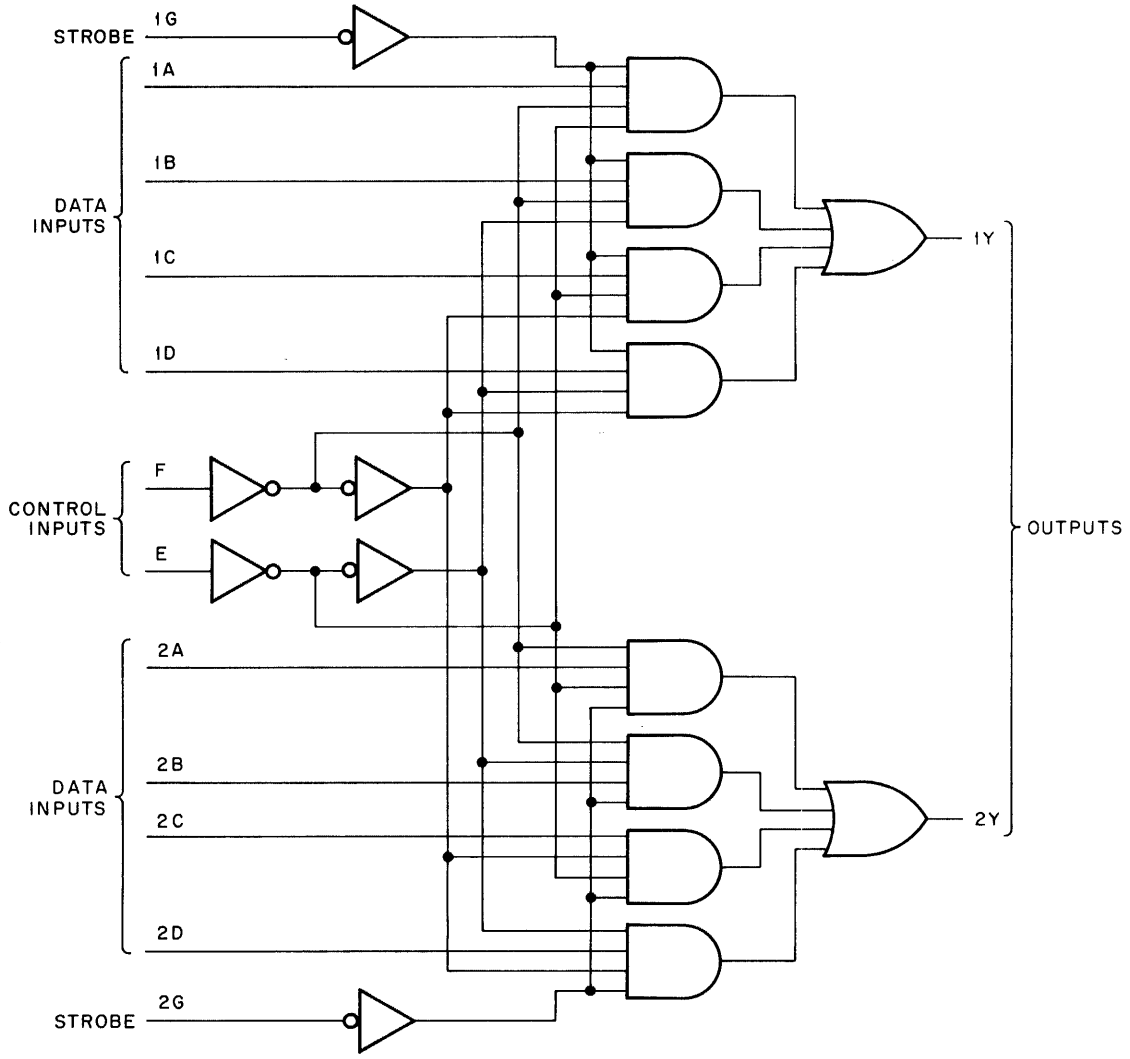
The DEC 74153 IC is a Dual 4-Line to 1-Line Data Selector/Multiplexer (see below for truth table, logic diagram, and pin numbers). The IC can be used in one of two modes, a 4-line to 1-line multiplexer or a parallel-to-serial converter. A strobe enable signal line is provided to select each of the input lines as an output. In the TM8-E, the strobe lines are tied together to allow the selection of signals from the MD lines, Data Bus, or data read from the TU10 Transport.

CONTROL INPUT		STROBE	OUTPUT
E	F	G	Y
LOW	LOW	LOW	A
HIGH	LOW	LOW	B
LOW	HIGH	LOW	C
HIGH	HIGH	LOW	D
DON'T CARE		HIGH	LOW

TRUTH TABLE (EACH HALF)



DEC 74153 IC (Sheet 1)



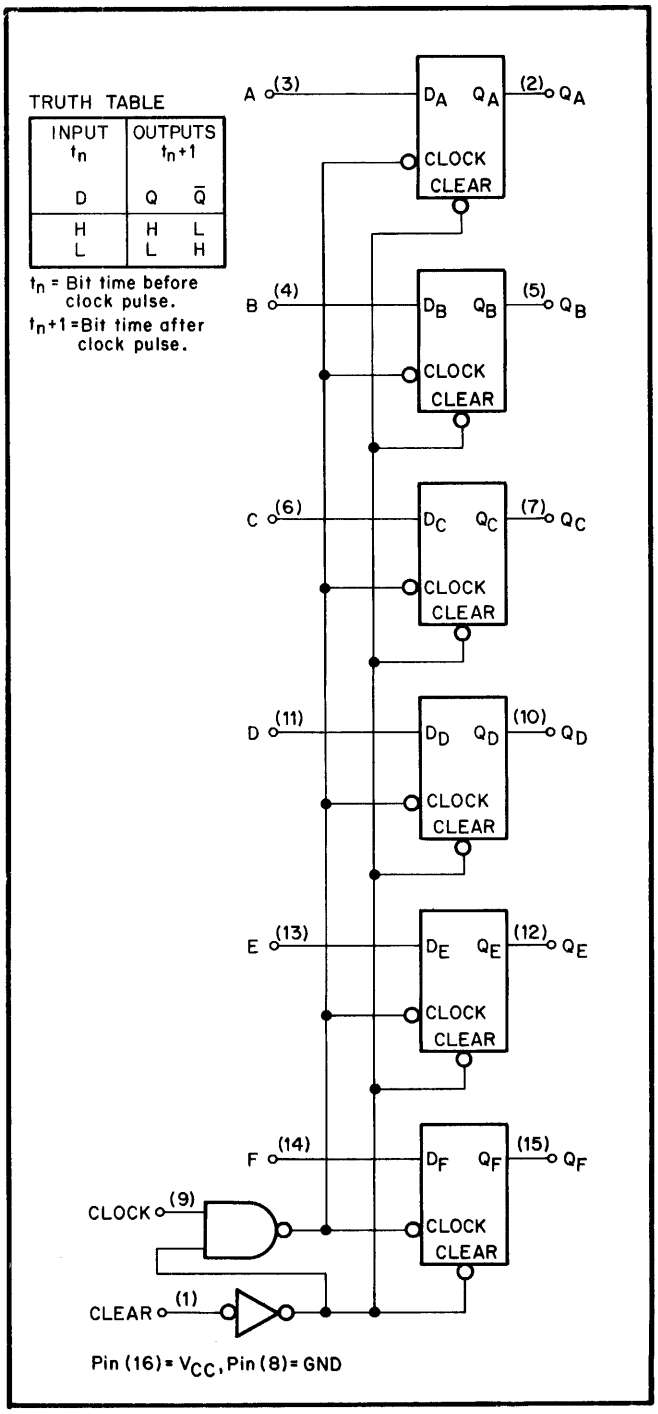
LOGIC DIAGRAM

DEC 74153 IC (Sheet 2)

DEC 74174 IC

The 74174 IC contains six flip-flops with single rail output with a buffered clock and direct clear input. Each flip-flop has an individual data input. The truth table and logic diagram are shown below.

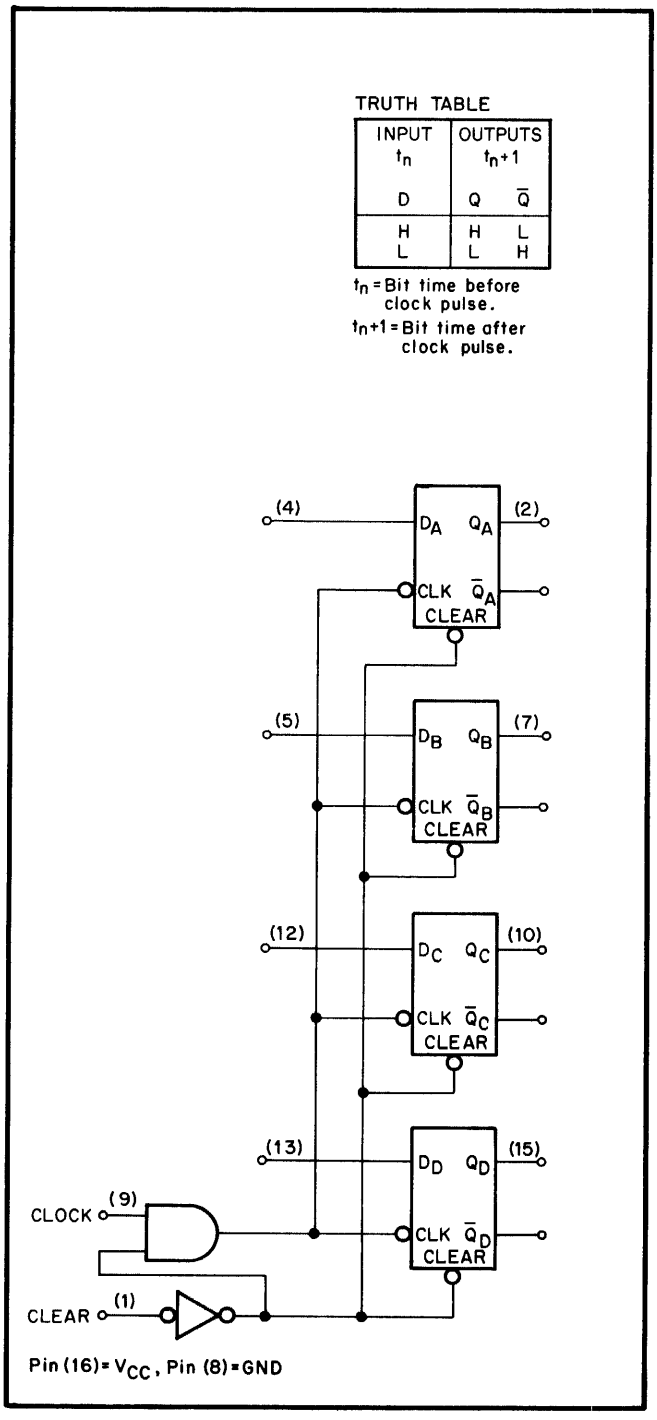
Input t_n	Outputs t_{n+1}	
D	Q	Q
H	H	L
L	L	H



11-1112

DEC 74175 IC

The 74175 IC contains four flip-flops with double rail outputs with a buffered clock and direct clear input. Each flip-flop has an individual input. The truth table and logic diagram are shown below.



DEC 74175 IC

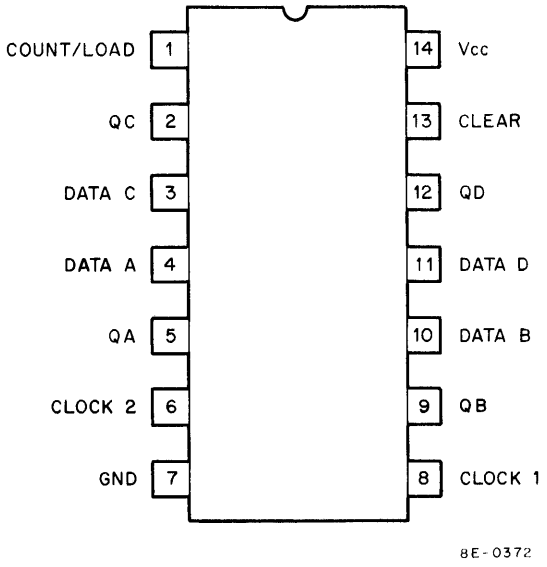
DEC 74197 IC

The DEC 74197 IC is a pre-settable binary counter that can also be used as a latch. The IC consists of four dc-coupled master-slave flip-flops connected to provide a divide-by-2 counter and a divide-by-8 counter. The logic diagram, a truth table, and a pin locator are shown in the 74153 description.

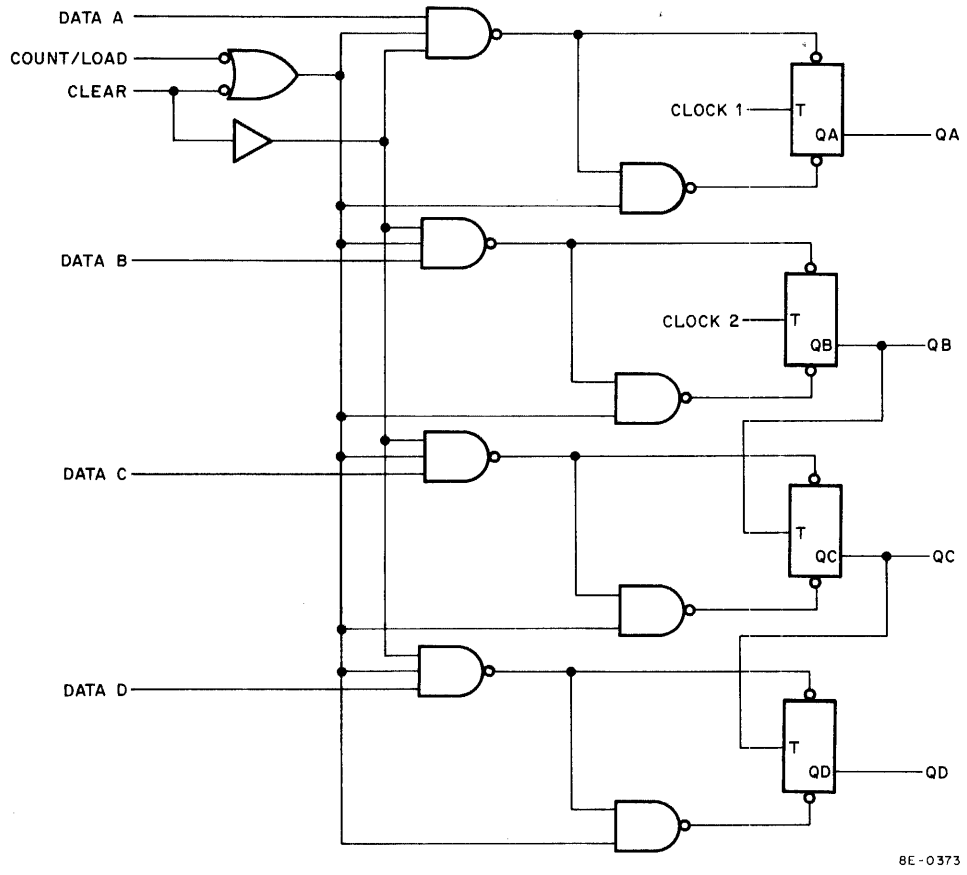
The 74197 can be used in any one of three modes, viz; the divide-by-2/divide-by-8 mode, requiring no external interconnection or IC pins, the latch mode, and the binary counter mode. If the first listed mode is used, an input at pin 8 is divided by 2 by flip-flop A and the result is taken from pin 5; an input at pin 6 is divided by 8 by flip-flops B, C, and D and the result is taken from pin 12. Transfer of information to the outputs takes place on the negative-going (trailing) edge of the clock pulse.

To use the latch mode, enter data at the four data inputs (pins 4, 10, 3, and 11) and enter a strobe pulse at pin 1. The output pins, 5, 9, 2, and 12, respectively, will follow the inputs when pin 1 is low, but will remain unchanged when pin 1 is high and the clock inputs are inactive.

Count Clock 1 Input	Output			
	QD	QC	QB	Q4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1



DEC 74197 IC (Sheet 1 of 2)



DEC 74197 IC (Sheet 2 of 2)

CHAPTER 10
TA8-E CASSETTE SYSTEM INTERFACE

SECTION 1 INTRODUCTION

The TA8-E interfaces the PDP-8/E, M, or F Computers and the TU60 Cassette Tape Transport System (2 drives) (Figure 10-1). To perform this function, the TA8-E:

a. Decodes IOT instructions to generate control signals and transfer data.

b. Transmits control signals to the TU60 and receives signals from the TU60 that indicate TU60 status.

c. Selects (in conjunction with the TU60) one of the TU60 drives to perform an operation (i.e., read or write).

d. Provides flags to indicate ERRORS and generates SKIP or INTERRUPT REQUEST.

e. Buffers the input/output data.

f. Provides TU60 and TA8-E status information to the computer.

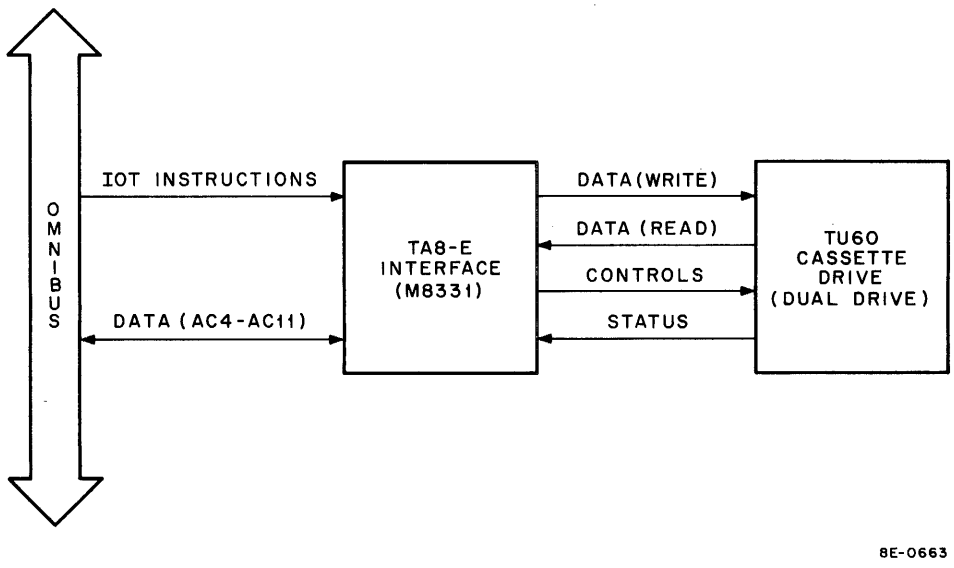


Figure 10-1 TA8-E Interface and TU60 Cassette Drive, Block Diagram

10.1 PHYSICAL DESCRIPTION

The TA8-E consists of the M8331 Interface Module that is inserted into the OMNIBUS to provide an interface for the TU60. The TA8-E and TU60 can be ordered in two rack mounted configurations. These configurations are outlined below:

- TA8-AA – M8331 Module, TU60 AA, and 2 BC08R cables (rack mounted), 115 Vac
- TA8-AB – M8331 Module, TU60 AB, and 2 BC08R cables (rack mounted), 230 Vac

The basic system consists of one TU60 Cassette Tape Transport System (2 drives) and one M8331 Interface Module with interface cables. Jumpers on the M8331 module permit the selection of IOT device codes 70 through 77. These device codes allow the user to install a maximum of eight TA8-E modules on one processor and to use eight dual drive cassettes (16 drives).

10.2 POWER REQUIREMENTS

The M8331 module requires +5V at 2.4A. This logic power is supplied by the processor power when the M8331 module is inserted into the OMNIBUS. Power is not supplied to the TU60 by the TA8-E or vice versa.

10.3 TAPE FORMAT

The tape format (Figure 10-2) is 8-bit serial words with programmable block length (Figure 10-3). Block length is limited only by the length of the tape, and up to 92K words can be recorded on one cassette cartridge. Each block of data is preceded by a PREGAP and PREAMBLE to identify the data block. A Cyclic Redundancy Check (CRC) character is recorded at the end of the data block and is followed by a POST GAP. Gaps are erased areas on the tape that are used to separate blocks of data and to provide a space to start and stop the tape drive.

The CRC character is computed by the TU60 hardware during a write operation and written at the end of a block of data. The CRC character computed during a write operation is compared with the CRC character computed during read operations to determine if data bits were picked up or lost. The CRC character is generated and checked by the TU60 electronics, and if a CRC ERROR occurs, the CRC BLOCK ERROR flag is set by a signal from the TU60. The *TU60 Maintenance Manual* contains a complete discussion of CRC character generation and error checking operations.

The PREAMBLE is a word generated by the TU60 to identify a block of data and to provide sync pulses to read and write data.

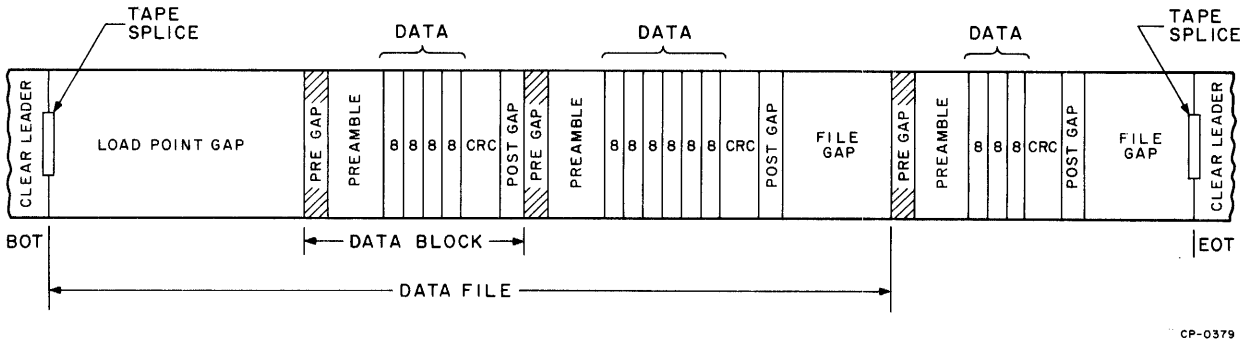


Figure 10-2 Typical TU60 Format

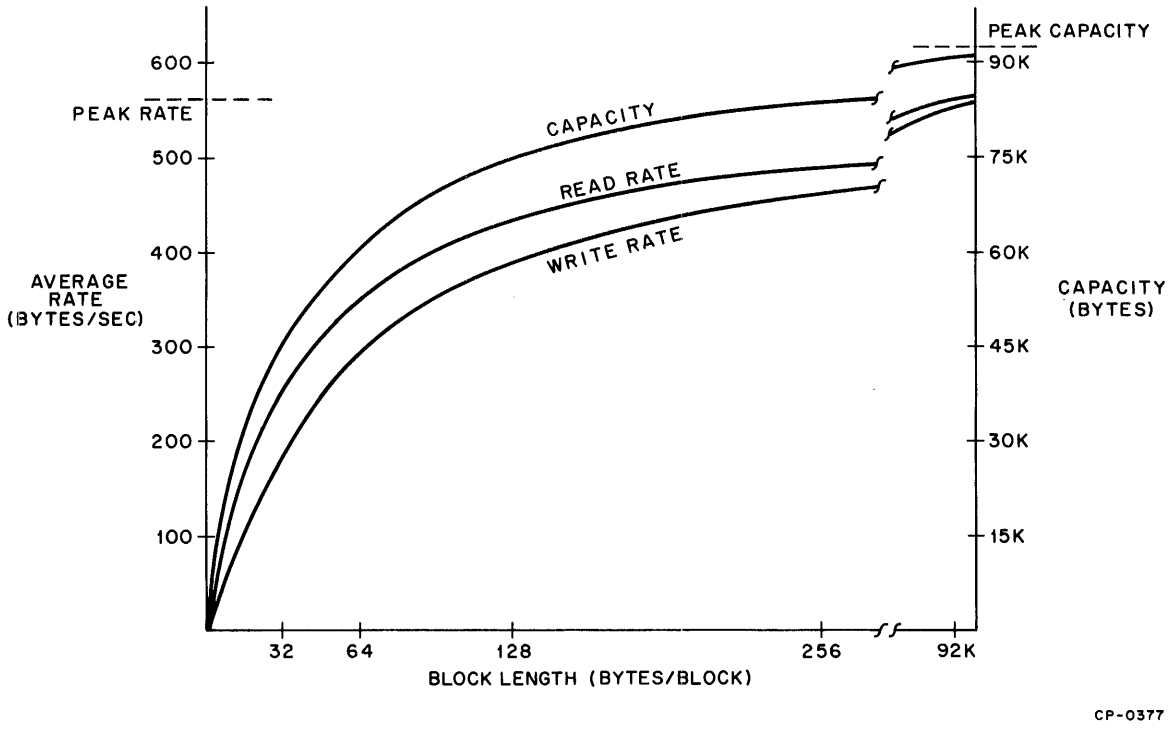


Figure 10-3 TU60 Capacity and Data Rate vs Block Length

10.4 DOCUMENTATION

Reference documents are required to program and maintain the TA8-E as follows:

a. PDP-8/E, PDP-8/F, and PDP-8/M Small Computer Handbook – DEC, 1973

b. PDP-8/E, PDP-8/F, and PDP-8/M Maintenance Manual Volume 1, DEC-8E-HR1B-D

c. DEC Engineering Drawing, TA8-E Cassette System Interface, B-DD-TA8-E-0-0

d. TA8-E Diagnostic, MAINDEC-08-DHTAA-A

e. TA8-E Data Reliability Test, MAINDEC-08-DHTAB-A

f. TU60 Cassette Tape Transport Maintenance Manual, DEC-00-TU60-DA

g. TU60 Engineering Drawings, B-DD-TU60-0-0

SECTION 2 INSTALLATION AND ACCEPTANCE TEST

The TA8-E Cassette System Interface is installed on site by DEC Field Service personnel. The customer should not attempt to unpack, inspect, checkout, or service the equipment.

10.5 INSTALLATION

Install the TA8-E as follows:

1. Ensure PDP-8/E power is off.
2. Ensure the correct device code select jumpers are installed (see Table 10-1 and refer to drawing M8331-0-1).
3. Connect the BC08R cable to the M8331 module as shown in Figure 10-4.
4. Insert the M8331 module into the OMNIBUS. Refer to Table 2-3 in Volume 1 of the *PDP-8/E Maintenance Manual* for module installation priority and placement on the OMNIBUS.
5. Unpack and install the TU60 Cassette Drives as specified in Chapter 2 of the *TU60 Maintenance Manual.*
6. Connect the other end of the cable to the TU60 Cassette Drive as shown in Figure 10-4.

Table 10-1
Device Code Selection Jumper Installation

Device Code	Install Jumpers					
	A	B	C	D	E	F
70	X		X		X	
71	X		X			X
72	X			X	X	
73	X			X		X
74		X	X		X	
75		X	X			X
76		X		X	X	
77		X		X		X

X designates jumper to be installed.

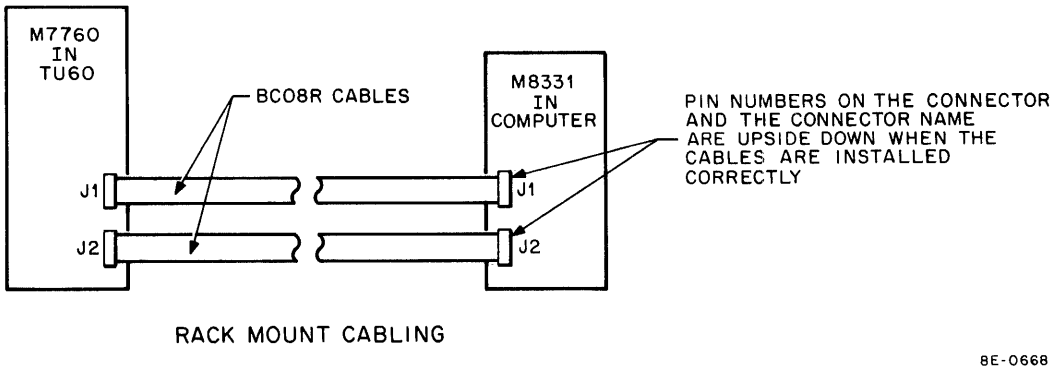


Figure 10-4 TA8-E and TU60 Cabling

10.6 ACCEPTANCE TEST

To test the TA8-E, run the following diagnostics in the order shown. The instructions for running the diagnostics are on the document accompanying the binary tape.

a. TA8-E Diagnostic, MAINDEC-08-DHTAA-A

b. TA8-E Data Reliability Test, MAINDEC-08-DHTAB-A

Refer to the Field Installation and Acceptance Test procedure in the TA8-E print set for acceptance test requirements.

10.7 TA8-E INTERFACE

The rack-mounted system is provided with two BC08R cables to connect the TA8-E on the OMNIBUS to the TU60 Cassette Drives. The signals on these cables are shown in Table 10-2, and a complete description of each signal is provided in Paragraph 10.10.

Table 10-2
TA8-E Input and Output Signals

M8331, J1 Pin Number	M8331, J2 Pin Number	TA8-E Input or Output	Signal
F		*	R/W 05 L
J		Input	DRIVE EMPTY L
E		Output	BACK BLOCK GAP L
R		Output	WRITE MODE L
X		Input	REWIND L
BB		Output	BACK FILE GAP L
DD		Output	REWIND CMD L
FF		Input	WRITE LOCK OUT L
LL		*	R/W 01 L
NN		*	R/W 02 L
RR		*	R/W 03 L
TT		*	R/W 04 L
	D	Output	READ/WRITE CRC L

Table 10-2 (Cont)
TA8-E Input and Output Signals

M8331, J1 Pin Number	M8331, J2 Pin Number	TA8-E Input or Output	Signal
	F	Output	READ/WRITE FILE GAP L
	R	Output	START L
	T	Output	INIT L
	V	Output	TRANSFER L
	Z	Input	EOF L (End of FILE)
	BB	Input	EOT/BOT L (End of Tape or Beginning of Tape)
	DD	Input	TIME ERROR
	LL	*	R/W 06 L
	NN	*	R/W 08 L
	RR	*	R/W 07 L
	TT	*	CRC BLK ERR L

*R/W 01 through R/W 08 are bidirectional lines used to transfer data in both directions.

NOTE

Pins not listed are tied to ground.

SECTION 3 FUNCTIONAL DESCRIPTION

This section provides a functional description of the major groups of logic, a list of TA8-E instructions, and a description of each signal transmitted and received by the TA8-E.

10.8 FUNCTIONAL DESCRIPTION

The TA8-E logic is divided into functional areas for descriptive purposes. Figure 10-5 is useful in understanding signal flow and the interrelationship of groups of logic. Section 4 provides detailed discussion of each group of logic.

10.8.1 IOT Decoder

There are eight sets of I/O device codes that determine which of eight possible TA8-E modules is being addressed. The decoding is done by jumpers connected to MD6, MD7, and MD8 (Table 10-1). When the correct code for the TA8-E goes to the I/O decoder and I/O PAUSE is present, a SELECT H signal is generated to allow the decoding of MD09–MD11 and to generate an INTERNAL I/O L. I/O PAUSE is present anytime an IOT instruction is executed by the program. INTERNAL I/O L prevents the processor from executing other IOTs while this instruction is executed. MD09–MD11 are decoded to control data transfers and to generate control signals that enable the TA8-E to load the Status A Register. The Status A Register generates control signals that are transmitted to the TU60.

The IOT decoder also controls the C0 and C1 lines, which control the direction of data transfers between the AC and the TA8-E registers.

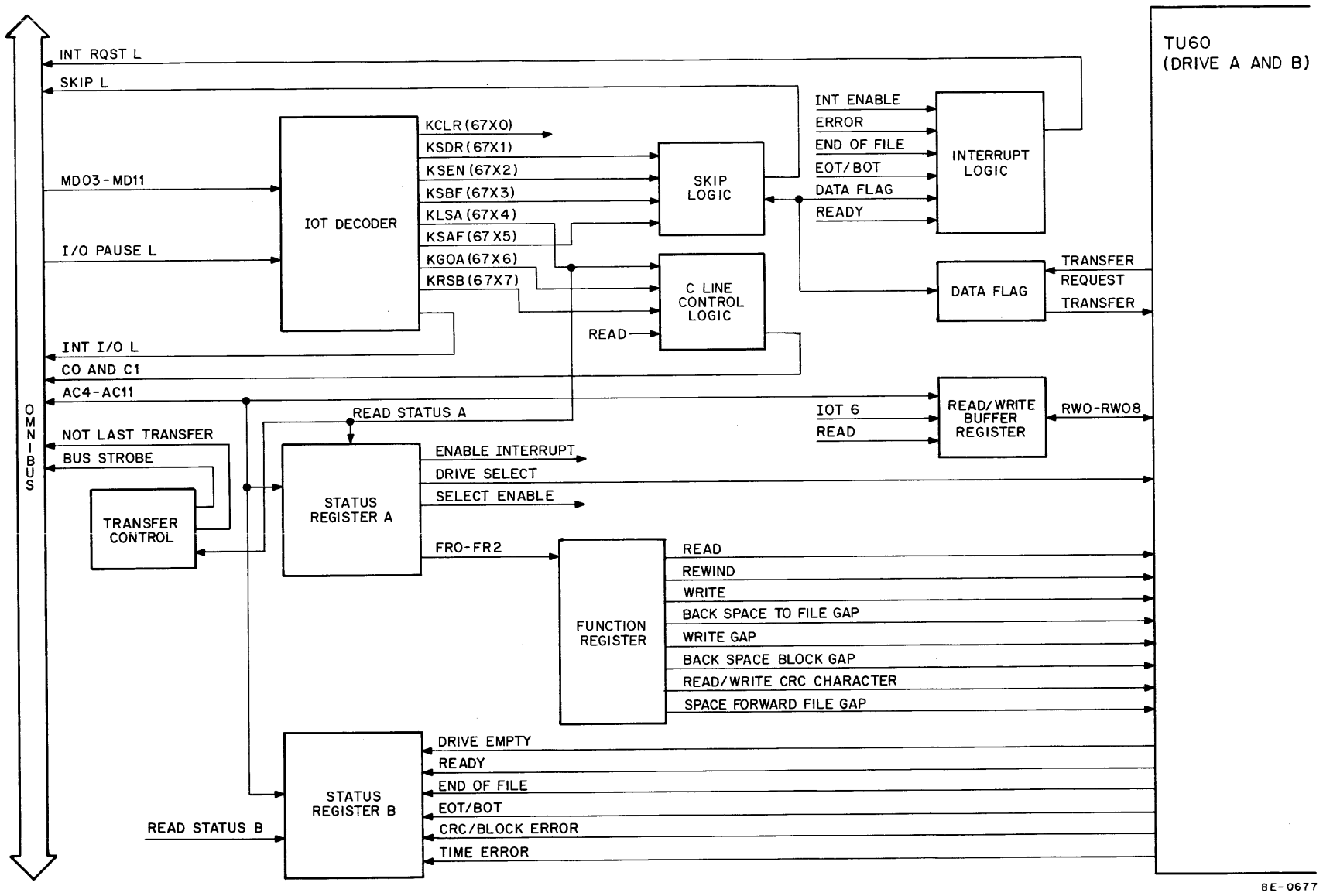


Figure 10-5 TA8-E Block Diagram

10.8.2 Status A Register

The Status A Register (Figure 10-6) is loaded from AC04–AC11 by the KLSA instruction and used to enable interrupts, select one of two drives (drive A or B), enable the TU60 transmitters and receivers, and provide signals FR0–FR2 to the Function Register. Signals FR0–FR2 are decoded to select one of the TU60 functions. The KLSA instruction also transfers the complement of the Status A Register to the AC during maintenance operations.

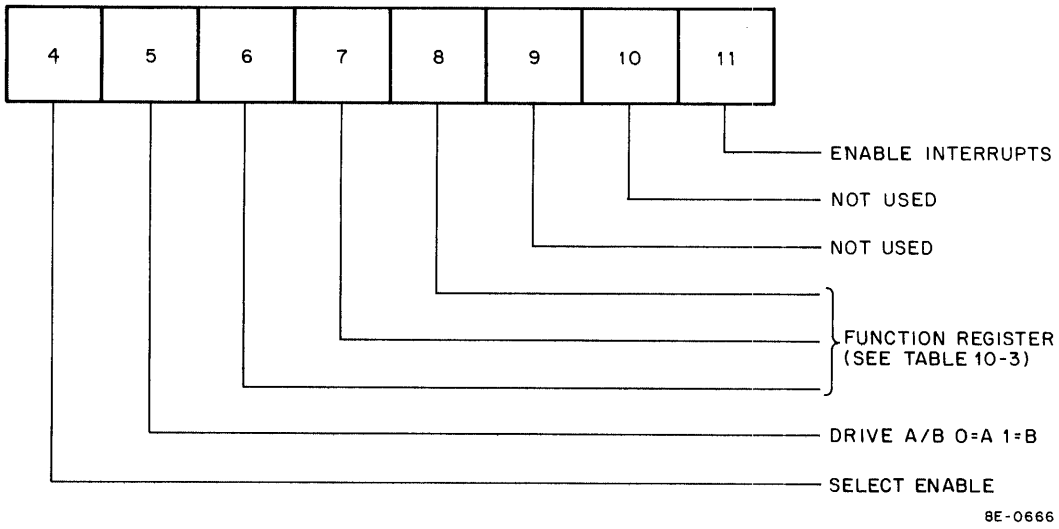


Figure 10-6 Contents of the Status A Register

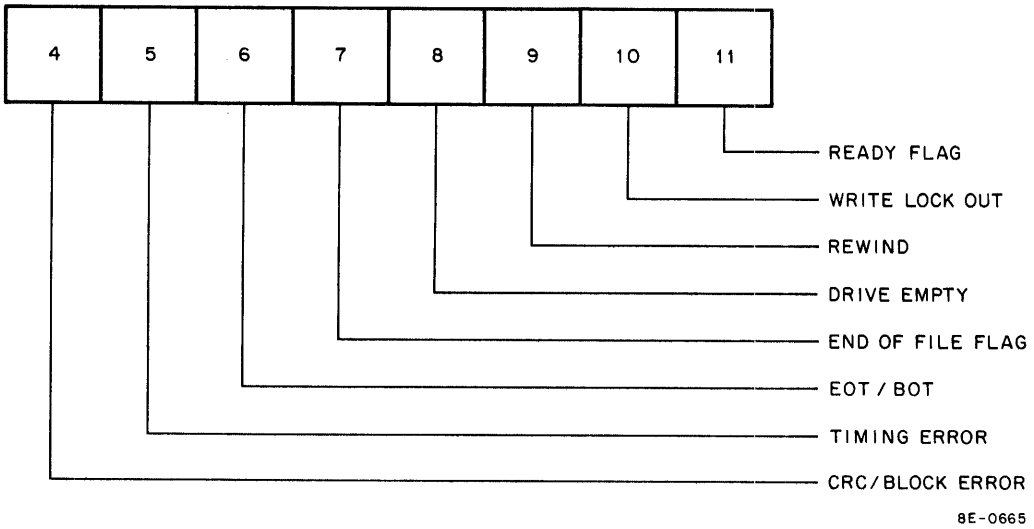


Figure 10-7 Contents of the Status B Register

10.8.3 Function Register

The Function Register (Table 10-4) decodes FR0—FR2 and provides control signals to the TU60. These control signals determine the operation the TU60 will perform, i.e., read or write.

10.8.4 Status B Register

The Status B Register contains the current status of TU60 (Figure 10-7), which can be transferred to the AC for evaluation by the program. The KRSB instruction transfers the contents of this register to AC4—AC11.

10.8.5 Read/Write Buffer Register

The Read/Write Buffer Register provides temporary storage of data to be written on the tape or read from the tape. Without this register the TA8-E would have to transfer data to the processor within 230 μs in order to prevent a TIME ERROR. Using the Read/Write Buffer Register, 1.84 ms is allowed between transfers, or the time required by the TU60 to read or write an 8-bit byte.

10.8.6 Data Flag

The Data flag is set for every byte read or written including the two CRC bytes. The Data flag is cleared by the KGOA instruction. Data flags normally occur once every 1.84 ms (Paragraph 10.11.1.10).

10.9 INSTRUCTION AND STATUS BITS

The instructions used to program the TA8-E are shown in Table 10-3. The status bits associated with these instructions are explained in Tables 10-4 and 10-5.

The KLSA instruction (Table 10-3) has two functions: 1) to transfer data from AC4—AC11 to the Status A Register and 2) to clear the AC and transfer the complement of the Status A Register to the AC. To accomplish this, the C lines, C0 and C1, must be switched during execution of the instruction. Processor timing must be stopped during TS3 by NOT LAST TRANSFER L to allow time to switch the C lines. After the C lines are switched, processor timing is restarted by BUS STROBE and the complement of the Status A Register is read into the AC.

10.9.1 Programming Sequence

Figure 10-8 is a flow diagram of TA8-E operations showing the TA8-E programming and operation sequences.

10.10 INPUT AND OUTPUT INTERFACE SIGNALS

The input and output signals are 0.0V (low) when true and +3V (high) when false. Note that the following signals must be present at the TU60 during an entire operation.

a. SELECT ENABLE L
b. DRIVE B L
c. BACK BLOCK GAP L
d. BACK FILE GAP L
e. READ/WRITE FILE GAP L

REWIND L, READ/WRITE CRC L, TRANSFER C, and WRITE MODEL signals are transmitted to the TU60 and stored in the TU60 until an operation is completed.

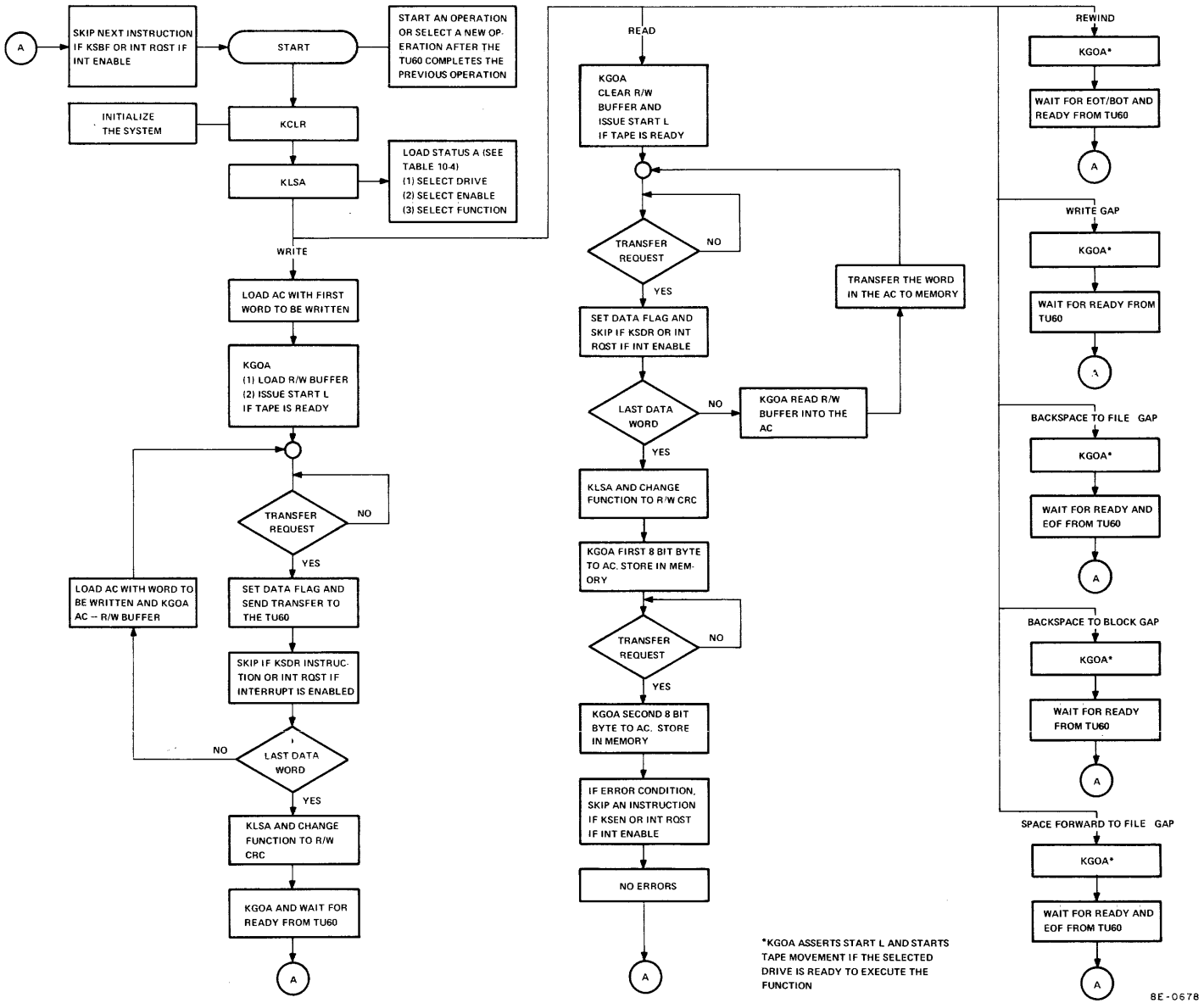


Figure 10-8 TA8-E Flow Diagram

Table 10-3
TA8-E Instructions

Mnemonic	Octal Code	Operation
KCLR	67X0	Clear All: Clear the Status A and Status B Registers (Tables 10-4 and 10-5).
KSDR	67X1	Skip the next instruction if the Data flag is set during read or write operations.
KSEN	67X2	Skip the next instruction if any of the following are true: a. Tape is at EOT/BOT (End of Tape or Beginning of Tape). b. The TU60 is not ready or the selected drive is empty.
KSBF	67X3	Skip the next instruction if the Ready flag is set.
KLSA	67X4	Load Status A from AC4–AC11, clear the AC, and load the complement of Status A back into the AC (Table 10-4).
KSAF	67X5	Skip on any flag or error condition.
KGOA	67X6	Assert the contents of the Status A Register and transfer data into the AC during a read operation or out of the AC to the Read/Write Buffer during a write operation. This instruction has three functions. a. Enables the command in the Status A Register to be executed by the TU60. b. For read operations, the first KGOA instruction causes the tape to start moving, and when the Data flag sets, a second KGOA transfers the first byte from the Read/Write Buffer to the AC. The Data flag sets after each 8-bit byte is read from the TU60. c. For write operations, the Status A Register is set up for a write, and the AC contains the first byte to be written on tape. When the KGOA instruction is executed, the tape starts to move and the first byte is transferred to the TU60.
KRSB	67X7	Transfer the contents of the Status B Register into AC4–AC11 (Table 10-5).

10.10.1 Output Interface Signals

The TA8-E provides the following output signals to control the TU60.

10.10.1.1 SELECT ENABLE L – This signal, at a logical 1, enables the TU60 input/output transmitters and receivers if bit 04 in the Status A Register is set (1).

10.10.1.2 DRIVE B L – This signal is asserted by bit 05 in the Status A Register to select one of the dual tape drives. A logical 1 (low) selects drive B or a logical 0 (high) selects drive A.

10.10.1.3 START L – This signal, at a logical 1, is used in conjunction with a specific command to initiate command execution. If a command is to be performed, the drive must be in the READY state (READY L asserted) and the command must be present and stable one microsecond prior to START L. If this is the case, when START L is received, the TU60 removes the READY L signal and initiates execution of the tape command. When READY L is removed, the TA8-E then removes START L. While the command is being executed, any additional START L signals are ignored by the drive.

10.10.1.4 REWIND L – This signal, at a logical 1 (low), is clocked by the START L signal to cause the TU60 to rewind to Beginning Of Tape (BOT).

Table 10-4
Contents of the Status A Register

AC Bit	Function
11	When bit 11 is a 1, enable the interrupt logic.
10	Not Used.
09	Not Used.
08–06	AC08–AC06 are applied to the Function Register to select one of the TU60 operations as follows:
05	Select TU60 Drive A if bit 5 is a 0 and Drive B if bit 5 is a 1 (high).
04	Enable the TU60 input receivers and most of the output transmitters.

AC06 (FR0)	AC07 (FR1)	AC08 (FR2)	Operation
0	0	0	Read
0	0	1	Rewind
0	1	0	Write
0	1	1	Back Space to File Gap
1	0	0	Write Gap
1	0	1	Back Space to Block Gap
1	1	0	Read/Write CRC Character
1	1	1	Space Forward to File Gap

Table 10-5
Contents of the Status B Register

AC Bit	Function
11	Ready flag: The Ready flag is set (1) when the selected drive is ready to accept commands from the TA8-E. A cassette must be installed and the selected tape drive must be stopped, which would indicate that previous tape operations have been completed.
10	WRITE LOCK: WRITE LOCK is set (1) if the selected drive is empty or if the cassette installed is write protected.
09	REWIND: REWIND is set (1) if the selected drive is performing a rewind operation.
08	DRIVE EMPTY: DRIVE EMPTY is set (1) if the selected drive does not have a cassette installed or the cassette installed is not a digital grade cassette.
07	End of File: The End of File (EOF) flag is set (1) if a file gap is detected or the TU60 reads a blank space on the tape.
06	EOT/BOT: End of Tape or Beginning of Tape (EOT/BOT) is asserted if the photosensor on the TU60 is uncovered when the tape is at the beginning or end of tape (Figure 10-2).
05	TIMING ERROR: TIMING ERROR is set (1) if the TA8-E does not respond to a TRANSFER REQ from the TU60 within 230 μs.
04	CRC/BLOCK ERROR: CRC/BLOCK ERROR is set (1) if a CRC ERROR is detected during a read operation.

10.10.1.5 BACK BLOCK GAP L – This motion command signal, at a logical 1 (low), is clocked by the START L signal to cause reverse tape motion at read/write speeds across a data block to the preceding PREGAP.

10.10.1.6 BACK FILE GAP L – This signal, at a logical 1 (low), is clocked by the START L signal to cause reverse tape motion at search speed across a data file and the tape drive stops at two-thirds of the preceding file gap.

10.10.1.7 READ/WRITE FILE GAP L – This signal, at a logical 1 (low), is used in conjunction with the WRITE MODE L signal to initiate either forward tape motion or a write file gap operation. If WRITE MODE L is a logical 1 when this signal is clocked by the START L signal, 535 ms of tape is erased. If the gap is a load point gap (at the Beginning Of Tape), 1.4 seconds of tape is erased. If WRITE MODE L is a logical 0 when this signal is clocked, tape on the selected drive moves forward, stopping at the beginning of the next file gap.

10.10.1.8 WRITE MODE L – This signal selects either the read or write logic. For a write or write file gap operation, this signal, at a logical 1, is clocked by the START L signal to set the TU60 Write flip-flop.

For a read operation, this signal, at a logical 0, allows the START L signal to reset the Write flip-flop in the TU60. Once the specific operation is initiated, the Write flip-flop remains either set or reset until the next operation is started.

10.10.1.9 TRANSFER L – During a write operation, this signal, at a logical 1, is transmitted to the TU60 in response to a TRANSFER REQ L signal. If this is the case, TRANSFER L sets the TRANS REQ flip-flop and the 8-bit byte is loaded into the TU60 Data Buffer.

During a read operation, this signal, at a logical 1, is transmitted to the TU60 in response to a TRANSFER REQ L signal. TRANSFER L sets the TRANS REQ flip-flop to indicate that the 8-bit byte has been loaded into the Read/Write Buffer.

10.10.1.10 READ/WRITE CRC L – During a write operation, this signal, at a logical 1, causes the accumulated CRC character to be recorded on the tape. R/W CRC L is transmitted to the TU60 while the final data byte is being recorded. When this occurs, the next TRANSFER REQ L signal is inhibited and the CRC character is recorded after the final data bit is written (Paragraph 10.8.6).

During a read operation, this signal, at a logical 1, tests the CRC Register for an error. At the start of a read operation, the CRC ERR flip-flop is set and remains set while the data block is being read. After the first eight CRC bits have been read, the TA8-E interface transmits READ/WRITE CRC L. READY L inhibits CRC ERROR (if one occurs) until the transfer is completed. When the final TRANSFER REQ L signal is generated, the CRC Register is checked for 0. If the register is not 0 (data read incorrectly), the CRC ERR flip-flop remains set and when READY L is generated, a CRC ERROR L signal is also generated. If the data has been read correctly, the CRC ERR flip-flop resets and a CRC ERROR L signal is not generated.

10.10.1.11 INITIALIZE L – This signal, at a logical 1, removes all TU60 flags (except EOT/BOT or CRC ERROR), generates READY L, and except for a rewind operation stops tape motion regardless of the tape position.

10.10.2 Input Interface Signals

The following input signals are received from the TU60 and applied to Status B, the interrupt logic, and the skip logic.

10.10.2.1 OFF LINE L – This signal, at a logical 1, indicates that the appropriate tape cassette is not properly loaded on the selected drive, or that the clear leader sensing lamp has failed.

10.10.2.2 READY L – This signal, at a logical 1 (low), indicates that the appropriate tape cassette has been properly loaded and tape motion is not occurring on the selected drive. In general, READY L is generated when all command functions have been completed and the drive is ready for the next operation, or when a clear leader on the tape is encountered.

10.10.2.3 END FILE L – This signal, at a logical 1, indicates that a file gap has been detected or the tape is blank.

10.10.2.4 EOT/BOT L – This signal, at a logical 1, indicates that the drive has reached the End-of-Tape or Beginning-of-Tape (clear leader uncovers photosensor). When this occurs, tape motion stops and the READY L and EOT/BOT L signals are generated.

10.10.2.5 REWIND L – This signal, at a logical 1, indicates that the selected drive is performing a rewind operation.

10.10.2.6 WRITE PROTECT L – This signal, at a logical 1, indicates that a write-protected cassette is loaded on the selected drive, or that the drive is empty. If the cassette is write protected, the selected drive will not perform any write operations.

10.10.2.7 WRITE STATUS L – This signal, at a logical 1, indicates that a write or write file gap operation is being performed on the selected drive.

10.10.2.8 TRANSFER REQUEST L – During a write operation, this signal, at a logical 1, indicates that the drive is ready to receive an 8-bit byte from the Read/Write Buffer Register. The TRANSFER REQ L signal is generated one bit time before a byte is needed, and this signal is removed when the interface responds with a TRANSFER L signal. During a read operation, TRANSFER REQ L, at a logical 1 (low), indicates that a byte from the drive is ready to be transferred to the Read/Write Buffer Register. The TA8-E must then respond with a TRANSFER L signal within one bit (230 μs) after the TRANSFER REQ L signal is generated or a TIME ERROR occurs.

10.10.2.9 TIME ERROR L – This signal, at a logical 1, indicates that the interface has not responded to a TRANSFER REQ L signal within the allotted time (230 μs).

10.10.2.10 CRC BLOCK ERROR L – This signal, at a logical 1, indicates that a CRC error has occurred during a read operation. At the start of the read operation, the CRC ERR flip-flop is set. When the final CRC character is read, the CRC Register is checked for 0. If the register is not 0, the CRC ERR flip-flop remains set, and when READY L is generated, a CRC ERROR L signal is also generated.

SECTION 4 DETAILED LOGIC

10.11 DEVICE SELECT AND IOT DECODER

The IOT decoder (Figure 10-9) decodes TA8-E IOT instructions from the Memory Data Bus and generates signals to control the TA8-E and TU60. Bits MD3–MD11 are gated by I/O PAUSE when an I/O instruction is generated. MD3–MD8 generate signal SELECT H and enable bits MD9–MD11 to be applied to the IOT decoder. The device code 67X, where X is equal to 0–7, is selected by the jumpers on the output of NAND gates E7 (Table 10-1). The IOT decoder is a DEC 7442 IC (see Section 7 for truth table and logic diagram). The DEC 7442 IC is a BCD-to-decimal decoder that decodes MD9–MD11 and produces a low or one on the output line to indicate which instruction has been executed by the program. As an example, MD9 low, MD10, and MD11 high (100) produce a low on pin 4, which indicates a KLSA instruction was programmed.

10.12 CONTROL LOGIC

10.12.1 C Line Select Logic

The C line select logic (Figure 10-9) controls the direction of data flow between the AC and the Data Bus and determines whether or not the AC is cleared. Table 10-6 gives the status of C0 and C1 (high or low) for transferring data between the AC and Data Bus, using the TA8-E instructions. As previously stated, when the KLSA instruction is executed by the program, the C lines must be changed and this change must take place during the time that the instruction is being executed. To accomplish this, flip-flop E14 (DIR) is cleared at TP3 time of the instruction cycle (Figure 10-10), causing C0 L and C1 L to go low and asserting NOT LAST TRANSFER L. NOT LAST TRANSFER L stops processor timing to allow the Status A Register to settle and the C lines to switch before the complement of the Status A Register is applied to the AC via the Data Bus. ENABLE H is negated (low) to prevent the contents of the Status A Register from being applied to the Data Bus while the C lines are switching.

Table 10-6
C Line Select Levels for Transfers to the AC

Instruction	C0	C1	Transfer Operation
KLSA	low	high	AC→DATA BUS then 0→AC
	low	low	DATA BUS→AC
KGOB	low	high	WRITE: AC→DATA BUS
	low	low	READ: DATA BUS→AC
KRSB	low	low	DATA BUS→AC

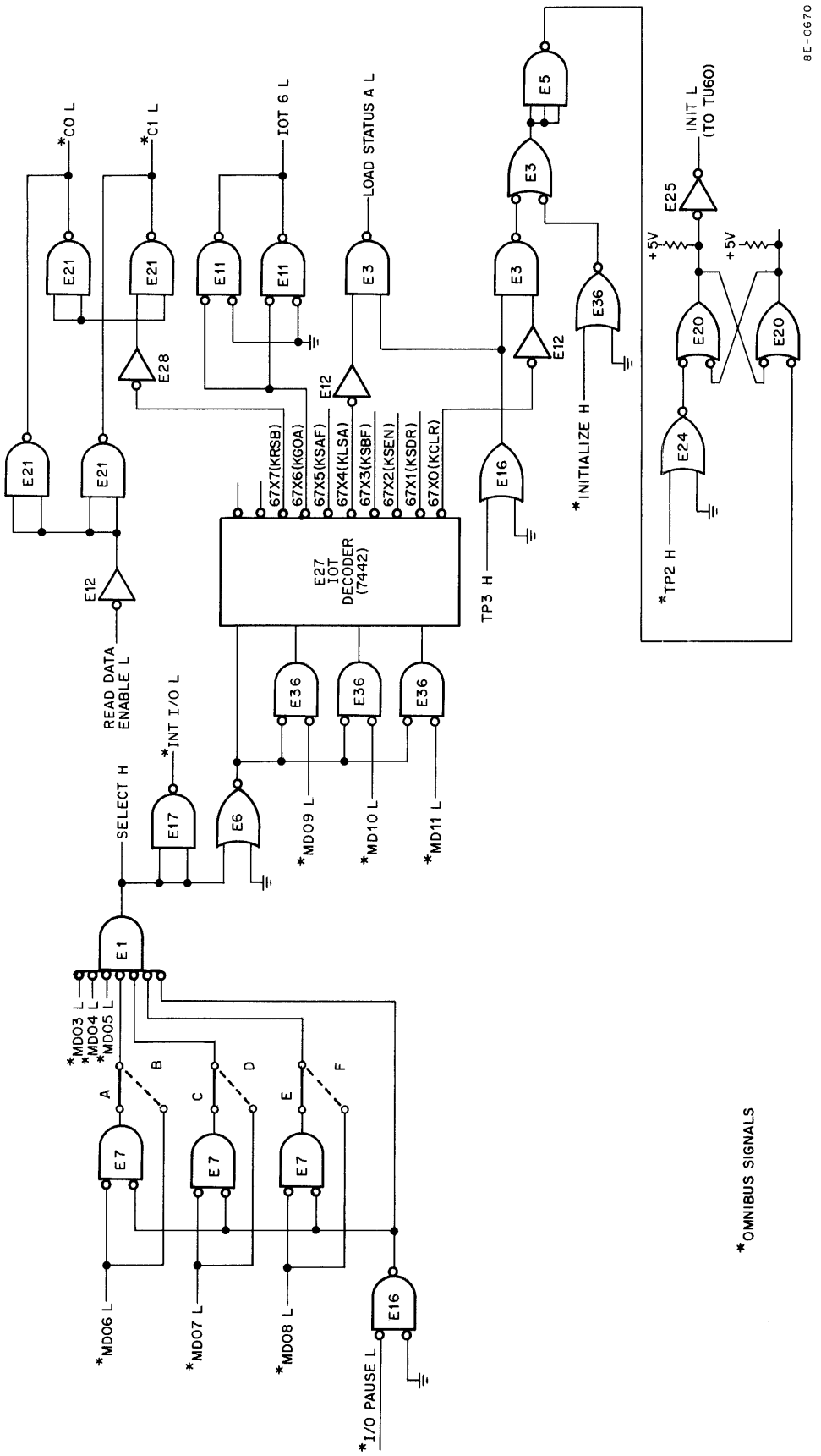


Figure 10-9 Device Select and IOT Decoder Logic

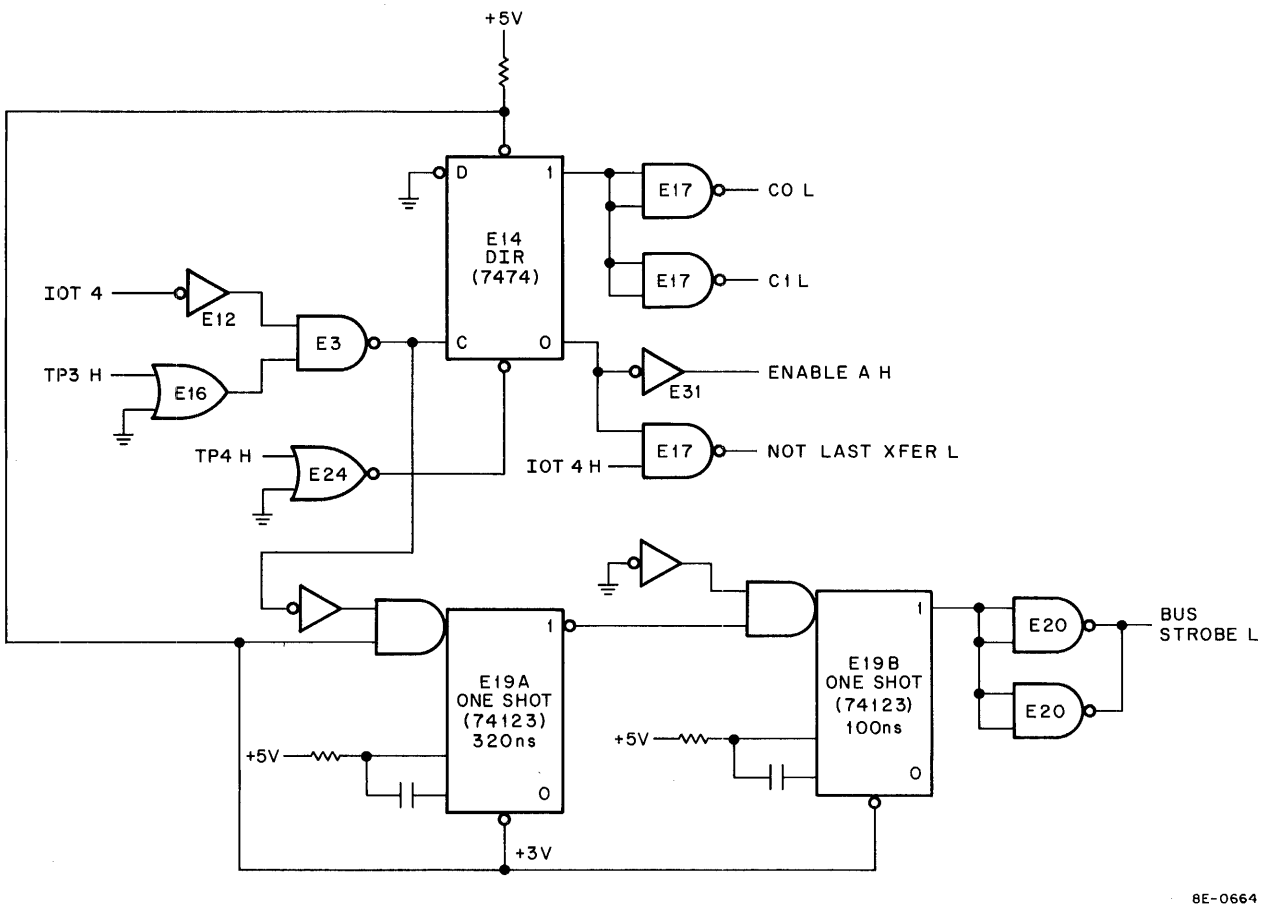


Figure 10-10 Data Transfer Control Logic

At the same time E14 (DIR) is cleared, the 74123 IC (see Appendix A, Volume 1 for logic diagram) is triggered (the 74123 IC is a dual one-shot multivibrator). E19A outputs a 320 ns pulse when triggered by the high to low transition on the output of E3 NAND gate at TP3 time. The trailing edge of the pulse out of E19A triggers E19B and generates a 100 ns pulse. The 100 ns pulse out of E19B asserts BUS STROBE L to restart processor timing. E14 changes state at TP4 time, and the C lines are switched to transfer the information on the Data Bus to the AC.

10.12.2 Time Pulse Logic

Time pulses, TP2, TP3, and TP4, are used throughout the module to enable gates and enable the execution of instructions.

10.12.3 Initialize and Clear All Logic

INITIALIZE clears all TA8-E and TU60 logic when the power is first turned on, when the CLEAR key on the programmer's console is depressed, or when the CAF instruction is executed. CLR ALL L is asserted when INITIALIZE L is asserted, or when the KCLR instruction is executed to clear all logic on the TA8-E and TU60.

INIT L to the TU60 (Figure 10-9) is asserted longer than CLR ALL in the TA8-E to allow enough time for the signal to be transferred to the TU60 and to clear the logic in the TU60. Flip-flop E20 is cleared by CLR ALL L to assert INIT L at TP3 time and remains cleared until the next TP2 time. TP2 H sets flip-flop E20 and removes INIT L from the TU60 during the next instruction cycle.

10.13 STATUS A REGISTER

The Status A Register (Figure 10-11) is loaded from the AC by a KLSA instruction, the AC is cleared, and the complement of Status A is transferred back to the AC. Thus, one instruction is used to load and read the Status A Register. The output of the Status A Register is used to enable interrupts, select a tape operation, select a tape drive, and enable the TU60 transmitters and receivers.

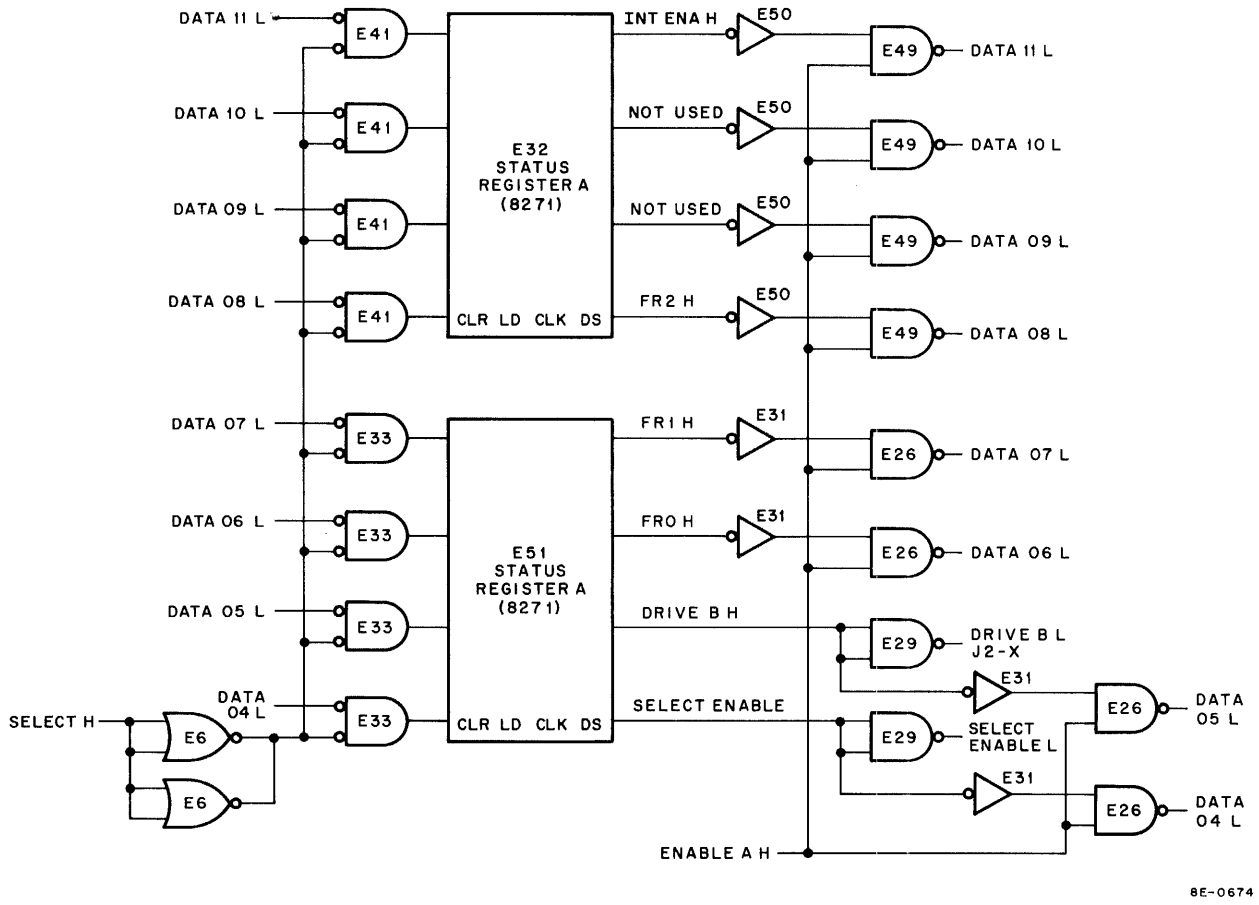


Figure 10-11 Status A Register

10.14 FUNCTION REGISTER

The Function Register (Figure 10-12) decodes FR0–FR2 from the Status A Register to select one of the TU60 operations (Table 10-4). The Function Register is a DEC 7442 IC (see Section 7 for truth table and logic diagram) that decodes FR0–FR2. The 7442 IC is a BCD-to-decimal decoder that produces a low on one output line for each combination of bits that are supplied as inputs. As an example, if FR0 is low and FR1 and FR2 are high (100), the Back Space To File Gap line is asserted (low) and the TU60 is commanded to execute this operation. The output signals applied to the TU60 are explained in Paragraph 10.10.

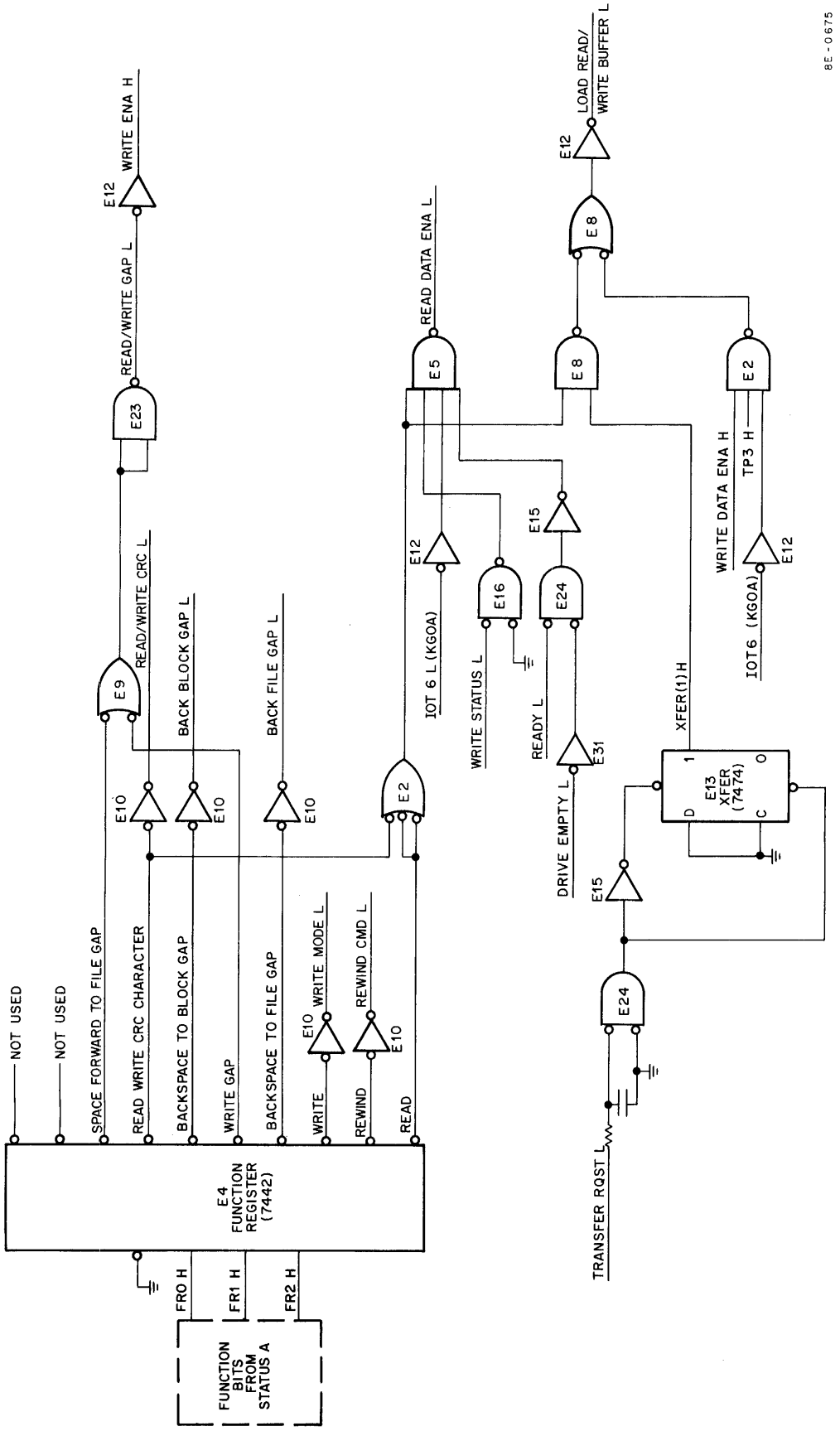


Figure 10-12 Function Register

10.15 START LOGIC

Before any operation can be started by the TA8-E and TU60, START L must be asserted (Figure 10-13). To set the START flip-flop, the TU60 must be in the READY state and there must be a cassette installed on the selected drive. When these conditions are met and the KGOA instruction is executed by the program, the START flip-flop will set at TP3 time and assert START L (low). START L is applied to the TU60 and the operation selected by the program when the Status A Register was loaded is started. The TU60 ignores any START L signals that are generated after an operation is started.

START is cleared by CLR ALL when it is asserted by INIT L from the processor or when the KCLR instruction is executed by the program.

END L is applied to Status B to indicate to the program that the selected drive is ready for an operation and the previous operation is complete. Note that READY L is negated if the TU60 is performing an operation.

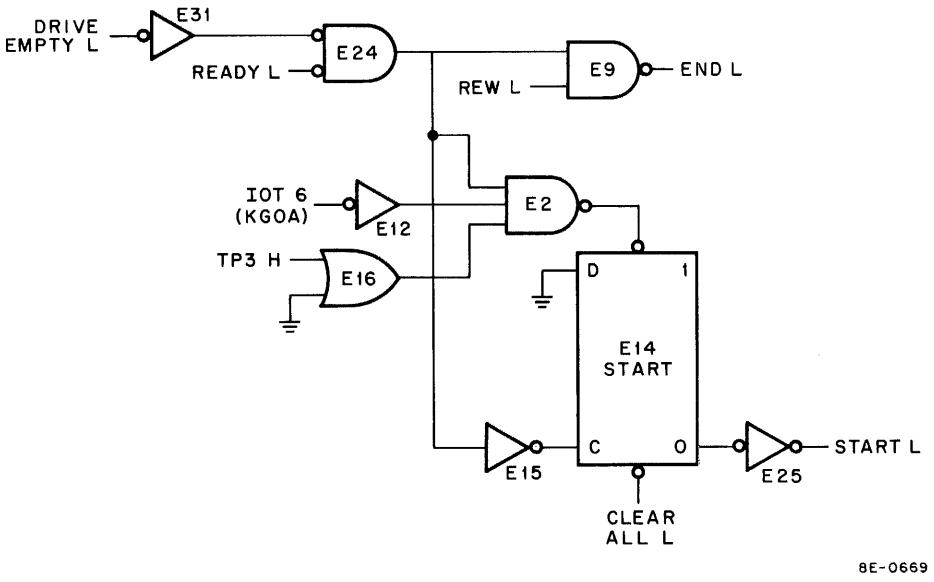


Figure 10-13 Start Logic

10.16 READ/WRITE BUFFER REGISTER

The Read/Write Buffer Register (Figure 10-14) is used during write operations to store an 8-bit byte until the drive is ready to write it on the tape. During read operations, this register stores a word read from the tape until the processor transfers the 8-bit byte to the AC. The Read/Write Buffer Register is an 8271 IC (see Appendix A, Volume 1 for truth table, logic diagram, and pin locations) which is parallel loaded when LOAD R/W BUFFER L is asserted (Figure 10-13).

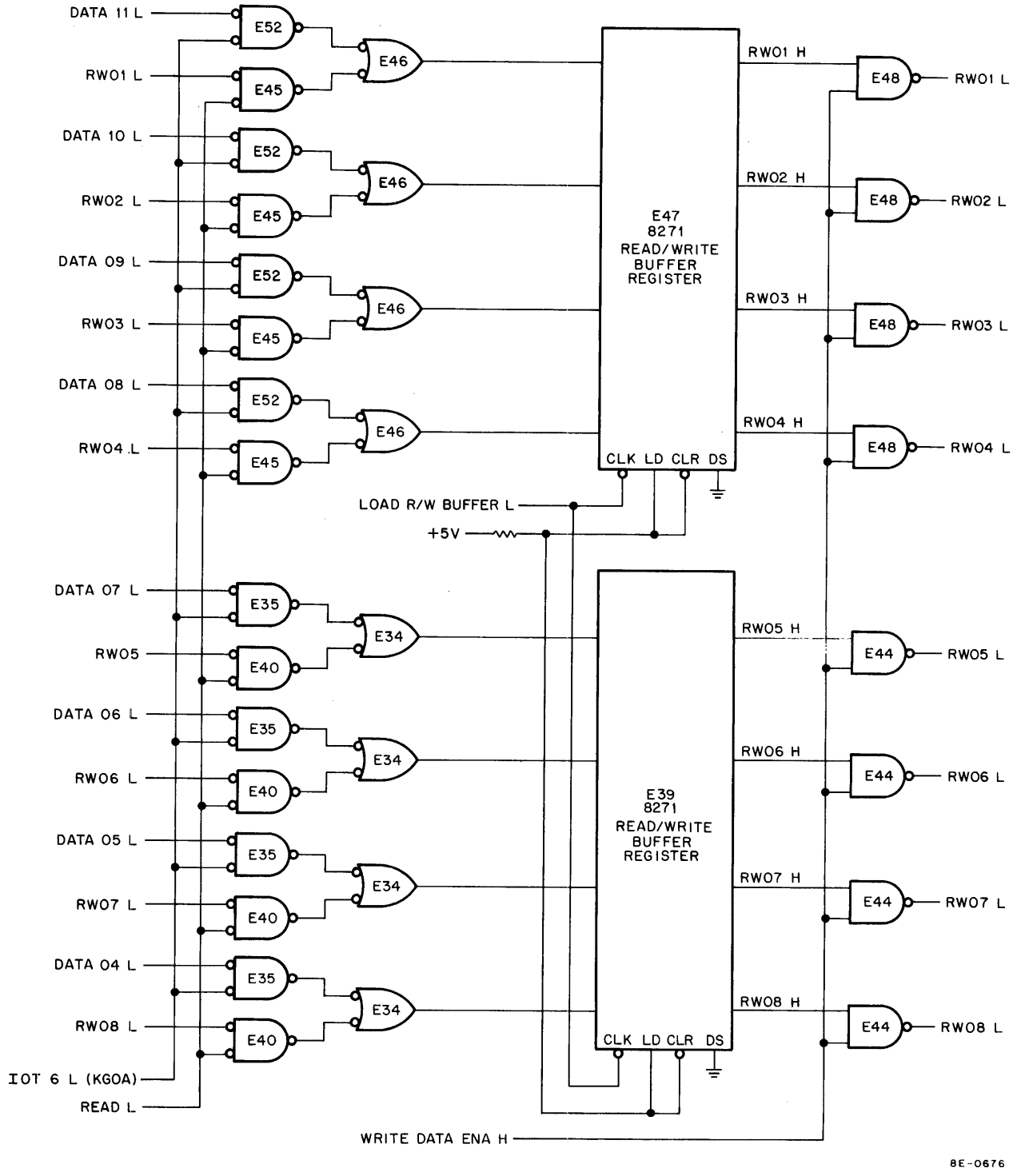


Figure 10-14 Read/Write Buffer Register

LOAD R/W BUFFER L is asserted when one of the following conditions are met:

a. During read operations, the XFER flag (Figure 10-15) must be set (1) and a read operation must be selected by the program. XFER is set by TRANSFER RQST L each time a word is read from tape and applied to the Read/Write lines (R/W 01—R/W 08). The selected drive must not be in a write status.

b. During write operations, if WRITE DATA ENA H (Figure 10-12) is asserted by the Function Register and the KGOA instruction is executed by the program. The selected drive must be in a write status.

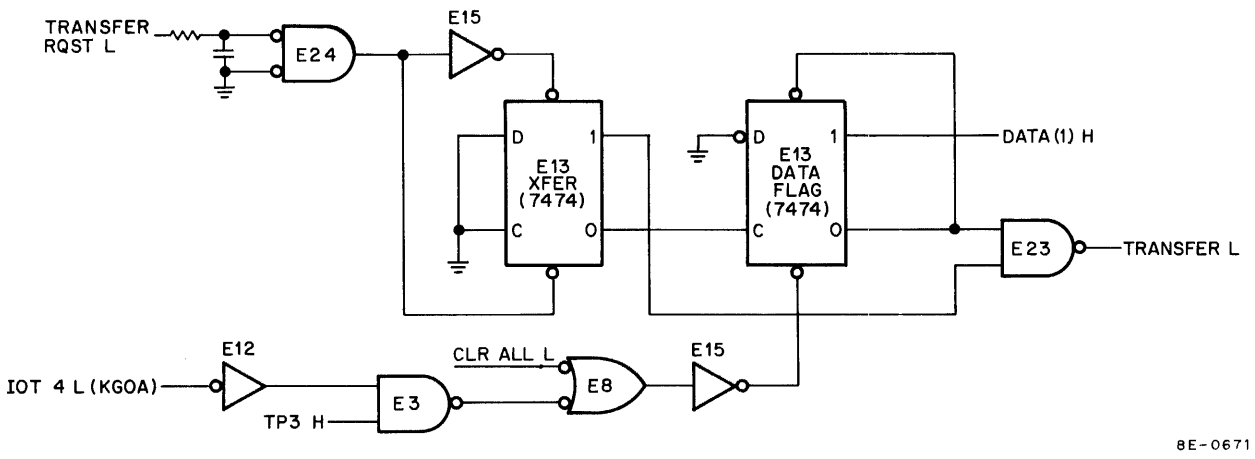


Figure 10-15 TA8-E Flags

10.16.1 Data Flag

The Data flag (Figure 10-15) is set each time a TRANSFER RQST is made by the TU60. When the Data flag sets, the program is interrupted by an INT RQST if the interrupt system is turned on (bit 11 in Status A must be 1) or a SKIP is generated if one of the SKIP IOTs are executed by the program. During read operations, the program must execute the KGOA instruction and transfer data to the AC from the Read/Write Buffer Register. During write operations, the KGOA instruction is executed and data is transferred from the AC and applied to the Read/Write lines via the Read/Write Buffer Register. WRITE DATA ENA H enables data to be applied to the Read/Write lines during write operations. During read operations, READ DATA ENA L (Figure 10-16) is asserted to transfer data from the Read/Write lines to the OMNIBUS.

10.17 INTERRUPT LOGIC

An INT RQST (Figure 10-16) is made by the TA8-E if bit 11 in the Status A Register is set (1), and the following conditions exist:

a. One of the following Error flags is set.

   1. TIME ERR
   2. WRITE LOCK (If a write operation)
   3. CRC/BLK ERR
   4. DRIVE EMPTY

b. The tape is REWINDING.
c. The tape is at EOT/BOT.
d. The Data flag is set.
e. END L is asserted (low).

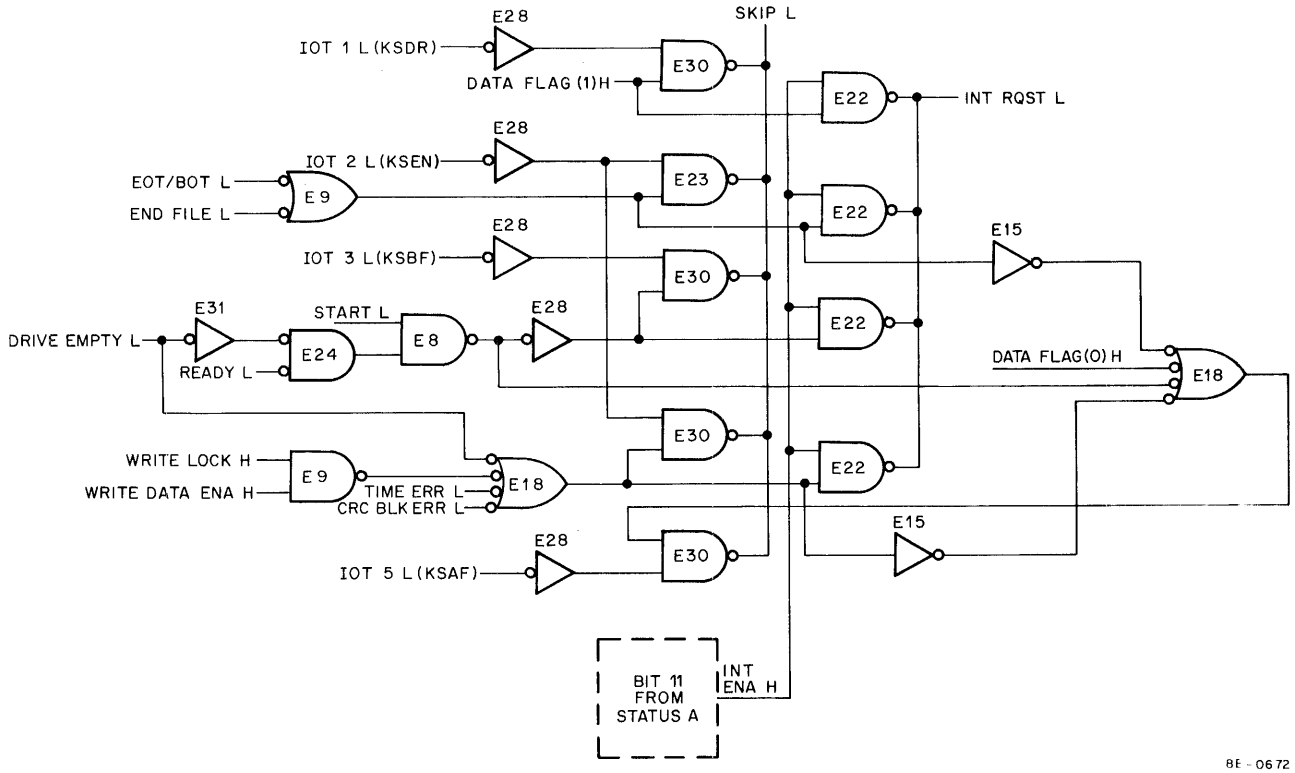


Figure 10-16 Interrupt and Skip Logic

10.18 SKIP

SKIP L (Figure 10-16) is asserted and the program will skip the next instruction if one of the following conditions exist:

a. The program executes a KSDR instruction and the Data flag is set (1). The Data flag is set when the program must execute a data transfer during read and write operations.

b. The program executes a KSEN instruction and the tape is at EOT/BOT or End of File (EOF).

c. The program executes a KSBF and the selected drive is not empty; tape drive is in the READY state and not rewinding.

d. The program executes a KSAF instruction and any flag is set.

10.19 OUTPUT DATA MULTIPLEXER

The Output Data Multiplexer (Figure 10-17) is used to apply read data to the Data Bus during read operations or the contents of Status B to the Data Bus when the KRSB instruction is executed by the program. The Output Data Multiplexer consists of two 8235 ICs (see Appendix A, Volume 1 for truth table, logic diagram and pin locations) that select one of two sets of inputs to be applied to the Data Bus. If the program executes a KRSB instruction, the IOT 7 L signal is asserted and the contents of the Status B Register are applied to the Data Bus. During read operations, READ DATA ENA L is asserted (low) and the data on the Read/Write lines is transferred to the Data Bus.

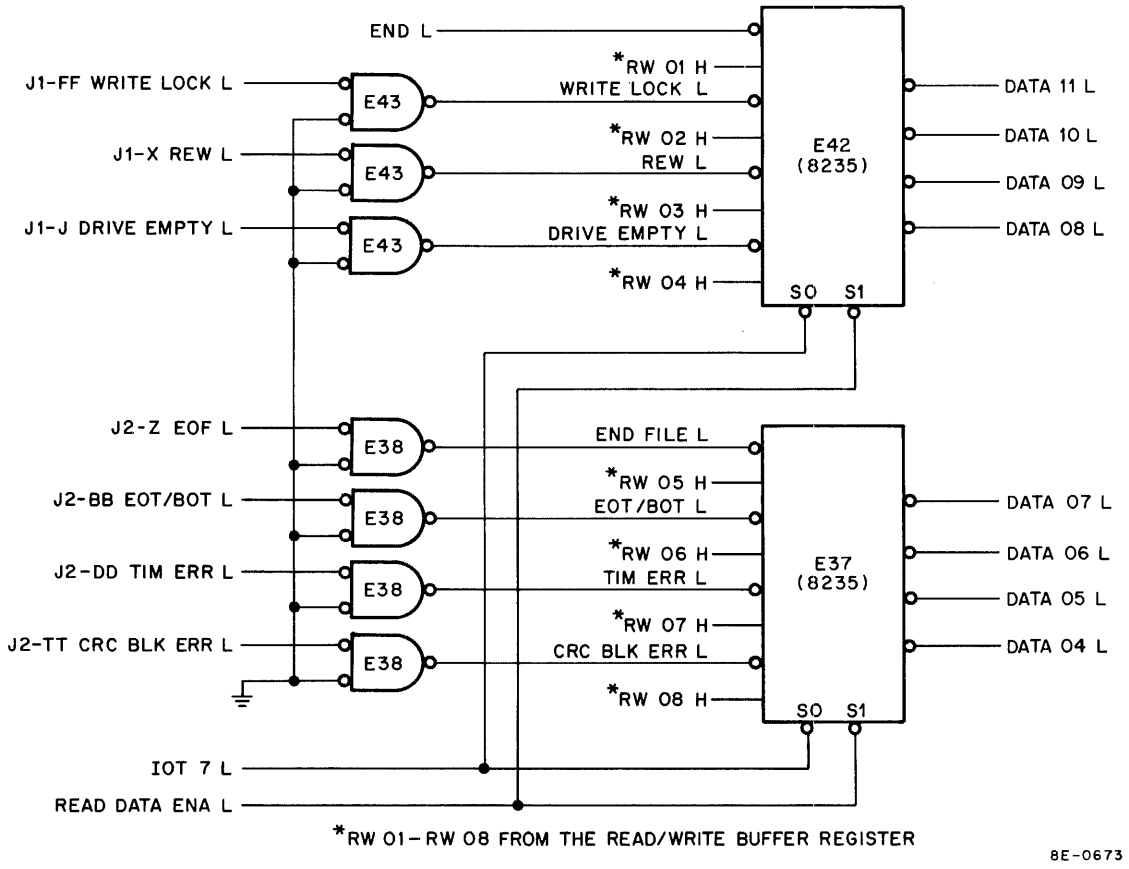


Figure 10-17 Output Data Multiplexer

SECTION 5 MAINTENANCE

10.20 PREVENTIVE MAINTENANCE

Recommended preventive maintenance should be scheduled at regular intervals to maintain reliability and performance in the TU60 Cassette Tape Transport System. Preventive maintenance schedules are found in the *TU60 Cassette Tape Transport Maintenance Manual* (DEC-00-TU60-DA).

The TA8-E Diagnostic (MAINDEC-08-DHTAA-A) and the TA8-E Data Reliability Test (MAINDEC-08-DHTAB-A) are supplied to checkout and test the TA8-E. The diagnostic programs and reliability tests check all logic and the ability to read or write data. TA8-E signals can be monitored with an oscilloscope while the diagnostics are running to aid in the location of malfunctioning components. When a malfunction is suspected, the TA8-E diagnostics should be used to checkout and troubleshoot the TA8-E. Refer to the *TU60 Cassette Tape Transport Maintenance Manual* for test equipment, troubleshooting aids, and adjustments.

10.21 CORRECTIVE MAINTENANCE

The following programs are provided to aid in troubleshooting the TA8-E.

NOTE

A Tektronix 453A or equivalent oscilloscope with X10 scope probe and an IC test clip are required for these tests.

10.21.1 IOT Decoder Check

To check the IOT decoder, perform the following steps:

1. Deposit the following program into core memory, starting at location 0200.

Memory Location	Instruction	Operation
0200	7604	LAS
0201	3202	DCA switches in 202
0202	0000	Contents of switches
0204	5200	JMP-3 to beginning

2. Set the Switch Register (SR) to 6700.

3. Load address 0200, then press CLEAR and CONT.

4. Set up the oscilloscope to monitor signals on channel A. Monitor SELECT H on pin 3 of E1. SELECT H should be present for 500 ns (Figure 10-18).

5. SYNC on channel A (SELECT H signal) and monitor pin 1 of E27 with channel B. Pin 1 is the output line of the IOT decoder for the 6700 (KCLR) instruction (Figure 10-9).

6. Change SR to 6701 and monitor logic for the 6701 instruction.

7. Set the Switch Register to octal values for each of the IOT instructions (Table 10-3) and monitor the logic associated with each instruction. Refer to the M8331 module prints (D-CS-M8331-0-1).

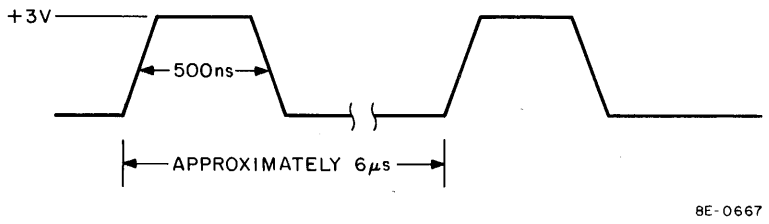


Figure 10-18 IOT Decoder Output Signal

10.21.2 Status A Register Check

To check the Status A Register, perform the following steps:

1. Deposit the following program into core memory, starting at location 0400.

Memory Location	Instruction	Operation
0400	7604	LAS
0401	6704	KLSA, Load Status A
0402	5200	JMP-2 to beginning

2. Set SR to 0377.

3. Monitor logic associated with E32 and E51 (Status A Register). Set SR4 through SR11 to both 0s and 1s to be certain both can be transferred. Monitor the gates associated with Status A Register (D-CS-M8331-0).

10.21.3 Status B Check

To check Status B signals, perform the following steps:

1. Deposit the following program into core memory.

Memory Location	Instruction	Operation
0600	6707	KRSB, Read Status B
0601	5200	JMP-1 to beginning

2. With a jumper or clip lead, ground pin 4 of E38. AC bit 4 should read a 1.

3. With a jumper or clip lead, ground pin 7. AC bit 5 should read a 1.

4. Check all of the status bits by grounding the pins of the E38 and E42 ICs (D-CS-M8331-0).

10.21.4 Read/Write Buffer Check

To check the Read/Write Buffer, perform the following steps:

1. Deposit the following program into core memory.

Memory Location	Instruction	Operation
1000	7200	CLA
1001	1300	TAD AC, WRITE
1002	6704	KLSA, Load Status A
1003	7604	LAS, Get Switches
1004	6706	KGOA, Load Read/Write Buffer from AC
1005	7200	CLA
1006	1301	TAD AC, Read
1007	6704	KLSA, Load Status A
1010	6706	Read Read/Write Buffer Register
1011	5200	JMP-9, to beginning
1100	0020	Constant
1101	0000	Constant

2. Monitor pin 13 of E44 and toggle SR4. Pin 13 on E44 should follow SR4.

3. Repeat step 2 for R/W 07 through R/W 01 gates with SR5 through SR11 (D-CS-M8331) for pins for R/W 07 through R/W 01.

10.21.5 Command Decoder Check

To check the command decoder, perform the following steps:

1. Deposit the program used to check the Status A Register beginning at location 400.

2. Monitor FR0–FR2 and toggle SR6–SR8. The level of FR0–FR2 should change when the bit in the SR associated with it changes.

SECTION 6 SPARE PARTS

The spare parts for the TA8-E are listed in Table 10-7.

Table 10-7
TA8-E Spare Parts

DEC Part No.	Description	Quantity
19-10436	DEC IC 74123	1
19-00046	DEC IC 7442	1
19-09973	DEC IC 97401	2
19-09972	DEC IC 6314	1
19-09971	DEC IC 6380	2
19-09935	DEC IC 8235	1
19-09929	DEC IC 7417	1
19-09705	DEC IC 8881	1
19-09686	DEC IC 7404	1
19-09615	DEC IC 8271	1
19-05579	DEC IC 7440	1
19-05577	DEC IC 7420	1
19-05576	DEC IC 7410	1
19-05575	DEC IC 7400	1
19-05547	DEC IC 7474	1

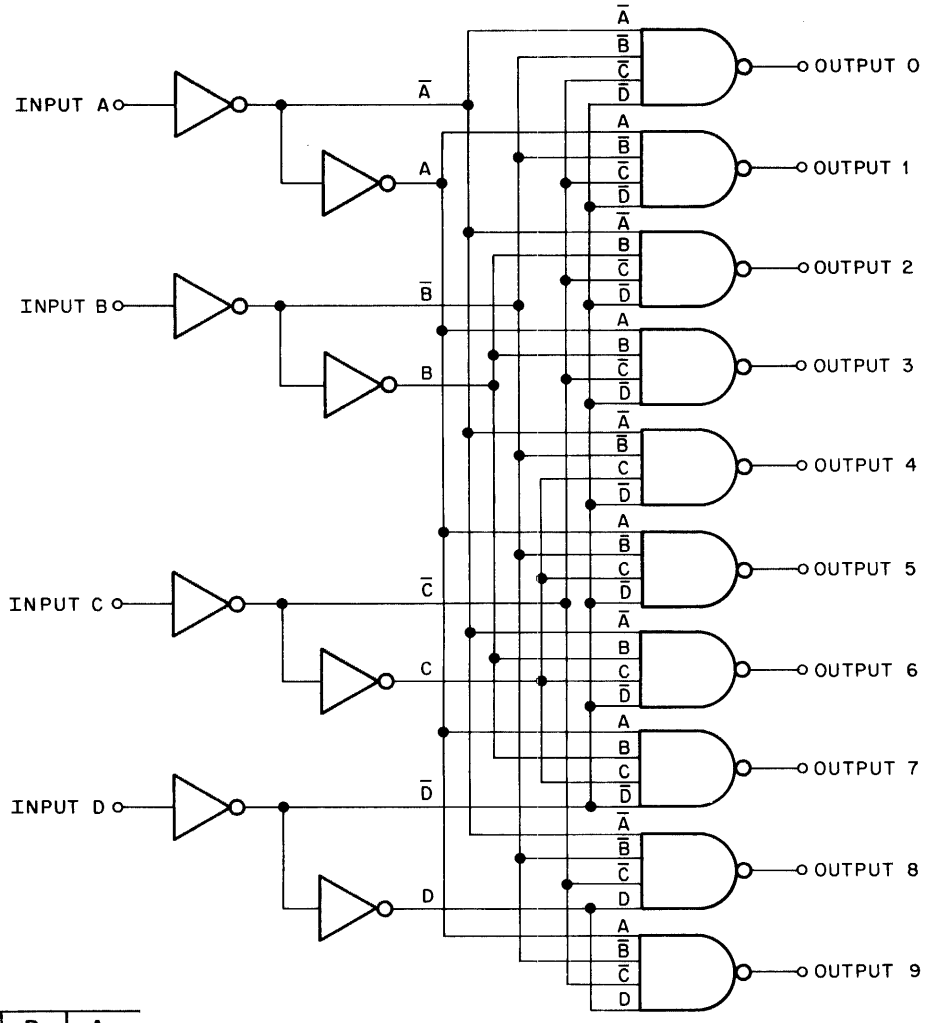
SECTION 7 IC DESCRIPTIONS

This section contains a description of those ICs used on the TA8-E that are not used in the PDP-8/E. ICs not included in this section are contained in Appendix A, Volume 1 of the *PDP-8/E Maintenance Manual.*

DEC 7442 IC

The DEC 7442 IC is a BCD-to-decimal decoder (Figure 10-19) that consists of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD data available for decoding by the NAND gates. Full decoding of valid input signals ensures that all outputs remain off for invalid input conditions.

In the TA8-E, the 7442 IC has a 3-bit input with the fourth bit (pin D) used as an enabling signal that allows the IC to have an output only when it is enabled. Thus, there will be no erroneous signals out of the decoder.



D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Truth Table

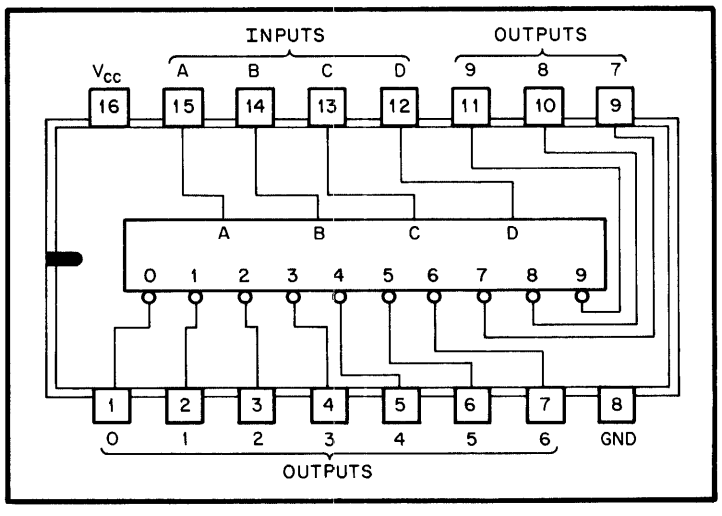


Figure 10-19 DEC 7442 IC

PART 8

DISKS

CHAPTER 11
RK8-E DISK DRIVE CONTROLLER

SECTION 1 INTRODUCTION

11.1 PURPOSE

The RK8-E (Figure 11-1) provides the interface between the PDP-8/E OMNIBUS and the RK05 Disk Drive. As a part of this function the RK8-E

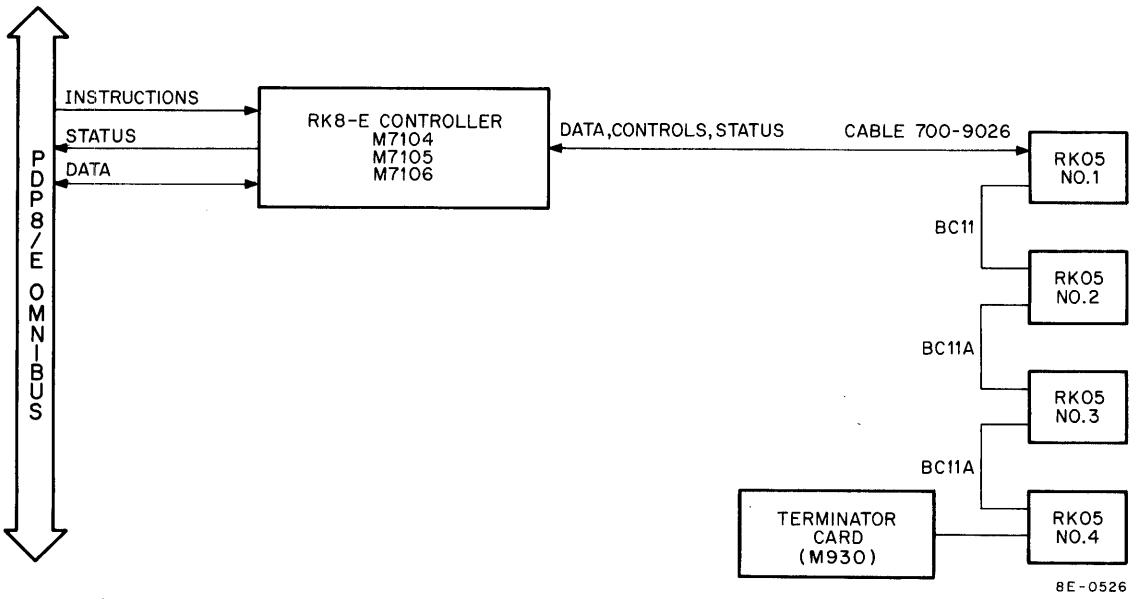


Figure 11-1 RK8-E Controller and RK05 Disk Drive System Block Diagram

a. Decodes programmed IOT instructions.

b. Accepts and stores current address, command, and extended memory address words.

c. Selects the designated RK05 and starts the designated operation.

d. Jointly (with the selected RK05) locates the disk address (track, sector, and surface).

e. Generates interrupts and skips for status checking operations.

f. Generates break requests to initiate single cycle data breaks (data transfers to or from memory).

g. Buffers the input/output data and performs related conversions (serial to parallel and parallel to serial).

h. Performs housekeeping chores for single cycle data break data transfers (i.e., increments Current Address Register and provides sequential memory addresses).

i. Counts bits and words in a transfer to determine when to end a data transfer.

j. Generates and checks CRC (parity) for each sector.

k. Provides flags to indicate current conditions and error status.

l. Provides logic to aid in the maintenance of the RK8-E and RK05.

11.2 PHYSICAL DESCRIPTION

The RK8-E consists of the following quad modules, which are inserted into the OMNIBUS and used to control up to 4 (maximum) RK05 Disk Drives.

- M7104, RK8-E Data Buffer Register and Status Module
- M7105, RK8-E Major Registers Module
- M7106, RK8-E Control Module

The RK8-E modules are inserted into the OMNIBUS and connected together with H851 Top Connectors. The RK8-E is connected to the RK05 Disk Drives by a 7009026 cable.

11.2.1 RK05 Disk Drive

The RK05 Disk Drive contains the drive electronics and mechanism for accepting and releasing the disk, positioning the read/write heads, and reading and writing data from the RK8-E control. The drive contains a removable disk cartridge, control logic, and a power supply. No power is supplied to the RK05 by the RK8-E, and the RK05 supplies no power to the RK8-E. Table 11-1 lists the RK05 Disk Drive specifications.

NOTE

The specifications in Table 11-1 apply to the RK05 when it is used with the RK8-E and a 16-sector cartridge. The RK05 may be used in other systems with other controllers and sector formats.

11.3 RECORDING METHODS AND FORMATS

This section describes the recording methods and the format used to write data on and read data from the RK05 Disk Drives.

Table 11-1

RK05 Disk Drive Specifications

Characteristic	Specification
Cylinder, Track, and Sector	
Cylinder Density	200 CPI
Cylinders/Drive	203
Tracks/Cylinder	2
Sectors/Track	16
Sectors/Cylinder	32
Bit Density and Storage	
Bit Density	2200 BPI
Bits/Cylinder	120,000
Bits/Sector	3750
Bits/Drive	24 million
Data Word Storage	
Words/Sector	400_8 or 256_{10}
Words/Track	$10{,}000_8$ or 4096_{10}
Words/Cylinder	20,000 or 8192_{10}
Words/Disk	1616K
Transfer Rate	
Word Transfer	8.32 usec
Bit Transfer Rate	1440 kHz
Recording Method	Double Frequency

11.3.1 Double Frequency Recording Method

The RK8-E uses the double frequency recording method. During a write operation, the RK8-E control generates timing pulses called Write Data Clock pulses (Figure 11-2). The time between the pulses is called a bit cell (space for writing data). A pulse within the bit cell represents a data 1 and the absence of a pulse represents a data 0. The clock pulse and data (0 or 1) are sent to the drive as Write Data and Clock pulses. Each pulse is recorded on the disk as a flux transition. A pulse representing a data 1 and the clock pulses cause a change in direction of current flow through the write heads and thus a change in the magnetic flux on the surface of the disk. Zero data bits do not cause a change in current flow through the write head; thus, there is no change in the magnetic flux on the surface of the disk.

During a read operation, the drive electronics separates the bit cell flux transitions and the data flux transitions. The bit cell flux transitions are sent to the RK8-E as Read Data Clock pulses and the data transitions are sent as Read Data pulses (serial bits of data).

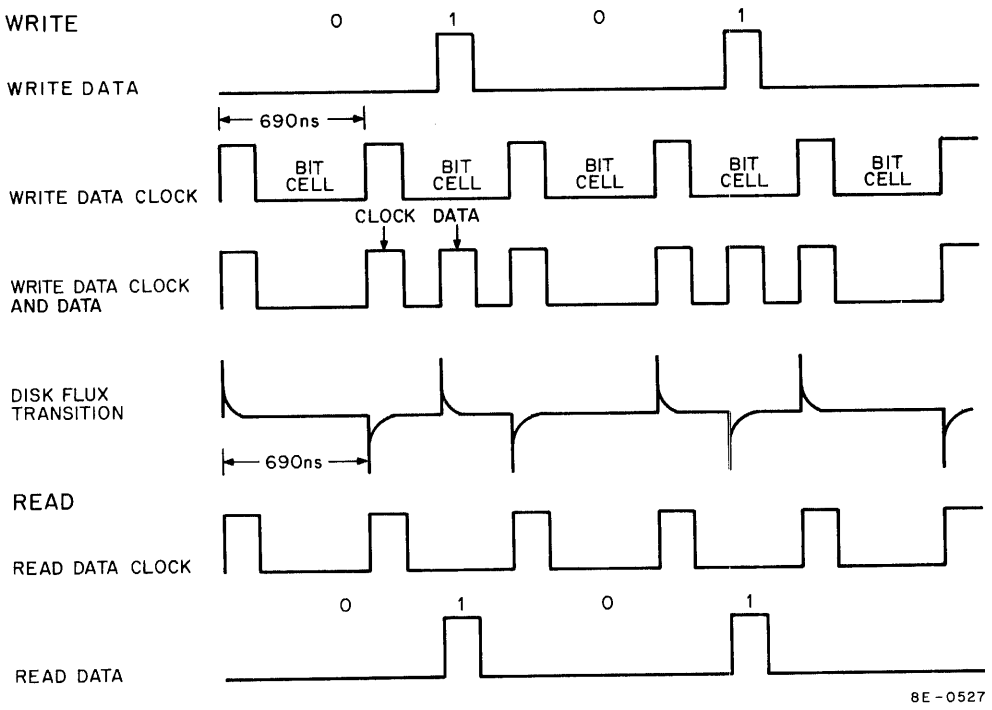


Figure 11-2 Double Frequency Recording Method

11.3.2 Disk Addressing

The surfaces of the RK05 Disk Cartridge are divided into 203 tracks and 16 sectors (Figure 11-3). Each surface has one read/write head.

A drive can be commanded to seek one of 203 cylinder addresses. The drive generates a signal and supplies it to the RK8-E when it is on the correct cylinder address. When the drive completes a seek, it is advisable to check the cylinder address to ensure the heads are positioned correctly.

The RK8-E can be commanded to read the cylinder address (HEADER) from the first cylinder it finds and check this against the cylinder address it previously sent to the disk drive. If the two addresses agree, the controller starts a data transfer; if they do not agree, an ERROR flag is set. The program must determine what to do about the ERROR flag.

A drive performing a seek can be deselected and another drive selected and commanded to seek; thus, overlapped seeks are possible.

11.3.3 Sector Format

The sector format (Figure 11-3) consists of a 140 μs PREAMBLE of zero data bits (time pulses only), a SYNC bit (data bit = 1), a 16-bit HEADER word containing the cylinder address, 256 12-bit data words, a 16-bit Cyclic Redundancy Check (CRC) character, and a 25 μs POSTAMBLE (erase delay zone).

11.3.3.1 HEADER Word – The HEADER is a 16-bit word containing 5 zero bits and a 8-bit cylinder address followed by 3 zero bits.

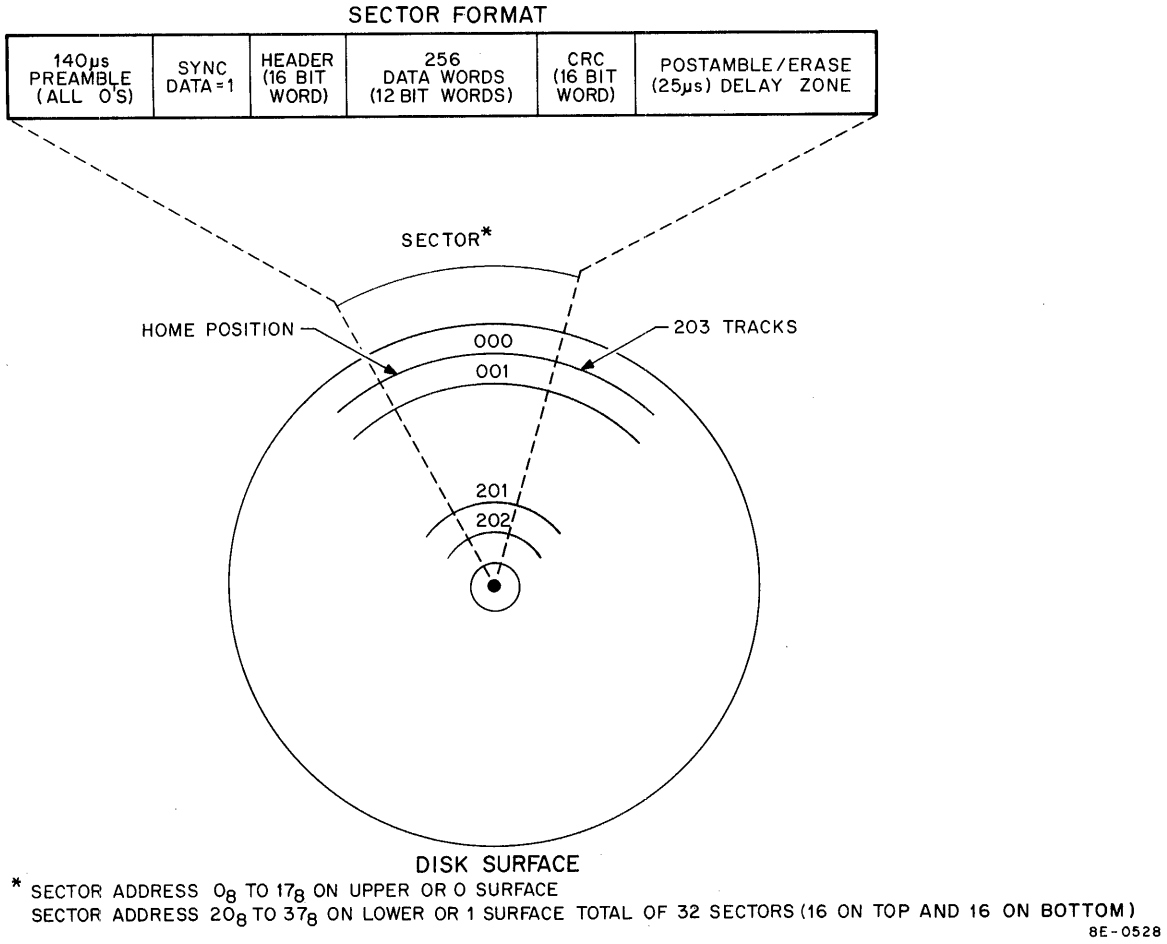


Figure 11-3 Disk Format

11.3.3.2 CRC Character – Data is recorded on the RK05 in blocks of 256 12-bit words (serial data); thus, each block contains 3072 bits of data recorded in a single string, with no separations to indicate word boundaries or record error checking bits.

A long string of data bits is susceptible to single bit errors caused by dropins, dropouts, or burst errors. Burst errors are caused by unwanted physical motion of the read/write heads. The RK8-E generates a Cyclic Redundancy Check (CRC) character to check for these errors. The CRC is a block check character that is calculated by the RK8-E during a read or write operation. The CRC character calculated during a write operation is written immediately following the data (Figure 11-3) and becomes part of the data string. The process used to calculate the block check word is such that if no errors occur, the CRC word calculated while reading data is identical to that calculated during a write operation.

To calculate a CRC word, the data block is treated as a number 3072 bits long which is divided by a polynominal ($X^{16} + X^{15} + X^2 + 1$). The hardware required to do this is a shift register with Exclusive OR gating (division being shift and subtract).

A maintenance instruction allows the program to read the CRC character written on the disk or the CRC character read from the disk.

11.3.3.3 Formatting A Cartridge – A disk cartridge is "formatted" when the cylinder address of a sector is written in the HEADER word of each sector. A special bit in the Command Register allows the program to write HEADER words in each sector (format). The program need only set the bit and write something in each sector. The RK8-E control writes the cylinder address automatically in the HEADER area (Figure 11-3) of each sector. The formatting program writes coded information in the data region of each sector and reads it back to verify that the disk is formatted correctly.

During a normal read or write operation, the disk seeks a cylinder specified by the RK8-E and reads the HEADER word of the first sector it finds after the seek is complete. This HEADER word is compared with the cylinder address specified by the RK8-E to ensure the correct cylinder has been found. The control then waits until the sector containing the address specified by the program passes under the read/write heads before reading or writing data.

11.3.3.4 Write Protect – WRITE PROTECT is turned on at the RK05 Disk Drive or by a bit in the Command Register when it is loaded by the program. WRITE PROTECT must be turned off by pressing a manual control (WT PROT) on each disk drive. If the program attempts to write on a disk that is write protected, the write operation is inhibited and an error condition is produced. WRITE PROTECT may be turned on manually at the RK05 by pressing the WT PROT switch.

11.4 MAJOR REGISTERS

The major registers of the RK8-E are in two broad categories: those that are loaded or read by user software and those that are transparent to user software. The first category includes the Command Register, Current Address Register, Disk Address Register and Status Register. The second category includes the 4-word Data Buffer Register, the CRC Register, Major State Register, Modulo 12- and Modulo 16-bit counters, and the Modulo 128- or 256-Word Count Register.

The major registers must be loaded from the AC by IOT instructions in the correct sequence before they perform any control function. The individual flip-flops in the registers are set by a 1 (true) and cleared by a 0 (false) bit from the AC. Refer to Section 3 for a list of IOT instructions and a detailed discussion of the contents of each major register.

11.4.1 Command Register

The Command Register (Figure 11-4) is loaded from the AC by IOT 6746. This IOT also clears the AC and the Status Register.

11.4.2 Current Address Register

The Current Address Register is a 12-bit register loaded from the AC with IOT 6744, which also clears the AC. This register and 3 bits of the Command Register (Figure 11-4) are combined to make up a 15-bit Memory Address Register. The contents of the CA Register and the 3 bits in the Command Register are applied to the OMNIBUS to select a memory location during a data transfer. The CA Register is incremented before each data transfer to select the next sequential memory location. The EMA bits in the Command Register are not incremented, and these bits must be changed by the program to select new memory fields. If the CA Register is incremented past the last memory location in a field, it will wrap around in the same field. The data is stored in location 000 and starts incrementing through the field again.

11.4.3 Disk Address Register

The Disk Address Register is loaded from the AC by IOT 6743, which also clears the AC and enables the contents of the Command Register to be applied to the control logic.

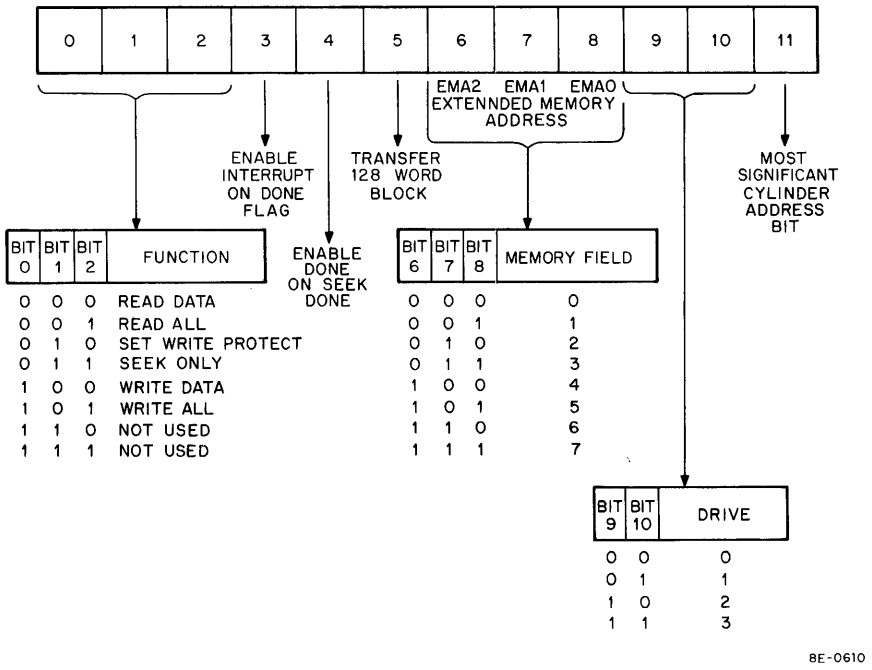


Figure 11-4 Contents of Command Register

The Disk Address Register selects a sector to be used in a data transfer. To select an individual sector, the following must be selected (Figure 11-5).

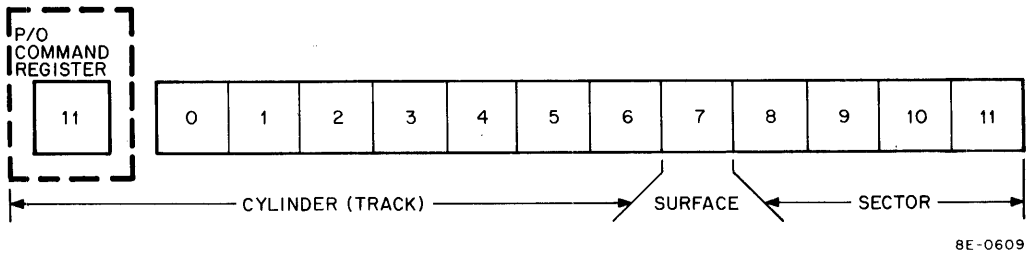


Figure 11-5 Disk Address Register

a. 1 of 203 cylinders

b. 1 of 2 surfaces

c. 1 of 16 sectors

The Disk Address Register and bit 11 in the Command Register (Figure 11-4) are combined to select a cylinder, surface, and sector. The largest valid address is 14537_8 (cylinder address 202_{10}).

11.4.4 Status Register

The Status Register (Figure 11-6) contains all the information needed for the program to evaluate the operation of the RK8-E and RK05.

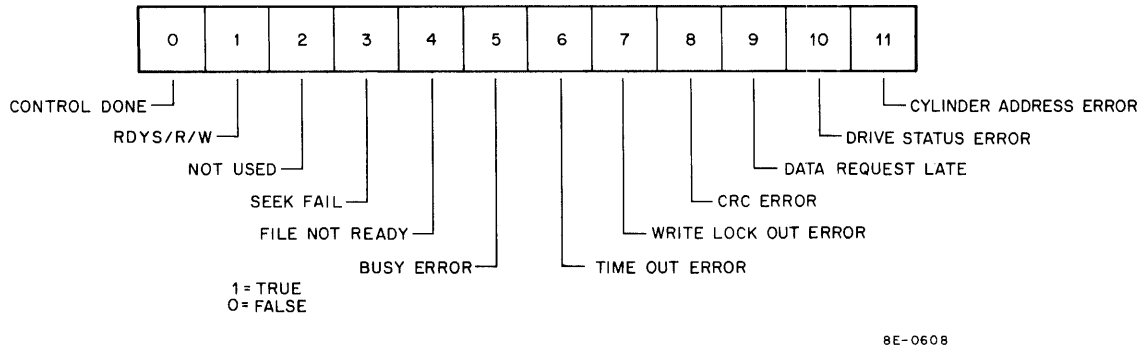


Figure 11-6 Contents of Status Register

11.4.5 Data Buffer Register

All data transfers between memory and a drive pass through the 4-word Data Buffer Register (DB1 through DB4). This 4-word register increases the latency of the RK8-E control from 6.2 μs with a single serial register and one data buffer to 22.5 μs with 4 Data Buffer Registers. Latency is defined as the maximum time the RK8-E control waits for access to the computer memory before data is lost. The numbers given above are for a memory cycle time of 1.2 μs.

During a read operation, Data Buffer 1 accepts the serial data from the drive and transfers a complete word to the last unused buffer, which is eventually removed from Data Buffer 4 and transferred to computer memory. On a write, data from computer memory enters Data Buffer 1 in parallel mode, transfers to the last unused buffer, and is shifted out to the drive as a 12-bit serial word from Data Buffer 4.

During maintenance operations, the contents of the CRC Register, Command Register, and the Surface/Sector Register (disk address) are shifted into Data Buffer 4 by the maintenance IOT for transfer to the AC or memory.

11.4.6 CRC Register

The CRC Register is a 16-bit register used to calculate the CRC character that is written onto the disk after the last data word. During a read, it calculates the CRC of the read data and does a bit-by-bit comparison with the CRC word read from the disk. It also contains the cylinder address loaded from the AC by the Load Address and GO instructions. The CRC Register does a bit-by-bit comparison of the HEADER word to confirm that the selected drive has found the correct cylinder address.

NOTE

The CRC Register and the Disk Address Register are physically the same logic with multipurposes.

11.4.7 Major State Register

The Major State Register (Table 11-2 and Figure 11-7) is the control sequencer of the RK8-E; with its associated gating, this register performs the major portion of the control functions of the RK8-E. The Major State Register is incremented from one state to another, and its decoded outputs gate signals to or from the disk and perform housekeeping tasks such as determining whether the control is in the HEADER region, data region or CRC region of the disk format.

Table 11-2

Major States

Major State	Function	Operation				
		Seek	Seek Check Read	Seek Check Write	Seek Read	Seek Write
IDLE	Control is not busy until the GO Command (DLAG) is issued and the contents of the AC are loaded into the CRC. The CRC Register contains the Cylinder/Surface Address (Disk Address)	X	X	X	X	X
STROBE	Strobe the Cylinder Address from the CRC Register to the Disk Drive and wait for the Disk Drive ADDRESS ACKNOWLEDGE signal.	X	X	X	X	X
DRIVE SEEKING	Wait for DISK READY to SEEK, READ, or WRITE from the Disk Drive to indicate the heads are positioned over the Cylinder Address.		X	X	X	X
HEADER A	Wait for the first Sector Mark, then start READ DELAY.		X	X		
HEADER B	At the end of READ DELAY turn the READ flip-flop on. Zeros are read until the SYNC bit is read at the beginning of a block of data.		X	X		
HEADER C	Read the 16-bit HEADER word and compare it with the cylinder address in the CRC Register.		X	X		
SECTOR SEEK	If the HEADER word does not equal the cylinder address set CYLINDER ADDRESS ERROR and go to IDLE state. At each sector mark compare the sector address with the Disk Sector Address lines If the addresses are equal go to the next state. If this is a write operation transfer data from the processor to the Data Buffer Register.		X	X	X	X

Table 11-2 (Cont)

Major States

Major State	Function	Operation				
		Seek	Seek Check Read	Seek Check Write	Seek Read	Seek Write
HEADER D (Read)	At the beginning of the sector start READ DELAY (85 μs). At the end of READ DELAY set the READ flip-flop. Note zeros are read until the SYNC bit is read.		X		X	
HEADER D (Write)	At the beginning of the sector start SYNC DELAY. Zeros are written during SYNC DELAY time and after SYNC DELAY times OUT (140 μs) a one SYNC bit is written.			X		X
HEADER E (Read)	Count and ignore the first 16 bits.		X		X	
HEADER E (Write)	Write the HEADER word contained in the CRC Register.			X		X
DATA STATE (Read)	Read 256 12-bit data words and a 16-bit CRC character from the Disk and compute a CRC. The 12 bit data words are transferred to the Data Buffer Register and the controller tries to keep the Data Buffer Register empty by transferring data to the processor via the single cycle data break.		X		X	
DATA STATE (Write)	Write 256 data words on the Disk Drive. The Data words are transferred.from the processor via the Single Cycle Data Break.			X		X
CRC STATE (Read)	Read the CRC from the Disk Drive and compare it with the CRC computed by the controller.		X		X	
CRC STATE (Write)	Write the computed CRC on the disk after 256 data words have been written.			X		X

Table 11-2 (Cont)

Major States

Major State	Function	Operation				
		Seek	Seek Check Read	Seek Check Write	Seek Read	Seek Write
END STATE (Read)	If the CRC character read from the Disk Drive does not equal the computed CRC, set the CRC ERROR flag and clear Read. When the Data Buffer Registers are transferred into processor memory, set the DONE flag and go to the IDLE state.		X		X	
END STATE (Write)	Start ERASE DELAY and Write zeros. At the end of ERASE DELAY (25 μs) clear WRITE, set the DONE flag and go to the IDLE state.			X		X

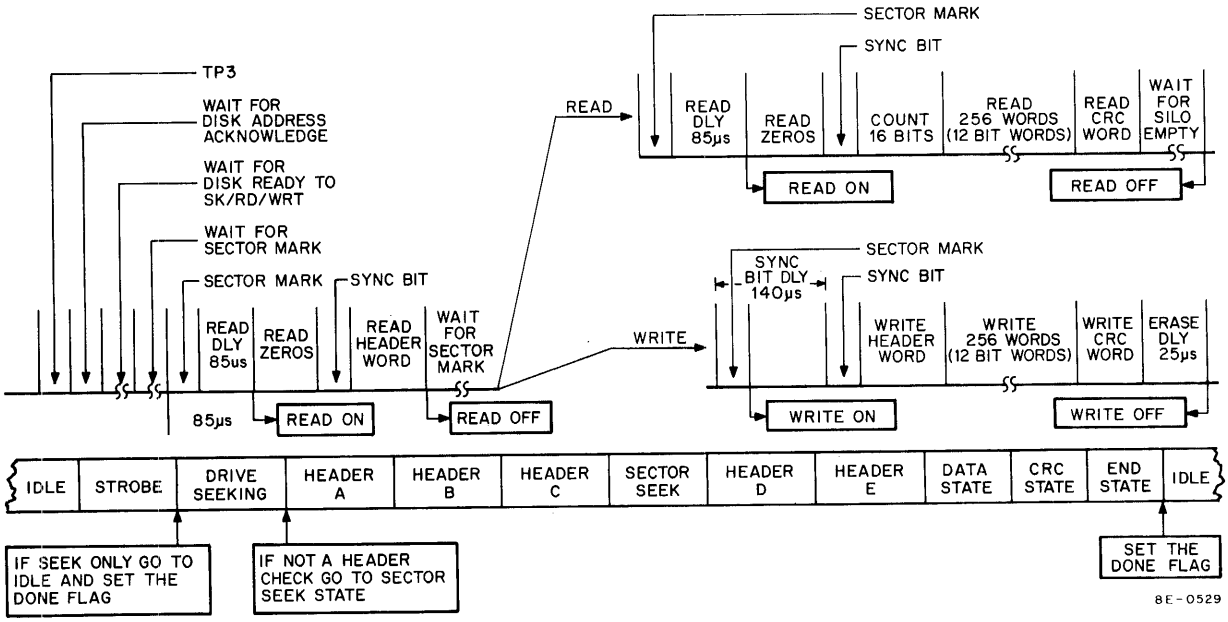


Figure 11-7 Read and Write Flow Diagram

11.4.8 Bit Counters

The Modulo 12-bit counter determines PDP-8/E data word boundaries. The Modulo 16-bit counter determines where the HEADER and CRC character are, so that the control knows when to check the HEADER and CRC characters.

11.4.9 128- or 256-Word Counter

This register counts the output of the 12-bit counter to determine when the correct number of data words (normally 256 words) have been transferred to or from the disk. When the half block bit is set in the Command Register, the 128th word stops the data transfer instead of the usual 256th word.

11.5 COMPANION DOCUMENTS

The following is a list of companion documents needed to operate and maintain the RK8-E.

a. PDP-8/E, PDP-8/F, and PDP-8/M Small Computer Handbook – DEC 1973.

b. PDP-8/E Maintenance Manual, Volumes I and II.

c. Introduction to Programming – DEC 1973 Volumes I and II.

d. DEC Engineering Drawings, M7104-0-1, M7105-0-1, and M7106-0-1.

e. RK05 Disk Drive Maintenance Manual (DEC-00-RK05-DA).

11.5.1 Software

The following programs and associated documents are used in the maintenance of the RK8-E.

a. RK8-E Diskless Control Diagnostic, MAINDEC-08-DHRKA-A-PB or D

b. RK8-E Drive Control Diagnostic, MAINDEC-08-DHRKB-A-PB or D

c. RK8-E Disk Formatter, MAINDEC-08-DHRKD-A-PB or D

d. RK8-E Data Reliability Test, MAINDEC-08-DHRKC-A-PB or D

NOTE

The MAINDEC number is followed by PB for papertape and D for Document, i.e., MAINDEC-08-DHRKA-A-PB for binary tape and MAINDEC-08-DHRKA-A-D for the diagnostic document. The latest revision of these documents and programs should be used to run RK8-E diagnostics.

SECTION 2 SITE PREPARATION, INSTALLATION, AND ACCEPTANCE TEST

The RK8-E is installed on site by DEC Field Service personnel. The customer should not attempt to unpack, inspect, install, checkout, or service the equipment.

11.6 SITE PREPARATION

Adequate site planning and preparation simplifies the installation process and results in a more efficient and more reliable RK8-E installation. DEC Sales Engineers or Field Service Engineers are available for counseling and consultation with the user regarding the installation.

Site planning should include a list of the actual components to be used in the installation. This list should include such items as storage cabinets, Teletype supplies, work tables, etc.

Primary requirements for installation of the RK8-E are:

a. A Teletype, Programmer's Console, and at least 4K of read/write memory must be available to run the RK8-E diagnostics.

b. Adequate space and power must be supplied for the RK05 Disk Drives (refer to Chapter 10 of the *RK05 Disk Drive Maintenance Manual* for power and space requirements).

NOTE
The RK8-E receives +5V, 3A of power from the OMNIBUS.

c. RK8-E diagnostics and documents must be available to checkout the RK8-E and RK05 (Paragraph 11.5).

d. Software to format RK05 disk cartridges must be available (Paragraph 11.5).

11.7 INSTALLATION

Perform the following steps to install the RK8-E:

Step	Procedure
1	Unpack and inspect RK05, using the *RK05 Disk Drive Maintenance Manual,* Volume 2, Paragraph 2.1, RK05 Field Installation and Acceptance Procedure.
2	Using the inventory list shipped with the equipment, verify all items have been received.
3	Ensure that PDP-8/E power is turned off.
4	Ensure correct jumpers are installed to select the device code assigned to this RK8-E. The M7104 is normally shipped with the 674X device code selected, but 675X through 677X device codes may be used (Table 11-3).
5	Install jumpers to select priority assigned to this RK8-E (Table 11-4).
6	Connect the 7009026 cable to the Berg connector on the M7106 module.
7	Insert the RK8-E modules into the OMNIBUS (Figure 11-8). Refer to Table 11-5 in Volume I of the *PDP-8/E Maintenance Manual* for module installation priority.
8	Install H851 Top Connectors between the modules (Figure 11-8).

11.8 ACCEPTANCE TEST

The following diagnostics must be run in the order shown and the specified number of passes to check the RK8-E. (Refer to the diagnostic document for instructions to run the diagnostic).

a. RK8-E Diskless Control Diagnostic, MAINDEC-08-DHRKA-A-PB (2 passes)

b. RK8-E Drive Control Diagnostic, MAINDEC-08-DHRKB-A-PB (1 pass)

c. RK8-E Formatter, MAINDEC-08-DHRKD-A-PB (1 pass)

d. RK8-E Data Reliability Test, MAINDEC-08-DHRKC-A-PB (1 pass)

Table 11-3

Device Select Jumper Installation

Octal Code	Install following Jumpers on M7104 Module
674X	W2
	W4
	W6
675X	W2
	W4
	W3
676X	W2
	W1
	W6
677X	W2
	W1
	W3

Table 11-4

RK8-E Priority Selection

Priority	Install Jumpers
Priority 0 (highest)	W2
	W3
	W5
Priority 1	W1
	W4

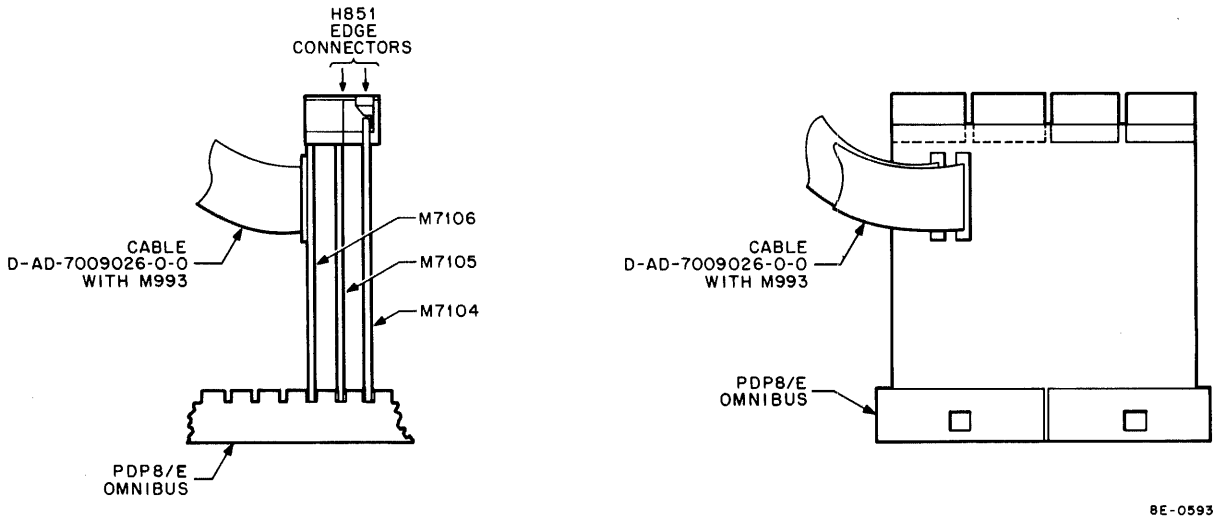


Figure 11-8 RK8-E Module Installation

11.9 RK8-E INTERFACE

One 7009026 cable is used to connect the RK8-E controller to the first RK05 Disk Drive (four maximum). Note that the RK8-E is connected to only one drive and the input to and output from the RK05 are daisy-chained to the other three disks (the connectors on all four disk drives are connected in parallel by BC11A cables). The 7009026 cable is connected from two Berg connectors on the M7106 module to slot A07, A08, B07, or B08 on RK05 Disk Drive located closest to the RK8-E (Tables 11-5 and 11-6). The RK8-E modules on the OMNIBUS are tied together by H851 Top Connectors. The signals of the pins of the top connectors are shown in Tables 11-7 through 11-10. These tables give the origin of signals on the top connectors for troubleshooting and signal monitoring.

An M930 Terminator Card must be installed in the unused interface slot of the last RK05 Disk Drive.

Table 11-5
RK8-E–RK05 Interface Cable (P2)

Connector J2 on RK8-E Pin No.	Signal	Description
A	GND	
B		
C	DSK CAP EX L	The address sent to the selected disk drive was greater than 312_8. (low=true)
E	DSK SEEK FAIL	Disk failed to seek the address specified
F	GND	
H	DSK ACKNOWLEDGE L	Disk has received and acknowledged the disk address
J	GND	
K	DSK SEC 2 L	Disk sector address bit 1 (low=1)
L	GND	
M	DSK DRIVE 3 L	Select disk drive 3 (low=true)
N	GND	
P	DSK RESTORE L	Recalibrate the selected disk drive (low=true)
R	GND	
S	DSK DRIVE 2 L	Select disk drive 2 (low=true)
T	GND	
U	DSK CYL ADD 4 L	Disk cylinder address bit 2 (low=1)
V	GND	

Table 11-5 (Cont)
RK8-E—RK05 Interface Cable (P2)

Connector J2 on RK8-E Pin No.	Signal	Description
W	DSK DRIVE 1 L	Select disk drive 1 (low=true)
X	GND	
Y	DSK CYL ADD 1 L	Disk cylinder address bit 0 (low=1)
Z	GND	
AA	DSK DRIVE 0 L	Select disk drive 0 (low=true)
BB	GND	
CC	DSK CYL ADD 32 L	Disk cylinder address bit 5 (low=1)
DD	GND	
EE	DSK RDY S/R/W L	Selected disk drive ready to read, write, or seek
FF	GND	
HH	DSK CYL ADD 128 L	Disk cylinder address bit 7 (low=1)
JJ	GND	
KK	DSK WRT CLK DATA L	Disk write clock data (low=true)
LL	GND	
MM	DSK CYL ADD 16 L	Disk cylinder address bit 4 (low=1)
NN	GND	
PP	DSK CYL ADD 64 L	Disk cylinder address 6 (low=1)
RR	GND	
SS	DSK CYL ADD 2 L	Disk cylinder address bit 1 (low=1)
TT	GND	
UU	DSK CYL ADD 8 L	Disk cylinder address bit 3 (low=1)
VV	GND	

Table 11-6
RK8-E—RK05 Interface Cable (P1)

Connector J1 on RK8-E Pin No.	Signal	Description
A	Not used	
B	Not used	
C	GND	
D	DSK DATA IN L	Serial Data from the disk drive
E	GND	
F	DSK RD CLK L	Clock pulses from the selected disk drive during a read operation
H	GND	
J	DSK WRT PROTECT L	Disk write protect (low=true). The selected disk drive does not write if this signal is true
K	GND	
L	DSK READ L	Disk read (low=true) causes the selected disk drive to read
M	GND	
N	Not used	
P	GND	
R	DSK WRT STATUS L	Disk Write Status L (low=true, Disk OK)
S	GND	
T	DSK SECTOR MK L	Disk sector mark (low=true) from the selected disk drive
U	GND	
V	DISK FILE RDY L	The selected disk drive is ready to read or write data (low=true)
W	GND	
X	DSK HEAD SEL 1	Disk head select bit; when this bit is a 1, the lower or 1 surface of the disk cartridge is selected

Table 11-6 (Cont)
RK8-E–RK05 Interface Cable (P1)

Connector J1 on RK8-E Pin No.	Signal	Description
Y	GND	
Z	DSK INDEX MK L	Disk index mark (low=true) from the selected disk drive
AA	GND	
BB	DSK WRT ERASE GATE L	Disk write erase gate (low=true)
CC	GND	
DD	DSK SEC 1 L	Disk sector address bit 0 (low=1) from the selected disk drive
EE	GND	
FF	DSK SEC 4 L	Disk address bit 2 (low=1) from the selected disk drive
HH	GND	
JJ	Not used	
KK	GND	
LL	DSK SEC 8 L	Disk sector address bit 3 (low=1) from the selected disk drive
MM	GND	
NN	Not used	
PP	GND	
RR	DSK STROBE L	Disk strobe enables the disk to receive disk address
SS	GND	
TT	Not used	
UU	GND	
VV	Not used	

Table 11-7
M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
12TH BIT OK H	HM1	M7106	Output of the divide by 12 counter each time 12 bits are read or written
6RK3 OK H	HS1	M7104	6RK3 (DLAG) load disk address and go if RK8-E is in the IDLE state
6RK3 OK L	HS2	M7104	Same as 6RK3 H except low is true
6RK4 L	JS2	M7104	6RK4 (DLCA) load Current Address Register
6RK6 H	HR1	M7104	6RK6 (DLDC) load Command Register
6RK7 H	JC1	M7104	6RK7 (DMAN) maintenance instruction
6RK7 OK H	HN2	M7104	6RK7 (DMAN) OK asserted only at TP3 time
WRT BRK L	HH1	M7105	Write break request (use DB1 for data transfer)
READ BRK L	HL2	M7105	Read break request (use DB4 for data transfer)
B DATA 10 H	JA2	M7104	Buffered data bus bit 10 (high=true) (1)
B DATA 10 L	JP2	M7104	Buffered data bus bit 10 (low=true) (1)
B DATA 11 H	JR1	M7104	Buffered data bus bit 11 (low=true) (1)
B DATA 11 L	JH1	M7104	Buffered data bus bit 11 (low=true) (1)
BRK DIR (0) H	HP2	M7105	Controls state of MD DIR L on the OMNIBUS
BTP3 OK H	HK1	M7104	Asserted at TP3 time if the RK8-E is in the IDLE state for timing
CLR DRV CMD L	JC2	M7104	Clear commands to the selected disk drive (see DCLR instruction and Table 11-11)
CLR ALL H	HD1	M7104	Clear all logic (see DCLR instruction and Table 11-11)
CLR ALL L	JU2	M7104	Same as CLR ALL H except low=true
DRV REVO H	JD2	RK05	Disk has read an index mark
DSK CAPACITY EX L	JK1	RK05	Disk capacity exceeded, a cylinder address greater than 312_8 was sent to the disk drive
DSK FILE RDY L	HE1	RK05	Selected disk drive is ready

Table 11-7 (Cont)
M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
DSK WRT STATUS	JD2	RK05	Selected disk drive is in a write status
SET IDLE PL L	JJ1	M7104	Set the IDLE state flip-flop
ENAB INT H	JB1	M7105	Enable the interrupt logic (see Table 3-2)
ENAB SEEK DONE H	JS1	M7105	Enable seek done if bit 3 in the Command Register is set
END STATE (0) H	JJ2	M7106	The RK8-E is in the END state
ERROR CLR L	JD1	M7104	Clear the ERROR flip-flop
HI RD CLK H	JM1	M7105	Maintenance clock or clock from the disk during a read
HI DATA IN H	JR2	M7105	Maintenance data or data from the disk during a read
IDLE (0) H	JN1	M7106	RK8-E is not in IDLE state when this signal is 0 (high)
IDLE (1) H	JL2	M7106	RK8-E is in IDLE state when this signal is 1 (high)
LAST WORD PL H	JN2	M7106	Output of the word counter each time 256 words are read or written
LD CMD REG H	JP1	M7105	Load Command Register asserted by 6RK6 (DLDC at TP3 time)
LO MAIN DATA H	HV2	M7105	Load main data
LO MAIN SHFT L	HP1	M7105	Shift main data
MAIN (0) H	JE1	M7105	Clear side of MAIN enable flip-flop. This signal is true when the MAIN flip-flop is cleared (normal operations)
MAIN (1) H	HA2	M7105	Set side of MAIN flip-flop. This signal is true when the MAIN flip-flop is set to enable maintenance operations
B DATA 01 H	HT2	M7104	Buffered data bus bit 1
NOT EQUAL (0) H	JF2	M7105	The cylinder address sent to the disk and the cylinder address read after seek is complete are not equal

Table 11-7 (Cont)
M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
RDY S/R/W L	HU1	RK05	Selected disk drive ready to seek, read, or write
B TP2 H	HC2	M7104	Buffered time pulse 2
SECTOR SEEK (0) H	JF1	M7106	RK8-E is in sector seek state if sector seek (0) is true high
SEEK FAIL H	HU2	RK05	Selected disk drive failed to seek
MAIN PL H	HT1	M7105	See maintenance instruction and Table 11-14
DATA ENABLE (1) H	HN1	M7105	Enable gate to apply MA and EMA bits to the OMNIBUS
DATA STATE (0) H	JM2	M7106	The RK8-E is not in data state when this signal is high (0)
B DATA STATE (1) H	HL1	M7106	The RK8-E is in the data state when this signal is high (1)
DB CONT 1 (0) H	HV1	M7106	Data buffer 1 control
DB CONT 4 (1) H	HE2	M7104	Data buffer 4 control
DEVICE RK H	JA1	M7104	If device RK is high (true), the RK8-E is selected for this operation
B TP3 H	JT1	M7104	Buffered time pulse 3
DRIVE STATUS BAD H	JH2	RK05	Selected disk drive not operational (Table 11-12)
WRITE (1) H	HM2	M7106	WRITE function is (1) high when a write operation is selected
WRT CMD L	JE2	M7106	WRT command to the disk during a write operation
WT BUFF TO DATA L	HD2	M7104	Transfer DB4 to the data lines (used during maintenance operations to transfer contents of DB4 to the AC)
RK DATA 11 H	HF1	M7104	Disk data bit 11
LD DISK ADDRESS H	JB2	M7106	Load Disk Address Register when asserted by 6RK3
SHFT WRT BUFF L	HR2	M7106	Shift write buffer (DB4)
AC7 (0) H	HB1	M7104	Bit 7 from the AC

Table 11-7 (Cont)
M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
RDY S/R/W SLO H	JL1	RK05	Selected disk drive ready to seek, read, or write
BRK RQ H	HA1	M7105	Break request
B BRK RQ H	HB2	M7104	Buffered break request
MAK (0) H	HJ1	M7105	Data BRK RQST accepted (RK8-E has priority)
DATA CLK OK H	HC1	M7106	Data clock OK

Table 11-8
M7105 to M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
12TH BIT OK H	HM1	M7106	Output of divide by 12 counter each time 12 bits are read or written
6RK3 OK H	HS1	M7104	6RK3 (DLAG) load disk address and go if RK8-E is in the IDLE state
6RK3 OK L	HS2	M7104	Same as 6RK3 H except low=true
6RK4 L	JS2	M7104	6RK4 (DLCA) Load Current Address Register
6RK6 H	HR1	M7104	6RK6 (DLDC) load command address
6RK7 H	JC1	M7104	6RK7 (DMAN) maintenance
6RK7 OK H	HN2	M7104	Same as 6RK7 except it is enabled at TP3 time
WRT BRK L	HH1	M7105	Write break request (use DB1 for data transfer)
READ BRK L	HL2	M7105	Read break request (use DB4 for data transfer)
B DATA 10 H	JA2	M7104	Buffered data bus bit 10 (high=true)
B DATA 10 L	JP2	M7104	Buffered data bus bit 10 (low=true)
B DATA 11 H	JR1	M7104	Buffered data bus bit 11 (high=true)
B DATA 11 L	JH1	M7104	Buffered data bus bit 11 (low=true)
BRK DIR (0) H	HP2	M7105	Controls MD DIR L on the OMNIBUS
B TP3 OK H	HK1	M7104	Buffered time pulse 3
CLR DRIVE CMD L	JC2	M7104	Clear selected disk drive (DCLD)
CLR ALL H	HD1	M7104	Clear all logic (see DCLR instruction and Table 11-11)
CLR ALL L	JU2	M7105	Same as clear all H except low=true
ENABLE DATA (1) H	HN1	M7105	Enable gates to apply MA and EMA bits to the OMNIBUS
DATA STATE (0) H	JM2	M7106	The RK8-E is in the DATA state (data transfers are enabled)
B DATA STATE (1) H	HL1	M7106	Buffered DATA state

Table 11-8 (Cont)
M7105 to M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
DB CONT 1 (0) H	HV1	M7104	Data buffer 1 control
DB CONT 4 (1) H	HE2	M7104	Data buffer 4 control
DEVICE RK H	JA1	M7104	If device RK is high (true), the RK8-E is selected for this operation
B TP3 H	JT1	M7104	Buffered time pulse 3
DRIVE STATUS BAD H	JH2	M7105	The selected disk drive is not ready (Table 11-12 bit 10)
WRITE (1) H	HM2	M7106	The write function is selected
WRT CMD L	JE2	M7106	Write command to selected disk drive
WT BUFF TO DATA L	HD2	M7104	Transfer contents of write buffer (DB4) to the Data lines
RK DATA 11 H	HF1	M7104	Disk data bit 11 (serial data to disk)
LD DISK ADDRESS H	JB2	M7106	Load Disk Address Register when asserted by 6RK3
SHFT WRT BUFF L	HR2	M7106	Shift the Write Buffer out to the disk drive
AC7 (0) H	HB1	M7104	Bit 7 from the AC
RDY S/R/W H	JL1	M7105	Selected disk drive ready to seek, read, or write
BRK RQ H	HA1	M7105	Break request
B BRK RQ H	HB2	M7105	Buffered break request
MAK (0) H	HJ1	M7105	Data BRK RQST has been accepted (RK8-E has highest priority)
DATA CLK OK H	HC1	M7106	DATA clock OK
DRV REVO H	JK2	M7106	Disk index mark is applied to RK8-E during IDLE state
DSK CAPACITY EX L	JK1	RK05	Disk capacity exceeded, address greater than 312_8 sent to the disk drive
DSK FILE RDY L	HE1	RK05	Selected disk drive is ready (on-line)
DSK WRT STATUS L	JD2	RK05	Disk drive write status (low=true)

Table 11-8 (Cont)
M7105 to M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
SET IDLE PL L	JJ1	M7104	Set IDLE state flip-flop
ENAB INT H	JB1	M7105	Enable interrupt logic (Table 11-12)
ENAB SEEK DONE H	JS1	M7105	Enable seek done if bit 3 in Command Register is set
END STATE (0) H	JJ2	M7106	RK8-E in the END state when asserted
ERROR CLR L	JD1	M7104	Clear the ERROR flip-flop
HI RD CLK H	JM1	M7105	Main clock OR clock from the disk during a read
HI DATA IN H	JR2	M7105	Serial DATA from the disk drive during a read
IDLE (0) H	JN1	M7106	RK8-E is not in the IDLE state when this signal is high
IDLE (1) H	JL2	M7106	RK8-E is in the IDLE state when this signal is 1 (high)
LAST WORD PL H	JN2	M7106	Output of word counter each time 256 words are read or written
LD CMD REG H	JP1	M7106	Load Command Register (DLDC)
LO MAIN DATA H	HV2	M7105	Maintenance data (Table 11-14)
LO MAIN SHFT L	HP1	M7105	Maintenance shift pulse (Table 11-14)
MAIN (0) H	JE1	M7105	Maintenance command (DMAN instruction)
MAIN (1) H	HA2	M7105	Maintenance command (DMAN instruction)
B DATA 01 H	HT2	M7104	Buffered data bit 2
NOT EQUAL (0) H	JF2	M7105	The cylinder address sent to the disk and the cylinder address read after seek is complete are not equal
RDY S/R/W L	HU1	RK05	Selected disk drive ready to seek, read, or write
B TP2 H	HC2	M7104	Buffered time pulse 2
SECTOR SEEK (0) H	JF1	M7106	RK8-E is in sector seek state if sector seek (0) is true high
SEEK FAIL H	HU2	RK05	Selected disk drive failed to seek
MAIN PL H	HT1	M7105	See maintenance instruction and Table 11-14

Table 11-9
M7105 to M7106 Top Connector Signal List

Signal	Pin No.	Origin	Description
12TH BIT OK H	FA1	M7106	Output of divide by 12 counter each time 12 bits are read or written
6RK3 OK H	FA2	M7104	6RK3 (DLAG) load disk address and go if RK8-E is in IDLE state
B DATA 7 H	ER2	M7104	Buffered data bit 7 (high=true) (1)
B DATA 10 H	EK1	M7104	Buffered data bit 10 (high=true) (1)
B DATA 11 H	EJ1	M7104	Buffered data bit 11 (high=true) (1)
CLR DRIVE CMD L	FB2	M7104	Clear commands to the selected drive
CLR ALL L	EH1	M7104	Clear all logic (see the DCLR instruction and Table 11-11)
DATA STATE (0) H	FP1	M7106	Data state (read or write data)
B TP3 H	FJ1	M7104	Buffered time pulse 3
DRV REVO H	FC2	M7106	Disk index mark is applied to the RK8-E during IDLE state
DSK FILE RDY L	FB1	RK05	Selected disk drive is operational
DSK WRT STATUS L	FD2	RK05	Selected disk drive is in a write status (low=true)
SET IDLE PL L	FK1	M7104	Set the IDLE state flip-flop
END STATE (0) H	FD1	M7106	END state (true=0)
ERROR CLR L	FE2	M7104	Clear the ERROR flip-flop
IDLE (0) H	FR2	M7106	The RK8-E is not in the IDLE state when this signal is (0) high
IDLE (1) H	EC1	M7106	The RK8-E is in the IDLE state when this signal is (1) high
LAST WORD PL H	FE1	M7106	LAST WORD is asserted when 256 words are read or written
MAIN (0) H	FP2	M7105	Clear side of MAIN flip-flop. This signal is true when the RK8-E is not in the maintenance mode
RDY S/R/W H	ED1	M7105	Selected disk drive is ready to seek, read, or write

Table 11-9 (Cont)
M7105 to M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
DATA ENABLE (1) H	EU1	M7105	Enable gates to apply MA and EMA bits to the OMNIBUS
SECTOR SEEK (0) H	FF2	M7106	The RK8-E is in the sector seek state if SECTOR SEEK is true (high)
LAST BRK (1) H	FN2	M7105	Last break (1=true) ends data transfer operations
WRITE (1) H	FF1	M7106	The write function is selected by the program
WRT CMD L	FV2	M7106	Write command to the RK05
B TP2 H	FH2	M7104	Buffered time pulse 2
B DATA 8 H	EM1	M7104	Buffered data bus bit 8
B DATA 9 H	EL1	M7104	Buffered data bus bit 9
BRK ENABLE CLK H	FK2	M7106	Break enable clock pulse
BRK IN CLK H	FU2	M7106	Break in clock pulse
CLR CNTRS L	FS1	M7106	Clear counters asserted by CLR ALL, DATA CLR, or HEADER E during STATE ENABLE
CLR SECTOR AD L	EF1	M7105	Clear Sector Address Register
CRC 16 (1) H	EN2	M7105	CRC Register bit 16
CRC DATA H	EA1	M7106	Serial CRC data
DATA IN (0) H	FR1	M7106	Serial data from the disk during a read
RD CLK (1) H	EB1	M7105	Read clock from the disk during a read
RD SHFT DB L	FS2	M7106	Shift Data Buffer during read operations
SECTOR ADDR 01 H	EP2	M7105	Sector address bit 0 high
SHFT SURF SEC H	FU1	M7105	Shift Surface Sector Register
ENAB DATA L	EV1	M7105	Enable data to the buffers
SHFT CRC L	FN1	M7106	Shift CRC out to the disk drive
FILE RDY H	EE1	RK05	Selected disk drive is READY

Table 11-9 (Cont)
M7105 to M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
STROBE (1) H	EF2	M7106	Asserted when file is ready and GO bit is set (1)
FUNCTION 00 H	EU2	M7106	Function bit 00)) Select disk drive
FUNCTION 01 H	EV2	M7106	Function bit 01) operation, i.e., read)
FUNCTION 02 H	ET2	M7106	Function bit 02)
HALF BLOCK H	ES2	M7105	Transfer 128 words instead of 256
DATA CLK OK H	FM1	M7106	Data clock OK
LO MAIN SHFT L	FL1	M7106	Maintenance shift
DSK DRIVE 2 L	EP1	M7105	Select disk drive 2 when low (true)
DSK DRIVE 3 L	EN1	M7105	Select disk drive 3 (low=true)
DSK CYL AD 128 L	EE2	M7106	Disk cylinder address bit 7 (MSB)
DSK CYL AD 64 L	EB2	M7106	Disk cylinder address bit 6
DSK CYL AD 32 L	EJ2	M7106	Disk cylinder address bit 5
DSK CYL AD 16 L	EC2	M7106	Disk cylinder address bit 4
DSK CYL AD 8 L	ET1	M7106	Disk cylinder address bit 3
DSK CYL AD 4 L	EH2	M7106	Disk cylinder address bit 2
DSK CYL AD 2 L	EK2	M7106	Disk cylinder address bit 1
DSK CYL AD 1 L	ES1	M7106	Disk cylinder address bit 0 (LSB)
DSK CAPACITY EX L	FC1	RK05	Disk capacity exceeded, address sent to the disk greater than 312_8
HI MAIN SHIFT L	FT2	M7106	Maintenance shift pulse
B LAST BRK H	FL2	M7106	Buffered last break
LD DSK ADDRS H	EM2	M7106	Load Disk Address Register when asserted by 6RK3
RK DATA 11 H	FH1	M7105	Disk data bit 11
B TP3 OK H	FM2	M7104	Asserted during TP3 time of the IDLE state only for timing and execution of instructions

Table 11-9 (Cont)
M7105 to M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
SHFT WRT BUFF L	FJ2	M7104	Shift write buffer (DB4)
STATE ENABLE B H	FV1	M7106	Buffered STATE ENABLE
DSK RDY S/R/W L	EL2	RK05	Selected disk drive ready to seek, read, or write
DSK SEEK FAIL L	EA2	RK05	The seek operation on the selected disk drive failed
DSK DRIVE 0 L	ED2	M7105	Select disk drive 0 when low (true)
DSK DRIVE 1 L	ER1	M7105	Select disk drive 1 when low (true)

Table 11-10
M7106 Top Connector Signal List

Signal	Pin No.	Origin	Description
12TH BIT OK H	FA1	M7106	Output of divide by 12 counter each time 12 bits are read or written
6RK3 OK H	FA2	M7104	6RK3 (DLAG) load disk address and go
B DATA 7 H	ER2	M7104	Buffered data bus bit 7 (high=true)
B DATA 10 H	EK1	M7104	Buffered data bus bit 10 (high=true)
B DATA 11 H	EJ1	M7104	Buffered data bus bit 11 (high=true)
CLR DRIVE CMD L	FB2	M7104	Clear commands to the selected disk drive clear all logic (see the DCLR instruction and Table 11-11)
CLR ALL L	EH1	M7104	Clear all logic on the RK8-E
DATA STATE (0) H	FP1	M7106	Data state (read or write data)
B TP3 H	FJ1	M7104	Buffered time pulse 3
DRV REVO H	FC2	M7106	Disk INDEX MARK is applied to the RK8-E during the IDLE state
DSK FILE RDY L	FB1	RK05	Selected disk drive is operational
DSK WRT STATUS L	FD2	RK05	Selected disk drive is in a write status (low=true)
SET IDLE PL L	FK1	M7104	Set the IDLE state flip-flop
END STATE (0) H	FD1	M7106	The RK8-E is in the END state
ERROR CLR L	FE2	M7104	Clear the ERROR flip-flops
IDLE (0) H	FR2	M7106	RK8-E is not in the IDLE state when this signal is high
IDLE (1) H	EC1	M7106	RK8-E is in the IDLE state when this signal is high
LAST WORD PL H	FE1	M7106	Output of the word counter each time 256 words are read and written
MAIN (0) H	FP2	M7105	Clear side of MAIN flip-flop. The RK8-E is not in the maintenance mode when this signal is high
RDY S/R/W H	ED1	RK05	Selected disk drive ready to seek, read, or write
DATE ENABLE (1) H	EU1	M7105	Enables MA and EMA bits to be applied to the OMNIBUS during a data break

Table 11-10 (Cont)
M7106 Top Connector Signal List

Signal	Pin No.	Origin	Description
SECTOR SEEK (0) H	FF2	M7106	Sector seek state
LAST BRK (1)	FN2	M7105	Last break
WRITE (1) H	FF1	M7106	The Write function is selected
WRT CMD L	FV2	M7106	Write command
HI MAIN SHFT L	FT2	M7105	Maintenance shift (DMAN pulse)
B LAST BRK H	FL2	M7106	Buffered last break
LD DISK ADDRS H	EM2	M7106	Load disk address
RK DATA 11 H	FH1	M7104	Data bit 11 from the disk
B TP3 OK	FM2	M7104	Buffered time pulse 3 OK
SHFT WRT BUFF L	FJ2	M7104	Shift Write Buffer (DB4)
STATE ENAB B H	FV1	M7106	State enable
DSK RDY S/R/W L	EL2	RK05	Selected disk drive ready to seek, read, or write
DISK SEEK FAIL L	EA2	RK05	The selected disk did not complete a seek operation (Table 11-12)
DSK DRIVE 0 L	ED2	M7105	Select disk drive 0 when low (true)
DSK DRIVE 1 L	ER1	M7105	Select disk drive 1 when low (true)
DSK DRIVE 2 L	EP1	M7105	Select disk drive 2 when low (true)
DSK DRIVE 3 L	EN1	M7105	Select disk drive 3 when low (true)
DSK CYL AD 128 L	EE2	M7106	Disk cylinder address bit 7
DSK CYL AD 64 L	EB2	M7106	Disk cylinder address bit 6
DSK CYL AD 32 L	EJ2	M7106	Disk cylinder address bit 5
DSK CYL AD 16 L	EC2	M7106	Disk cylinder address bit 4
DSK CYL AD 8 L	ET1	M7106	Disk cylinder address bit 3
DSK CYL AD 4 L	EH2	M7106	Disk cylinder address bit 2

Table 11-10 (Cont)
M7106 Top Connector Signal List

Signal	Pin No.	Origin	Description
DSK CYL AD 2 L	EK2	M7106	Disk cylinder address bit 1
DSK CYL AD 1 L	ES1	M7106	Disk cylinder address bit 0
DSK CAPACITY EX L	FC1	RK05	Disk capacity exceeded, cylinder address greater than 312_8
DATA CLK OK H	FM1	M7106	Data clock OK during DATA state only
LO MAIN SHIFT L	FL1	M7105	Main shift (DMAN pulse)
B TP2 H	FH2	OMNIBUS	Buffered time pulse 2
B DATA 8 H	EM1	M7104	Buffered data bus bit 8
B DATA 9 H	EL1	M7104	Buffered data bus bit 9
BRK ENABLE CLK H	FK2	M7106	Break enable clock
BRK IN CLK H	FU2	M7106	BREAK IN clock
CLR CNTRS L	FS1	M7106	Clear counters asserted by CLR ALL, DATA CLR, or HEADER E during STATE ENABLE
CLR SECTOR AD L	EF1	M7105	Clear Sector Address Register
CRC 16 (1) H	EN2	M7105	CRC Register bit 16
CRC DATA H	EA1	M7106	Serial CRC DATA
DATA IN (0) H	FR1	M7106	DATA IN from the disk
RD CLK (1) H	EB1	M7105	Read clock from the disk
RD SHFT DB L	FS2	M7106	Shift Read Data Buffer (DL1)
SECTOR ADDR 01 H	EP2	M7105	Sector address bit 0
SHFT SURF SEC H	FU1	M7105	Shift Surface Sector Register
ENAB DATA L	EV1	M7105	Enable data to the buffers
SHFT CRC L	FN1	M7106	Shift CRC Register
FILE RDY H	EE1	RK05	Selected disk drive is READY

Table 11-10 (Cont)
M7106 Top Connector Signal List

Signal	Pin No.	Origin	Description
STROBE (1) H	EF2	M7106	Asserted when file is ready and GO bit is set (1)
FUNCTION 00 H	EU2	M7106	Function bit 00)) Select disk drive
FUNCTION 01 H	EV2	M7106	Function bit 01) operation, i.e., read
FUNCTION 02 H	ET2	M7106	Function bit 02))
HALF BLOCK H	FS2	M7106	Transfer 128 words instead of 256

11.10 SINGLE CYCLE DATA BREAK DESCRIPTION

All data transfers between the RK8-E and memory are via the single cycle data break interface. The concepts of data transfers and interrelationships of the data break interface and peripherals are explained in Chapter 10 of the *Small Computer Handbook 1973.* A detailed description of the data break interface (KD8-E) is explained in Chapter 10, Volume II of the *PDP-8/E Maintenance Manual.* The data break interface option operation is identical to the single cycle data break control logic used in the RK8-E.

11.11 INSTRUCTIONS AND STATUS BITS

The following are used to program the RK8-E.

Skip on Disk DONE or ERROR flag (DSKP)

Octal Code: 6741

Operation: Skip the next instruction if the TRANSFER DONE or ERROR flag is set.

Clear All (DCLR)

Octal Code: 6742

Operation: Transfer bits 10 and 11 from the AC to the clear logic in the RK8-E (see Table 11-11) and clear the AC.

Table 11-11
Clear Operations Using the DCLR Instruction

AC Bit 10	AC Bit 11	Operation
0	0	DCLS; clear tha AC and Status Register. This bit combination is normally used to clear program interrupts.
0	1	DCLC; clears the AC and all RK8-E control logic but does not clear the selected RK05 control logic. This bit combination is used only to simulate a power clear or if the controller does not respond to normal commands. Note this instruction stops the control even if it is rewriting a HEADER word; it should be used with care. The Status Register contains all zeroes after the DCLR instruction is executed with this bit combination in the AC.
1	0	DCLD; clears the AC and recalibrates the selected drive by forcing it to cylinder 000 (home position). This bit combination is used to recover from cylinder address errors and select errors.
1	1	Accomplishes same operation as 0 0.

CAUTION

The following programming sequence should be used to recalibrate the selected disk drive with a DCLR instruction.

a.	DCLR with AC 0000	Clears Status Register and AC
b.	STL	Set AC LINK bit to 1
c.	RTL	Rotate AC and LINK left two. One in the LINK goes to AC bit 10 position
d.	DCLR with AC 0010	The selected drive is recalibrated as explained in Table 11-11
e.	DSKP	The program skips an instruction when the TRANSFER DONE flag is set when the read/write heads are at the cylinder 000
f.	JMP-1	
g.	DCLR with AC 0000	Clears Status Register and the AC
h.	DSKP	Skip on TRANSFER DONE
i.	JMP-1	
j.		Recalibrate procedure is finished. Read/write heads are at cylinder 000 (home position) and the AC is cleared

Load Address and GO (DLAG)

Octal Code: 6743

Operation: Transfer the contents of the AC to the Disk Address Register, clear the AC, and enable the command in the Command Register to be executed. The Disk Address Register specifies one of 16 sectors, one of 2 surfaces, and one of 203 cylinders. The AC must be loaded with the disk address before this instruction is executed. In a normal read or write operation, the following occurs:

a. The selected drive seeks the track specified by AC bits 0 through 6 and bit 11 in the Command Register.

b. When the selected drive signals it has completed a SEEK, the HEADER word is checked on the first sector to pass under the read/write heads.

c. If the track specified checks with the HEADER word (read/write heads are on the right cylinder), the control waits for the next sector pulse.

d. The control reads the sector address of each sector passing under the read/write heads and when the correct sector is found a read or write operation is performed.

Load Current Address (DLCA)

Octal Code: 6744

Operation: Transfer the contents of the AC to the Current Address Register and clear the AC. The contents of the Current Address Register along with the EMA bits in the Command Register are applied to the OMNIBUS MA and EMA lines to select a location in memory for a data transfer. Note that the AC must be loaded with the address of the first memory location used in a data transfer.

Read Status Register (DRST)

Octal Code: 6745

Operation: Clear the AC and transfer the contents of the Status Register to the AC (Table 11-12).

Table 11-12
Contents of Status Register

Bit	Indication
0	TRANSFER DONE is set (1). a. At the end of a data transfer b. When an ERROR occurs while the controller is executing an operation c. When the selected drive completes a seek only operation d. When the selected drive completes a recalibrate operation if bit 4 in the Command Register is set **NOTE** **The TRANSFER DONE flag causes a program to interrupt if bit 3 in the Command Register is set.**
1	RDYS/R/W indicates the selected disk drive heads are in motion and the selected drive is RDY to SK, RD, or WR.
2	Not used.
3	SEEK FAIL is set (1) to indicate the selected drive failed to seek a cylinder address specified by the program. This bit is set by DSK SEEK FAIL L from the selected drive. The recalibrate operation must be performed to clear bit 3. If the DLAG instruction is executed by the program and bit 3 is set (1) the ERROR flag sets.
4	FILE NOT READY indicates the selected drive is not ready or inoperative. This bit is set (1) if DSK FILE DRY L from the selected drive is high. If the DLAG instruction is executed by the program, the ERROR flag sets if bit 4 is set (1). To clear bit 4, some action must be taken by the operator, i.e., power up the selected disk drive.

Table 11-12 (Cont)
Contents of Status Register

Bit	Indication
5	CONTROL BUSY ERROR is set (1) if the program executes the DLAG, DLCA, or DLDC instructions while the control is BUSY (IDLE is cleared). If a CONTROL BUSY ERROR occurs, the current operation is completed and the TRANSFER DONE flag sets at the end of the operation. This error occurs most often when programs are debugged, and requires rewriting of the program to eliminate the error. **CAUTION** **IOT DCLR with AC bit 11 should not be used to clear a CONTROL BUSY ERROR. If the DCLR instruction is issued by the program, the operation is aborted even if the program is writing a HEADER word.**
6	TIME OUT ERROR is set (1) if the control has been busy for more than 280 ms. If TIME OUT ERROR sets, the TRANSFER DONE flag sets. TIME OUT ERROR indicates a hardware problem and can be cleared by the DCLR instruction.
7	WRITE LOCK ERROR indicates the program tried to write on a write-protected disk drive. To write on a disk drive that has been write protected, the operator must manually clear the write lock protect by pressing the WT PROT switch on the drive which produced the error.
8	CRC ERROR is set (1) if the CRC character read from the disk does not agree with the CRC character calculated by the RK8-E as data is read from the disk. CRC ERROR sets the TRANSFER DONE flag immediately and the operation is stopped. If a CRC ERROR occurs, a new read operation must be initiated to reread the data; if this is not successful, the data must be rewritten.
9	DATA REQUEST LATE is set (1) if the processor does not respond to a break request within 22.5 μs. The 4-word Data Buffer Register is filled within 22.5 μs, and if one of the registers is not freed within this time period, a DATA REQUEST LATE ERROR occurs. DATA REQUEST LATE sets the TRANSFER DONE FLAG and stops the operation. A new operation must be initiated to transfer the same data. Note that if the Data Buffer Register is full during a read operation, the processor must grant a BRK RQST within 6.5 μs after the register is filled; or if the Data Buffer Register is empty during a write operation, the processor must grant a BRK RQST within 6.5 μs after the register is emptied. Either one of these conditions causes a DATA REQUEST LATE error. If the register is half-filled or half-empty, the latency would be 13 μs.
10	DRIVE STATUS ERROR is set (1) when the DLAG instruction is executed by the program if: a. The DRIVE NOT READY for one of the following reasons: 1. Power is not turned on 2. The drive does not exist (incorrect address) 3. The selected drive does not have a cartridge installed 4. The door on the selected drive is not closed (interlock open)

Table 11-12 (Cont)
Contents of Status Register

Bit	Indication
	5. Disk is not up to speed (disk rotation less than 1500 rpm) 6. Load switch on the selected disk drive is in the RUN position. The TRANSFER DONE flag is not set as a result of DRIVE NOT READY b. The WRITE CHECK ERROR is set to indicate the drive has one of the following error conditions. 1. Erase or write current without a WRITE GATE 2. The head position transducer lamp is inoperative. If WRITE CHECK ERROR is set, the WT PROT switch on the selected drive must be depressed to remove the error. WRITE CHECK ERROR does not set the TRANSFER DONE flag. 3. If disk capacity is exceeded (cylinder address greater than 312_8 was sent to the selected drive), the program must select a new disk address that is less than 312_8. The TRANSFER DONE flag is set if the disk capacity is exceeded. 4. If a SEEK FAILURE occurs in the drive, this indicates a seek was not completed because of some disk drive malfunction. If the control is busy at the time a SEEK FAILURE occurs, the TRANSFER DONE flag is set and the disk drive must be recalibrated using the recalibrate IOT DCLR with AC = 10.
11	CYLINDER ADDRESS ERROR is set (1) if the HEADER word of a sector does not agree with the cylinder address sent to the drive (either the HEADER word was read wrong or the read/write heads were positioned to the wrong address). The TRANSFER DONE flag is set and the HEADER word is retained in the CRC Register. The selected drive should be recalibrated using the DCLR instruction (AC = 0010), and the disk drive should be addressed again using the DLAG instruction. The cylinder address in the CRC Register is transferred to the AC by the maintenance instruction for the program to compare the disk address with the cylinder address requested by the program (refer to the 6747 maintenance IOT).

Load Command Register (DLDC)

Octal Code: 6746

Operation: Transfer the contents of the AC to the Command Register and clear the AC and Status Register. Note the AC must be loaded with information to be transferred to the Command Register (Table 11-13 and Figure 11-4) before this instruction is executed. Each of the functions selected by the Command Register are discussed in detail in Paragraph 11.11.1.

Table 11-13
Command Functions

Bit	Function
0,1,2	Bits 0, 1, and 2 of the Command Register are decoded and used to select disk operations as follows:

Bit 0	Bit 1	Bit 2	
0	0	0	Read Data – Seek disk address, check the HEADER, and read one sector.
0	0	1	Read All – Seek disk address, do not check the HEADER, and read one sector.
0	1	0	Write protect the selected drive.
0	1	1	Seek disk address, and if bit 4 is 1, set the TRANSFER DONE flag when seek is completed.
1	0	0	Write Data – Seek disk address, check HEADER, and write one sector.
1	0	1	Write all, seek disk address, do not check the HEADER, and write one sector.
1	1	0	Not used
1	1	1	Not used

3	If bit 3 is a 1, enable interrupt on ERROR flag or TRANSFER DONE.
4	If bit 4 is 1, set TRANSFER DONE flag when seek is complete.
5	If bit 5 is a 1, the controller writes or reads 128 words in a sector instead of 256. The TRANSFER DONE flag is set at the end of a sector and the last 128 words of the sector contains all zeroes.
6,7,8	Bits 6, 7, and 8 are used to address extended memory as follows:

Bit 6 (EMA2)	Bit 7 (EMA1)	Bit 8 (EMA0)	
0	0	0	Field 0
0	0	1	Field 1
0	1	0	Field 2
0	1	1	Field 3
1	0	0	Field 4
1	0	1	Field 5
1	1	0	Field 6
1	1	1	Field 7

Table 11-13 (Cont)
Command Functions

Bit	Function
	These bits are *not* incremented and the program must reload the Command Register to select a new memory field when the Current Address Register overflows (reads all zeroes).
9,10	Bits 9 and 10 are used to select a disk drive as follows: **Bit 9** **Bit 10** 0 0 Drive 0 0 1 Drive 1 1 0 Drive 2 1 1 Drive 3
11	Bit 11 is the extended cylinder address bit (Figure 11-15). It is added to the 7-bit Cylinder Address Register to allow the program to address cylinders 00_8 to 312_8. Note an address greater than 312_8 causes an ADDRESS ERROR.

Maintenance IOT (DMAN)

Octal Code: 6747

Operation: Transfers the contents of the AC to the RK8-E maintenance control logic. The maintenance operation performed is determined by contents of the AC (Table 11-14); therefore, the AC must be loaded before this instruction is executed. Table 11-14 gives the purpose of each bit, and the operations are discussed in detail in Paragraph 11.11.2.

11.11.1 Command Functions

When the Command Register is loaded by a DLDC instruction, the operation to be performed by the RK8-E is determined by bits 0, 1, and 2 from the AC. The following paragraphs explain each of these functions. A flow diagram illustrating all RK8-E operations is shown in Paragraph 11.15, Figure 11-15.

11.11.1.1 Read Data – A normal read operation (Table 11-13) is initiated when all zeroes (000) are transferred from AC0–AC2 to the Command Register by a DLDC instruction. The RK8-E and RK05 must interact to SEEK (find the correct cylinder), check the HEADER (find the correct surface), and read serial data from the disk drive. The serial data from the disk drive is read into Data Buffer 1 and transferred to the last empty buffer as a 12-bit parallel word. The parallel words are eventually moved into Data Buffer 4 and transferred to memory via the single cycle data break.

The RK8-E tries to keep the Data Buffer Register empty, by initiating single cycle data breaks, so that a register will be empty when each new word is received from the disk drive. If data is read from the disk drive while the Data Buffer Register is full, the DATA REQUEST LATE flag is set and the sector must be read again.

A read operation continues until 256 words have been read from the disk drive and the TRANSFER DONE flag sets. If the half block bit is set, 256 words are read, but only the first 128 words are data words. The second 128 words are all zeroes and are not transferred to memory.

Table 11-14
Maintenance Functions

Bit	Function
0	Enables maintenance logic and disables IOT DLAG (GO).
1	Enable a shift to lower buffer (DB4) by setting the DB4 control flip-flop.
2	Check CRC Register
3	Check Command Register
4	Check Surface and Sector Register
5	Check Data Buffer
6	Check Data Break Request
7	Transfer contents of Data Buffer 4 to the AC
8	Not used
9	Not used
10	Maintenance data bit
11	Not used

11.11.1.2 Read All – Read All is initiated when 001 is transferred from AC0–AC2 to the Command Register by the DLDC instruction. Read All is identical to a normal read operation except the HEADERs are not checked. This allows a disk cartridge that has been formatted to be checked by the program to verify the HEADERs have been written on the cartridge correctly.

11.11.1.3 Write Data – Write Data (Table 11-13) is initiated when a 100 is transferred from AC0–AC2 to the Command Register by a DLDC instruction. The RK8-E and RK05 must interact to SEEK (find the correct cylinder), check the HEADER (find the correct sector), and write data transferred from memory to Data Buffer 1 as a 12-bit parallel word via the single cycle data break. The 12-bit word is transferred from Data Buffer 1 to the last empty buffer. The 12-bit word is eventually transferred into Data Buffer 4 where it is shifted out to the disk drive as a 12-bit serial word to be written on the disk cartridge.

The RK8-E tries to keep the Data Buffer Register full during a write operation so that there will always be a word available when the drive is ready to write. If the disk drive calls for data when the Data Buffer Register is empty, the DATA REQUEST LATE flag is set and the sector must be rewritten.

The write operation continues until 256 words have been written on the cartridge and the TRANSFER DONE flag sets. If the half block bit is set, 128 words of data from memory are written on the disk cartridge and 128 words of all zeroes are written on the remainder of the sector.

11.11.1.4 Write All – Write All (Table 11-13) is initiated when a 101 is transferred from AC0–AC2 to the Command Register by the DLDC instruction. This function is identical to the write function except the HEADERS are not checked by the RK8-E. Write All is used to format a new disk cartridge. To format a disk cartridge, a HEADER word must be written at the beginning of each sector. The word to be written is determined by the program (Paragraph 11.12.1).

11.11.1.5 Write Protect – A 010 transferred from AC0–AC2 to the Command Register by a DLDC instruction turns on the WRITE PROTECT for the selected disk drive. If the program attempts to write on a disk drive that has WRITE PROTECT set, a WRITE LOCK ERROR occurs and stops the write operation. The only way to enable writing on a disk drive that has been write protected is to push OFF the WRT PROT OFF switch on the drive that was write protected.

11.11.1.6 Seek Only – When a 011 is transferred from AC0–AC2 to the Command Register by a DLDC instruction, the selected disk drive seeks the cylinder contained in the Cylinder Address Register but does not check the HEADER or start a read or write operation. Cylinder (2 tracks) seek electronics are self-contained in each disk drive so once the seek operation has been started a new disk drive can be selected. Thus, more than one disk drive can be doing a seek operation and the control can select another disk drive for a read or write operation. If seek only is specified and the DLAG instruction is executed by the program (this instruction starts all disk operations), the TRANSFER DONE flag is set after IOT DLAG is executed. TRANSFER DONE is set again when the seek is complete if bit 4 in the Command Register is set (1).

11.11.1.7 Interrupt Enable – The program interrupt system is enabled if bit 3 in the Command Register is set. When this bit is set (1), program interrupt is initiated if the TRANSFER DONE or ERROR flags are set.

11.11.1.8 TRANSFER DONE on SEEK COMPLETE – If bit 4 in the Command Register is set (1), the TRANSFER DONE flags set when the selected drive has completed a seek operation.

NOTE

Programming precautions must be taken when using this bit because it is possible to select another drive just as the drive that was previously selected completes a seek. If this happens, the unsophisticated program thinks there is a SEEK COMPLETE on the newly selected drive (see Paragraph 11.12.5 for information on programming around this hazard).

11.11.1.9 Read or Write Half Block (128 Words) – If bit 5 in the Command Register is set, a half block (128 words) of data is specified for a data transfer instead of the usual 256 words contained in one sector. When writing, the first 128 words of a sector come from memory and the second 128 words are all zeroes. The TRANSFER DONE flag is set after a complete sector (256 words) is written. When reading, the first 128 words read from the disk cartridge are transferred to memory. The TRANSFER DONE flag is set at the end of the sector when 256 words have been read. The delay before setting the TRANSFER DONE flag during a read or write half block operation is to allow the generation and checking of a CRC character at the end of the sector.

11.11.1.10 Extended Memory Addressing – Bits 6, 7, and 8 of the Command Register are used to address extended memory (Table 11-13). The extended memory address bits (EMA0–EMA2) are not incremented; thus, the Command Register must be reloaded to select a new memory field. If the Current Address Register overflows, the data is wrapped around in the same field. During a write operation, if data has already been written in those locations it will be written over; also the data read from memory during a write operation is duplicated (reread).

11.11.1.11 Unit Select – Bits 9 and 10 of the Command Register are decoded to select one of four disk drives (Table 11-13). Signals to and from a disk drive are inhibited except when the drive is selected.

11.11.1.12 Extended Cylinder Address – Bit 11 of the Command Register is an extension of the 7-bit Cylinder/Surface/Sector Address Register (Figure 11-4). The maximum number of usable cylinders is decimal 203, designated as 00_{10} to 202_{10} or 00_8 to 312_8. When the program specifies a cylinder address greater than 312_8, the CYLINDER ADDRESS ERROR flip-flop is set.

11.11.2 Maintenance Functions

The maintenance IOT 6747 (DMAN) ANDed with the contents of the AC allows program access to the major registers in the RK8-E. The maintenance instruction transfers data to the major registers (i.e., Data Buffer Register) or reads the contents of the registers into the AC or memory. Data can also be transferred to or from memory using the maintenance IOT. A DCLC instruction (clear control) must be used when changing from read to write or write to read.

The major registers are described in Paragraph 11.4. Note that the CRC Register is a multipurpose register that contains the cylinder address loaded from the AC and the cylinder address that is written or read as a HEADER word. This register also calculates the CRC character. The CRC Register also contains the CRC character read from the disk drive to be compared with the CRC that has been calculated. When the CRC Register is used as the Cylinder Address Register, bits 1–3 and 12–16 are zeroes and bits 4–11 contains the cylinder address.

The contents of the CRC, Command, and Surface/Sector Register must be shifted into Data Buffer 4 before they can be transferred to the AC or memory. These operations are explained in the following paragraphs.

11.11.2.1 Maintenance Mode – If the DMAN instruction is executed and AC00 is a 1, the controller is in the maintenance mode, the maintenance functions are enabled, and the DLAG (GO) IOT is disabled. The maintenance control bit is cleared by the clear control IOT (DCLC).

NOTE
Maintenance functions cannot be microprogrammed.

11.11.2.2 Shift Enable – If AC bit 01 is set when IOT DMAN is executed by the program, the lower Data Buffer (DB4) control flip-flop sets to enable a shift to the lower buffer.

11.11.2.3 Check CRC Register – When AC bit 02 is a 1 and the DMAN IOT is executed by the program, AC bit 10, the CRC Register, and Data Buffer 4 are logically connected as a 29-bit shift register that is shifted one position with each DMAN IOT. AC bit 10 shifts into the CRC and the CRC shifts into Data Buffer 4.

The program must count the bits shifted to determine when to read Data Buffer 4. AC bit 02 does not set a control bit so a clear is not necessary.

11.11.2.4 Check Command Register – When AC bit 03 is set and the DMAN IOT is executed by the program, the Command Register and Data Buffer 4 are logically connected as a 24-bit shift register that is shifted one position with each DMAN IOT. The program must count the bits shifted to determine when to read Data Buffer 4. AC bit 03 does not set a control bit so a clear is not necessary.

11.11.2.5 Check Surface/Sector Register – When AC bit 04 is 1 and the DMAN IOT is executed by the program, the surface bit, the Sector Register, and Data Buffer 4 are logically connected as a 17-bit shift register that is shifted one position with each DMAN IOT. The surface bit shifts into the Sector Register and the Sector Register shifts into Data Buffer 4.

The program must count the bits shifted to determine when to read the lower Data Buffer. AC bit 04 does not set a control bit so a clear is not necessary.

11.11.2.6 Check Data Buffer – When AC bit 05 is a 1 and the DMAN IOT is executed by the program, AC bit 10 and Data Buffer 1 are connected logically as a 13-bit shift register that is shifted one position with each DMAN IOT. In addition, the bit counter and word counter are incremented. The word counter is incremented by the overflow of the 12-bit counter.

After 12 shifts, the 12-bit counter overflows setting a control bit indicating that the upper Data Buffer 1 is full. The contents of Data Buffer 1 transfers to Data Buffer 4 which is read into memory. After 4 words if Data Buffer 4 is not read, and another bit is shifted into Data Buffer 1, the DATA REQUEST LATE ERROR flag is set. If Data Buffer 4 is read either into the AC or memory, information transfers into the buffer filling Data Buffer 4 and emptying Data Buffer 1. When the word counter overflows after 256 transfers, the TRANSFER DONE flag sets.

AC bit 05 does not directly set a control bit but its results do. A DCLC IOT should be issued before and after a sequence using AC bit 05.

11.11.2.7 Check Data Break Request – When AC bit 06 is a 1, and IOT DMAN is executed by the program, a single cycle data break request is initiated. The direction of transfer is controlled by the function bits in the Control Register. If a read is specified, the contents of Data Buffer 4 is transferred into the memory location specified by the Current Address Register and the Extended Memory Address Register. A write transfers data into Data Buffer 1. The data transfers into the buffer and the Data Buffer fills after four data break requests unless it is emptied by a read into the AC. It cannot be emptied by a read into memory if the DCLC is executed before switching from read to write or write to read. IOT DCLC clears the Data Buffer control bits so the buffer appears to be empty. AC bit 06 does set a control bit, but it is automatically cleared after the data break is completed.

11.11.2.8 Check Lower Data Buffer – When AC bit 07 is a 1 and IOT DMAN is executed by the program, the contents of Data Buffer 4 are read into the AC. AC bit 07 does not set a control bit so a clear is not necessary.

11.11.2.9 Maintenance Data – AC bit 10 is used in conjunction with other AC bits as data when the DMAN IOT is executed by the program.

11.12 PROGRAMMING SEQUENCES

11.12.1 Format A New Disk Cartridge

The RK8-E control contains the logic required to format a disk cartridge. All the program must do is address every sector on the disk and write on every sector using the Write All mode. The track address (cylinder and surface when DLAG was issued) is automatically written on the particular sector HEADER word selected by the control. The data written is not important except that the data should contain addressing information so a check can be made to determine if the RK8-E and drive found the correct sector on the correct surface and cylinder.

To write a new disk, the Command Register function bits (bits 0, 1, 2) should contain octal 5 (Write All). To read a newly formatted disk, the function bits should contain octal 1 (Read All). These function bits prevent the RK8-E from reading HEADER words and reporting HEADER errors that exist on an unformatted disk.

Sequence of instructions to format a disk:

1. Set up Current Address Register.
2. Set up Command Register 5000 for Write All, 1000 for Read All.
3. Set up first disk address and GO.
4. Wait for TRANSFER DONE flag, check for errors.
5. Set up current address again.
6. Set up second disk address and GO, etc.

11.12.2 Normal Read/Write

The programming sequence for a Write Data or Read Data mode is very similar to the sequence to format a disk. The sequence is:

1. Set up current address.
2. Set up Command Register 0000 for Read Data, 4000 for Write Data.
3. Set up required disk address and GO.
4. Wait for TRANSFER DONE flag and check for errors.

11.12.3 Bootstrap Loader

Many computers of the PDP-8 family include a clear with key start. On those machines, the clear of step 1 is not required.

1. Clear Control.
2. Load the Command Register with AC = 0000. This also clears the Status Register.
3. Load disk address and GO.
4. JMP.

Most bootstrap loaders for the RK8-E are in sector 0, surface 0, and cylinder 0; thus, with the control cleared, a two instruction bootstrap loader is all that is required.

11.12.4 Seek Only

The sequence for Seek Only (Command Register function bits equal 011) is different from Write All, Read All, Write Data or Read Data. It is necessary to put two skip or interrupt sequences in the program.

The programming sequence is:

1. Set up Command Register, 3000 for Seek Only and desired unit number.
2. Load disk address and GO.
3. Wait for TRANSFER DONE flag. TRANSFER DONE is set during a Seek Only when DISK ADDRESS ACKNOWLEDGE is received from the drive.
4. Clear Status Register DONE flag.
5. Drive is not seeking but if the TRANSFER DONE flag is to be set when the seek is complete, bit 4 of the Command Register must be a 1, issue a load Command DLDC instruction with selected drive number in AC 10–11 and AC bit 4=1.
6. Wait for TRANSFER DONE.

The alternative to steps 5 and 6 above is to check the condition of Status Register bit 1, which is 0 when the seek is complete.

11.12.5 Overlapped Seeks

Overlapped seeks make use of the seek only feature. The program starts multiple drives seeking and then periodically selects a different drive to determine if it has completed seeking. A different drive may be selected after Paragraph 11.12.4 step 3, but in general, programs operating with other program interrupt devices could be confused as to which drive actually completed a seek. For example, if bit 4 of the Command Register is a 1 (allowing seek complete to set the TRANSFER DONE flag) and multiple drives are seeking, it is possible to select a different drive just as one previously selected completes its seek. The TRANSFER DONE flag sets but the unsophisticated program incorrectly thinks the newly selected drive has completed a seek.

A program has two methods of getting around this problem.

a. Before selecting a new drive, the program changes the Command Register to make bit 4 a 0 without changing the drive number. It then changes the drive number with bit 4 equal to 1. If the new drive has completed a seek, there is no confusion as to which drive set the TRANSFER DONE flag.

b. Leave bit 4 of the Command Register set and check bit 1 of the Status Register to determine if the drive selected or the drive previously selected set the TRANSFER DONE flag. Bit 1 of the Status Register is 0 if the selected drive has completed the seek.

11.12.6 Recalibrate Selected Drive

The programming sequence for recalibrating a selected drive to cylinder 000 is similar to the sequence for Seek Only. The sequence follows:

1. Issue IOT 6742 with the AC equal to 0002.
2. Wait for TRANSFER DONE flag.
3. Clear status.
4. Drive is now seeking cylinder 000. If the TRANSFER DONE flag is to be set when the seek is complete, bit 4 of the Command Register must be set, i.e., issue DLDC instruction with AC 10–11 set to the selected drive and AC bit 4=1.
5. Wait for TRANSFER DONE.

The alternative to steps 4 and 5 is to check bit 1 of the Status Register. Bit 1 is 0 when the recalibrate seek is complete.

11.12.7 Data Transfers on Consecutive Sectors

Octal 1 or octal 4 (Read All or Write All) in the function portion of the Command Register allows a program to format a new disk cartridge by disabling the checking of headers. This feature is also used to transfer data on consecutive sectors. Assume a program is required to transfer 512 words of data on two consecutive sectors. The program should use Read Data and Write Data (octal 0 and 4 in the function portion of the Command Register) for the transfer of the first 256 words of data. When the first 256 words have been transferred and the TRANSFER DONE flag is set, there is a minimum of 100 μs for the program to set up the control for transfer to the next consecutive sector. The function portion of the Command Register should be changed to octal 1 or octal 5 (Read All or Write All), the Status Register cleared, and the next sector specified along with surface and cylinder when issuing DLAG. The control does check the header of the next sector but transfers 256 words of data. It is not necessary to change the Current Address Register, if a 512-word buffer is available in memory.

11.13 PROGRAMMING EXAMPLES

The following paragraphs provide examples to be used in programming the RK8-E Controller and the RK05 Disk Drive.

11.13.1 Write All

The programming sequence that follows could be used to write information on a disk sector in the Write All mode.

Example

```
BGN, CLA CLL IAC        / enable clear control AC10=0 AC11=1
     DCLR               / IOT 6742 clear control
     TAD CURENT         / desired current address AC0–11
     DLCA               / IOT 6744 load current address
     TAD DRIVE          / get drive number in AC9–11
     TAD WRTALL         / get Write All function in AC
     TAD FIELD          / get field in AC6–8
     TAD EXBIT          / get extended cylinder address bit in AC11
     DLDC               / IOT 6746 load Command Register
     TAD TRACK          / get desired track in AC0–11
     DLAG               / IOT 6743 load disk address and GO
     DSKP               / IOT 6741 skip on DONE or ERROR flag
     JMP .-1            / wait for flag
     DRST               / IOT 6745 read Status Register
     CIA                / change AC for testing
     TAD K4000          / compare to expected value
     SZA CLA            / skip if status OK
ERROR, HLT              / ERROR, disk status
     JMP DONE           / to other seek, read, or write routines.

FIELD, 0000             / desired field in AC6–8
TRACK, 0000             / desired cylinder, surface, and sector
K4000, 4000             / expected status
CURENT, 0000            / any desired current address
WRTALL, 5000            / write all function AC0–2
```

11.13.2 Recalibrate

The programming sequence that follows could be used to "recalibrate" (return the read/write heads to cylinder 0) a disk drive.

Example

```
BGN, CLA CLL IAC        / enable clear control AC10=0 AC11=1
     DCLR               / IOT 6742 clear control
     TAD DRIVE          / get drive number in AC9–10
     DLDC               / IOT 6746 load Command Register
     CLA CLL CML RTL    / enable recalibrate AC10=1 AC11=0
     DCLR               / IOT 6742 recalibrate
     DSKP               / 6741 IOT skip on DONE or ERROR flag
     JMP .-1            / wait for flag
     TAD K0200          / get enable set DONE bit in AC4
     TAD DRIVE          / get drive number in AC9–10
     DLDC               / IOT 6746 load Command Register
     DSKP               / IOT 6741 skip on DONE or ERROR flag
     JMP .-1            / wait for flag
     DRST               / IOT 6745 read Status Register
     CIA                / change AC for testing
```

```
    TAD K4000          / compare to expected value
    SZA CLA            / skip if status OK
ERROR, HLT             / ERROR, disk status
    JMP DONE           / read routines, to other seek, write

DRIVE, 0000            / desired drive in AC9–10
K0200, 0200            / enable set DONE AC4
K4000, 4000            / expected status only DONE flag.
```

11.13.3 Seek Only

The programming sequence that follows could be used for a Seek Only operation.

Example

```
BGN, CLA CLL IAC       / enable clear control AC10=0 AC11=1
    DCLR               / IOT 6742 clear control
    TAD DRIVE          / get drive number in AC9–10
    TAD SEEK           / get seek function in AC0–2
    TAD EXBIT          / get extended cylinder address bit in AC11
    DLDC               / IOT 6746 load Command Register
    TAD TRACK          / get desired track in AC0–11
    DLAG               / IOT 6743 load disk address and GO.
    DSKP               / IOT 6741 skip on DONE or ERROR flag
    JMP .-1            / wait for flag
    TAD K0200          / get enable set DONE on seek complete in AC4
    TAD DRIVE          / get drive number in AC09 and AC10
    DLDC               / IOT 6746 load Command Register
    DSKP               / IOT 6741 skip on DONE or ERROR flag
    JMP .-1            / wait for flag
    DRST               / IOT 6745 read Status Register
    CIA                / change AC for testing
    TAD K4000          / compare to expected value
    SZA CLA            / skip if OK
ERROR, HLT             / ERROR, disk status
    JMP DONE           / seek complete, now to read or write routine
                       / or another seek routine

K0200, 0200            / enable set DONE bit (AC bit 4)
K4000, 4000            / known good or expected status
DRIVE, 0000            / desired drive in AC bits 9–10
SEEK, 3000             / seek only function in AC bits 0–2
EXBIT, 0000            / extended cylinder bit in AC bit 11
TRACK, 0000            / any desired cylinder, surface, and sector.
```

11.13.4 Overlap Seek

The programming sequence that follows could be used for an Overlap Seek operation with multiple drives (Note: four (4) drives are assumed).

Example

```
BGN, CLA CLL IAC        / enable clear control AC10=0 AC11=1
     DCLR               / IOT 6742 clear control
     DCA DRIVE          / start with drive 0
     TAD M4             / 4 drive counter constant
     DCA CNTRL          / set up the counter
OUT, TAD DRIVE          / get drive number pointer
     CLL RAL            / put AC10–11 in AC9–10
     AND K0006          / mask 9–10
     DLDC               / IOT 6746 load Command Register
     TAD DRIVE          / get drive number pointer
     CLL RAL            / put AC10–11 in AC9–10
     AND K0006          / mask 9–10
     TAD SEEK           / get seek function in AC0–2
     TAD EXBIT          / get extended cylinder address bit in AC11
     DLDC               / IOT 6746 load Command Register
     TAD TRACK          / get desired track in AC0–11
     DLAG               / IOT 6743 load disk address and GO.
     DSKP               / IOT 6741 skip on DONE or ERROR flag
     JMP .-1            / wait for flag
     ISZ DRIVE          / update drive number pointer
     JMP CNTRL          / count drives
     JMP OUT            / send next drive out
     JMP WAIT           / to drive wait routine to wait for drives

DRIVE, 0000             / drive number pointer
SEEK, 3000              / seek only function in AC0–2
EXBIT, 0000             / extended cylinder bit in AC11
K0006, 0006             / mask 9–10
M4, 7774                / minus 4 constant
CNTRL, 0                / counter
```

Routine to wait for drives doing an Overlap Seek.

```
WAIT, CLA CLL IAC       / enable clear control AC10=0 AC11=1
     DCLR               / IOT 6742 clear control
     DCA DRIVE          / start with drive 0
     TAD M4             / 4 drive counter constant
     DCA CNTRL          / setup drive counter
IN, TAD DRIVE           / get drive number pointer
     CLL RAL            / put AC10–11 in AC9–10
     AND K0006          / mask 9–10
     DLDC               / IOT 6746 load Command Register
```

```
RDSTA, DRST          / IOT 6745 read Status Register
      CLL RAL        / transfer AC01 to AC00
      SZA CLA        / skip if drive not busy
      JMP RDSTA      / drive still busy AC bit 1
      ISZ DRIVE      / drive completed seek
      ISZ CNTRL      / update drive counter
      JMP IN         / wait for next drive
      JMP DONE       / all drives complete. To other read, write, or
                     /seek routines

DRIVE, 0000          / drive number pointer
K0006, 0006          / mask
M4, 7774             / drive counter constant
CNTRL, 0             / counter
```

11.13.5 Write Data

The programming sequence that follows could be used to write information on a disk sector in the Write Data mode.

Example

```
BGN, CLA CLL IAC     / enable clear control AC10=0 AC11=1
      DCLR           / IOT 6742 clear control
      TAD CURENT     / desired current address AC0–11
      DLCA           / IOT 6744 load Current Address
      TAD DRIVE      / get drive number in AC9–11
      TAD WRTDAT     / get Write Data function in AC
      TAD FIELD      / get field in AC6–8
      TAD EXBIT      / get extended cylinder address bit in AC11
      DLDC           / IOT 6746 load Command Register
      TAD TRACK      / get desired track in AC0–11
      DLAG           / IOT 6743 load Disk Address and GO.
      DSKP           / IOT 6741 skip on DONE or ERROR flag
      JMP .-1        / wait for flag
      DRST           / IOT 6745 read Status Register
      CIA            / change AC for testing
      TAD K4000      / compare to expected value
      SZA CLA        / skip if status OK
ERROR, HLT           / ERROR, disk status
      JMP DONE       / to other seek, read, or write routines

FIELD, 0000          / desired field in AC6–8
TRACK, 0000          / desired cylinder, surface, and sector
K4000, 4000          / expected status
CURENT, 0000         / any desired current address
WRTDAT, 4000         / write data function AC0–2
```

11.13.6 Read All

The programming sequence that follows could be used to read information from a disk sector in the Read All mode.

Example

```
BGN, CLA CLL IAC        / enable clear control AC10=0 AC11=1
     DCLR               / IOT 6742 clear control
     TAD CURENT         / desired current address AC0–11
     DLCA               / IOT 6744 load current address
     TAD DRIVE          / get drive number in AC9–10
     TAD REDALL         / get Read All function in AC
     TAD FIELD          / get field in AC6–8
     TAD EXBIT          / get extended cylinder bit in AC11
     DLDC               / IOT 6746 load Command Register
     TAD TRACK          / get desired track in AC0–11
     DLAG               / IOT 6743 load disk address and GO.
     DSKP               / IOT 6741 skip on DONE or ERROR flag
     JMP .-1            / wait for flag
     DRST               / IOT 6745 read Status Register
     CIA                / change AC for testing
     TAD K4000          / compare to expected value
     SZA CLA            / skip if status OK
ERROR, HLT              / ERROR, disk status
     JMP DONE           / to other seek, read, or write routines.

FIELD, 0000             / desired field in AC6–8
TRACK, 0000             / desired cylinder, surface, and sector
K4000, 4000             / expected status
CURENT, 0000            / any desired current address
REDALL, 1000            / Read All function AC0–2
```

11.13.7 Read Data

The following is an example of a programming sequence that could be used to read information from a disk sector in the Read Data mode.

Example

```
BGN, CLA CLL IAC        / enable clear control AC10=0 AC11=1
     DCLR               / IOT 6742 clear control
     TAD CURENT         / desired current address AC0–11
     DLCA               / IOT 6744 load current address
     TAD DRIVE          / get drive number in AC9–11
     TAD REDDAT         / get Read Data function in AC
     TAD FIELD          / get field in AC6–8
     TAD EXBIT          / get extended cylinder bit in AC11
     DLDC               / IOT 6746 load Command Register
     TAD TRACK          / get desired track in AC0–11
     DLAG               / IOT 6743 load Command Register
     DSKP               / IOT 6741 skip on DONE or ERROR flag
     JMP .-1            / wait for flag
     DRST               / IOT 6745 read Status Register
     CIA                / change AC for testing
```

```
        TAD K4000       / compare to expected value
        SZA CLA         / skip if status OK
ERROR,  HLT             / ERROR, disk status
        JMP DONE        / to other seek, read, or write routines.

FIELD,  0000            / desired field in AC6–8
TRACK,  0000            / desired cylinder, surface, and sector
K4000,  4000            / expected status
CURENT, 0000            / any desired current address
REDDAT, 0000            / read data function AC0–2
```

SECTION 4 THEORY OF OPERATION

This chapter contains a block diagram description (functional level) and a detailed description of the RK8-E logic. Figure 11-9 shows the signal flow between the functional groups of logic.

11.14 BLOCK DIAGRAM DESCRIPTION

The RK8-E consists of 8 major groups of logic:

- I/O Bus Interface
- Command Register
- Status Register
- Data Break Control
- Data Buffer Registers
- CRC Register
- Control Sequencer (Major States Register and Counters)
- Maintenance Logic

11.14.1 I/O Bus Interface

The I/O bus interface (Figure 11-9) provides the following:

a. A buffer for MD00–MD11 from the OMNIBUS

b. IOT decoder

c. Timing pulses for the execution of instructions and maintenance operations.

MD00–MD11 are decoded by the IOT decoder when instructions are executed by the program and generate signals to load the RK8-E registers, execute skips and interrupts, and generate timing pulses for maintenance operations. The outputs of the IOT decoder are used as control signals in other sections of the RK8-E. During the data break of a write operation, the buffered memory data bits (MD00–MD11) are applied to the Data Buffer Register for transfer to the selected disk drive. This block of logic also contains bus drivers for signals to the OMNIBUS (i.e., BRK RQST, INT RQST, SKIP, and INT I/O L) and provides a buffer for signals from the OMNIBUS (i.e., I/O PAUSE and the time pulses).

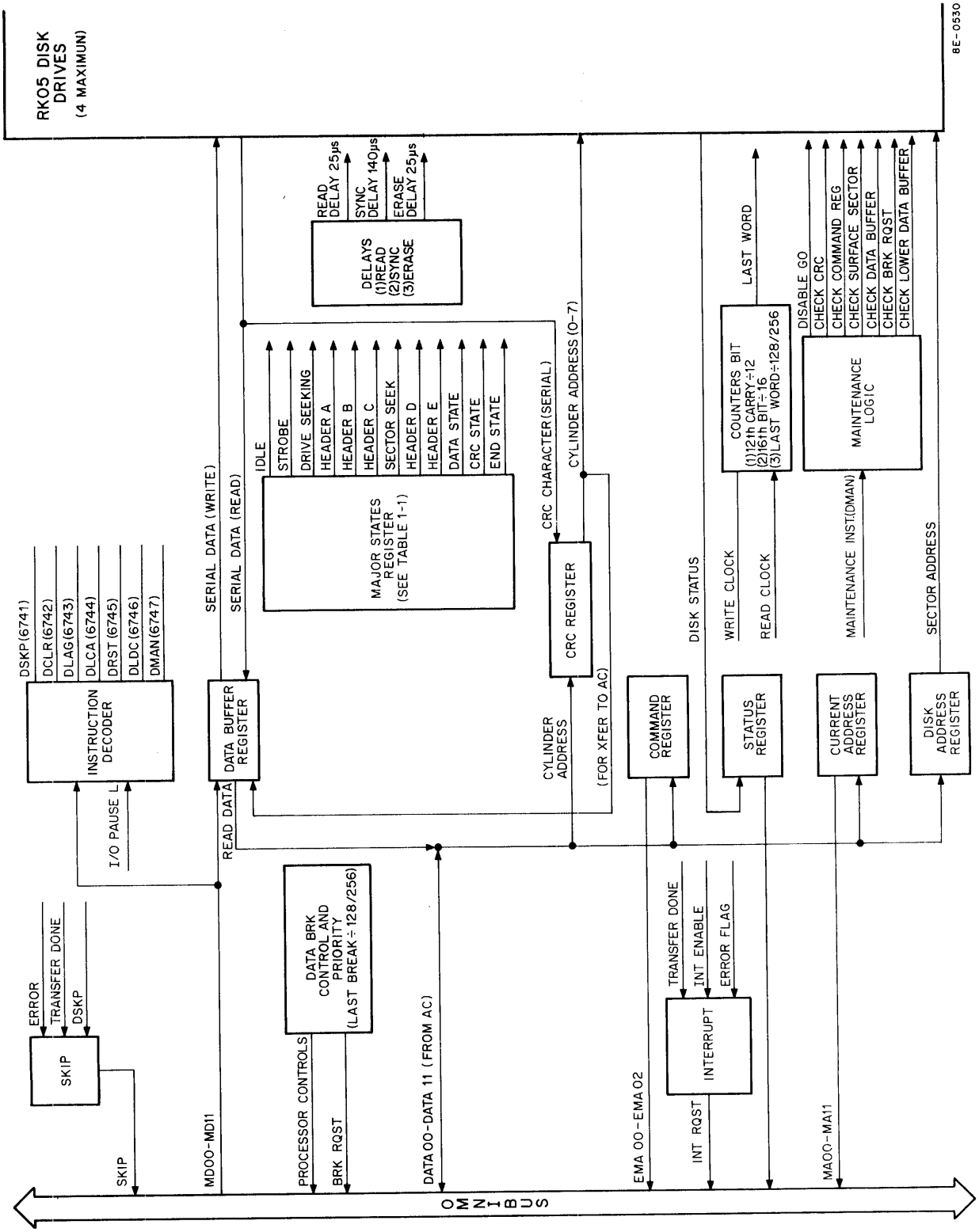


Figure 11-9 RK8-E Block Diagram

11.14.2 Command Register

The Command Register (Table 11-13) enables all disk drive operations, i.e., read, write and seek, selects a disk drive unit, selects a memory field for data transfers, enables interrupts, provides the most significant cylinder address bit, and determines the number of words to be transferred (128 or 256). The Command Register (Figure 11-9) is loaded from the AC by a DLDC instruction with DATA 0—DATA 11. Note that the contents of the Command Register are decoded and used after the program executes the DLAG instruction (load disk address and GO).

During maintenance operations, the contents of the Command Register are transferred to the AC using the DMAN instruction (Table 11-14).

11.14.3 Status Register

The Status Register (Figure 11-9) contains the current status of the selected disk drive (Table 11-12). The program determines the status of the RK8-E and disk drive by transferring the contents of the Status Register to the AC using a DRST instruction. The Status Register receives its input from the RK05 Disk Drive and the data break control logic. The DONE and ERROR flags are applied to the I/O bus interface to generate skips and interrupts if the skip or interrupt logic is enabled. Note that bit 3 in the Command Register must be set (1) to enable an interrupt when the DONE or ERROR flag sets.

11.14.4 Data Break Control Logic

The data break control logic (Figure 11-10) determines the break priority of the RK8-E, controls direction of data transfer (to or from memory), and selects a location in memory for the data transfer.

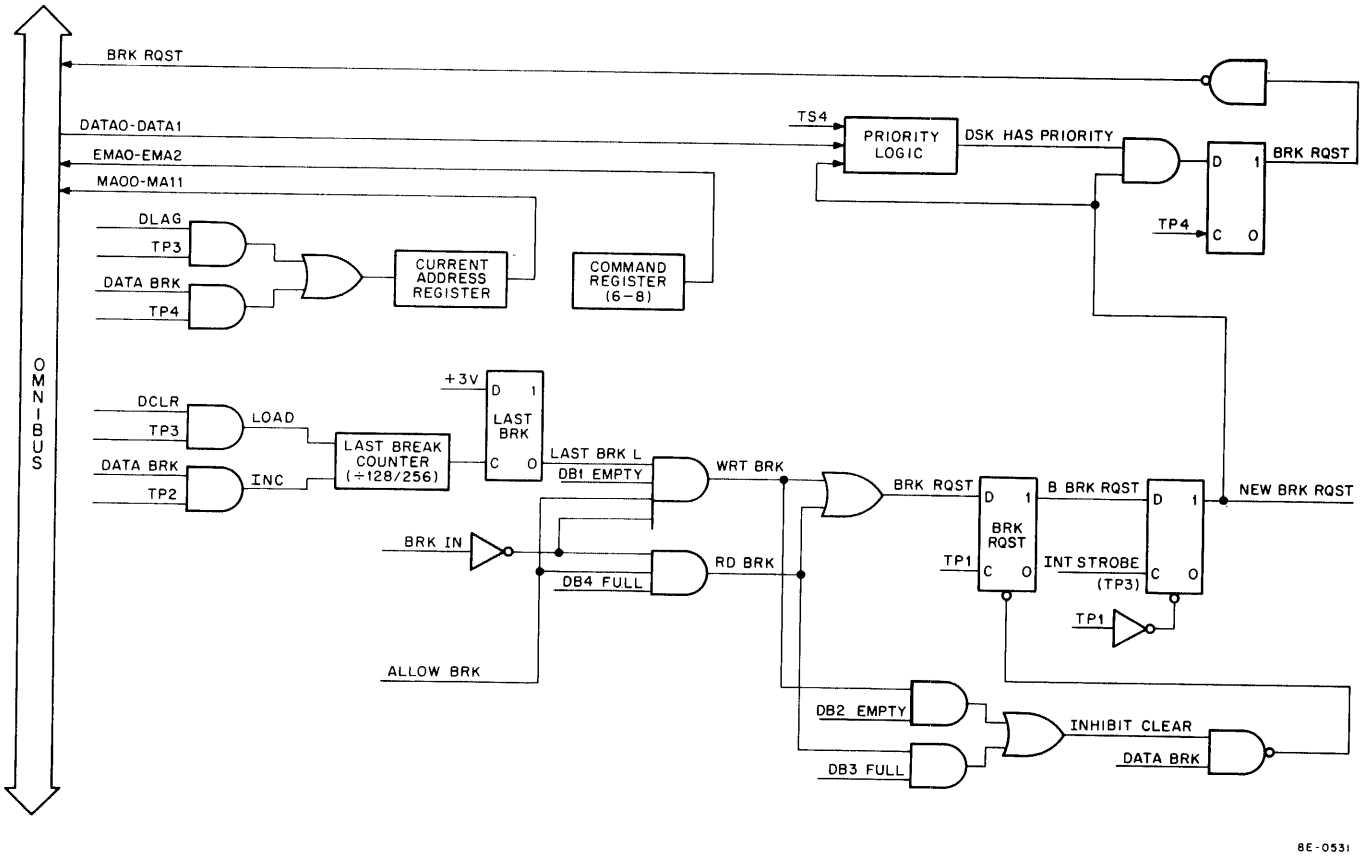


Figure 11-10 Data Break Control

The Current Address Register is loaded from the AC by a DLCA instruction with the initial address to be used in a data transfer. The Current Address Register is incremented after each data break and applied to the MA lines (MA00—MA11) to sequentially select memory locations for data transfers. Note that the memory field is selected by bits in the Command Register (Table 11-13) and not incremented when the CA Register is incremented. The direction of data transfer is determined by the decoded function bits in the Command Register, i.e., during a read operation, data is transferred from the Data Buffer Register to memory via the data bus. Time pulses from the OMNIBUS and control signals from the Data Buffer Register determine the timing of the single cycle data break. The data break control also generates signals to stall the processor and stop the execution of instructions during a data transfer.

The data break priority is returned to the OMNIBUS as DATA 0 (priority 0) or DATA 1 (priority 1) to indicate the priority of the RK8-E. Data break control provides a DATA LATE signal to the Status Register if the processor does not respond to a BRK RQST within 22.5 μs. The last break counter counts the words in a data transfer and sets the LAST BRK flip-flop when 128 (half block) or 256 words have been transferred.

11.14.5 Data Buffer Register

The Data Buffer Register (Figure 11-11) provides four Data Buffer Registers (DB1—DB4) for temporary storage of data that is being transferred between memory and the disk drive. The four registers increase the data break latency of the RK8-E control from 5.6 μs to 22.5 μs. Latency is defined as the maximum time the RK8-E can wait for a BRK RQST to be accepted by the processor. During a write operation, parallel bits of data (MD00—MD11) are received from the OMNIBUS and applied to DB1. The parallel data is dropped into DB4 and shifted out of DB4 on RK DATA 11 as serial data to the selected disk drive. During a read operation, serial data from the disk is shifted into DB1 and dropped into DB4. The parallel bits out of DB4 are transferred to the data bus for transfer to memory during a single cycle data break. The control logic associated with the Data Buffer Register controls the registers and generates signals that are applied to the data break control logic. During maintenance operations, the contents of the CRC Register, Command Register, and Surface/Sector Register can be shifted into DB4 and transferred to the AC or memory by the DMAN instruction. The shifting of data in these registers is accomplished by the MAIN pulse, which is generated by the DMAN instruction.

11.14.6 CRC Register

The CRC Register (Figure 11-12) is a 16-bit multipurpose register with the following functions:

a. The CRC Register receives a cylinder address from the AC when the DLAG (GO) instruction is executed by the program and transfers the cylinder address to the selected disk drive.

b. Makes a bit-by-bit comparison of the cylinder address specified by the program and the cylinder address from the disk drive to determine if disk has found the correct cylinder.

c. During a write operation, a 16-bit CRC character is computed, transferred to the disk, and written at the end of the record.

d. During a read operation, a 16-bit CRC character is computed and compared with the CRC character written at the end of the record. If the two characters are different, NOT EQUAL is asserted to set the CRC ERROR flag. A CRC ERROR is produced if bits are lost or added during the read or write operation.

The disk address is transferred from the AC as a 12-bit parallel word and bit 11 from the Command Register is added to the 7 most significant bits of the CRC Register to form the 8-bit cylinder address (Figure 11-5) transferred to the selected disk drive. Bits 12 through 16 are not used for the disk address. The disk address is transferred to the disk drive on parallel lines during the STROBE major state.

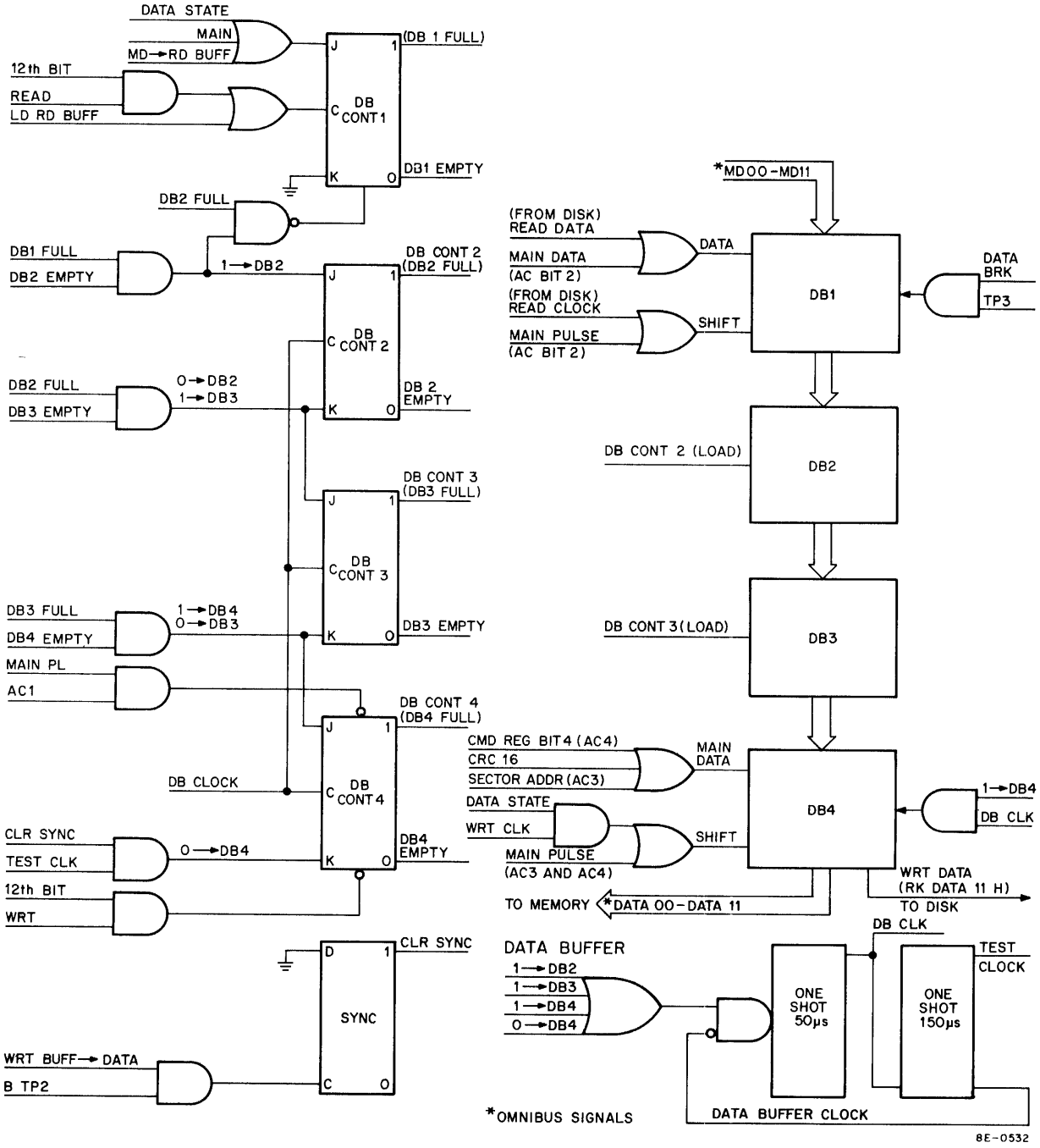


Figure 11-11 Data Buffer Register

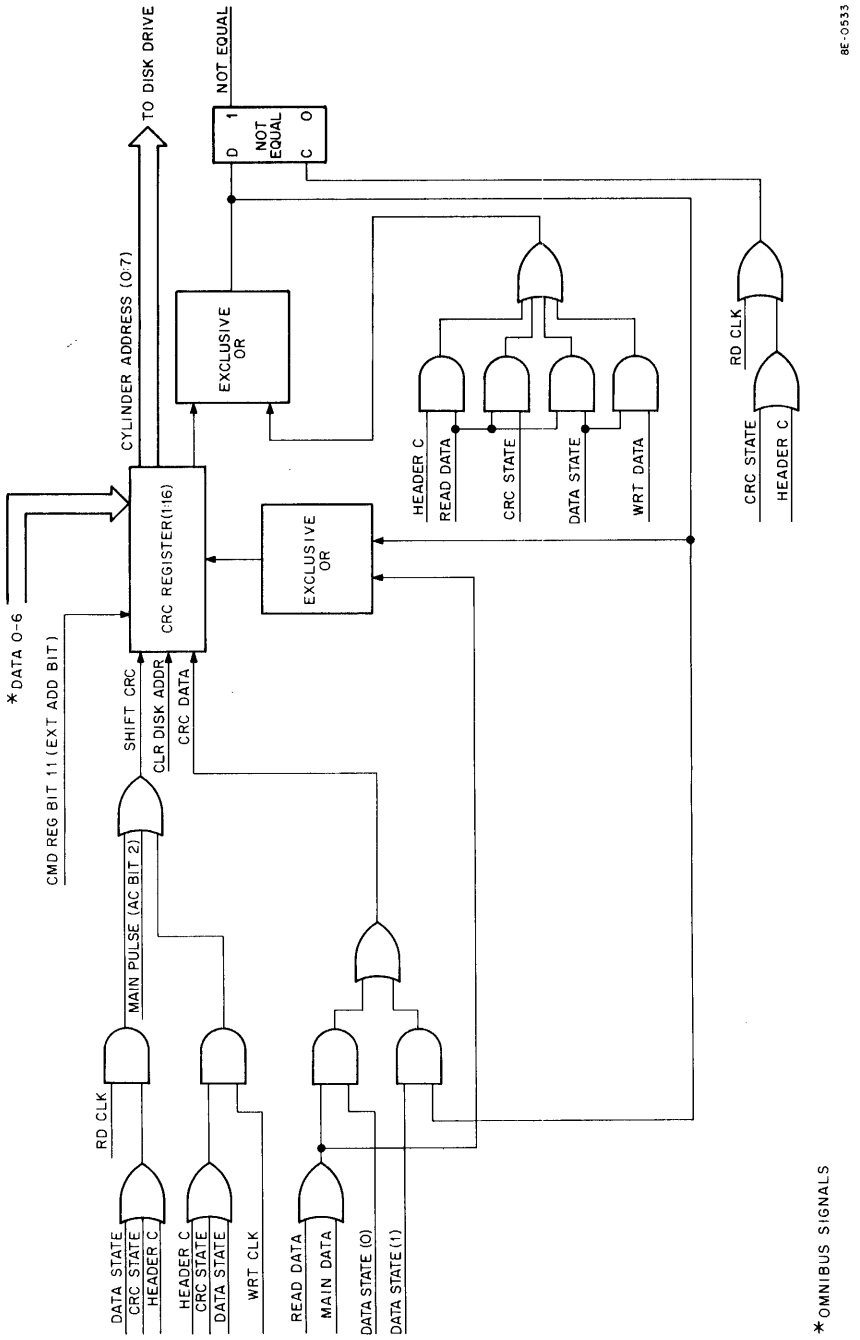


Figure 11-12 CRC Register

When the RK8-E moves into the DATA state, the CRC Register is cleared and the computation of a CRC character is started.

During write operations, the CRC character is transferred to the disk drive during the CRC state as a 16-bit serial word. The serial bits are shifted out of the CRC Register to the disk drive and written at the end of the data.

During read operations, the CRC character is computed from the data read from the disk and compared with the CRC character that was written at the end of the data. The CRC Register makes a bit-by-bit comparison of the two CRC characters, and if they are different, NOT EQUAL is asserted to set the CRC ERROR flag.

The contents of the CRC Register are checked using the maintenance instruction. The bits in the CRC Register are shifted into Data Buffer 4 and transferred to the AC (Table 11-14).

11.14.7 Control Sequencer

The control sequencer (Figures 11-13 and 11-14) comprises the Major States Register, word counter (128 or 256 words), and the bit counter. The word counter and bit counter keep track of the number of words transferred to or from the disk drive. The bit counter counts 12 bits from the disk drive and increments the word counter each time a word (12 bits) is read from the disk. After 256 words are read, the data transfer is stopped and the CRC character is written on the disk during a write, or read from the disk during a read. If bit 5 in the Command Register is set (1), the data transfer is stopped after 128 words are read or written, but the disk drive continues to write all zeroes during a write operation or read all zeroes during a read operation until 256 words have been written or read. This allows the RK8-E to process the CRC character, which is always written at the end of the data (Figure 11-7).

The Major States Register determines the format of the disk, i.e., PREAMBLE, HEADER, DATA, CRC, and POSTAMBLE.

11.14.7.1 Major States – The Major States Register (Figures 11-13 and 11-14) controls each step the RK8-E control progresses through to perform a seek, read, or write operation. Each major state causes specific operations to be performed (Table 11-2 and Figure 11-7).

The Major States Register is a shift register that shifts a binary 1 starting at the IDLE state and ending with the END states as shown in Figure 11-7 unless an error occurs (i.e., an ADDRS ERROR) or the function does not require all major states (i.e., sector, seek, and recalibrate).

11.14.7.2 IDLE State – The RK8-E must be in the IDLE state (Figure 11-13) to allow initiation of a disk function and returns to the IDLE state after an operation is completed. The IDLE state indicates that the control is not busy and that it is capable of accepting IOT instructions from the processor (Figure 11-14). The IDLE flip-flop is cleared when the program executes a DLAG instruction (load disk address and GO) or the CLR drive (DCLD) instruction. The DCLD instruction initiates a special state called RESTORE, which is discussed in Paragraph 11.15.3.

The IDLE state flip-flop is set by any of the following conditions to return the control to the IDLE state to wait for RK8-E instructions.

a. At the end of ERASE DELAY during a write function.

b. During last break of a read operation (after Data Buffer Register is empty).

c. When the selected disk drive asserts ACKNOWLEDGE during a seek only operation.

d. When the ERROR flag is set (Table 11-12).

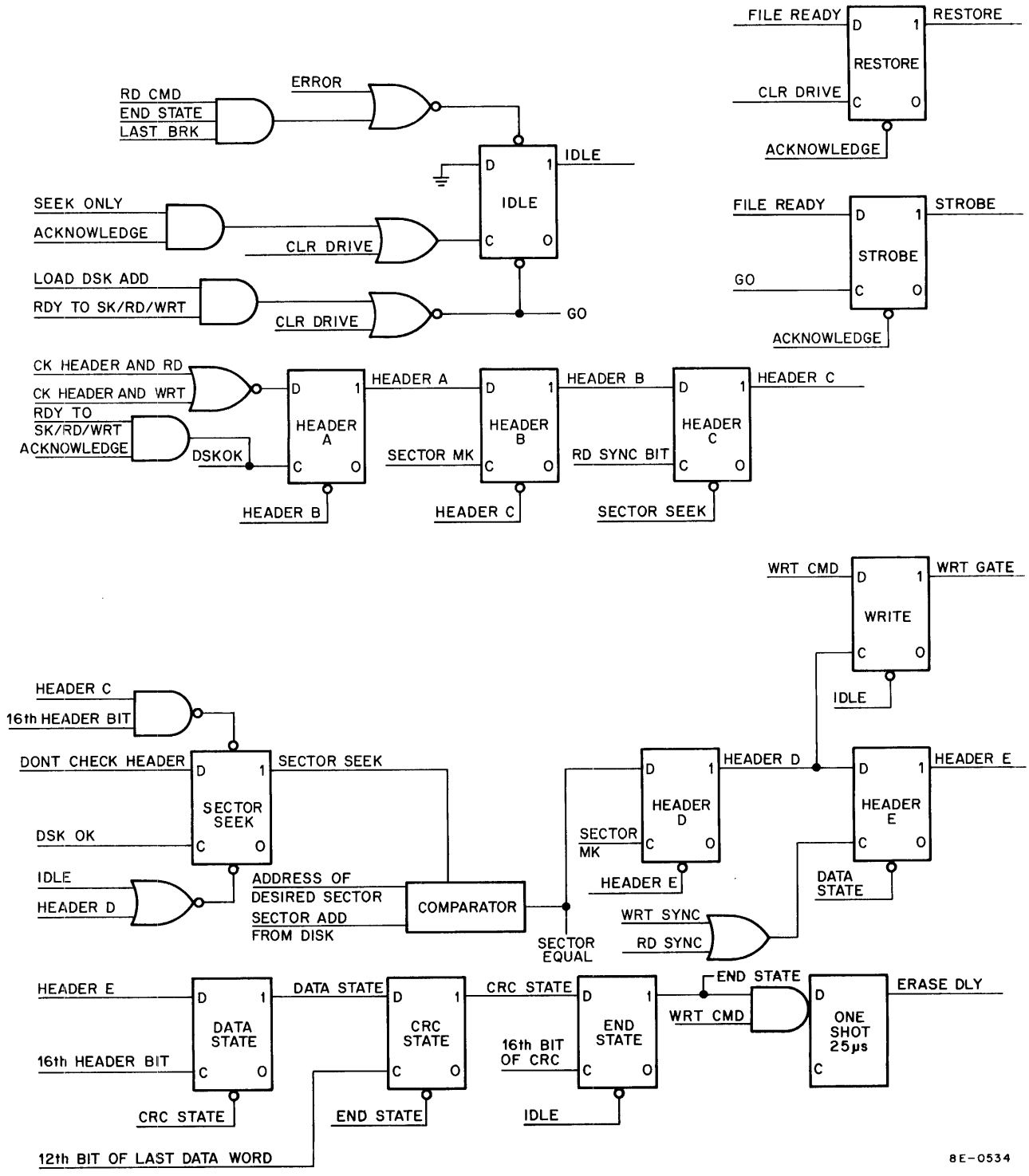


Figure 11-13 Major States Register

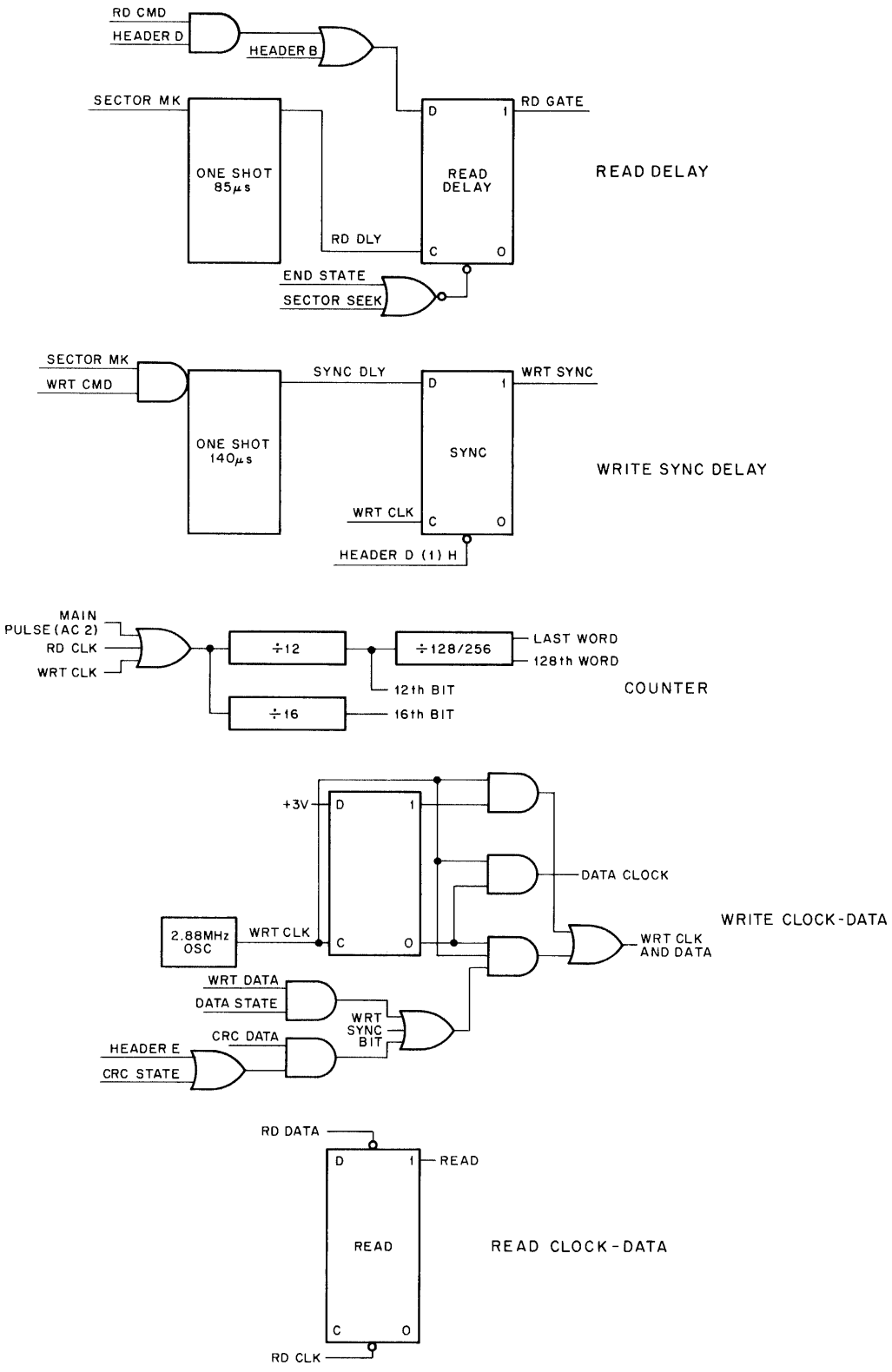


Figure 11-14 Read/Write Delays and Counters

11.14.7.3 RESTORE State – The RESTORE state is a special state (Figure 11-13) used to clear SELECT ERRORS and CYLINDER ADDRESS ERRORS. RESTORE is set by FILE READY and the CLR DRIVE command, generated by the DCLD instruction. When the selected disk asserts ACKNOWLEDGE, the RESTORE flip-flop is cleared and the Major States Register goes back to the IDLE state to wait for RK8-E instructions. Thus, the RK8-E uses only one state for the clear operation and the control is released (made not busy) while the disk drive returns to the home position.

11.14.7.4 STROBE State – The STROBE state (Figure 11-13) is used to transfer the cylinder address from the CRC Register to the disk drive and wait for the selected drive to ACKNOWLEDGE the cylinder address. The STROBE flip-flop is set by GO when the DLAG instruction is executed by the program if the selected disk drive is ready (FILE READY asserted). STROBE is cleared when ACKNOWLEDGE is received from the selected drive and the Major States Register moves to the HEADER A state or SECTOR SEEK state (Figure 11-7) when the selected drive is ready to seek, read or write (Figure 11-14).

11.14.7.5 HEADER A State – The HEADER A state (Figure 11-13) is used to start a read delay (Figure 11-15) and wait for a sector mark during read and write functions. When a sector mark is obtained from the disk drive, the HEADER B state is entered and the HEADER A state is cleared by HEADER B.

11.14.7.6 HEADER B State – The HEADER B state (Figure 11-14) is used to turn READ on at the end of READ DELAY (Figure 11-12) and read zeroes until a SYNC pulse is encountered. The SYNC pulse indicates the beginning of the HEADER area of the disk format.

During a write operation, the write sync delay is triggered when a sector mark is received from the disk (Figure 11-14). After a 140 μs (write sync delay), a one bit (SYNC pulse) is written on the disk to indicate where the HEADER area starts. When the SYNC pulse is read or written, the RK8-E advances to the HEADER C state and HEADER B is cleared.

11.14.7.7 HEADER C State – The HEADER C state (Figure 11-14) is used to read the 16-bit HEADER word and compare it bit-by-bit with the disk address in the CRC Register. HEADER C is cleared when the divide-by-16 counter (Figure 11-15) asserts 16th bit to indicate the 16th bit of the HEADER word has been read from the disk drive. When HEADER C clears, it sets SECTOR SEEK (Figure 11-14) and starts the SECTOR SEEK major state.

11.14.7.8 SECTOR SEEK State – When the control enters the SECTOR SEEK state, cylinder address ERROR is set if the cylinder address does not equal the HEADER word read from the disk during the HEADER C state (Figure 11-12). During the SECTOR SEEK state, the sector address lines from the RK05 are compared with the Surface/Sector Register.

11.14.7.9 HEADER D State – The HEADER D state is used to wait for the completion of READ DLY (85 μs) during a read function or the completion of SYNC DLY during a write operation. If this is a read function, the controller reads all zeroes until a SYNC bit is read. When the sync bit is read, the control advances to the HEADER E state. If this is a write function, the control writes zeroes and waits for SYNC DLY, then writes the SYNC bit (a data 1). When the SYNC bit is written, the RK8-E moves to the HEADER E state and clears the HEADER D flip-flop.

11.14.7.10 HEADER E State – The HEADER E state is used to read, but ignores 16 bits of data during a read operation. During a write operation, the 16-bit HEADER word in the CRC Register is written. When the 16-bit HEADER word has been read or written, the Major States Register advances to the DATA state.

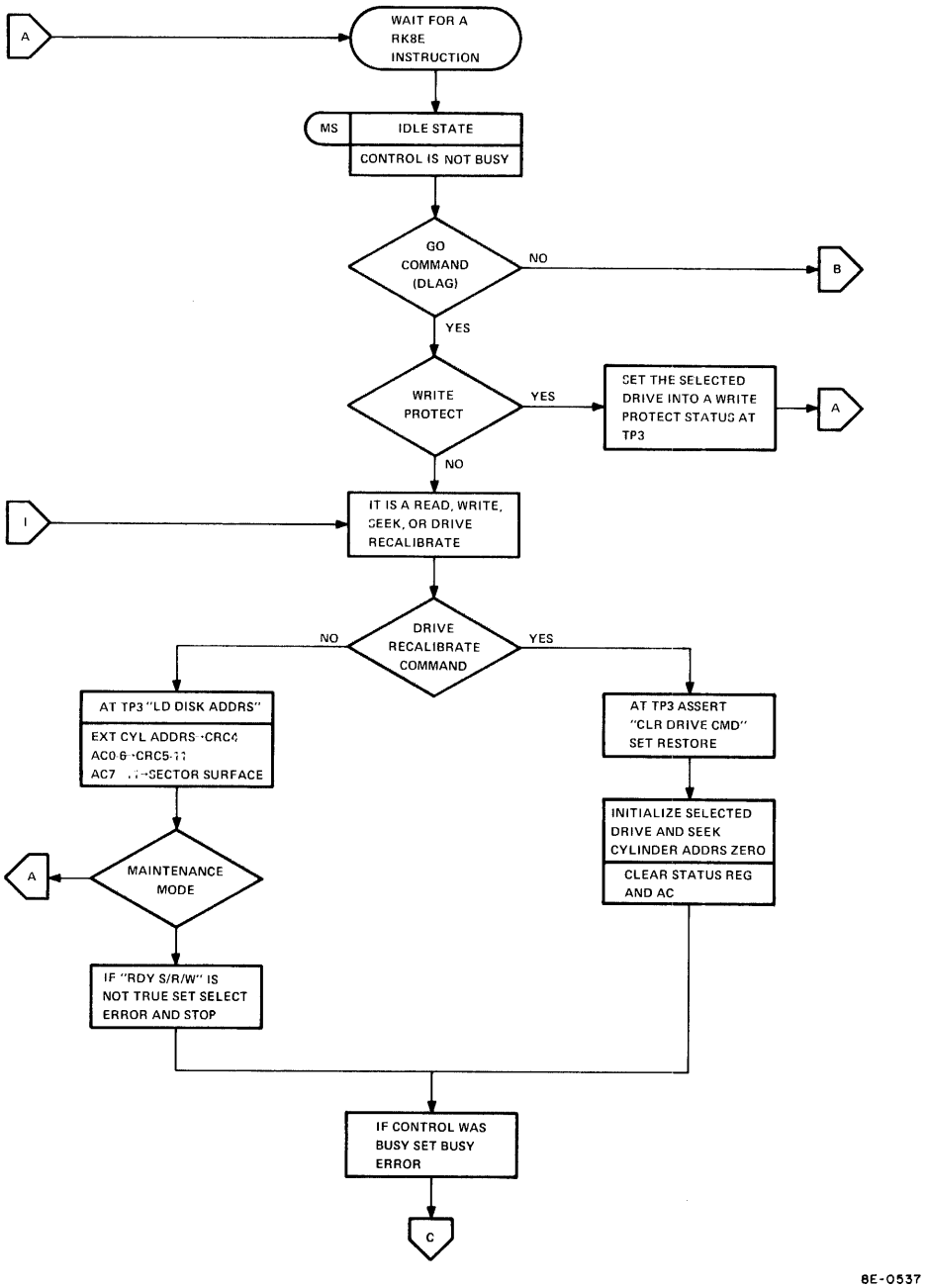


Figure 11-15 RK8-E Flow Diagram (sheet 1)

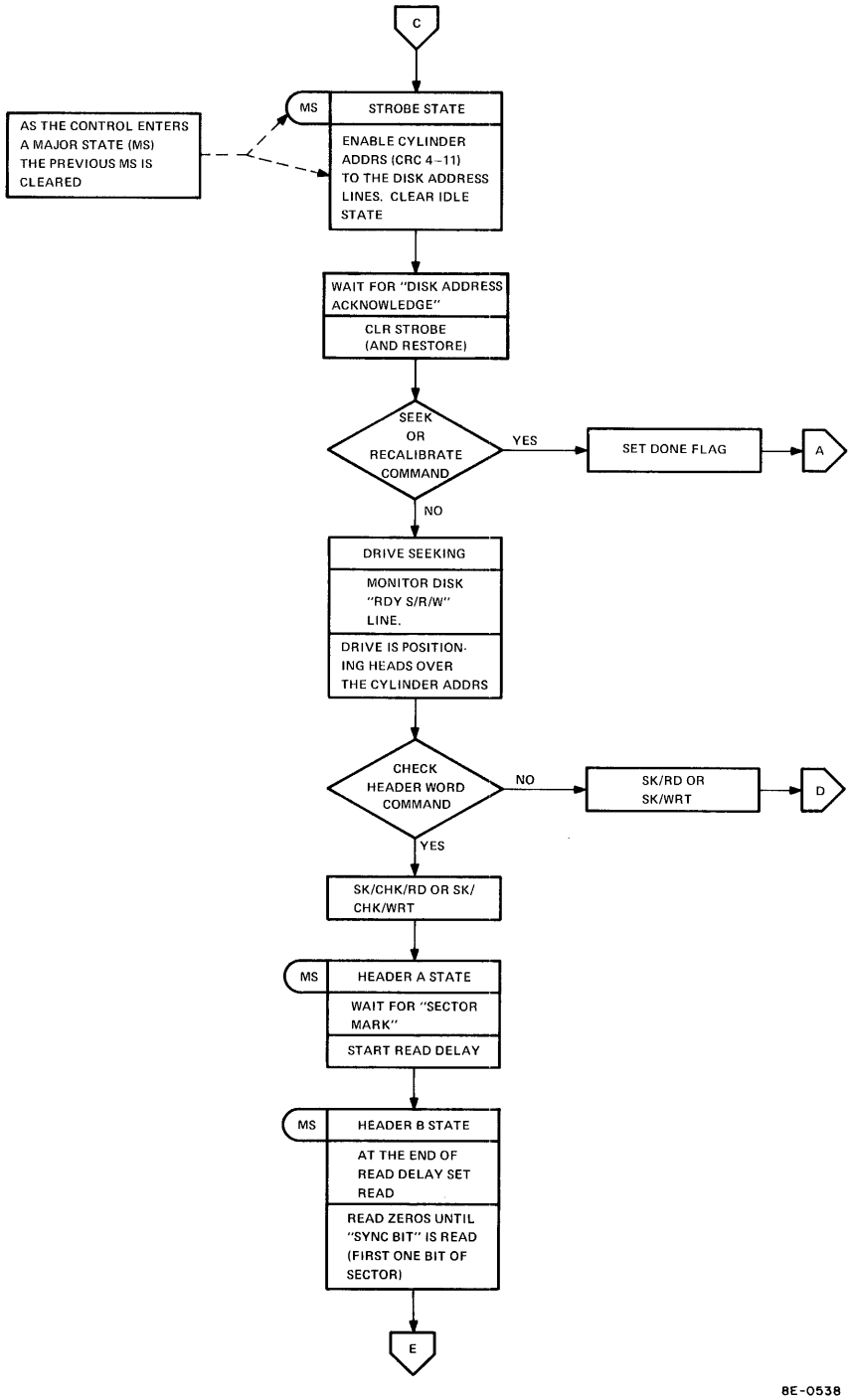


Figure 11-15 RK8-E Flow Diagram (sheet 2)

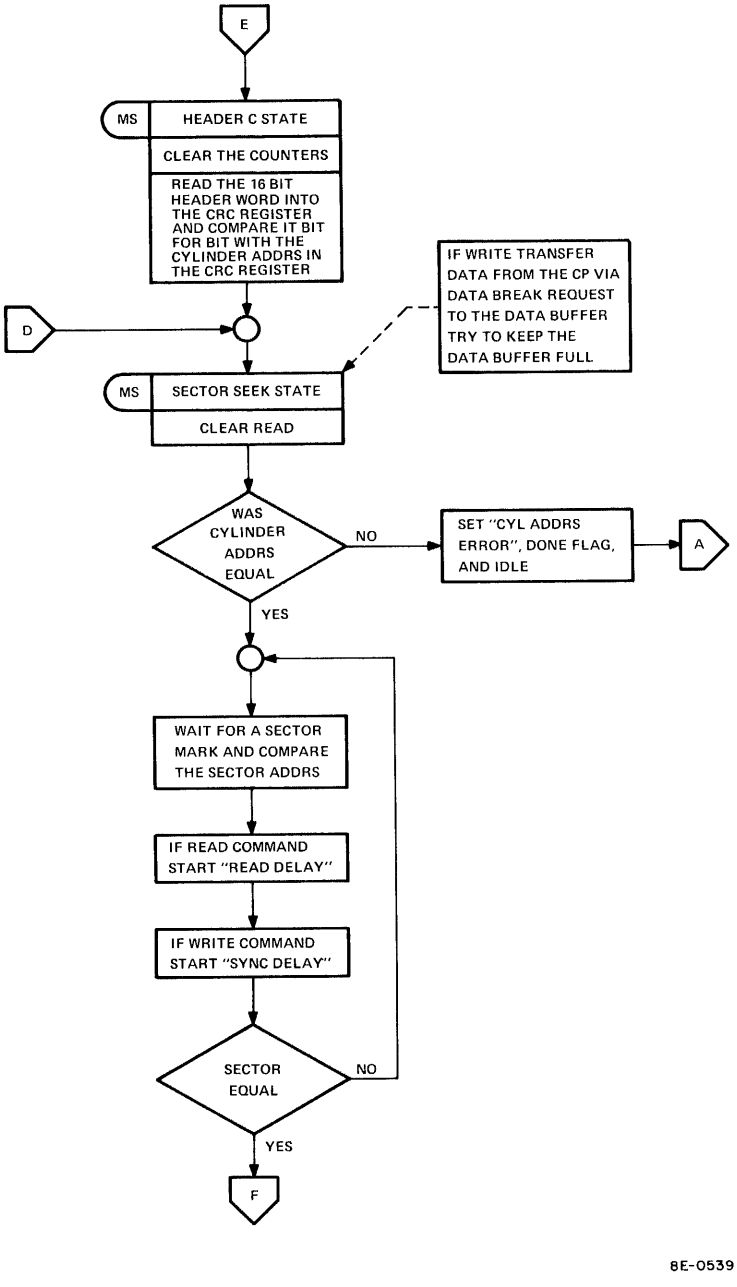


Figure 11-15 RK8-E Flow Diagram (sheet 3)

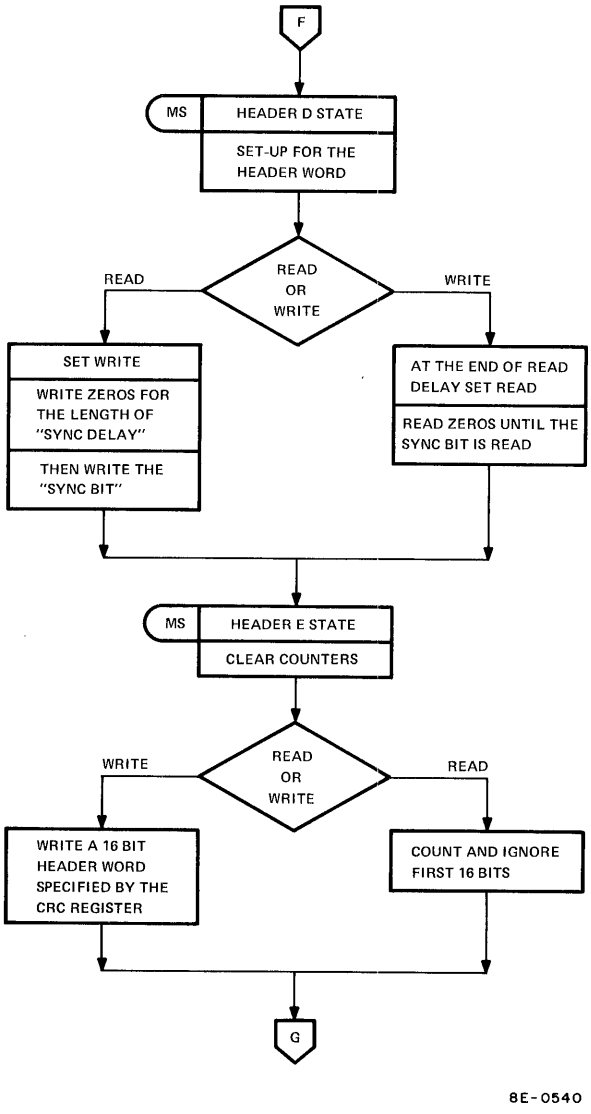


Figure 11-15 RK8-E Flow Diagram (sheet 4)

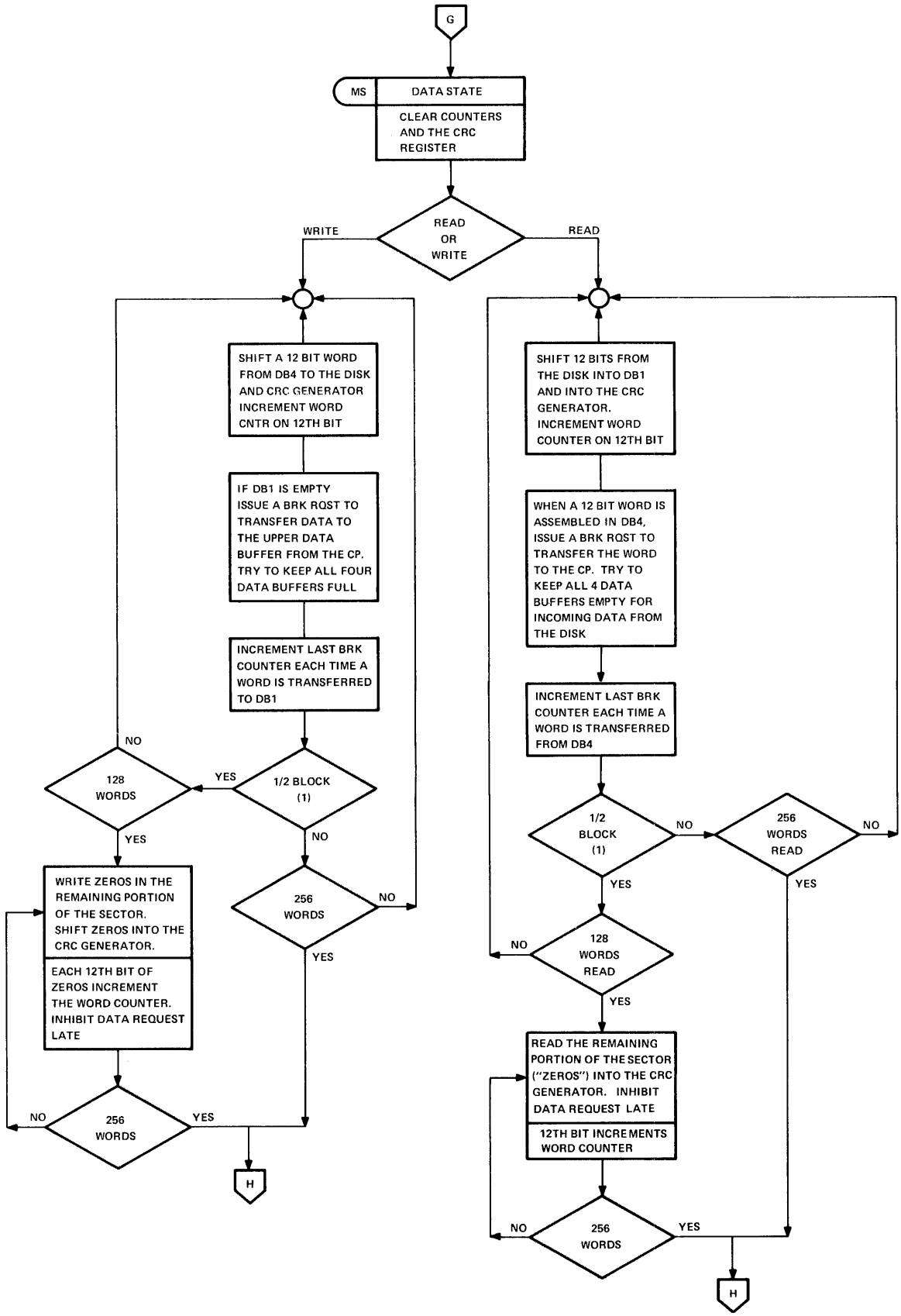


Figure 11-15 RK8-E Flow Diagram (sheet 5)

8E-0541

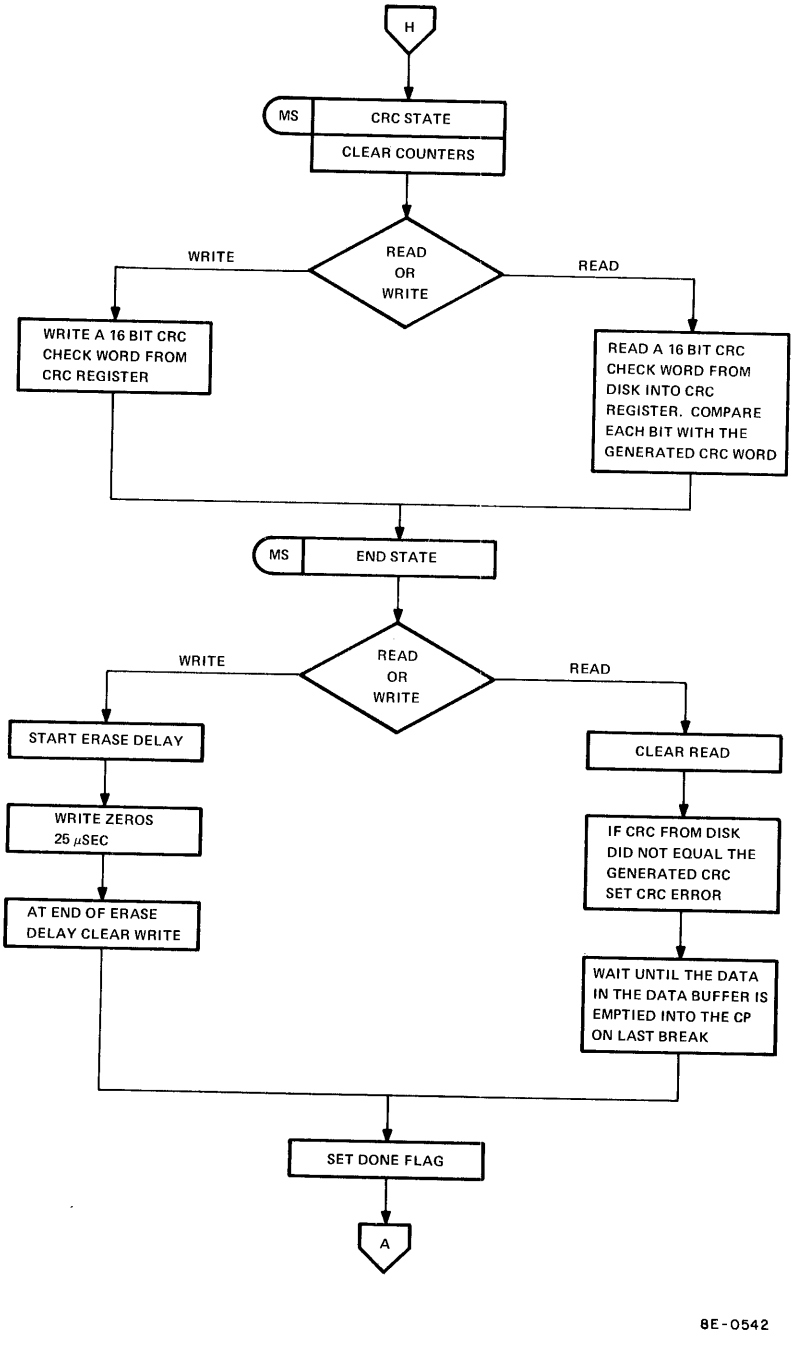


Figure 11-15 RK8-E Flow Diagram (sheet 6)

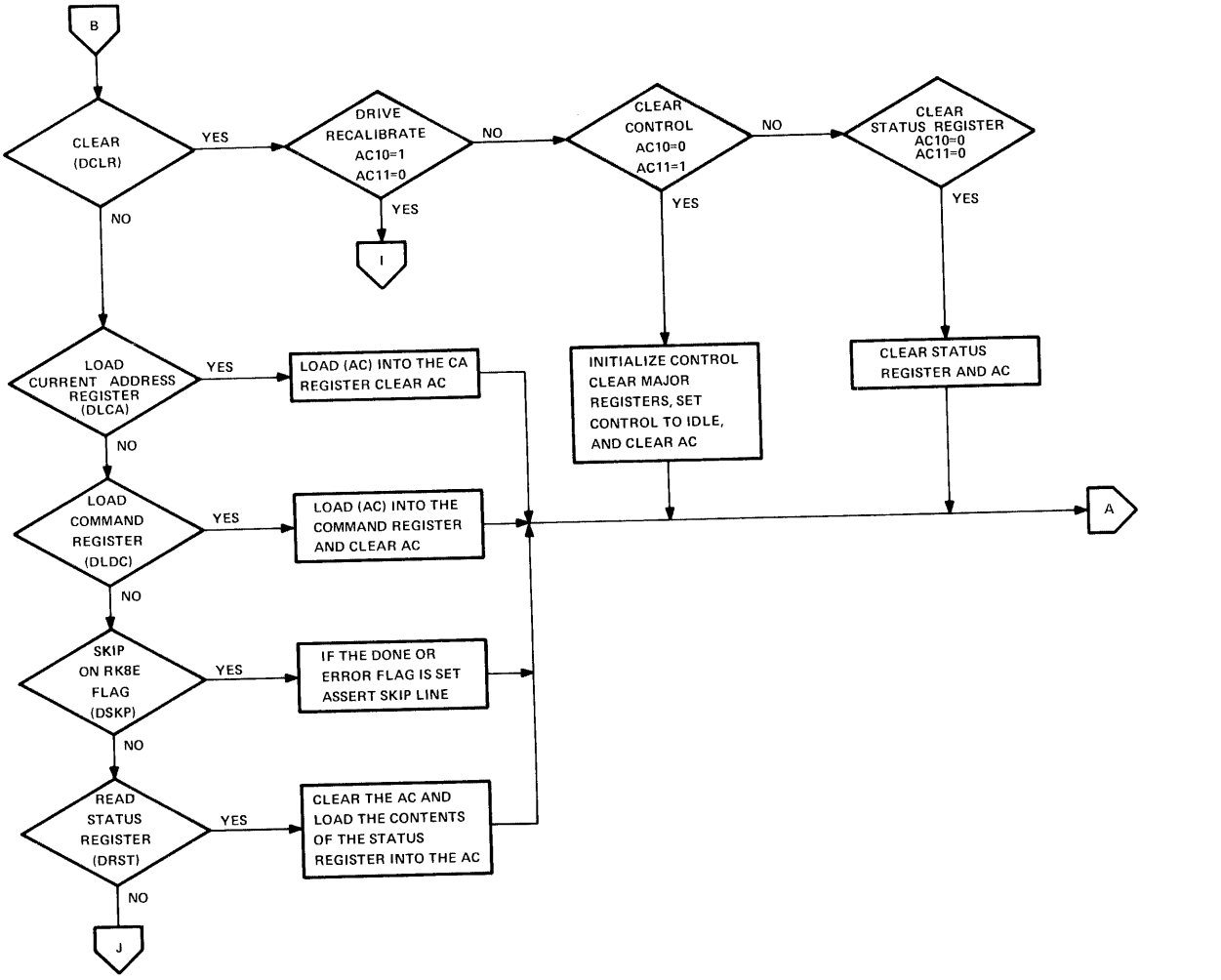


Figure 11-15 RK8-E Flow Diagram (sheet 7)

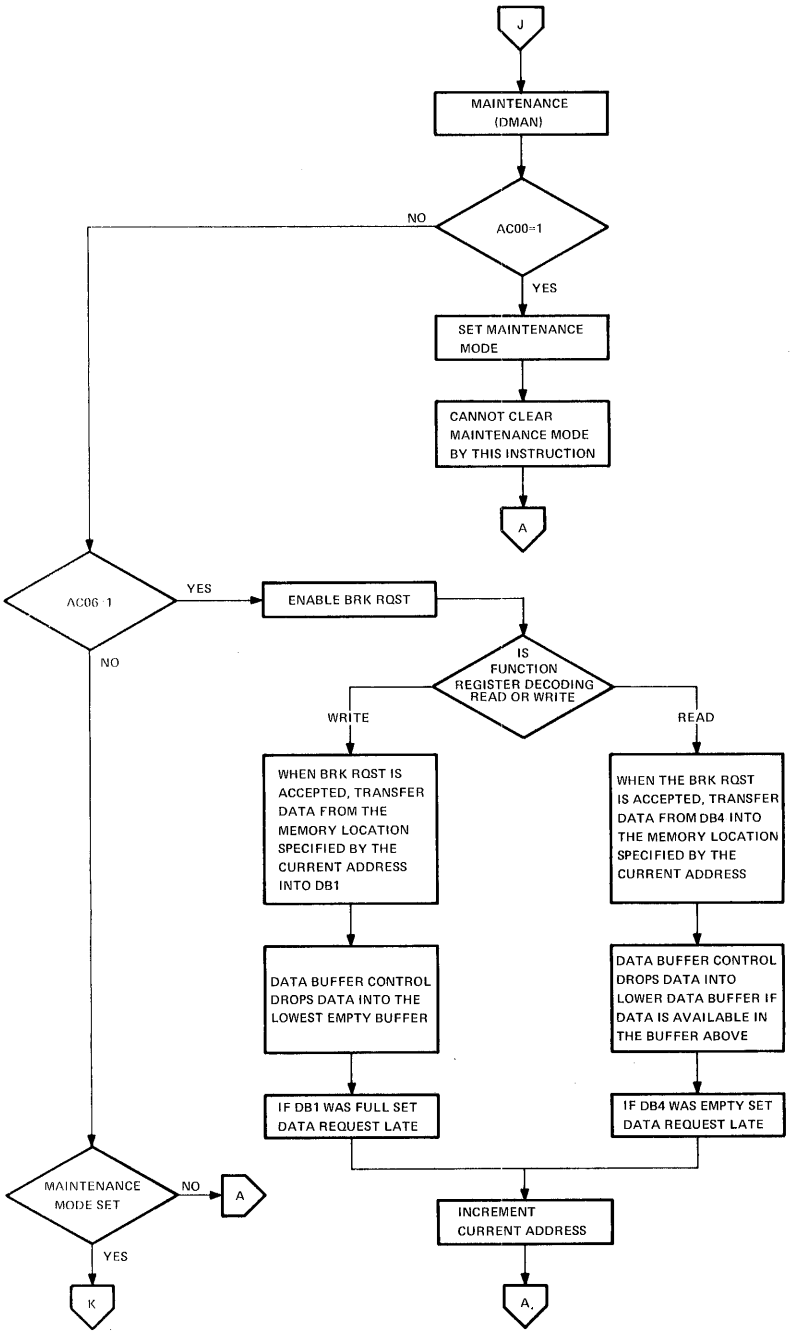


Figure 11-15 RK8-E Flow Diagram (sheet 8)

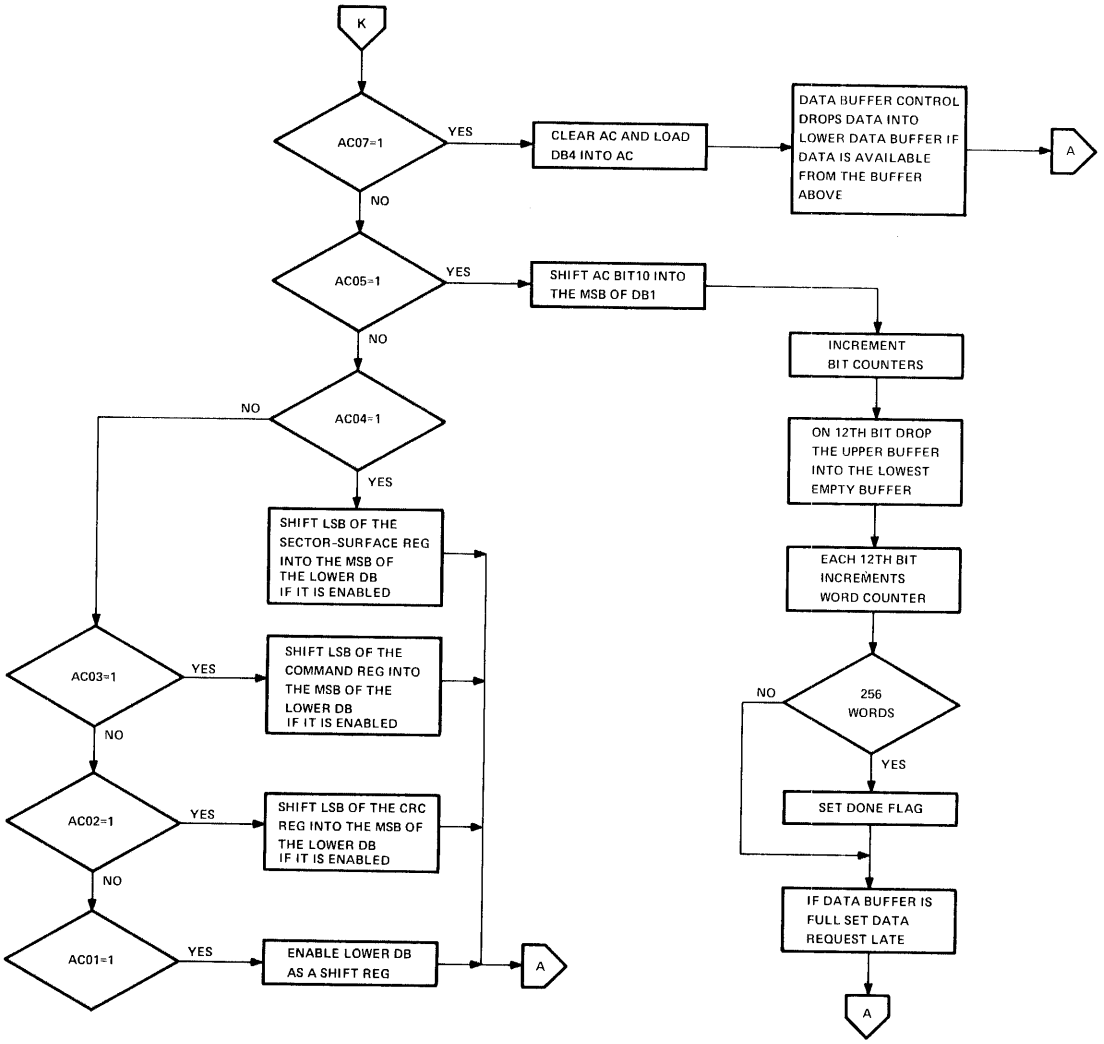


Figure 11-15 RK8-E Flow Diagram (sheet 9)

11.14.7.11 DATA State – The DATA state is used to transfer 256 data words from PDP-8/E memory to the disk drive during a write operation, or transfer 256 words of data from the disk drive to memory during a read operation. The data break control logic tries to keep the Data Buffer full during a write operation and tries to keep the Data Buffer empty during a read operation (the block diagram of the Data Buffer Register is discussed in Paragraph 11.14.5 and the block diagram of the Data Break control logic is discussed in Paragraph 11.14.4). The DATA state ends when 256 words have been transferred and the word counter asserts LAST WORD. If the RK8-E has been instructed to write 128 words, 128th word is asserted after 128 words (half block) have been transferred. The 128th word ends data transfer operations and the disk reads or writes zeroes until the full block of data (256 words) has been read or written. When LAST WORD is asserted, the RK8-E advances to the CRC state and clears the DATA state flip-flop.

11.14.7.12 CRC State – The CRC state (Figure 11-13) is used to write the CRC character, computed by the CRC Register (Figure 11-12) on the disk at the end of a sector during write operation. During read operations, the CRC character computed by the CRC Register during the data transfer is compared with the CRC character read from the disk. An Exclusive OR circuit on the CRC Register makes a bit-by-bit comparison of the CRC character read from the disk and the CRC character shifted out of the CRC Register. If the two characters are not equal, the CRC ERROR flag is set to indicate a CRC ERROR occurred during the data transfer. The program must check the Status Register to determine if the CRC ERROR set the ERROR flag. The Major States Register advances to the END state and clears the CRC state flip-flop when 16th BIT L is asserted.

11.14.7.13 END State – The END state is used by the read operation to allow the Data Buffer Register to be emptied by the single cycle data break, set the CRC ERROR flag if the CRC characters were not equal, clear READ, set the DONE flag, and return the RK8-E to the IDLE state (not busy). During a write operation, the controller starts ERASE DLY (Figure 11-13) and after 25 μs, WRITE is cleared, the DONE flag is set and the RK8-E is returned to the IDLE state. Note that there is no CRC character comparison during a write operation and no CRC ERROR should be detected.

11.14.8 Read/Write Delays, Clocks, and Counters

The read/write delays, clocks, and counters generate signals to assist the Major States Register in the control of disk operations and help to develop the disk format.

11.14.8.1 Write Data Clock – The write data clock (Figure 11-14) is a 2.88 MHz oscillator that is used to generate the WRT CLK pulses (Figure 11-2) during a write operation. The time between WRT CLK pulses (690 ns) is referred to as a bit cell, which is used to write data. The WRT DATA CLK and a SYNC bit, CRC DATA bit, or a DATA bit are written on the disk cartridge.

11.14.8.2 Write Sync Delay – Write sync delay (Figure 11-14) is a 140 μs delay that is started when a SECTOR MARK from the disk drive is detected during write operations. After 140 μs, WRT SYNC is asserted and the SYNC bit is written on the disk drive.

11.14.8.3 Read Delay – The read delay (Figure 11-14) is an 85 μs delay that is started when the SECTOR MK from the disk drive is detected, if the RK8-E is in the HEADER D state of a read operation. The 85 μs delay allows the control to wait for a SYNC bit before advancing to the HEADER E state. RD DLY asserts the RD gate to allow the RK05 to read.

11.14.8.4 Read Clock Data – The READ flip-flop (Figure 11-14) is set by RD DATA from the RK05 and cleared by RD CLK to generate the READ signal. The READ signal is used to enable READ data pulses to be applied to the Data Buffer Register. The READ data pulses are clocked into the Data Buffer Register by the RD CLK signal.

11.14.8.5 Counters – The RK8-E contains 4 counters (Figure 11-14) a divide-by-12-bit counter, a divide-by-16-bit counter, a divide-by-128- or 256-word counter and a break counter. The divide-by-12 counter counts the bits of data as they are read from the disk drive. Each time 12 bits (one word) are read, the word counter is incremented by 1. After 256 words are read, LAST WORD L is asserted to end a data transfer. If the HALF BLOCK bit (bit 5) in the Command Register is set, the 128th WORD signal is asserted after 128 words are read or written. This causes the RK8-E to stop data transfers between memory and the disk drive, but the disk drive continues to read or write all zeroes until LAST WORD L is asserted (256 words have been read or written). When LAST WORD is asserted, the data transfer is complete. The 16-bit counter asserts 16th bit when 16 bits are read from the disk or written on the disk. This is used when the PREAMBLE and CRC are read or written to count 16 bits instead of 12.

The break counter is incremented during TP2 time of a break cycle to count the single cycle data breaks. LAST BRK H is asserted after 128 or 256 words have been transferred to or from memory. There are 128 break cycles when the HALF BLOCK bit (bit 5) in the Command Register is a 1. Note that LAST BRK does not stop a read or write operation because 256 words must be read or written to end an operation. If HALF BLOCK is set (1), the last 128 words are all zeroes and not used.

11.14.9 Maintenance Logic

The maintenance logic (Figure 11-16) allows the program (software) to check the RK8-E operation. The program can transfer the contents of the Data Buffer Register, CRC Register, Command Register, and Surface/Sector Register to the AC or memory if the program executes the DMAN instruction. The operation performed when the DMAN instruction is executed by the program is determined by the contents of the AC (Table 11-14 and Figure 11-15). The maintenance logic allows the program to shift the contents of the CRC Register, Command Register, or Surface/Sector Register into the Data Buffer Register for transfer to the AC by a DMAN instruction or to memory by a data break. The shifting of registers is accomplished by the MAIN pulse, which is generated each time a DMAN instruction is executed. The program must keep track of the number of shifts and determine when to transfer the data to the AC or memory.

The maintenance logic checks all counters in the RK8-E control and allows data to be transferred from the AC to the Data Buffer Register.

The maintenance logic provides timing pulses to the major registers, data break control, and control sequencer to check these groups of logic. Note that the DMAN instruction disables the DLAG (GO) IOT and a clear operation must be performed to allow the program to continue after maintenance operations are executed by the program.

11.15 DETAILED LOGIC DESCRIPTION

The logic in the RK8-E is divided into functional groups for discussion purposes. The block diagram, Figure 11-9, and the flow diagram, Figure 11-15, should be used to understand the interaction of the logic, the signal flow within the RK8-E, and the input or output signals.

11.15.1 I/O Bus Interface

The I/O bus interface consists of the MD receivers, IOT decoder, interrupt and skip logic, and timing and control logic.

11.15.1.1 MD Receivers – The MD receivers allow data on the MD lines to be applied to the device select logic and I/O decoder when an RK8-E I/O instruction is executed by the program. The MD receivers also allow data on the MD lines to be applied to the Data Buffer Register during a write operation (MD → RD BUFF L and MD → RK L are asserted).

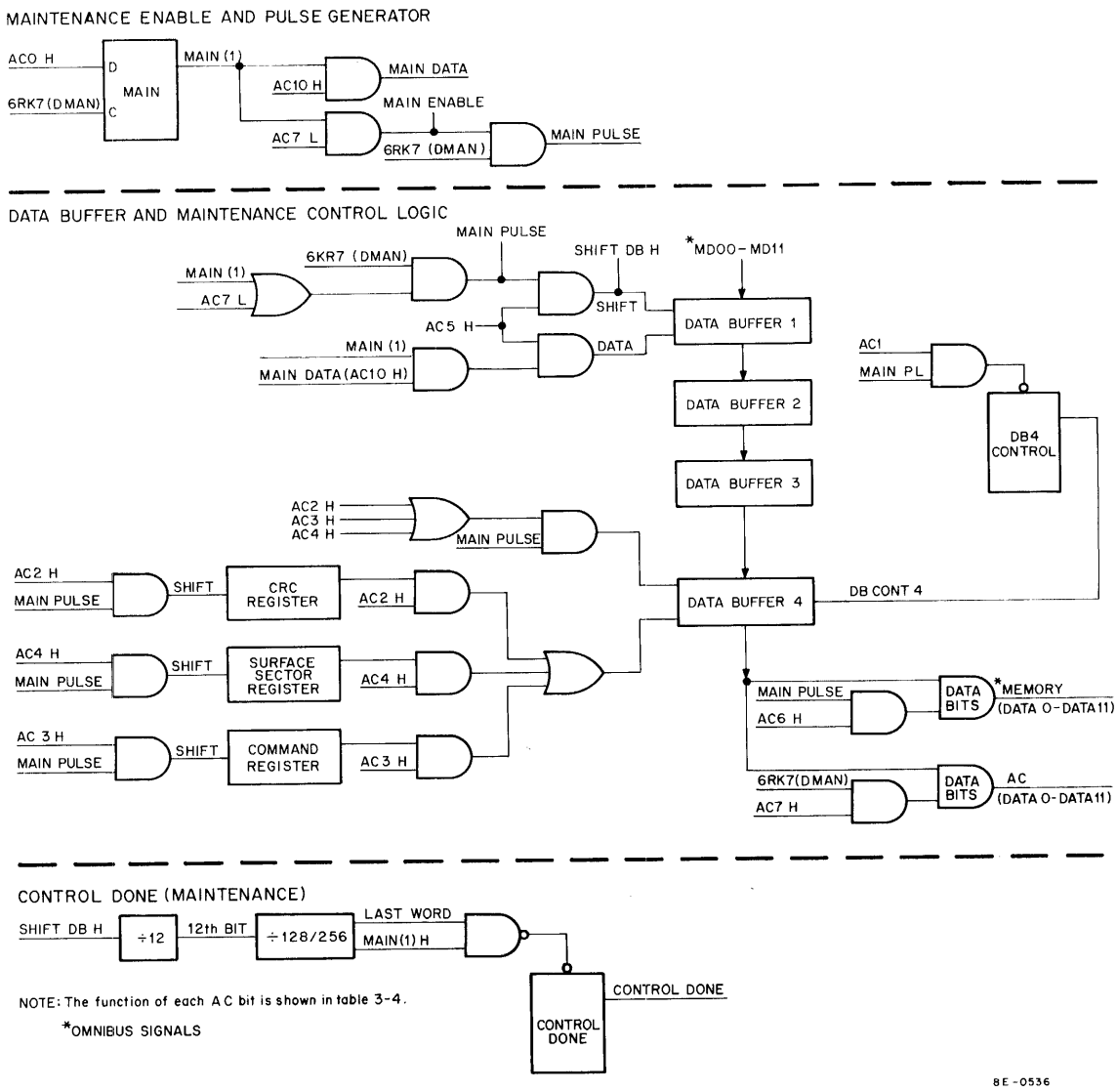


Figure 11-16 Maintenance Logic

11.15.1.2 IOT Decoder Logic – The IOT decoder (Figure 11-17) decodes MD bits (instructions) from the Memory Data Bus and generates signals to control the operation of the RK8-E. Bits MD3–11 are gated by MD → RK L when I/O PAUSE L is asserted by the processor. I/O PAUSE L is asserted anytime an IOT instruction is executed by the program. MD3–8 generates a signal DEVICE RK H and enables bits MD9–11 to be applied to the IOT decoder (an 8251 IC). The 8251 IC is a BCD to decimal decoder (see Volume I, Appendix A for truth table, logic diagram, and pin locations) that produces a low on one output line to indicate which instruction has been executed by the program. For example, MD9 low, MD10 and 11 high (100) produce a low on pin 9, which indicates a DLCA (6744) instruction was executed by the program. The jumpers on MD6–8 are used to select the device code for the RK8-E when multiple systems are installed (see Table 11-3 for jumpers to select the device codes). Internal I/O L is asserted by the DEVICE RK signal to prevent the processor from executing other IOT instructions while the RK8-E is executing an IOT instruction.

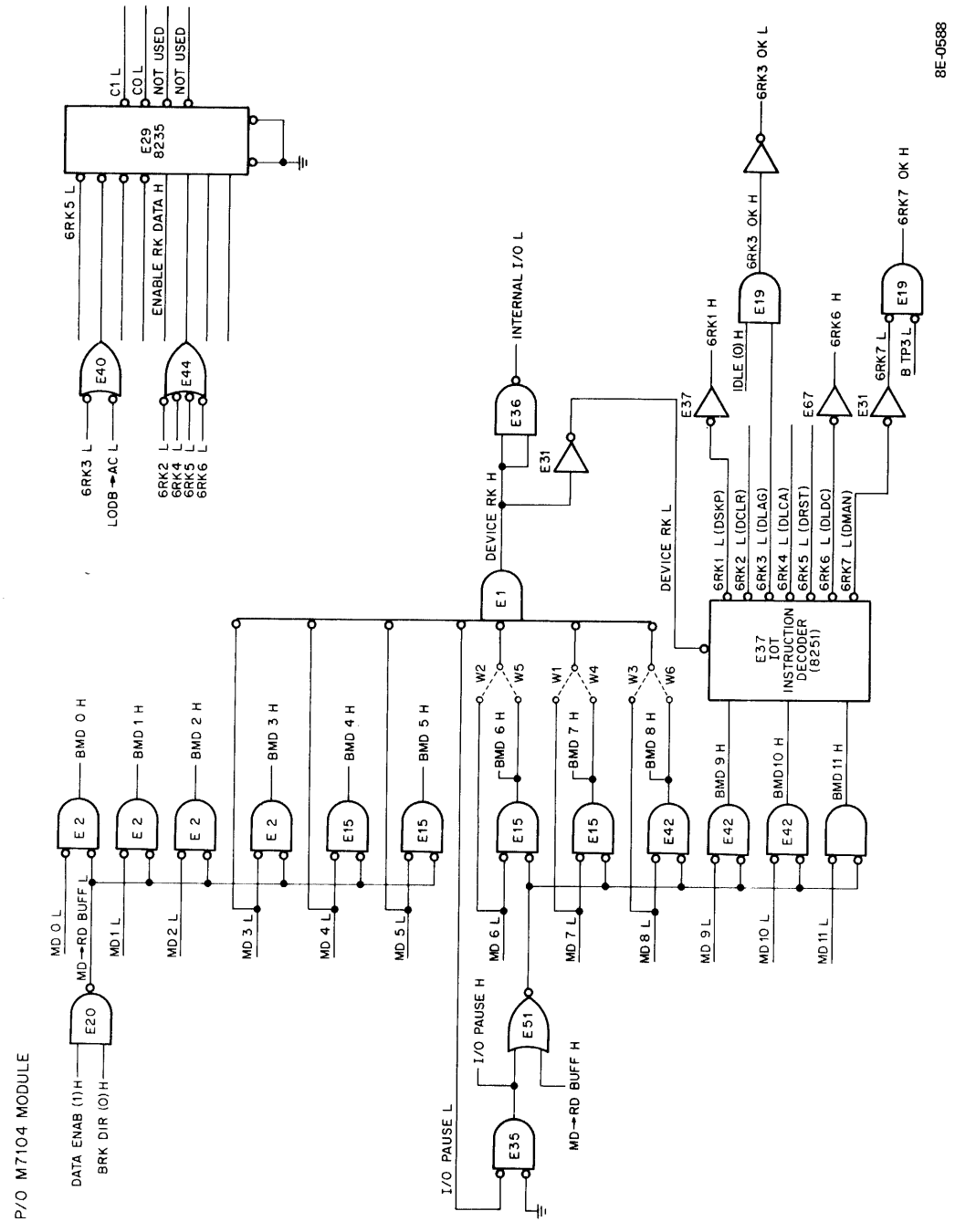


Figure 11-17 MD Receivers and IOT Decoder

11.15.2 Control Logic

11.15.2.1 C Line Select Logic – The C line select logic (Figure 11-17) controls the direction of data flow between the Data Bus and the AC and determines whether the AC is cleared or not. Table 11-15 shows the status of C0 and C1 to transfer data between the Data Bus and the AC using the RK8-E IOT instructions.

Table 11-15
C-Line Select Levels and Transfer Operations

Instruction	C0	C1	Transfer Operation
DCLR	Low	High	AC→ Data Bus, 0→ AC
DLAG	Low	High	AC→ Data Bus, 0→ AC
DLCA	Low	High	AC→ Data Bus, 0→ AC
DRST	Low	Low	Data Bus→ AC
DLDC	Low	High	AC→ Data Bus 0→ AC
DMAN	Low	High	AC→ Data Bus, 0→ AC

11.15.2.2 Time Pulse 3 (TP3) Logic – TP3 (Figure 11-18) is used throughout the RK8-E modules to enable gates for the execution of instructions. SHORT TP3 is used in the detection of a BUSY ERROR (Paragraph 11.15.4).

11.15.2.3 IDLE – The IDLE state indicates that the control is not busy; the control must be in the IDLE state to enable the execution of the 6RK2 (Figure 11-17), 6RK3, 6RK4, 6RK6, and 6RK7 (Figure 11-18) instructions.

11.15.2.4 Clear Logic – The logic of the RK8-E and/or the RK05 Disk Drives is cleared as follows:

a. By INITIALIZE during power up or if the CLEAR key is depressed on the PDP-8/E console.

b. The RK8-E logic is cleared by CLR ALL L if the 6RK2 (DCLR) instruction is executed by the program and AC bits 10 and 11 equal 01 (Table 11-11).

c. By CLR ALL L and CLR DRV CMD L if the 6RK2 (DCLR) instruction is executed by the program and AC bits 10 and 11 equal 10 (Table 11-11).

d. If a power failure is experienced and POWER OK H from the CPU goes low (Figure 11-18).

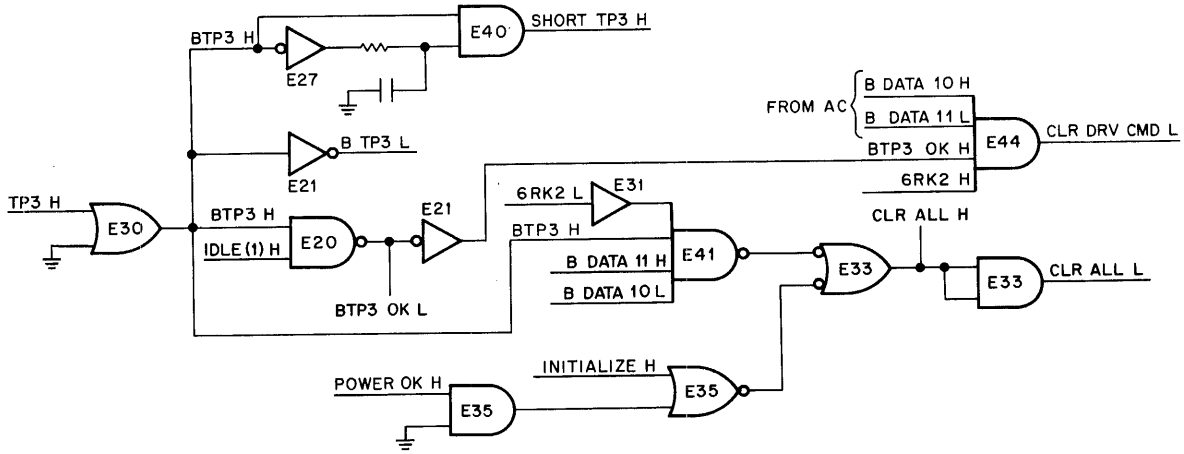


Figure 11-18 INITIALIZE, CLEAR ALL and Time Pulse 3 Logic

11.15.2.5 Interrupt Logic – INT RQST L (Figure 11-19) is asserted to interrupt the program if ENABLE INT H is asserted (bit 3 in the Command Register must be 1) and the ERROR or DONE flags are set.

11.15.2.6 Skip Logic – The SKIP line is grounded if the ERROR flag or the DONE flag is set and the DSKP instruction is executed by the program (Figure 11-19).

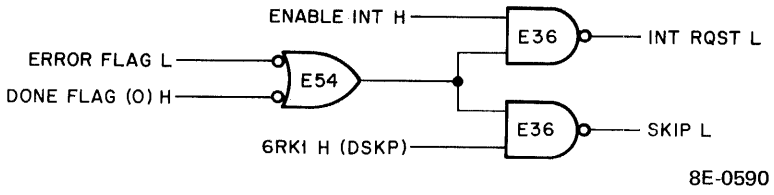


Figure 11-19 Interrupt and Skip Logic

11.15.3 Command Register

The Command Register (Figure 11-20) is loaded from the AC by a 6RK6 (DLDC) instruction. The Command Register (Table 11-13) is used to select a disk function, enable interrupts, read or write 128 words instead of 256, address extended memory, select a unit, and provide a bit (EXT CYL ADDRS) for cylinder addressing. The Command Register consists of three 8271 ICs (see Volume I, Appendix A for truth table, logic, and timing diagram) that contain 12-flip-flops, which are set or cleared by bits from the AC. The inputs to the flip-flops are enabled by DEVICE RK H, which asserts DATA ENAB L when the 6RK6 instruction is executed by the program to load the Command Register. The outputs of the Command Register are applied to a function decoder, unit select decoder, and the RK8-E control logic. Note that bit 11 is applied to the CRC Register to be used in cylinder addressing.

The contents of the Command Register can be shifted into Data Buffer 4 if the 6RK7 (DMAN) instruction is executed by the program and AC bit 3 is set. The MAIN PL H signal shifts the contents of the Command Register one bit position each time the DMAN instruction is executed by the program. The contents of the Command Register becomes a 12-bit serial word that is applied to DB4 in the Data Buffer Register as EXT CYL ADDRS H (Figure 11-25).

The Command Register is cleared anytime CLR ALL L is asserted (Paragraph 11.15.1.2).

11.15.3.1 Function Decoder – The function decoder (Figure 11-20) is an 74155 IC that decodes function bits 00–02 and determines what function is to be performed by the RK8-E and the selected RK05. The 74155 IC (see Section 7 for the truth table, pin locator, and logic diagram) is a 3-line to 8-line decoder that generates a low on one output line to select one of the RK8-E functions (Table 11-13). As an example, if F00 is high and F01 and F02 are low, the function is to seek a cylinder, check the HEADER, and write data on the specified sector.

11.15.3.2 Unit Select Decoder – The unit select decoder (Figure 11-20) decodes the unit select bits (UNIT SEL 0 and UNIT SEL 1) from the Command Register to select one of the RK05 Disk Drives. The unit select decoder is a 74155 IC that decodes the two unit select bits and grounds one of the unit select lines. The 74155 IC (see Section 7 for truth table, pin locator, and logic) is used as 2-line to 4-line decoder that grounds one of the unit select lines and selects one of the RK05 Disk Drives. As an example, if both unit select bits are high (11), pin 4 on the 74155 IC is grounded and drive 3 is selected for an operation.

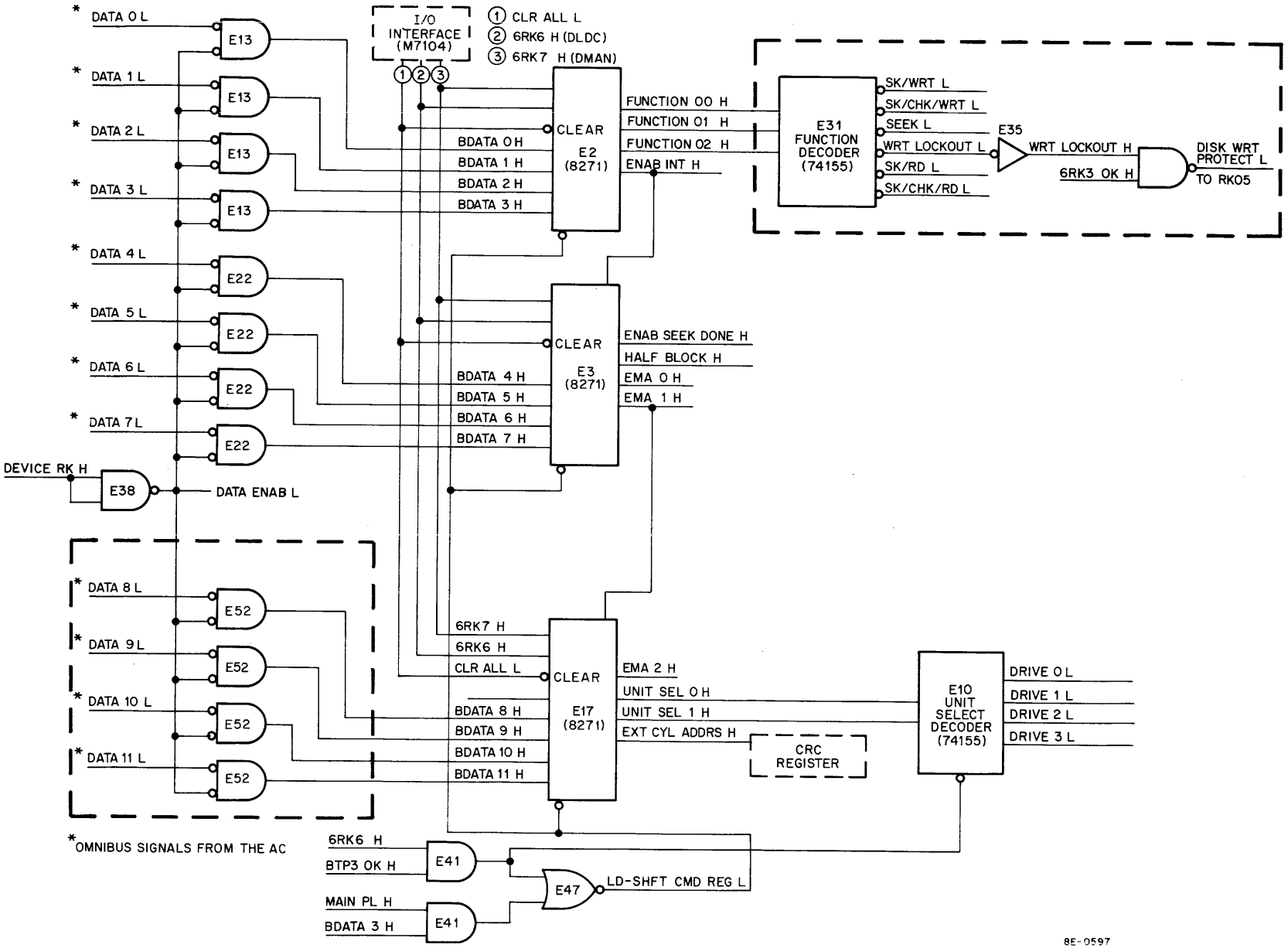


Figure 11-20 Command Register

11.15.4 Status Register

The Status Register (Figure 11-21) provides current status of the RK8-E and the selected RK05 Disk Drive to the program. The contents of the Status Register are transferred to the AC for evaluation by the program if the 6RK5 (DRST) instruction is executed by the program (Figure 11-27). The flip-flops that make up the Status Register supply inputs to the output data multiplexer (Figure 11-27) and are transferred to the AC via the Data Bus by the 6RK2 instruction. The flip-flops in the Status Register provide 1s (set) or 0s (cleared) to indicate error conditions.

11.15.4.1 TRANSFER DONE – The TRANSFER DONE flag (AC0) is set (Figure 11-21) during maintenance operations as follows:

a. By the LAST WORD PL H signal at the end of a data transfer operation. LAST WORD PL H is asserted after 256 words have been transferred. Note, if a half block or 128 words are transferred, the TRANSFER DONE flag is not set until 256 words have been read or written.

b. By IDLE (1) H if the IDLE flip-flop is set by the detection of an error during an operation or at the completion of an operation.

c. By IDLE (1) H and RDY S/R/W if bit 4 (ENABLE SEEK DONE) is set.

11.15.4.2 HEADS IN MOTION – HEADS IN MOTION H (AC1) is asserted when the read/write heads on the selected drive are in motion (Figure 11-21).

11.15.4.3 SEEK FAIL – SEEK FAIL (AC3) is set (1) when the DSK FAIL L signal from the RK05 is asserted (Figure 11-21). DSK FAIL is asserted by the selected disk drive if it fails to seek the cylinder address specified by program. A recalibrate operation must be executed by the program to clear this error condition.

11.15.4.4 DRIVE STATUS ERROR – The DRIVE STATUS ERR (AC6) is set when the selected disk drive is not ready (i.e., not turned on) by FILE READY L from the RK05 (Figure 11-21). Some action must be taken by the operator to clear this bit, i.e., power up the affected RK05.

11.15.4.5 CONTROL BUSY ERROR – CONTROL BUSY ERROR is set (1) if the program tries to do a DLAG, DCLR with AC=10, DLDC, or DLCA instruction while the IDLE flip-flop is cleared (Figure 11-21). Note that the control is busy unless the IDLE flip-flop in the Major States Register is set. This error occurs most often when new programs are debugged, a rewrite of the program or routine that caused the error should eliminate the problem.

11.15.4.6 TIME OUT ERROR – TIME OUT ERROR is set (1) if the control has been busy for more than 280 ms (Figure 11-21) or more than 7 revolutions of the disk cartridge. The DSK INDEX MK L signal is asserted once for each revolution of the disk and applied as the clock input to the 74193 IC (see Section 7 for pin locations and logic diagram). The 74193 IC is a 3-bit binary counter that sets the TIME OUT ERR bit in the Status Register if the Major States Register remains in some state other than IDLE for 280 ms. The binary counter is cleared each time the Major States Register goes to the IDLE state and starts a new countdown each time the IDLE flip-flop is cleared.

11.15.4.7 WRITE LOCK ERROR – WRITE LOCK ERROR (AC7) is set if the program tries to do a write operation on a disk drive that has been write protected (Figure 11-21). If the selected disk drive has been write protected, DSK WRT STATUS L from the write protected disk drive is high and the WRT LOCK ERR flip-flop sets when the WRT CMD is issued by the program. The WRT LOCK ERR flip-flop in the RK8-E is cleared by LD DISK ADDRS H if the affected disk drive is deselected. The WRT PROT switch of the affected disk drive must be depressed to allow data to be written on any drive that has been write protected. Note that a disk drive is write protected by programming the write protect function or by depressing WRT PROT switch on the RK05 (Table 11-13).

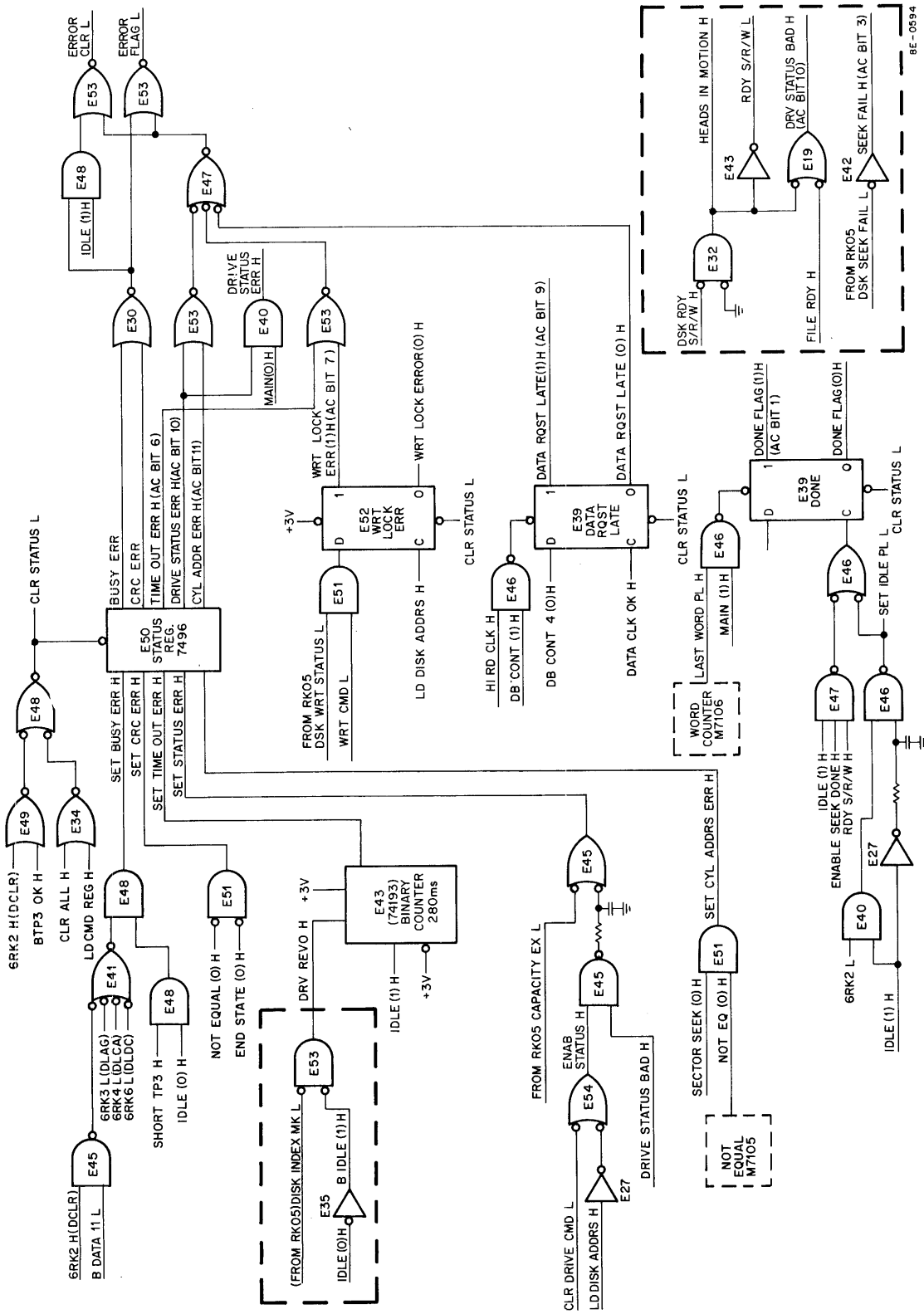


Figure 11-21 Status Register

11.15.4.8 CRC ERROR – The CRC ERROR (AC8) bit is set if the CRC character read from the disk drive does not equal the CRC computed by the CRC Register during a read operation. The CRC character read from the disk during the CRC state is compared bit-by-bit with the CRC character computed by the RK8-E (Figure 11-12). If the CRC characters are not equal, NOT EQUAL (0) H is asserted low and when the Major States Register enters the END state the CRC ERROR bit is set.

11.15.4.9 DATA REQUEST LATE – DATA REQUEST LATE (AC9) is set if the processor does not respond to a BRK RQST within 22.5 μs. If the processor does not respond in time, the Data Buffer Register is emptied during a write operation or filled during a read operation. This causes one or more data words to be lost. The DATA RQST LATE flip-flop (Figure 11-21) is set by one of the following:

a. HI RD CLK and DB CONT 1 (H) during a read operation. This condition indicates the Data Buffer Register is full and there is no room for new data.

b. DATA CLK OK H and DB CONT 4 (0) H during a write operation. This condition indicates the Data Buffer Register is empty and there is no data to be written on the disk cartridge.

11.15.4.10 DRIVE STATUS ERROR – DRIVE STATUS ERROR (AC10) is set if DRIVE STATUS BAD H is asserted and the program initiates a load disk address (DLAG), attempts a clear drive command operation, or if the disk capacity is exceeded (disk address greater than 312_8). The conditions that cause DRIVE STATUS BAD H to be asserted are given in Table 11-12, bit 10.

11.15.4.11 CYLINDER ADDRESS ERROR – CYLINDER ADDRESS ERROR (AC11) is set if the HEADER word of a sector does not agree with the cylinder address sent to the disk drive. The HEADER word is read from a sector during the HEADER C major state and compared with the cylinder address in the CRC Register. If the HEADER word and the cylinder address in the CRC Register (Figure 11-12) are NOT EQUAL, CYLINDER ADDRS ERR is set and the TRANSFER DONE flag sets.

11.15.5 ERROR Flag

The ERROR flag is asserted by any of the following errors, which also set bits in the Status Register.

a. BUSY ERR
b. CRC ERR
c. TIME OUT ERR
d. DRIVE STATUS ERR
e. CYL ADDRS ERR

If the ERROR flag is set and the DSKP instruction is executed by the program, the SKIP line is grounded. This causes the program to skip an instruction (Figure 11-19). If the INTERRUPT ENABLE bit in the Command Register (bits) is a 1 and the ERROR flag is set, the program will be interrupted by an INT RQST (Figure 11-19).

11.15.6 Sector Address Comparator

The sector address comparator (Figure 11-22) compares the address in the Surface Sector Register with the sector address read from the selected disk drive during the HEADER C major state. The comparator is a 7485 IC (see Section 7 for truth table, pin locator, and logic diagram) that asserts SECTOR EQ H when the two 4-bit inputs are equal.

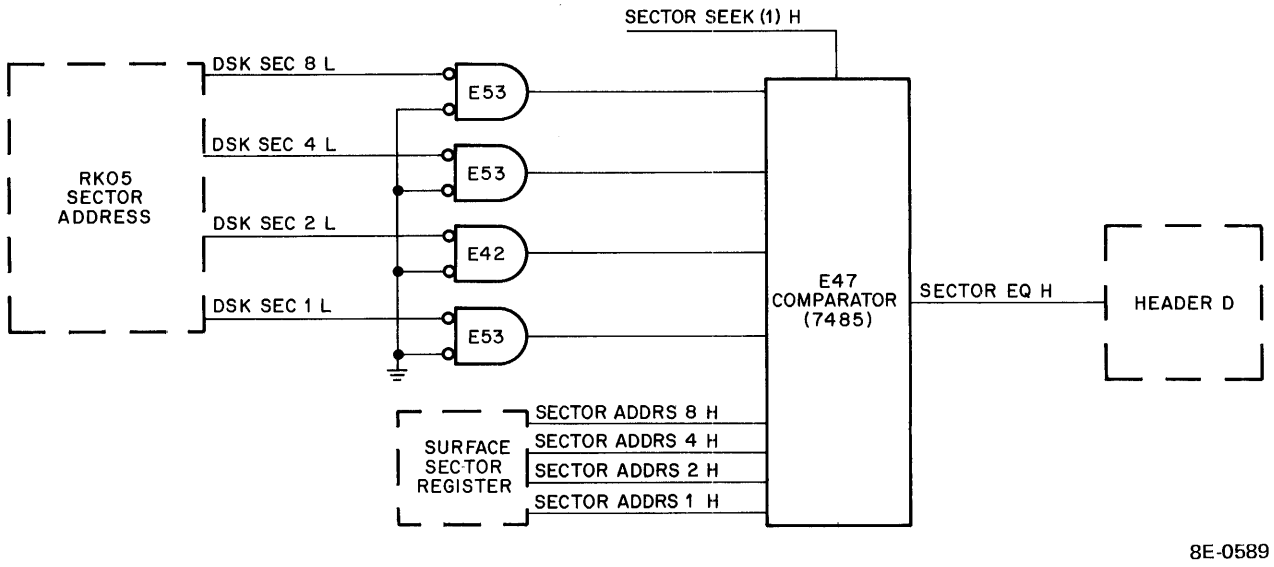


Figure 11-22 Sector Address Comparator

11.15.7 Data Break Control Logic

The data break control logic (Figure 11-23 and 11-24) enables the RK8-E to assume control of the CPU Major Register gating and directly address via the Current Address Register, memory locations associated with a data transfer. The priority network compares the priority of the RK8-E with other peripherals making BRK RQST at the same time. If the RK8-E has the highest priority, the controller asserts signals indicating the RK8-E has accepted the request at INT STROBE time. When the RK8-E asserts BREAK, the single cycle data break is started, a data word is transferred to or from the address indicated by the Current Address Register. If the transfer is from the RK05 to memory, the data is applied to the Data Bus (DATA0–DATA11) by the transfer control logic. Data transfers from memory to the RK05 are taken from the MD lines (MD00–MD11) and transferred to the RK05 via the Data Buffer Register.

11.15.7.1 Current Address Register – The Current Address Register (Figure 11-23) and the EMA bits (EMA0–EMA2) are used to select a location in memory to be used in a data transfer. The Current Address Register is loaded with the address of the first memory location to be used in a data transfer when the 6RK4 (DLCA) instruction is executed by the program. The RK8-E must be in the IDLE state (control not busy) when the CA Register is loaded. DATA ENABLE (1) H (Figure 11-24) is asserted at TP4 time to increment the CA Register and sequentially select locations in memory for data transfers. The contents of the CA Register are applied to the OMNIBUS when MAK (1) H is asserted during a data break.

The CA Register consists of three DEC 74161 ICs (see Section 7 for timing diagram, logic diagram, and pin locations). The DEC 74161 IC is a presetable binary counter with clock input for incrementing. Note that the clock input and the control input (load) must be asserted to load the CA Register.

The EMA bits (EMA0–EMA2) from bits 6 through 8 of the Command Register are applied to the OMNIBUS when DATA ENAB (1) H is asserted by the control logic (Figure 11-24) to select a memory field (0–7). The EMA bits are not incremented and the Command Register must be changed by the program to change memory fields.

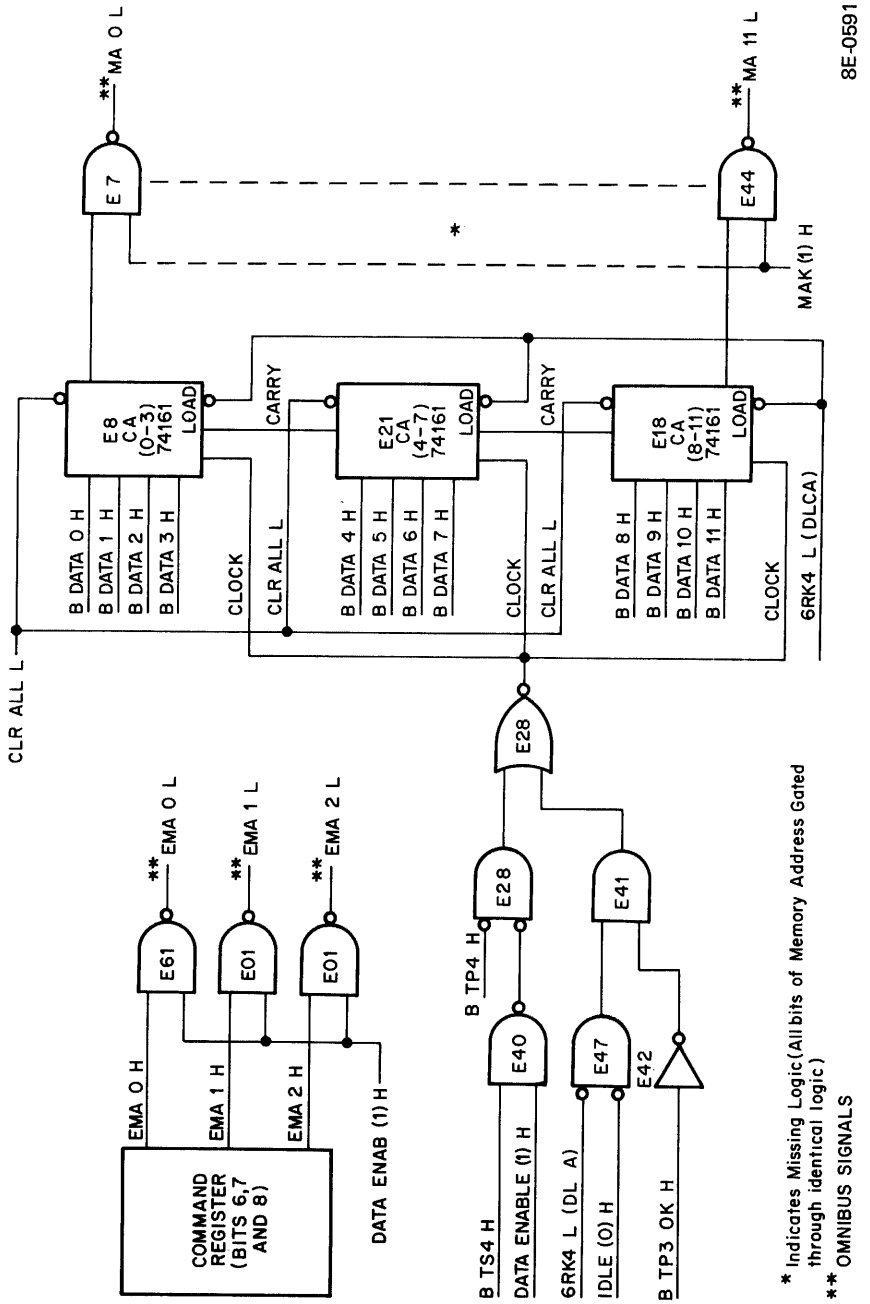


Figure 11-23 Current Address Register

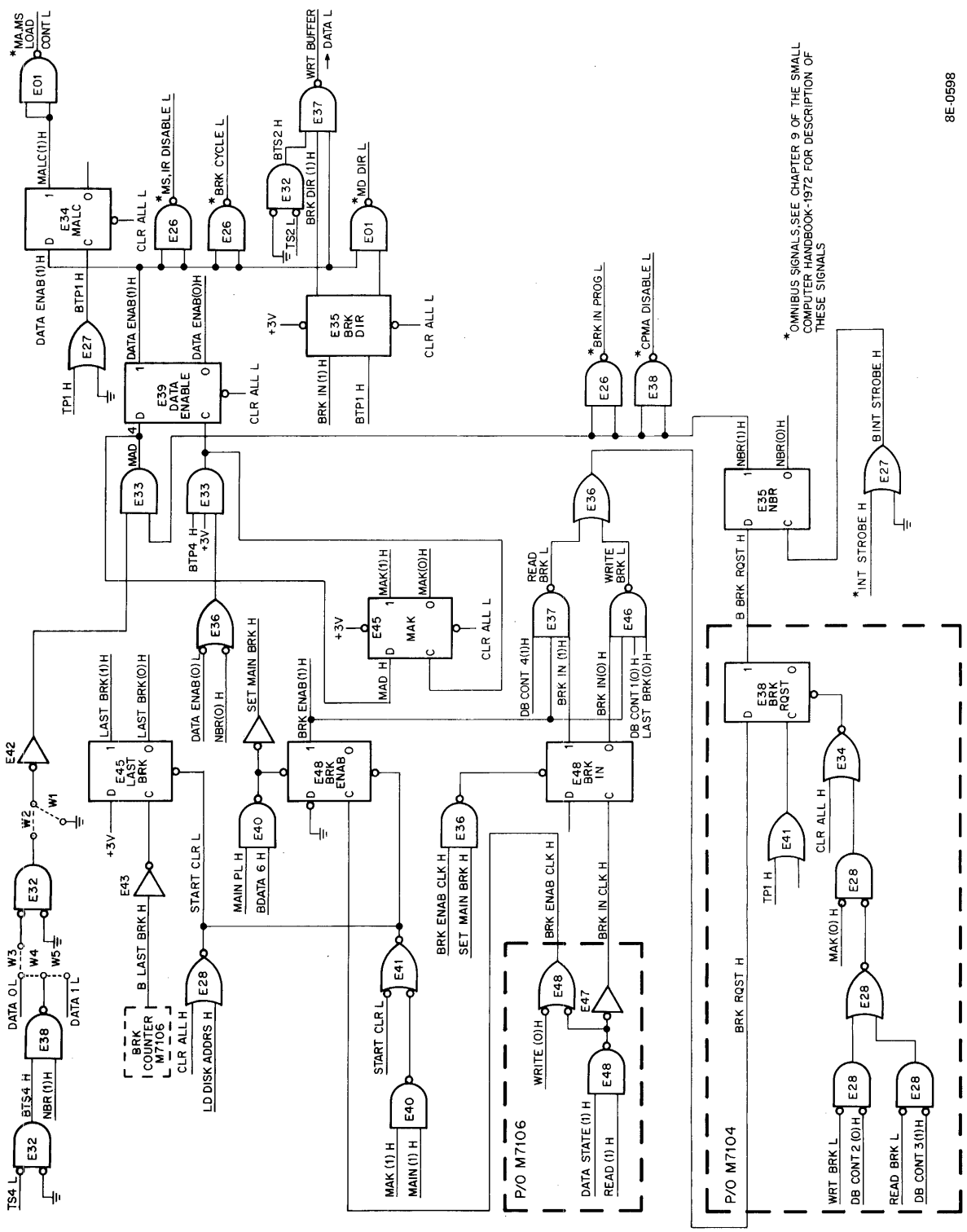


Figure 11-24 Single Cycle Data Break Control Logic

11.15.7.2 Data Transfer Control Logic – The data transfer control logic (Figure 11-24) determines the direction and type of data transfer. The BRK ENAB flip-flop is set immediately if a write operation is initiated or when the Major States Register enters the DATA state during read operations. BRK ENAB (1) H supplies an input to E37 and E46 to allow a BRK RQST if other conditions are met. BRK IN is set during read operations and cleared during write operation to enable either E37 during read breaks or E46 during write breaks. During read operations, E37 is enabled by DB CONT4 (1) H and BRK IN (1) H to assert READ BRK L and initiate a BRK RQST at TP1 time. DB CONT4 (1) H is asserted (high) when DB4 in the Data Buffer Register is full. A new BRK RQST is made each time DB4 is filled until the data transfer is complete. BRK RQST is cleared during a read break when MAK (0) H is low if DB3 in Data Buffer Register is empty. Note that DB CONT3 (1) H is low when DB3 is empty which enables E28 and allows BRK RQST to clear at TP4 time if the MAK flip-flop is set. If DB3 is full, BRK RQST is not cleared and a new break cycle is started to transfer new data. The data in DB3 is transferred to DB4 as soon as DB4 is empty; thus, the data in DB3 is in DB4 when the next break cycle starts.

During write operations, E46 is enabled to assert WRT BRK L if BRK IN is cleared, BRK EN is set, LAST BRK (0) H is asserted, and DB1 in the Data Buffer Register is empty. DB CONT1 (0) H is true to enable E46 and make a BRK RQST at TP1 time when DB1 is empty. BRK RQST is cleared at TP4 time if MAK is set to negate MAK (0) H (low) and DB2 is full. If DB2 is empty, DB CONT2 (0) H disables E28 and the BRK RQST flip-flop is not cleared. If DB2 is empty, the data in DB1 is transferred immediately to DB2 and a new break cycle is started to fill DB1 if the RK8-E has the highest priority.

The data transfer control logic tries to keep the Data Buffer Register full during a write operation and empty during a read operation via the single cycle data break.

11.15.7.3 Priority Logic – The RK8-E must have the highest priority to allow a break cycle when a BRK RQST is made. DISK PRIORITY H (Figure 11-24) is asserted by a ground (W1 installed) on the input of E42 if the RK8-E is assigned the highest priority (0). DATA 0 L (highest priority) or DATA 1 L are asserted by the output of E38 when the NBR flip-flop is set to prevent other peripherals from doing a break cycle when the RK8-E has priority. If priority 1 is selected for the RK8-E, jumper W3 is installed. When a peripheral with priority 0 makes a BRK RQST, E32 is enabled to supply a high to the input of E42. A high on E42 negates PRIORITY H and the RK8-E must wait until DATA 0 L is negated by the peripheral with the highest priority.

Thus, when DISK PRIORITY H is asserted and a BRK RQST is made (NBR is set), a break cycle is started. NBR is set at INT STROBE time if BRK RQST is set. When NBR sets, CPMA DISABLE L and BRK IN PROG L are asserted on the OMNIBUS to start a break cycle. The OMNIBUS signals are explained in Chapter 10 of the *Small Computer Handbook – 1973.*

11.15.7.4 CPU Control Logic – The CPU control signals are asserted by the RK8-E at TP4 time if DISK PRIORITY H is asserted. DATA ENABLE is set at TP4 time to assert BRK CYCLE L and MSIR DISABLE L (see Chapter 10 of the *Small Computer Handbook – 1973* for description of signals). BRK DIR is set during read breaks by BRK IN (1) H to assert MD DIR L. MD DIR L is asserted to allow data to be transferred from memory to the RK8-E (write) and is negated to transfer data from the RK8-E to memory.

The next TP1 pulse after DATA ENABLE is set causes the MAK flip-flop to set and assert MA, MS LOAD CONT L. This inhibits loading of the MA, MS Registers by the processor and allows the contents of the CA Register applied to the MA lines to select a location in memory for this data transfer.

MAK is set at the same time as DATA ENABLE. The clear side of MAK is used to clear BRK RQST at the end of a BRK cycle if DB2 is full during write operations or DB3 is empty during read operations.

The LAST BRK flip-flop is set and B LAST BRK H from the break counter is asserted when the data transfer is completed. The zero side of LAST BRK disables E46 and removes WRITE BRK L from the BRK RQST flip-flop to stop write breaks. READ BRK L is negated when E37 is disabled by the loss of DB CONT4 (1) H to stop read breaks.

The data break control logic is cleared when the load disk address (DLAG) instruction is executed by the program or by CLR ALL L which is asserted when the DCLR instruction is executed.

11.15.8 Data Buffer Register and Control Logic

The Data Buffer Register (Figure 11-25) and its associated control logic (Figure 11-26) has the following functions:

a. During read operations, serial data is shifted into DB1 by the RD CLK pulses and transferred to DB4 via DB2 and DB3 as 12-bit parallel words. The 12-bit words are then transferred to memory by the single cycle data break. The single cycle data break control logic tries to keep the Data Buffer Register empty so that there is space for temporary storage of data transferred from the disk.

b. During write operations, a 12-bit parallel word is transferred from memory to DB1. The 12-bit word is transferred to DB4 via DB2 and DB3. The 12-bit word is shifted out of DB4 by the WRT BUFF SHFT L signal. The output of DB4 is supplied to the write control logic as 12 bits of serial data to be written on the disk between clock pulses (Figure 11-2).

c. During maintenance operations, the contents of CRC Register, Command Register, or the Surface/Sector Register are shifted into DB4 by the LO MAIN SHFT L pulse. The DMAN instruction is used to generate the LO MAIN SHFT L signal (Table 11-14). The contents of DB4 are transferred to the AC via the Data Bus by the DMAN instruction. Thus, the program can read and evaluate the contents of the Command Register, CRC Register, and Surface/Sector Register during maintenance operations or error check routines. The flow diagram in Figure 11-15 illustrates these maintenance operations, and Table 11-14 gives the AC bit requirements to accomplish the maintenance operations.

11.15.8.1 Data Buffer Register Control Logic – The Data Buffer Register control logic (Figure 11-26) provides control signals to the Data Buffer Register (Figure 11-25). The DB control logic consists of a Control Register and a DB clock with gating logic to aid in the control operations. The Control Register consists of four J-K master slave flip-flops with clock inputs. The unique features of these flip-flops are: 1) a clock pulse will not cause any transition in the flip-flop if neither the J or K inputs are enabled during the clock pulse and 2) if both the J and K inputs are enabled during the clock pulse, the flip-flop will complement (change states). The J or K inputs are enabled only when the input is of a state different from the present condition of the flip-flop, i.e., if DB1 is in a 1 state only a 0 state input will cause the flip-flop to change state. When the flip-flops are in a 1 state, the Data Buffer Register associated with that flip-flop is considered to be full, i.e., if DB1 control is in a 1 state, DB1 is full. When the flip-flops are in the 0 state, the registers are considered to be empty.

The DB clock is made up of one 74123 IC (see Volume I, Appendix A for logic diagram and pin locations). This IC is a dual one-shot multivibrator that outputs a pulse of a specified duration each time the input is enabled. The duration of the output pulse is determined by an external capacitor and resistor, i.e., R7 and C38.

DB CLK H out of the first 74123 IC is a 50 ns pulse that is asserted when one of the inputs to E6 are enabled to cause the input to make a high-to-low transition. One of the inputs to E6 is enabled when one of the Data Buffer Control flip-flops is to be loaded. The pulse out of the first 74123 triggers the second 74123 IC and disables the input to the first IC, also disabling the 0 → DB4 signal for 150 ns. This allows the completion of a data transfer before a new DB CLK pulse is generated. Without this delay, the Control Register would attempt to load a register before the output of a register has been transferred into another register (i.e., DB2 → DB3) or to the Data Bus (i.e., DB4 → Data Bus). Note that the clock pulse is initiated only when the correct conditions exist to load one of the Data Buffer Registers and is disabled by the clear side of the second IC to allow time for a data transfer (register-to-register or register-to-disk or processor).

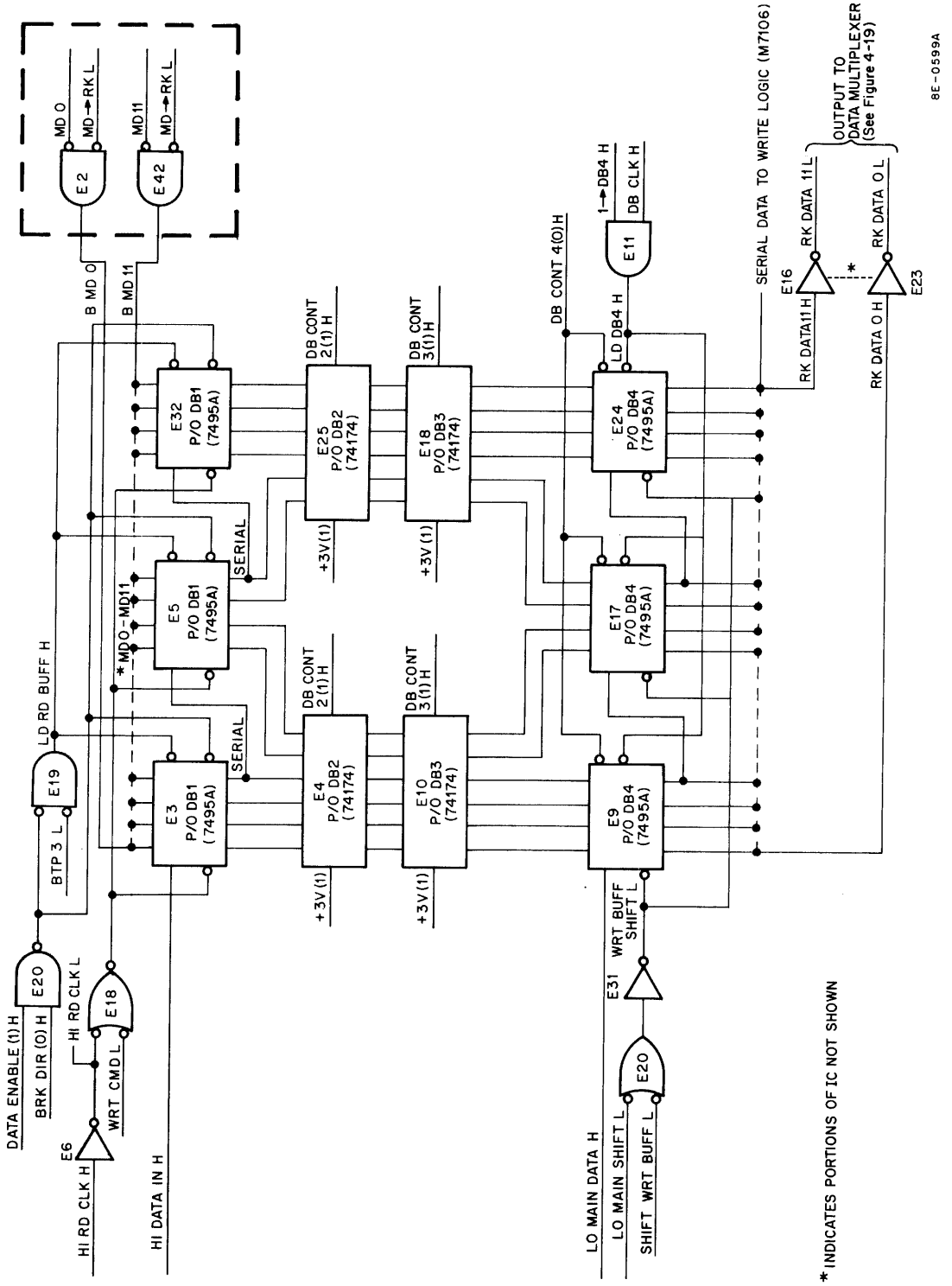


Figure 11-25 Data Buffer Register (sheet 1)

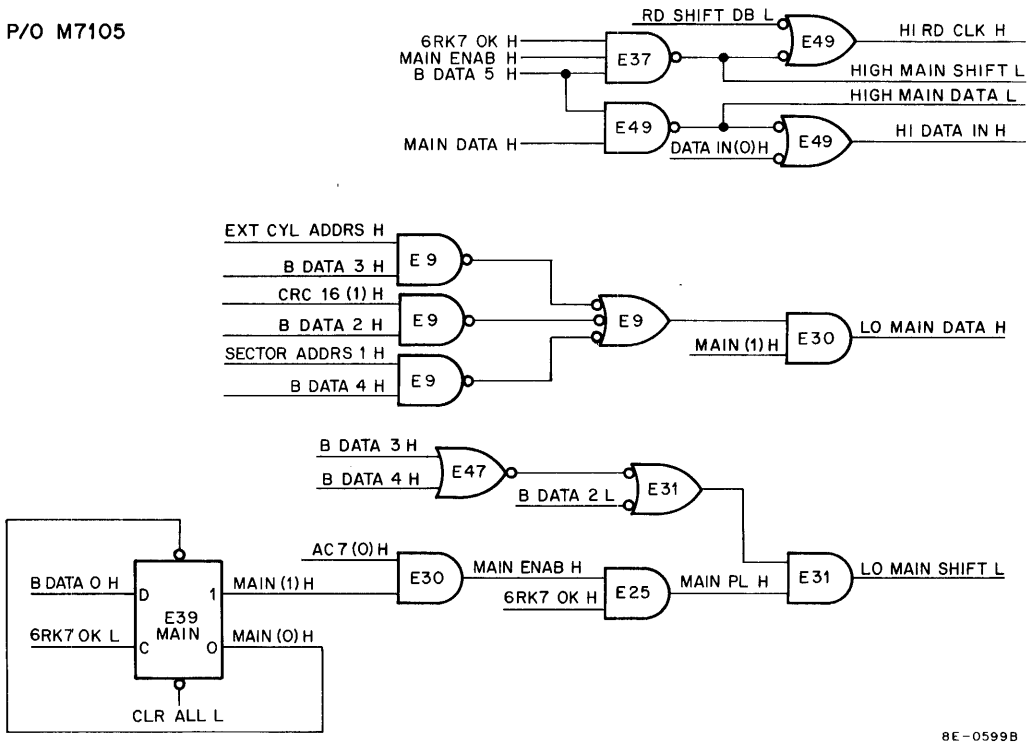


Figure 11-25 Data Buffer Register (sheet 2)

11.15.8.2 Data Buffer Control 1 and Data Buffer 1 – Data Buffer control 1 is used to control Data Buffer Register 1 (Figures 11-25 and 11-26). DB CONT1 is set to a 1 state when DB1 is loaded and remains in a 1 state until the data is transferred to DB2. DB1 is loaded (DB CONT1 goes to a 1 state) during write breaks by data from memory when LD RD BUFFER H is asserted by BRK DIR (0) H and DATA ENABLE (1) H (Figure 11-25). During read operations, DB1 is loaded with serial data so the input to DB CONT1 is not clocked in until 12 bits are read from the disk cartridge. When 12 bits are read and shifted into DB1 by the read clock, 12th BIT OK H is asserted and DB CONT1 goes to a 1 state (DB1 is full).

Note that during maintenance operations MAIN DATA can be shifted into DB1 by the 6RK7 (DMAN) instruction if bit 5 in the AC is a 1. This allows the program to check the Data Buffer Register and control logic.

Data Buffer Register 1 consists of three 7495A ICs (see Volume I, Appendix A for logic diagrams, pin locations, and truth table) connected in series to form a 12-bit register. During read operations, this register is loaded with 12 bits of serial data from the disk cartridge. The output of DB1 is a 12-bit parallel word that is transferred to DB2. DB1 is also loaded with a 12-bit parallel word from memory (write operations) that is transferred to DB2 when DB2 is empty.

11.15.8.3 Data Buffer Control 2 and Data Buffer Register 2 – DB CONT2 is set to a 1 state when DB CONT1 (1) H (DB1 full) and DB CONT2 (0) H (DB2 empty) are asserted. The output of NAND gate E13 (1 → DB2) triggers the 74123 IC and generates a 50 ns clock pulse, which clocks 1 → DB2 H into DB CONT2. Note that DB1 is not transferred to DB2 unless 1 → DB2 is asserted to cause a clock pulse to be generated. This stops a transfer from DB1 to DB2 unless DB2 is empty.

Data Buffer Register 2 consists of two 74174 ICs (see Volume I, Appendix A for logic diagram, truth table, and pin locations) that are connected in series to form a 12-bit register. This register is parallel loaded with 12 bits from DB1 when DB CONT2 is set to a 1 state. The parallel output of DB2 is transferred to DB3 when DB3 is empty.

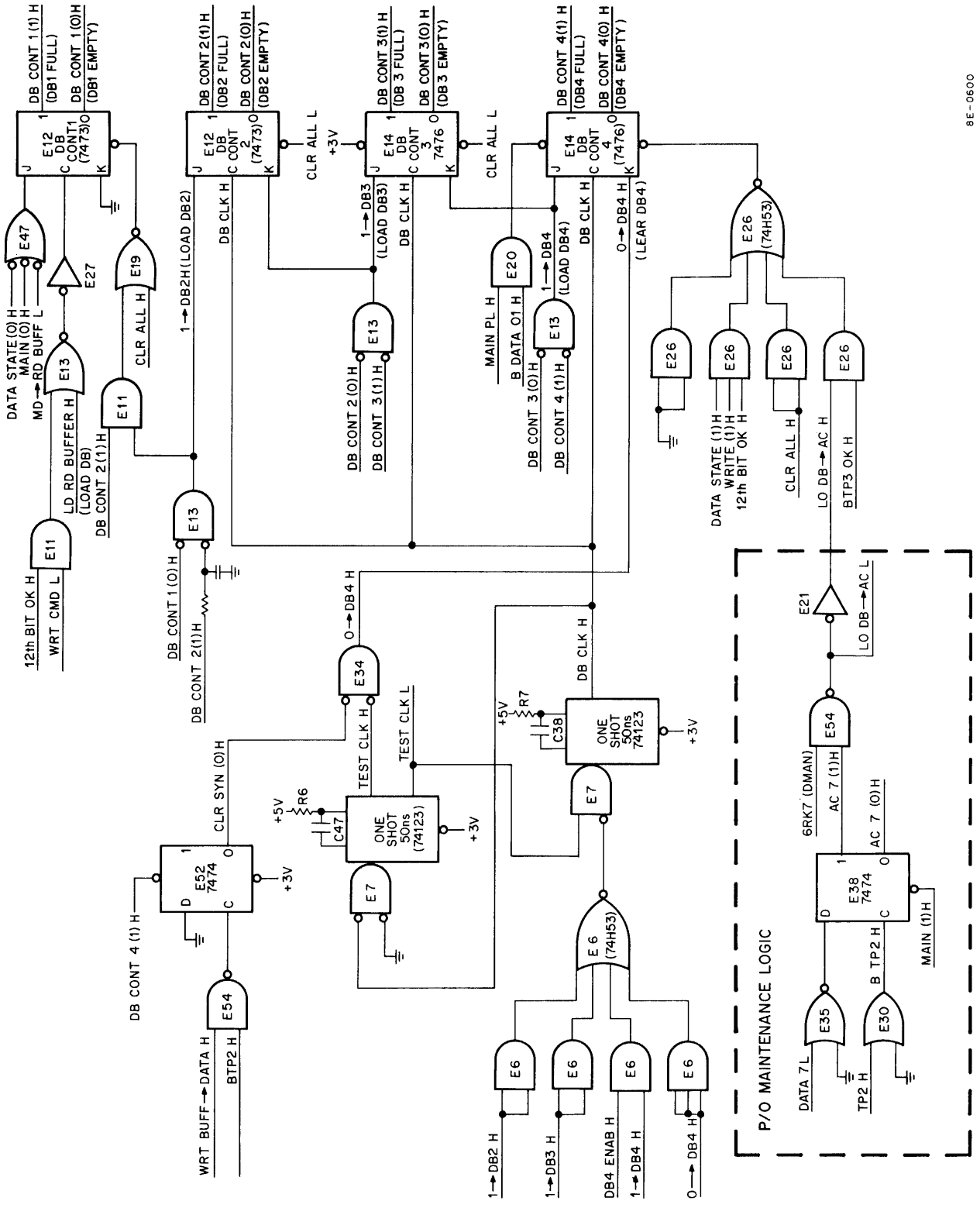


Figure 11-26 Data Buffer Register Control Logic

11.15.8.4 Data Buffer Control 3 and Data Buffer Register 3 – Operation of Data Buffer Control 3 and Data Buffer Register 3 is identical to DB2 CONT and DB2, except that DB3 H is qualified by DB3 (0) and DB2 (1). DB3 is loaded from DB2 when DB2 is full and DB3 is empty. The output of DB3 is transferred to DB4 when DB4 is empty (DB CONT4 in a 0 state) and DB3 is full (DB3 in a 1 state).

11.15.8.5 Data Buffer Control 4 and Data Buffer Register 4 – Data Buffer Control 4 (Figure 11-26) is used to control Data Buffer Register 4 (Figure 11-25). DB4 is loaded with the contents of DB3 if DB CONT3 (1) H (DB3 full) and DB CONT4 (0) H (DB4 empty) are negated to assert 1 → DB4 H. This causes DB CLK H to be asserted and DB4 goes to the 1 state (full).

During write operations, the contents of Data Buffer Register 4 are shifted out to the disk via the write logic (Figure 11-28) on the RK DATA11 line as serial data. WRT BUFF SHFT L is generated by the WRT CLK pulses (Figure 11-28), and shifts the data once for each clock pulse. When 12 bits of data have been shifted out to the disk, E26 is enabled and DB4 ENAB H is negated. This clears DB4 to the 0 state and DB4 can be loaded again from DB3.

During read operations, DB4 receives a 12-bit parallel word from DB3 for transfer to memory via the Data Bus. When WRT BUFF → DATA H is asserted to transfer the contents of DB4 to the Data Bus (DATA0–DATA11), CLR SYN (0) H is asserted to enable NAND gate E34. Signal 0 → DB4 H is asserted if the TEST CLK H pulse out of the 74123 IC is negated and 0 → DB4 returns DB CONT4 to the 0 state when the next DB CLK H pulse occurs. When DB CONT4 goes back to the 0 state, it is ready for new data to be transferred from DB3.

Data Buffer Register 4 consists of 3 7495A ICs (see Volume I, Appendix A for truth table, logic diagram, and pin locations) that are connected in series to form a 12-bit register. The register is loaded with 12 parallel bits from DB3 when DB4 is empty and DB3 is full. During write operations, the 12 bits are shifted out to the disk as serial data. During read operations, a 12-bit parallel word is transferred to memory via the Data Bus.

During maintenance operations, the contents of the Command Register, the CRC Register, and the Surface/Sector Register may be shifted into DB4 of the Data Buffer Register, for transfer to the AC. To accomplish this, the MAIN flip-flop must be set by transferring a 1 from the AC in bit position 1 using the DMAN instruction. This enables the maintenance logic (Figure 11-25) and allows bits from the AC to shift data into DB4. Signals MAIN PL H and B DATA 01 H are used to set DB CONT4 (Figure 11-26) and keep it in the 1 state, which disables transfers from DB3 while maintenance operations are underway. An input to DB4 is supplied by NOR gate E9 and NAND gate E30 as LO MAIN DATA H. When a DMAN instruction is executed by the program, the following events can occur:

a. If bit 3 in the AC is a 1 when the DMAN instruction is executed, bit 11 from the Command Register (EXT CYL ADDRS H) is applied to DB4. Each time the DMAN instruction is executed by the program, if bit 3 in the AC is set, a bit is shifted out of the Command Register and into DB4. When the contents of the Command Register are in DB4 (12 shifts), if the DMAN instruction is executed and bit 7 in the AC is a 1, LO DB → AC L is asserted to transfer the contents of DB4 to the AC via the Data Bus.

b. If bit 2 in the AC is a 1 and the DMAN instruction is executed, the contents of the CRC Register are shifted into DB4. This operation is the same as that listed above for the Command Register. Note that the program must keep track of the number of shifts required to shift all of the bits into DB4. The CRC Register is transferred to the AC with the same instruction and AC bit used for the Command Register.

c. If bit 4 in the AC is a 1 and the DMAN instruction is executed, the contents of the Sector/Surface Register are applied to DB4. This shift and transfer operation is the same as the other maintenance operations.

The MAIN flip-flop must be cleared using the DCLR instruction after maintenance operations are completed.

11.15.9 Output Data Multiplexer

The output data multiplexer (Figure 11-27) selects either the contents of the Status Register or DB4 to be applied to the Data Bus. The output data multiplexer consists of three 8235 ICs (see Volume I, Appendix A for truth table, logic diagram and pin locations) that are controlled by the 6RK5 (DRST) instruction and enable RK DATA L. If LO DB → AC is asserted during maintenance operations or WRT BUFF DATA L is asserted during read operations, RK DATA 0 L through RK DATA 11 L from DB4 are applied to the Data Bus. If the 6RK5 (DRST) instruction is executed by the program, the contents of the Status Register are applied to the Data Bus for transfer to the AC.

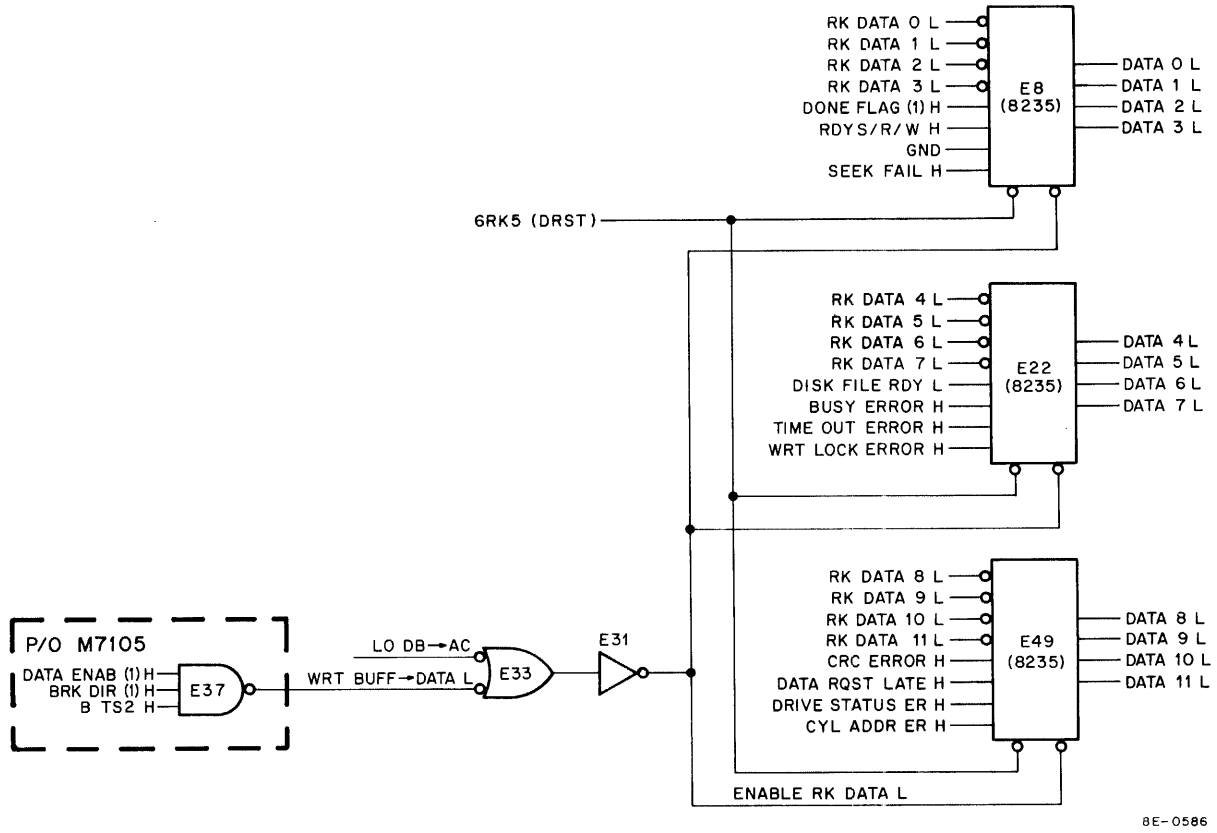


Figure 11-27 Output Data Multiplexer

11.15.10 Read/Write Logic

The read/write (Figure 11-28) logic provides a clock for generation of clock and data pulses to be written on the disk cartridge, the READ DLY logic, and logic to separate RD CLK pulses and READ DATA.

11.15.10.1 Write Clock – The write clock is a 2.88 MHz crystal-controlled oscillator that generates the WRT CLK pulses. When the WRITE flip-flop is set during SK/CHK/WRT or SK/WRT operations, the output of the write clock is enabled to clock E41. The set side of the E41 flip-flop is tied to the data input so that E41 is set and cleared on alternate clock pulses. This enables a NAND gate for WRT CLK pulses when E41 is set and a NAND gate for WRT DATA pulses when E41 is cleared. Thus, WRT CLK pulses and WRT DATA pulses are applied as an output to the RK05 from NOR gate E27. Note that the data pulses occur between clock pulses and a bit cell (Figure 11-2), and are written on the disk cartridge in this manner. The CRC bits (CRC 16 (1) H) from the CRC Register (during CRC state) and the SYNC bit (at end of write delay) are applied to E27 as data pulses to be written on the RK05 between WRT CLK pulses.

During the DATA state, the WRT CLK pulses are used to generate WRT SHFT CRC H, which is used to compute the CRC character (Paragraph 11.15.11).

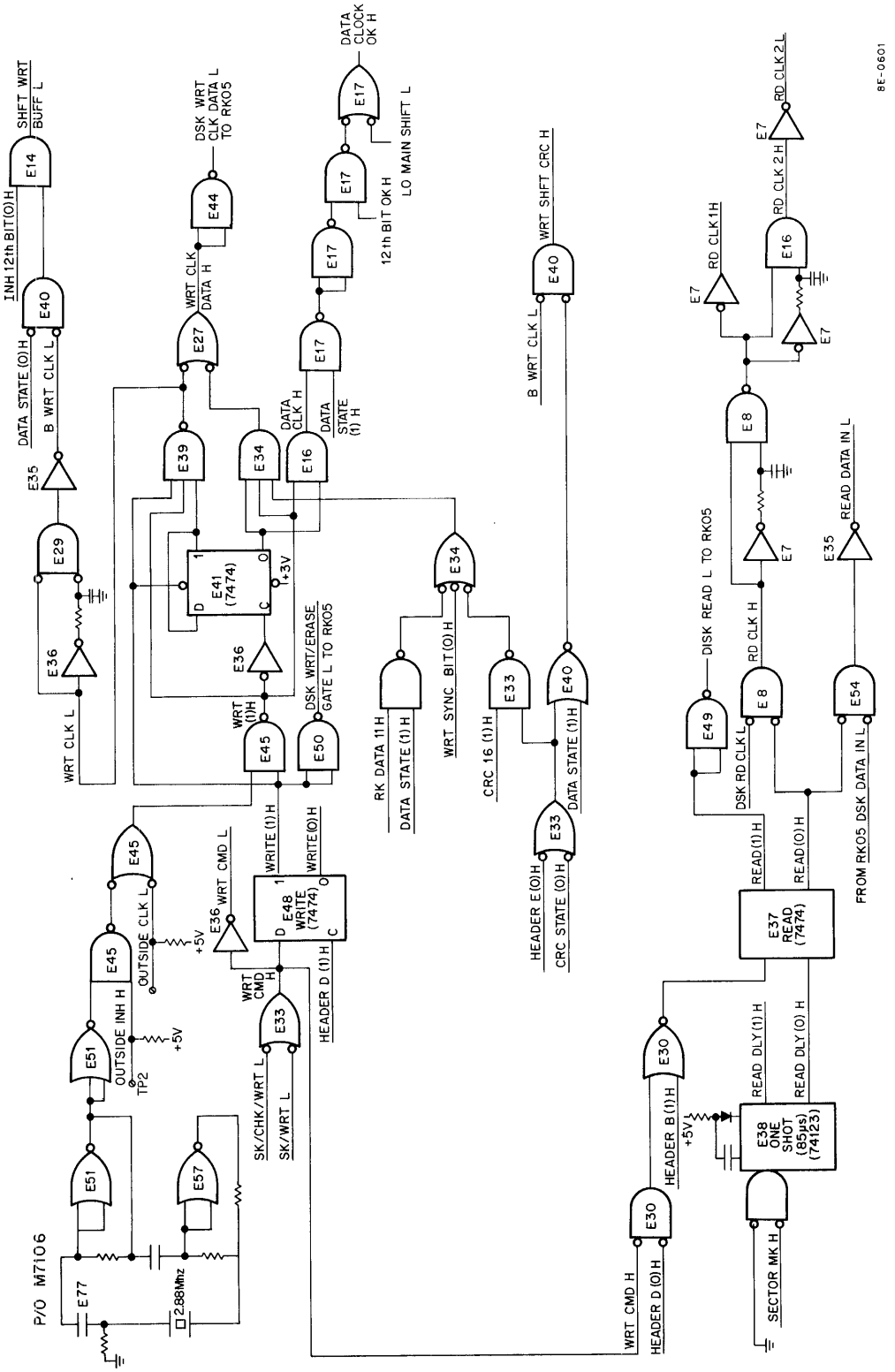


Figure 11-28 Read/Write Logic

11.15.10.2 Read Delay – The READ DLY is a 74123 IC that delays the setting of the READ flip-flop, and the read operation for 85 μs. This allows the controller to wait for the SYNC bit before the Major States Register advances to the HEADER E major state.

The 74123 is a one-shot multivibrator that is triggered when SECTOR MK H makes a low to high transition and outputs of 85 μs READ DLY pulse. After 85 μs, the READ flip-flop is set; after the SYNC bit is read, a read operation is started. The set side of READ is applied to the RK05 as DSK READ L to cause the RK05 to read data. The clear side of READ enables gates to allow RD CLK H and READ DATA IN L pulses to be applied to the RK8-E Data Buffer Register and control logic.

11.15.11 CRC Register

The CRC Register (Figure 11-29) is used to store the disk address and compute a CRC character during read and write operations. The CRC character is computed during write operations and written on the disk cartridge at the end of the data. During read operations, a CRC character is computed and compared with the CRC character that was written at the end of the data. If the two CRC characters are not equal, the CRC ERROR flag is set.

11.15.11.1 Disk Address – The CRC Register (Figure 11-29) is loaded with the 8-bit disk address when the DLDC instruction is executed by the program to assert LD DISK ADDRS H. The two 7496 ICs receive 7 bits (DATA0–DATA6) from the AC and one bit from Bit 11 (EXT CYL ADDRS H) of the Command Register. The disk address bits are applied to the RK05 Disk Drive during the STROBE major state (Figure 11-31) to select a cylinder and surface on the selected disk drive.

The CRC Register stores the disk address until the Major States Register enters the DATA state. At this time, the CRC Register is cleared by DATA STATE (0) H, which is negated (low). The CRC Register is also cleared by the 6RK3 (DCLR) instruction if it is executed by the program.

Note that the Load Disk Address instruction loads the Surface/Sector Register (Figure 11-29) at the same time the CRC Register is loaded.

During the HEADER C major state, the HEADER word is read from the selected drive as DATA IN H and applied to Exclusive-OR gate E24 (Figure 11-29). RD CLK 1 L asserts SHFT CRC H and shifts the contents of the CRC Register out to E24. Thus, the contents of the CRC Register (specified disk address) and the HEADER word read from the disk are compared bit-by-bit. If any bits are different, NOT EQUAL is set by the output of the Exclusive-OR (E24) and the CYLINDER ADDRESS ERROR flag is set (Figure 11-21).

The CRC Register contains the disk address specified by the program until the Major States Register moves to the DATA state. If CYLINDER ADDRESS ERROR is set, the TRANSFER DONE flag sets and the drive that produced the error must be recalibrated.

The disk address may be transferred to the AC for evaluation by the program using the DMAN instruction. When the disk address is transferred, the contents of the CRC Register are shifted out on CRC 16 (1) H to DB4 of the Data Buffer Register (Figure 11-25). Signal MAIN PL is asserted each time the DMAN instruction is executed by the program to shift the CRC Register one position and transfer one bit of the CRC Register to DB4. Note that AC bit 02 must be a 1 to enable the MAIN PL and assert CRC MAIN SHFT L. The program must keep track of the number of shifts and determine when to transfer DB4 to the AC.

Note that when the control is in any state except the DATA state, the Exclusive-OR gates for CRC 2 and CRC 15 have a ground on one input. The ground causes these gates to have an output that is the same as the input, which allows the contents of the CRC Register to be shifted and compared with the CRC DATA H input.

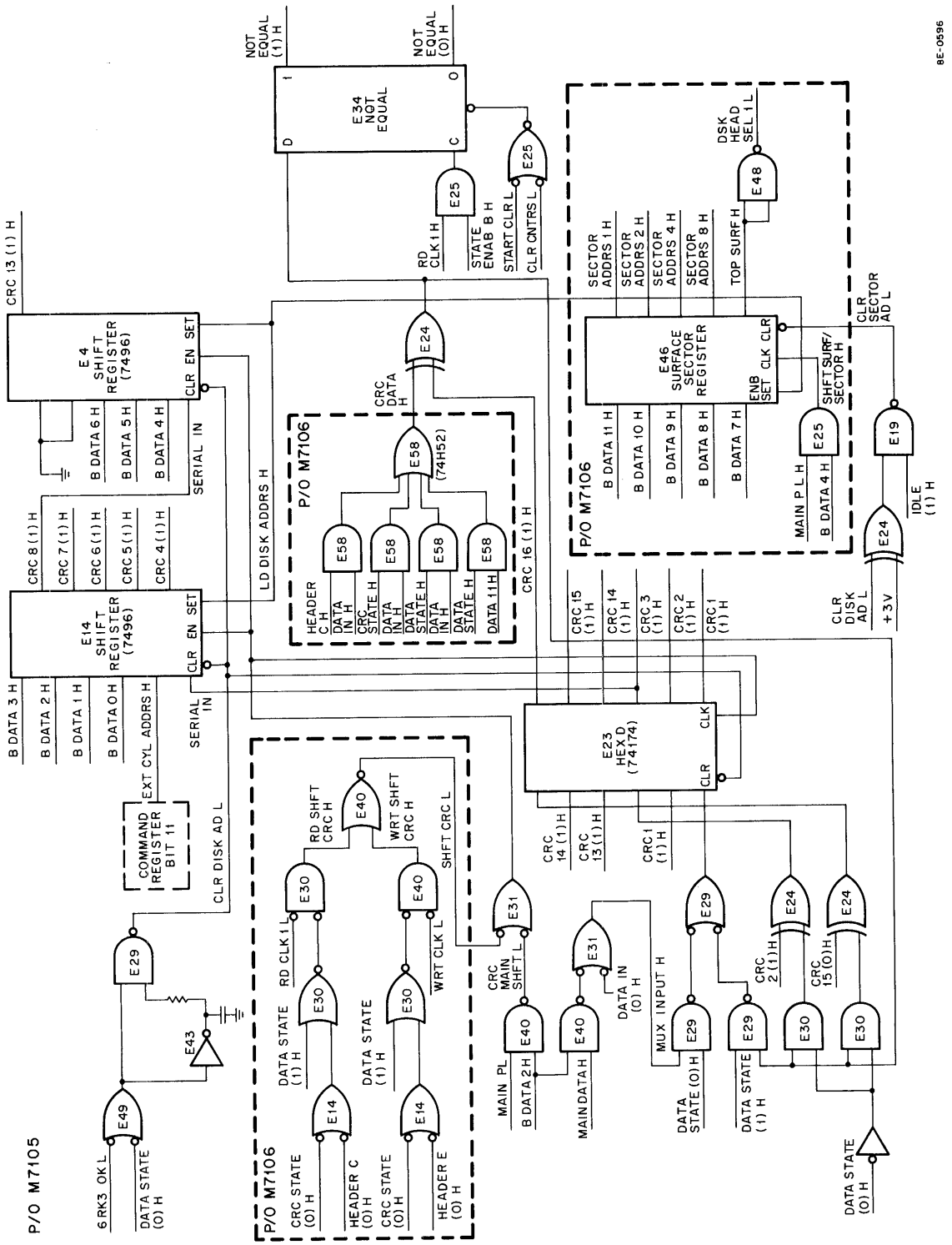


Figure 11-29 CRC and Surface Sector Register

The Exclusive-OR gates for CRC 2 and CRC 15 are used in the computation of the CRC character (Paragraph 11.15.11.2).

11.15.11.2 CRC Character Computation – To generate a CRC word, the block of data is treated as a number 3072 bits long which is divided (modulo 2) by a polynominal $X^{16} + X^{15} + X^2 + 1$. This division being shift and subtract (modulo 2) is accomplished by shifting the CRC Register and Exclusively ORing CRC 2, CRC 15, and CRC 16 (Figure 11-30) as follows:

a. The CRC Register is cleared at the beginning of the DATA state.

b. The CRC Register is shifted one bit position each time a bit is read or written by WRT CLK L or RD DLK 1 L.

c. The bit, which is read or written, is compared with CRC 16 (Exclusively ORed) and the result is Exclusively ORed with CRC 2 and CRC 15.

Using this method, a CRC character is generated for each block of data (256 words) that is written on or read from tape.

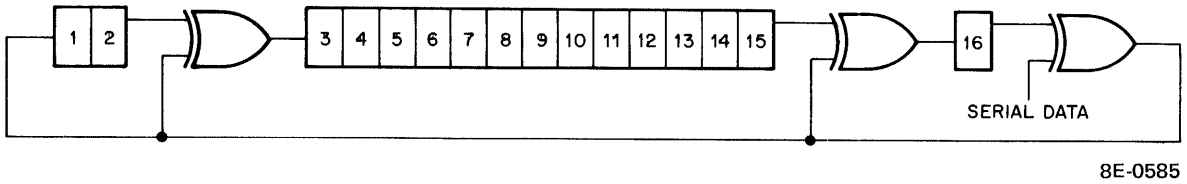


Figure 11-30 CRC Computation Block Diagram

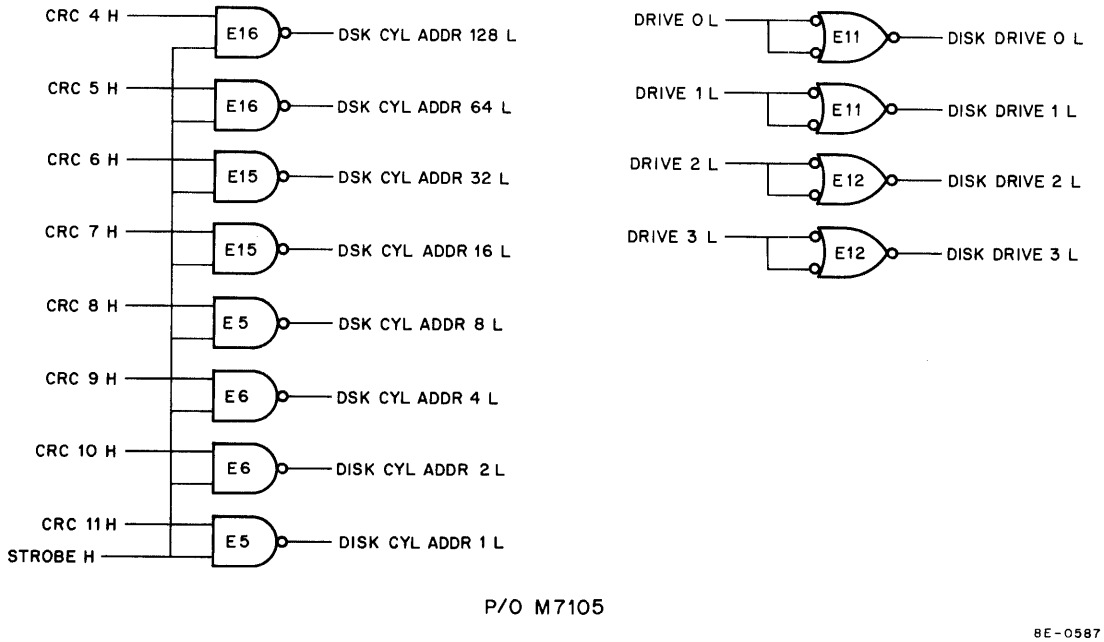


Figure 11-31 Disk Address Output Buffers

11.15.11.3 CRC Character Check – The CRC character that is computed for each block of data during a write operation is written on the disk cartridge after the data during the CRC state. This is accomplished by shifting the contents of the CRC Register out to the disk drive via the read/write logic (Figure 11-28). During the CRC state, the WRT CLK pulse is used to shift the contents of the CRC Register.

During read operations, a CRC is computed as explained above and when the control moves to the CRC major state, the CRC character written on the disk is read. DATA IN H is enabled by CRC STATE H (Figure 11-29) and applied to E24 Exclusive-OR gate. As the CRC character is read from the disk the CRC Register is shifted by RD CLK 1 H and a bit-by-bit comparison is made of the two CRC characters.

If any of the bits are different the output of the Exclusive-OR (E24) sets the NOT EQUAL flip-flop. If NOT EQUAL is set, the CRC ERROR flag sets during the END state (Figure 11-21).

The CRC character can be checked by the program using the DMAN instruction the same way the disk address was checked (Paragraph 11.15.11.1).

11.15.12 Major States

The operation of the Major States Register (Figure 11-32) and the determination of the disk format is discussed in Paragraph 11.14.7. The detailed logic is shown so that the reader can see all the signals required to enter each major state.

11.15.13 RK8-E Counters

The RK8-E counters (Figure 11-33) are used to count the bits and words in a data transfer and keep track of the number of data break cycles.

11.15.13.1 12-Bit Counter – The 12-bit counter (Figure 11-33) consists of 74161 IC (see Section 7 for truth table, timing diagram, and pin locations) used as a binary counter. The 12-bit counter is incremented by RD CLK 2 L (read) or WRT CLK L each time a bit is read or written. When 12 bits have been read or written, 12TH CARRY H is asserted to indicate a 12-bit word has been read or written. Signal 12TH CARRY H increments the word counter each time 12 bits are read or written until 256 or 128 words have been transferred. If HALF BLOCK H is asserted, 12th BIT OK H is negated after 128 words are read or written.

During maintenance operations, HI MAIN SHFT L is asserted if the program executes the DMAN instruction and AC bits 2, 3, or 4 are 1. This allows the program to check the counters and control logic.

The counters are cleared by CLR ALL L or CLR CNTRS L. Signal DATA CLR L is asserted each time the Major States Register advances to the DATA state by a pulse out of the 74123 IC. The 74123 IC (see Volume I, Appendix A for truth table, logic diagram, and pin locations) is a one-shot multivibrator that outputs a pulse each time the DATA state flip-flop sets. The counters are also cleared each time the Major States Register enters the HEADER E major state or when STATE ENAB B H is asserted when the Major States Register enters the CRC or HEADER C major state.

11.15.13.2 Word Counter – The word counter (Figure 11-33) consists of two 74161 ICs (see Section 7 for truth table, timing diagram, and pin locations) that are used as divide by 128 or 256 counters. The word counter is incremented by 12TH CARRY L each time 12 bits of data are read or written. LAST WORD H is asserted after 256 words have been read or written. Signal 128TH WORD H is asserted after 128 words are read or written, and if HALF BLOCK H is asserted (bit 5 in the Command Register must be a 1), the data transfer stops after 128 words. Note that the disk drive continues to read or write zeroes until 256 words are read or written, but this data is not transferred to memory. The TRANSFER DONE flag is not set until LAST WORD H is asserted after 256 words are read or written.

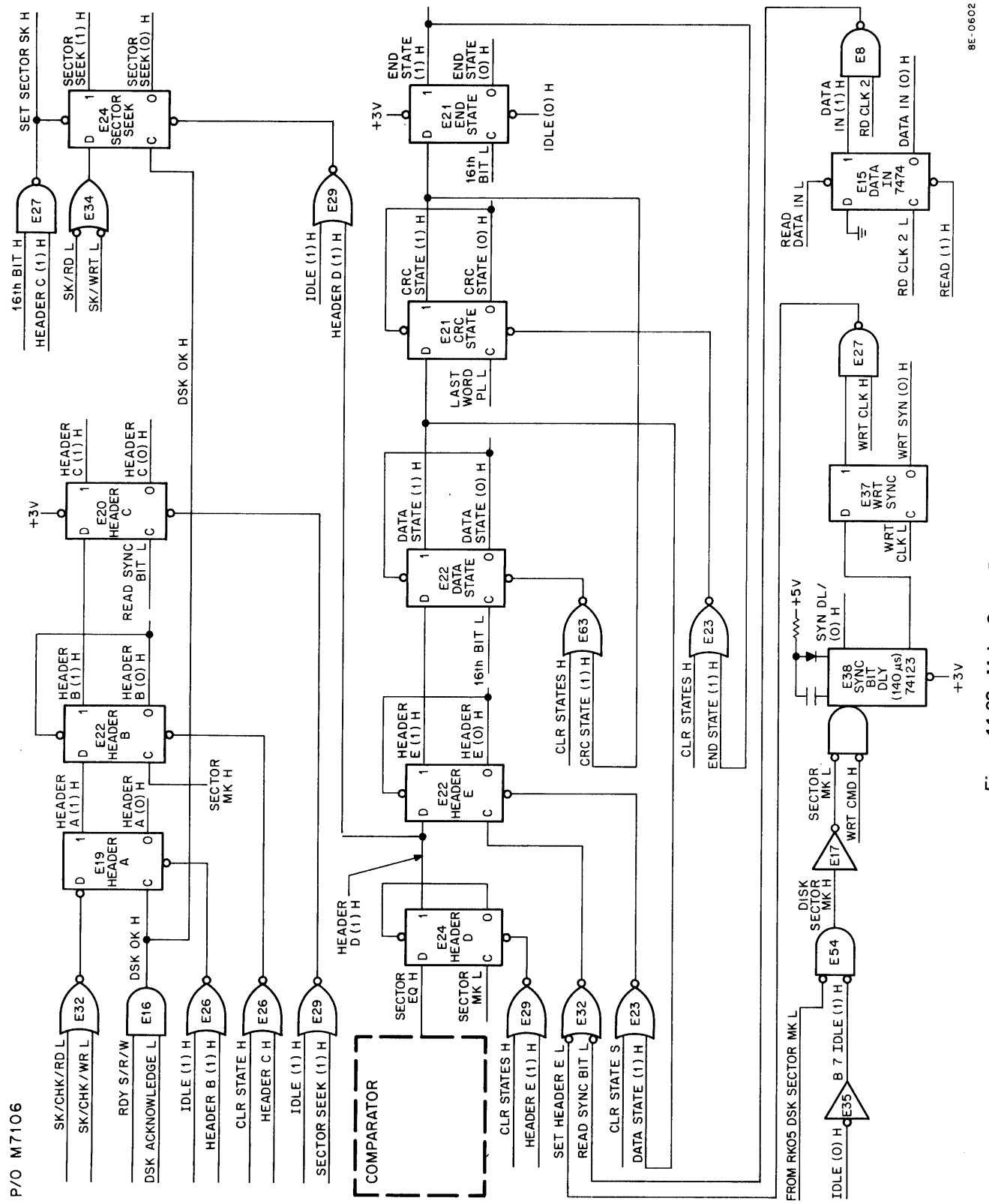


Figure 11-32 Major States Register (sheet 1)

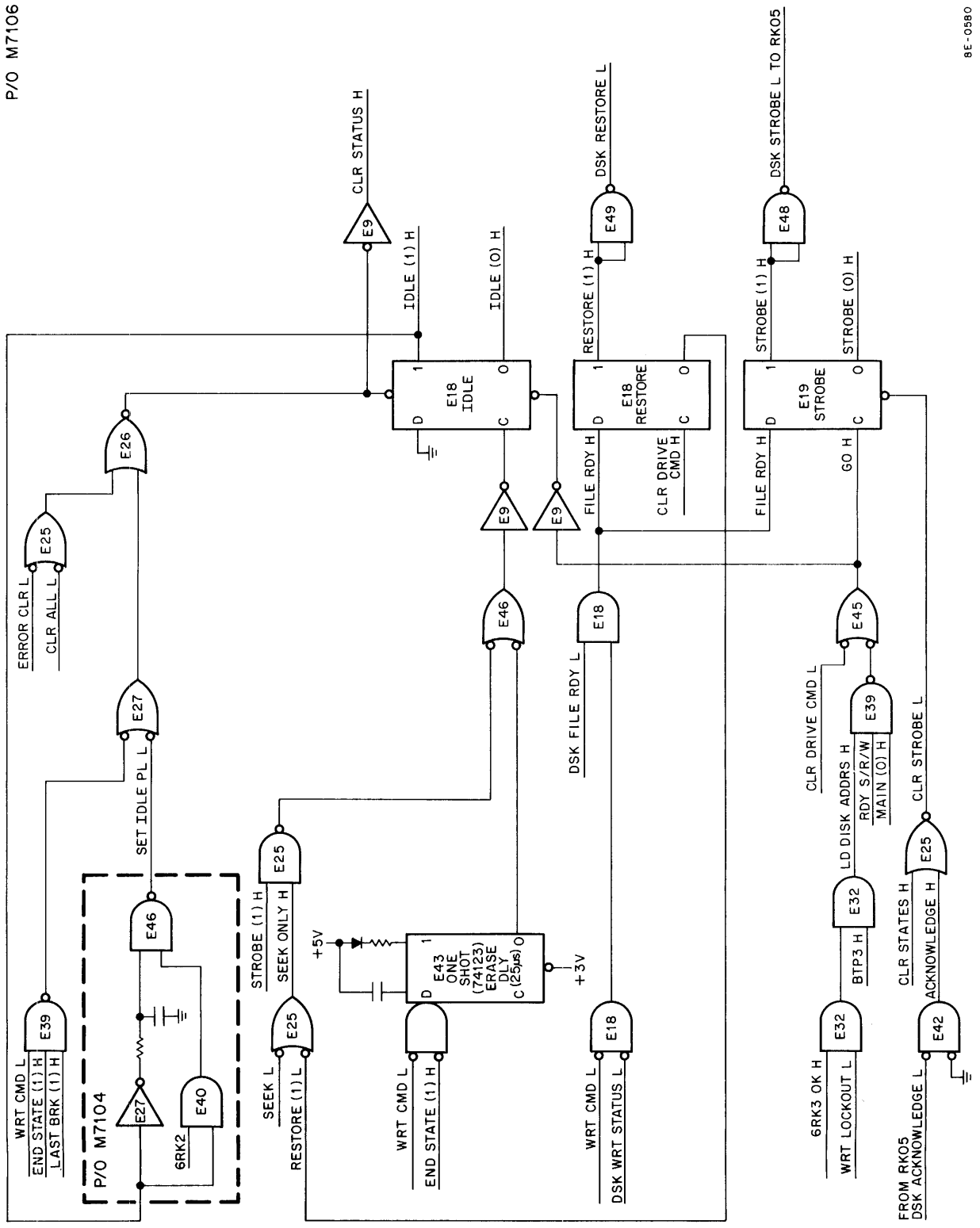


Figure 11-32 Major States Register (sheet 2)

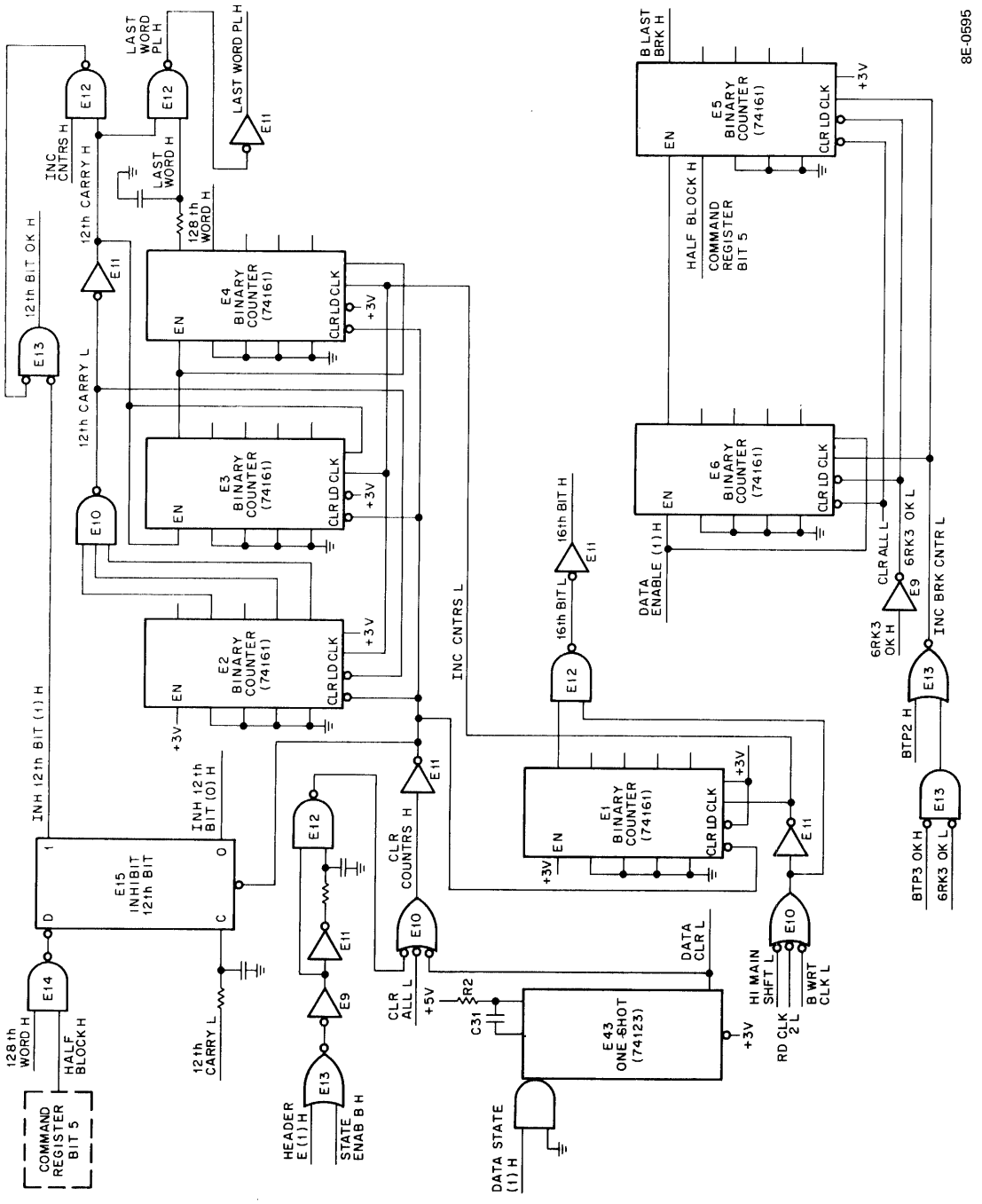


Figure 11-33 RK8-E Counters

11.15.13.3 16-Bit Counter – The 16-bit counter consists of a 74161 IC (see Section 7 for truth table, logic diagram, and pin location) that is used as a binary counter. The 16-bit counter counts the bits in a HEADER word or CRC character as they are read or written. The 16-bit counter is incremented by RD CLK 2 or the WRT CLK, which asserts INC CNTRS H. After 16 bits are read or written, 16TH BIT H is asserted and applied to the control logic.

During maintenance operations, the 16-bit counter is incremented by HI MAIN SHFT L when the DMAN instruction is executed by the program. This allows the program to check the 16-bit counter and associated logic.

11.15.13.4 Break Counter – The break counter (Figure 11-33) consists of two 74161 ICs (see Section 7 for truth table, logic diagram, and pin locations) that are used as a binary counter. The word counter is incremented at TP2 time of a break cycle (DATA ENABLE is set) to count the number of single cycle data breaks. B LAST BRK H is asserted after 256 words have been transferred to or from memory. If HALF BLOCK H is asserted (bit 5 in the Command Register must be a 1), data transfers stop after 128 words have been transferred. Signal B LAST BRK H sets the LAST BRK flip-flop (Figure 11-27) and stops data transfer operations.

SECTION 5 MAINTENANCE

11.16 PREVENTIVE MAINTENANCE

The recommended preventive maintenance should be scheduled on a regular basis to maintain the performance and reliability of the RK8-E and the RK05 Disk Drive system. Preventive maintenance schedules are found in the *RK05 Disk Drive Maintenance Manual* (DEC-00-RK05-DA). RK8-E diagnostics (Paragraph 11.5.1) are provided to test and troubleshoot the RK8-E controller. These diagnostics should be run at regular intervals to verify the operation of the RK8-E.

11.17 CORRECTIVE MAINTENANCE

The following programs may be loaded into memory from the Switch Register and used to monitor RK8-E signals during troubleshooting operations.

NOTE

The program to check the data buffers in Paragraph 11.17.1 should be run first.

11.17.1 Check Data Buffers

This program provides a scope loop to check the Data Buffers by shifting 12 bits of data (1s or 0s) from AC10 into DB1. When DB1 is full, a parallel transfer is made from DB1 to DB2, DB2 to DB3, DB3 to DB4. When DB4 is full, it is read into the AC with the maintenance IOT and stored in memory.

1. Clear disk control logic
2. Enable maintenance logic
3. Enable shift to data buffer 1
4. Set AC10 to equal data
5. Issue maintenance IOT 12 times
6. Read data buffer 4

Example:

Location	Contents	Mnemonic	Operation
7600	7301	CLA CLL IAC	/ ENABLE CLEAR CONTROL (AC10=0 AC11=1)
7601	6742	DCLR	/ IOT 6742 CLEAR CONTROL
7602	1230	TAD -12	/ DESIRED SHIFT COUNT
7603	3231	DCA COUNT	/ SET UP COUNTER
7604	7330	CML RAR	/ ENABLE MAINTENANCE MODE (AC00=1)
7605	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7606	7012	RTR	/
7607	7012	RTR	/
7610	7012	RTR	/ ENABLE CHECK DATA BUFFER (AC05=1)
7611	1232	TAD AC 10 DATA	/ GET DATA TO BE SHIFTED INTO DB1
7612	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7613	2231	ISZ COUNT	/ SHIFTED ONE WORD YET?
7614	5212	JMP -2	/ NO, SHIFT ANOTHER BIT.
7615	7200	CLA	/ YES, CLEAR AC
7616	1233	TAD K20	/ ENABLE DB4 TO AC TRANSFER (AC07=1)
7617	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7620	3234	DCA BUF REG	/ STORE DATA WORD
7621	7402	JMP START	/ (DEPOSIT A HLT TO MAKE ONE PASS)
		-12	7630 / 7766
		COUNT	7631 /
		AC10 DATA	7632 / 0000 OR 0002
		K20	7633 / 0020
		BUF REG	7634 /

11.17.2 Checking the Command Register

The following program is used to check the Command Register. The data is obtained from the Switch Register and loaded into the Command Register. It is then shifted into the lower Data Buffer, and read into memory using maintenance IOT instructions.

1. Clear disk control logic
2. Load Command Register with data from the Switch Register
3. Enable maintenance logic
4. Enable shift to lower buffer
5. Set AC03 (check Command Register)
6. Issue maintenance IOT 12 times
7. Read DB4

Example:

Location	Contents	Mnemonic	Operation
7600	7301	CLA CLL IAC	/ ENABLE CLEAR CONTROL (AC10=0 AC11=1)
7601	6742	DCLR	/ IOT 6742 CLEAR CONTROL
7602	1230	TAD -12	/ DESIRED SHIFT COUNT
7603	3231	DCA COUNT	/ SET-UP COUNTER
7604	7404	OSR	/ OR THE SWITCH REGISTER
7605	6746	DLDC	/ IOT 6746 LOAD COMMAND REGISTER
7606	7330	CLA CLL CML RAR	/ ENABLE MAINTENANCE MODE (AC00=1)
7607	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7610	7010	RAR	/ ENABLE SHIFT TO LOWER BUFFER DB4 (AC01=1)
7611	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7612	7012	RTR	/ ENABLE CHECK COMMAND REGISTER
7613	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7614	2231	ISZ COUNT	/ SHIFTED ONE WORD YET?
7615	5213	JMP -2	/ NO, SHIFT ANOTHER BIT
7616	7200	CLA	/ YES, CLEAR AC
7617	1232	TAD K20	/ ENABLE DB4 TO AC TRANSFER AC07=1
7620	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7621	3233	DCA CMD REG	/ STORE WORD
7622	5200	JMP START	/ LOOP OR HALT (HALT=1 PASS)
		-12	7630 / 7766
		COUNT	7631 /
		K20	7632 / 0020
		CMD REG	7633 /

11.17.3 Check Surface and Sector Register

This program is used to scope the Surface/Sector Register and Data Buffer 4. The data to be used is entered into the Console Switch Register (switches 5–11) then loaded into the Surface/Sector Register. It is then shifted into the lower Data Buffer (DB4 bits 5–11) where it is read into the AC and stored in memory.

1. Clear disk control logic
2. Enable maintenance logic
3. Load Surface/Sector Register with data from switches
4. Enable shift to lower Data Buffer
5. Enable shift Surface/Sector Register (AC04=1)
6. Issue maintenance IOT 12 times
7. Read DB4

Example:

Location	Contents	Mnemonic	Operation
7000	7301	CLA CLL IAC	/ ENABLE CLEAR CONTROL (AC10=0 AC11=1)
7001	6742	DCLR	/ IOT 6742 CLEAR CONTROL
7002	1230	TAD -12	/ DESIRED SHIFT COUNT
7003	3231	DCA COUNT	/ SET UP SHIFT COUNTER
7004	7330	CLA,CLL,CML,RAR	/ ENABLE MAINTENANCE MODE (AC00=1)
7005	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7006	7604	LAS	/ LOAD THE AC FROM THE SWITCH REGISTER
7007	6743	DLAG	/ IOT 6743 LOAD DISK ADDRESS
7010	7332	CLA,CLL,CML,RTR	/ ENABLE SHIFT TO LOWER BUFFER (AC01=1)
7011	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7012	7012	RTR	/ ROTATE AC AND LINK RIGHT TWO PLACES
7013	7010	RAR	/ ENABLE CHECK SURFACE AND SECTOR REGISTER / (AC04=1)
7014	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7015	2231	ISZ COUNT	/ SHIFTED ONE WORD YET?
7016	5214	JMP -2	/ NO, SHIFT ANOTHER BIT
7017	7200	CLA	/ YES, CLEAR THE AC
7020	1232	TAD K20	/ ENABLE DB4 TO AC TRANSFER (AC07=1)
7021	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7022	3233	DCA SS REG	/ STORE WORD
7023	5200	JMP START	/ LOOP OR HALT (HLT=1 PASS)
		-12	7030 / 7766
		COUNT	7031 /
		K20	7032 / 0020
		SS REG	7033 /

11.17.4 Check CRC Register

This program is used to scope the CRC Register logic. AC bit 10, CRC Register, and Data Buffer Register 4 are logically connected in series. A data bit is shifted 28 times through this series register to allow the last 12 bits to be read from DB4.

1. Clear disk control logic
2. Enable maintenance mode
3. Enable shift to lower buffer (DB4)
4. Load maintenance data into AC10
5. Check CRC Register (AC02=1)
6. Issue maintenance IOT 28 times
7. Read DB4
8. Shift 12 more data bits in
9. Read DB4
10. Jump back to step 8

Example:

Location	Contents	Mnemonic	Operation
7000	7301	CLA,CLL,IAC	/ ENABLE CLEAR CONTROL (AC10=0 AC11=1)
7001	6742	DCLR	/ IOT 6742 CLEAR CONTROL
7002	1230	TAD -28	/ DESIRED SHIFT COUNT
7003	3231	DCA COUNT	/ SET UP COUNT
7004	7330	LOOP-CLA,CLL, CML,RAR	/ ENABLE MAINTENANCE MODE (AC00=1)
7005	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7006	7010	RAR	/ ENABLE SHIFT TO LOWER DATA BUFFER (AC01=1)
7007	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7010	7010	RAR	/ ENABLE CHECK CRC REGISTER
7011	1232	TAD AC10 DATA	/ LOAD DATA BIT INTO AC10
7012	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7013	2231	ISZ COUNT	/ SHIFTED ONE 12 BIT WORD YET?
7014	5212	JMP -2	/ NO, SHIFT ANOTHER BIT
7015	7200	CLA	/ YES, CLEAR THE AC
7016	1233	TAD -12	/ DESIRED SHIFT COUNT
7017	3231	DCA COUNT	/ SET UP COUNT
7020	1234	TAD K20	/ ENABLE DB4 TO AC TRANSFER (AC07=1)
7021	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7022	3235	DCA CRC	/ STORE WORD
7023	5204	JMP LOOP	/ LOOP OR HALT (HALT=1 PASS)
		-28	7030 / 7744
		COUNT	7031 /
		AC10 DATA	7032 / 0000 OR 0002
		-12	7033 / 7766
		K20	7034 / 0020
		CRC	7035 /

11.17.5 Single Cycle Data Break Transfers (Read Operation)

This program transfers data from the RK05 to processor memory. It can be used to scope the data break control logic, Data Buffers, Current Address Register, Command Register, and the logic involved in read operation.

1. Clear control logic
2. Enable maintenance mode
3. Load AC from the Switch Register
4. Load Command Register
5. Enable shift to lower buffer
6. Set AC03 to 1 (check Command Register)
7. Issue maintenance IOT 12 times
8. Current address = 0000
9. Set AC06 to 1 (check data break request)
10. Issue maintenance IOT

Example:

Location	Contents	Mnemonic	Operation
7600	7301	CLA,CLL,IAC	/ ENABLE CLEAR CONTROL (AC10=0 AC11=1)
7601	6742	DCLR	/ IOT 6742 CLEAR CONTROL
7602	1230	TAD -12	/ LOAD DESIRED SHIFT COUNT
7603	3231	DCA COUNT	/ SET UP SHIFT COUNTER
7604	7604	LAS	/ TRANSFER SWITCH REGISTER CONTENTS TO THE AC
7605	6746	DLDC	/ STORE DATA IN LOCATION 0000
7606	7330	CLA CLL CML RAR	/ ENABLE MAINTENANCE MODE (AC0=1)
7607	6747	DMAN	/ IOT 6747 MAINTENTANCE IOT
7610	7010	RAR	/ ENABLE SHIFT TO LOWER DATA BUFFER (AC01=1)
7611	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7612	7012	RTR	/ ENABLE SHIFT TO COMMAND REGISTER (AC03=1)
7613	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7614	2000	ISZ COUNT	/ SHIFT ONE WORD YET?
7615		JMP -2	/ NO, SHIFT ONE MORE BIT
7616	7326	CLA CLL CML RTL	/ ENABLE MAINTENANCE MODE
7617	7006	RTL	/ ENABLE DB4 TO AC TRANSFER
7620	7006	RTL	/
7621	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7622	7000	NOP	/ NO OPERATION
7623	7000	NOP	/ NO OPERATION
7624	7402	JMP START	/ (DEPOSIT A HALT TO MAKE ONE PASS)

11.17.6 Single Cycle Data Break Transfers (Write Operation)

This program transfers data from processor memory to the Data Buffer. It is used to scope the write operation control logic, Current Address Register, Command Register, and the data break control logic.

1. Clear control logic
2. Enable maintenance logic
3. Set Command Register to write function
4. Load the AC from the Switch Register
5. Store data in location 0000 of memory
6. Enable break request bit
7. Issue maintenance IOT
8. Read DB4

Example:

Location	Contents	Mnemonic	Operation
7600	7301	CLA,CLL,IAC	/ ENABLE CLEAR CONTROL (AC10=0 AC11=1)
7601	6742	DCLR	/ IOT 6742 CLEAR CONTROL
7602	7330	CLA,CLL,CML,RAR	/ ENABLE MAINTENANCE MODE (AC0=1)
7603	6746	DLDC	/ IOT 6746 LOAD COMMAND REGISTER
7604	7604	LAS	/ LOAD AC FROM SWITCH REGISTER
7605	3000	DCA0	/ LOAD AC INTO LOCATION 0000
7606	7330	CLA,CLL,CML,RAR	/ ENABLE MAINTENANCE MODE (AC0=1)
7607	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7610	7012	RTR	/ ENABLE THE
7611	7012	RTR	/ MAINTENANCE DATA
7612	7012	RTR	/ BREAK REQUEST (AC06=1)
7613	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7614	7000	NOP	/ NO OPERATION
7615	7000	NOP	/ NO OPERATION
7616	7200	CLA	/ CLEAR AC
7617	1225	TAD K20	/ ENABLE DB4 TO AC TRANSFER (AC07=1)
7620	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7621	3226	DCA DATA	/ STORE DATA
7622	7402	JUMP START	/ (DEPOSIT A HALT TO MAKE ONE PASS)

11.17.7 Single Cycle Data Break Transfers (Write then Read)

This program transfers data in the Switch Register to DB1 of the RK8-E, then reads the data back into memory after it has transferred into DB4. The transfers are effected by causing one break request while the Command Register has a write command in it, then causing another break request with a read in the Command Register. Finally, check to see if the word read equals the word written.

1. Clear control logic
2. Load Command Register with a write function
3. Load memory location 0000 with data from the Switch Register
4. Enable maintenance logic
5. Initiate one single cycle data break request
6. Load Command Register with a read function
7. Initiate one single cycle data break request
8. Check data read with data from Switch Register

Example:

Location	Contents	Mnemonic	Operation
7600	7301	CLA CLL IAC	/ ENABLE CLEAR DISK CONTROL LOGIC
7601	6742	DCLR	/ IOT 6742 CLEAR CONTROL
7602	7330	CLA CLL CML RAR	/ ENABLE MAINTENANCE MODE AC00=1
7603	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7604	6746	DLDC	/ IOT 6746 LOAD COMMAND REGISTER (WRITE)
7605	7604	LAS	/ LOAD AC FROM SWITCH REGISTER
7606	3000	DCA 0	/ STORE WRITE DATA
7607	7326	CLA CLL CML RTL	/ ENABLE THE
7610	7006	RTL	/ MAINTENANCE DATA
7611	7006	RTL	/ BREAK REQUEST AC06=1
7612	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7613	7000	NOP	/ NO OPERATION
7614	7000	NOP	/ NO OPERATION
7615	7200	CLA	/ CLEAR AC
7616	6746	DLDC	/ IOT 6746 LOAD COMMAND (READ)
7617	7326	CLA CLL CML RTL	/
7620	7006	RTL	/ ROTATE AC AND LINK LEFT TWO
7621	7006	RTL	/ ENABLE MAINTENANCE DATA BREAK / REQUEST (AC06=1)
7622	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7623	7000	NOP	/ NO OPERATION
7624	7000	NOP	/ NO OPERATION
7625	5200	JMP START	/ (HALT=1 TIME) (NOP=CHECK DATA)
CHECK DATA			
7626	7300	CLA CLL	/ CLEAR AC AND LINK
7627	1000	TAD 0	/ LOAD AC WITH WRITE DATA

Location	Contents	Mnemonic	Operation
7630	7040	CMA	/ COMPLEMENT WRITE DATA
7631	3003	DCA 0003	/ STORE DATA FROM AC IN MEMORY
7632	1001	TAD 0001	/ LOAD AC WITH READ DATA
7633	0003	AND 0003	/ COMPARE READ AND WRITE DATA
7634	7440	SZA	/ SKIP ON ZERO AC (GOOD DATA)
7635	7402	HLT	/ HALT
7636	5200	JMP START	/ JUMP TO START

SECTION 6 SPARE PARTS

Table 11-16 lists recommended spare parts for the RK8-E. These parts can be obtained from any local DEC office, or from DEC, Maynard.

Table 11-16
RK8-E Spare Parts

DEC Part No.	Description	Quantity
11–00114	Diode, D664	1
19–05542	DEC IC, 7474	2
19–05575	DEC IC, 7400	2
19–05576	DEC IC, 7410	1
19–05579	DEC IC, 7440	1
19–05585	DEC IC, 7476	1
19–05587	DEC IC, 7473	1
19–09004	DEC IC, 7402	2
19–09055	DEC IC, 7495	1
19–09056	DEC IC, 74H00	1
19–09057	DEC IC, 74H10	1
19–09061	DEC IC, 74H52	1
19–09062	DEC IC, 74H53	1
19–09267	DEC IC, 74H11	1
19–09485	DEC IC, 380	2
19–09486	DEC IC, 384	1
19–09594	DEC IC, 8251B	1
19–09615	DEC IC, 8271	1
19–09667	DEC IC, 74H74	1
19–09686	DEC IC, 7404	2
19–09704	DEC IC, 314	1
19–09705	DEC IC, 8881	1
19–09931	DEC IC, 74H04	1
19–09935	DEC IC, 8235	1
19–10011	DEC IC, 7486	1
19–10018	DEC IC, 74193	1
19–10091	DEC IC, 7437	1
19–10155	DEC IC, 7408	1
19–10224	DEC IC, 7485	1
19–10363	DEC IC, 7496	1
19–10406	DEC IC, 75451	1
19–10436	DEC IC, 74123	1
19–10645	DEC IC, 75452	1
19–10650	DEC IC, 74161	1
19–10652	DEC IC, 74174	1
19–10656	DEC IC, 74155	1
18–10694	DEC Crystal Oscillator	1

11.18 DEC 74155 IC

The 74155 IC (Figure 11-34) is TTL circuit used as a 2-line to 4-line decoder (unit select decoder) and as a 3-line to 8-line decoder (function decoder) in the RK8-E. This IC may also be used as a 1-line to 8- or 4-line multiplexer, but it is not used this way in the RK8-E and will not be discussed here.

When the 74155 IC is used as a 2-line to 4-line decoder, as with the unit select decoder, the 1Y0 through 1Y3 outputs are selected by applying +3V to pin 1 and leaving pin 2 low. The inputs in this configuration are applied to pins 3 and 13 and the outputs (low) are taken from pins 4, 5, 6, and 7.

In the 3-line to 8-line configuration, as in the function decoder, external connections are installed to tie pin 1 to pin 15 and pin 2 to pin 14 (Figure 11-34). This allows both the 2Y and 1Y outputs to be used and provides for three inputs instead of two. In this configuration, the 74155 IC becomes a BCD to decimal decoder, which decodes three binary bits (Paragraph 11.15.3.1).

11.19 DEC 74193 IC

The DEC 74193 (Figure 11-35) monolithic circuit is a synchronous, reversible (up/down), 4-bit binary counter having a complexity of 55 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters. Figure 11-35 contains the logic diagram and pin locations.

The outputs of the four master/slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

The counter is fully programmable, i.e., the outputs may be preset to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs, independently of the count pulses. This feature allows the counters to be used as Modulo—N Dividers by simply modifying the count length with the preset inputs.

A CLEAR input has been provided which forces all outputs to the low level when a high level is applied. The CLEAR function is independent of the count and load inputs. An input buffer has been placed on the CLEAR, COUNT, and LOAD inputs to lower the drive requirements to one normalized load. This is important when the output of the driving circuitry is somewhat limited.

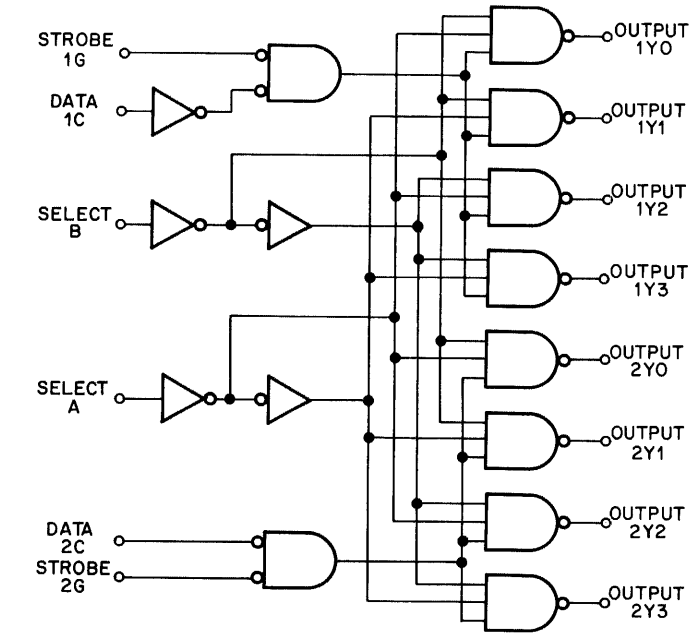
This counter was designed to be cascaded without the need for external circuitry. Both BORROW and CARRY outputs are available to cascade both the up- and down-counting functions. The BORROW output produces a pulse equal in width to the COUNT DOWN input when the counter underflows. Similarly, the CARRY output produces a pulse equal in width to the COUNT UP input when an overflow condition exists. The counters can then be easily cascaded by feeding the BORROW and CARRY outputs to the COUNT DOWN and COUNT UP inputs, respectively, of the succeeding counter.

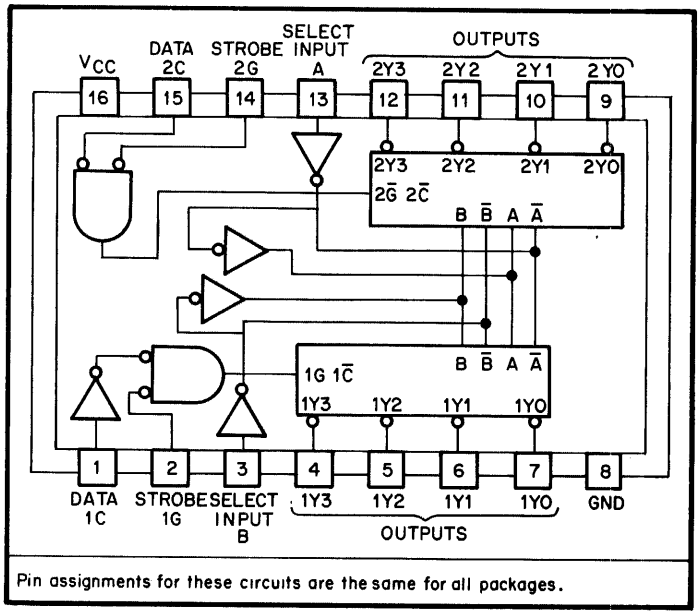
NOTE

Voltage values are with respect to network ground terminal.

11.20 DEC 7485 IC

The DEC 7485 IC performs magnitude comparison of straight binary and straight BCD codes. Three fully decoded decisions about two 4-bit words (A and B) are made and are externally available at three outputs. The delay time for a 4-bit comparison is 12 ns. Figure 11-36 shows the truth table, pin locator, and logic diagram.





Pin assignments for these circuits are the same for all packages.

8E-0605

Figure 11-34 DEC 74155 IC Illustration (sheet 1)

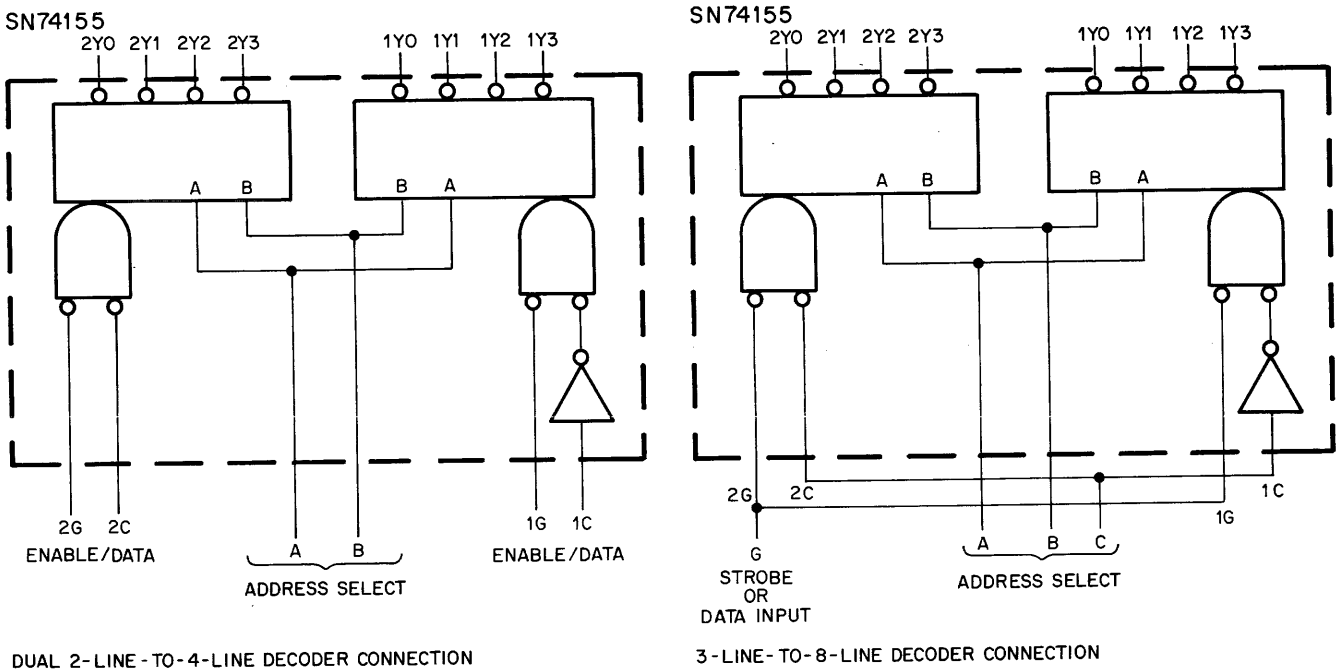


Figure 11-34 DEC 74155 IC Illustration (sheet 2)

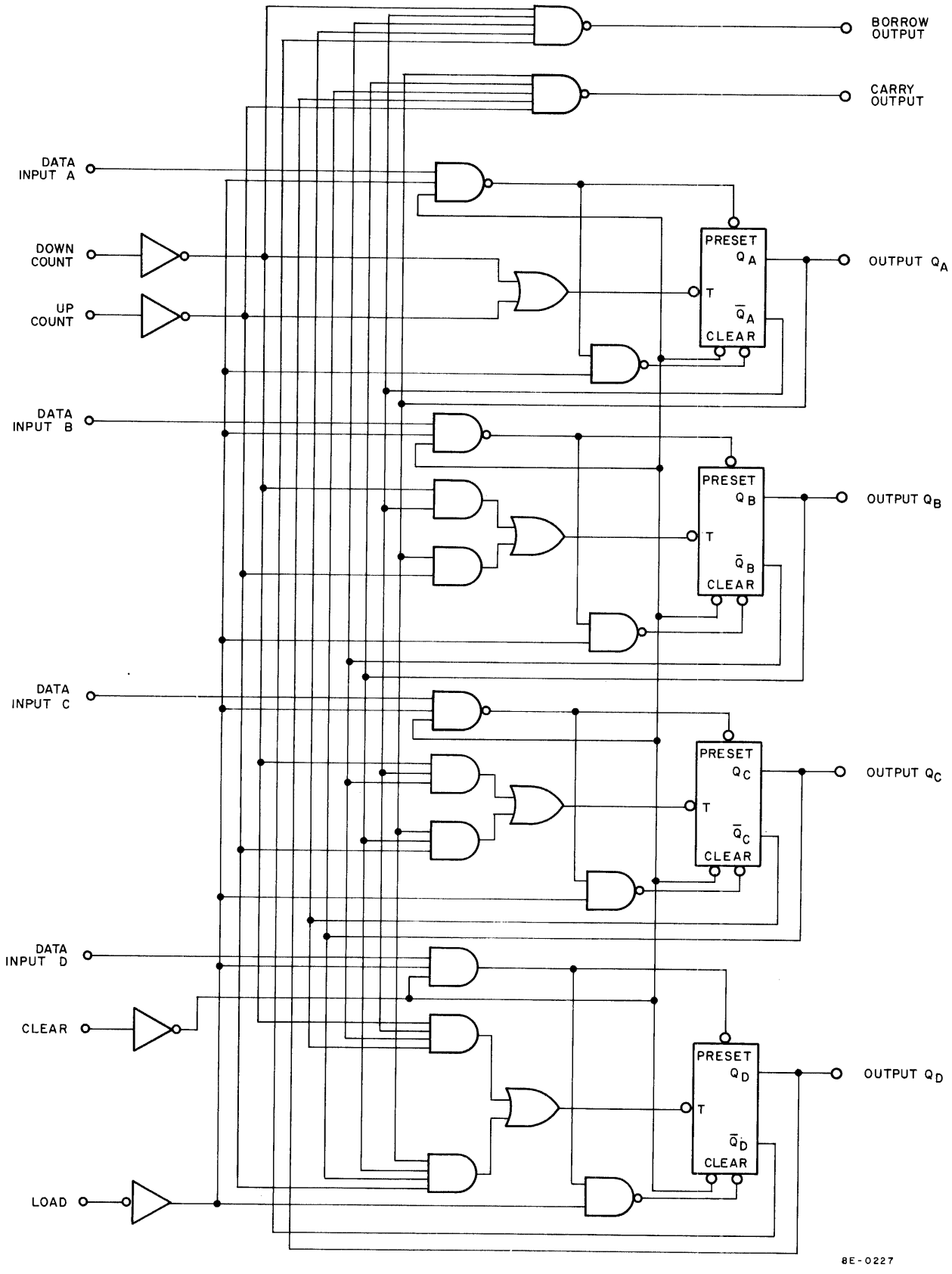
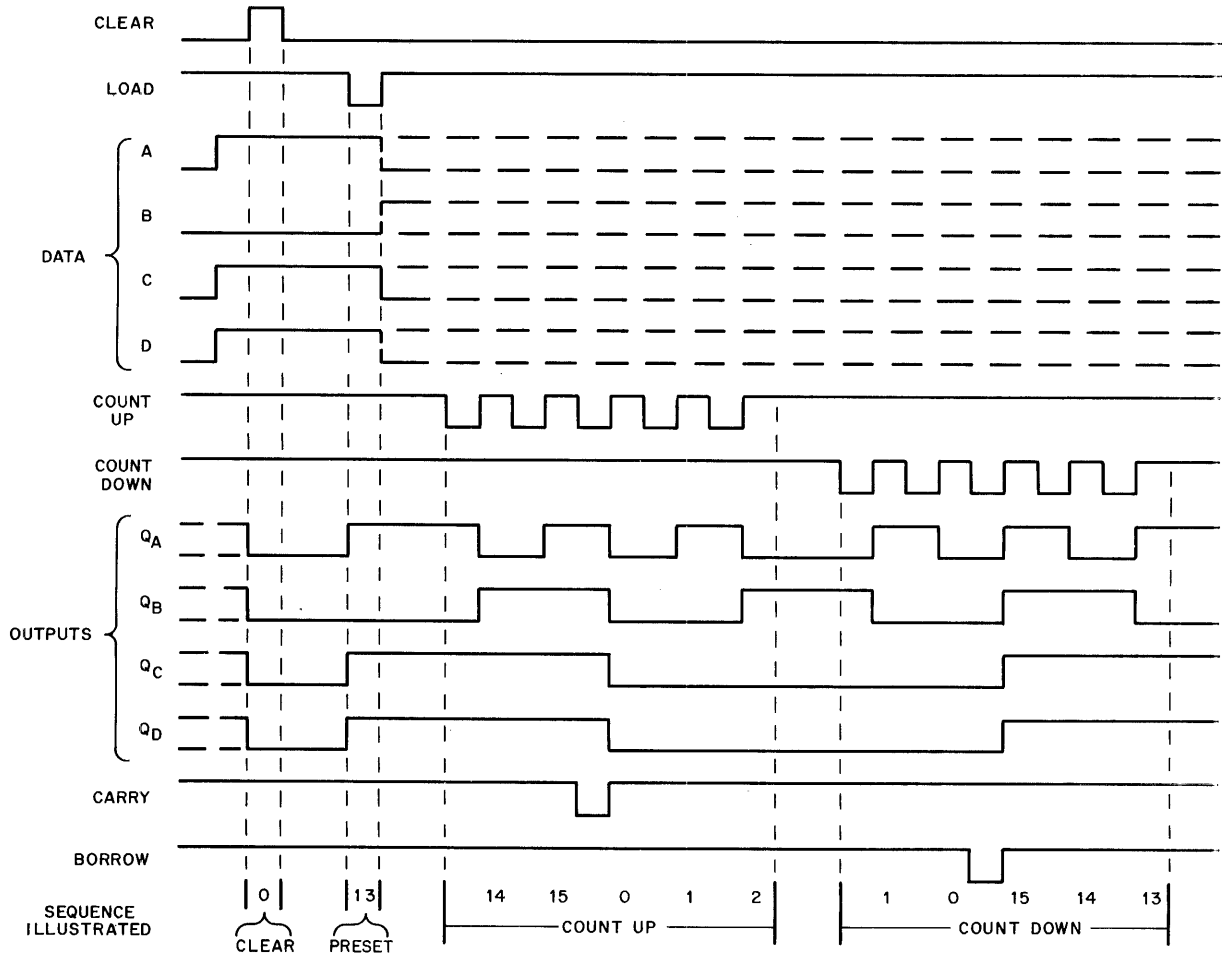


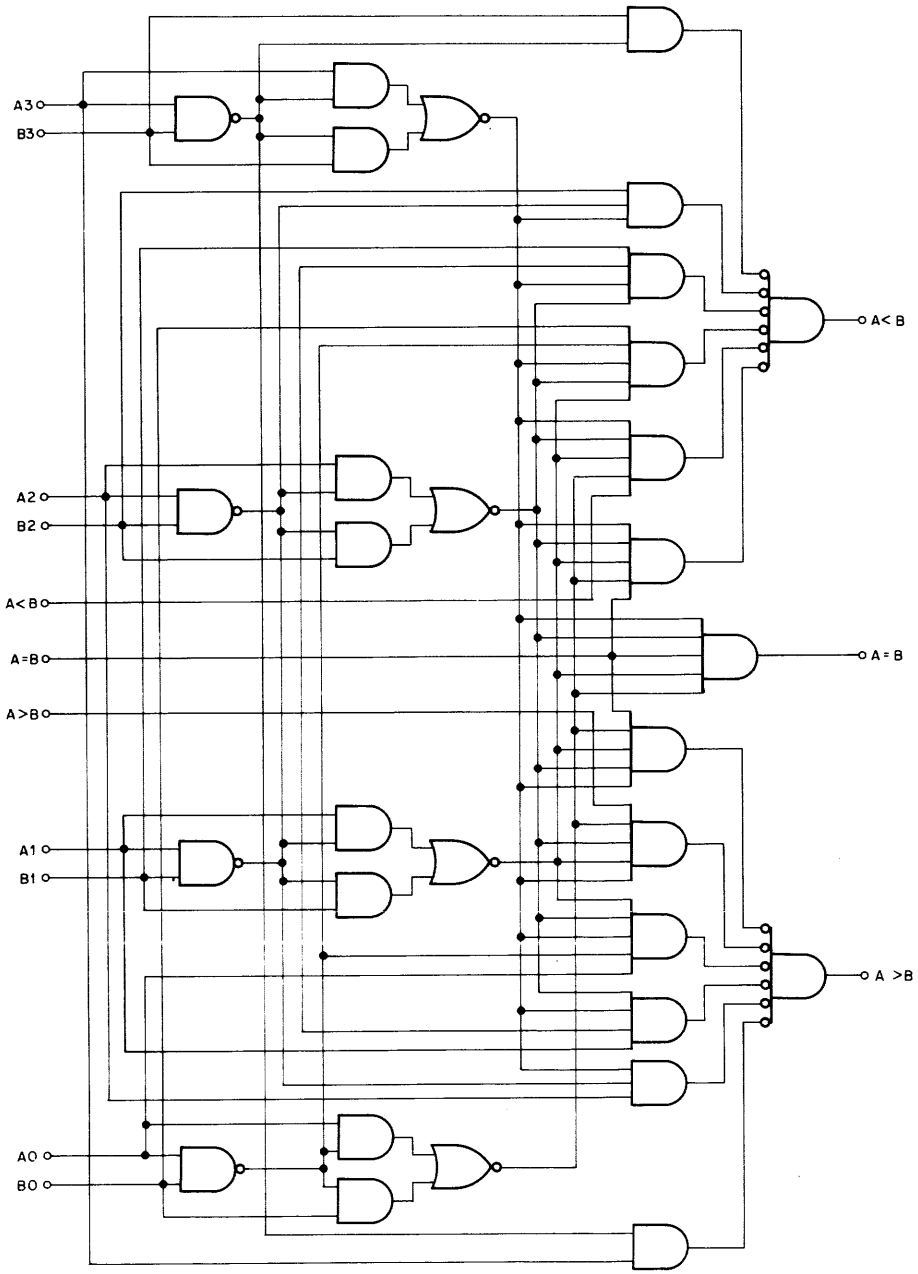
Figure 11-35 74193 IC Illustration (sheet 1)



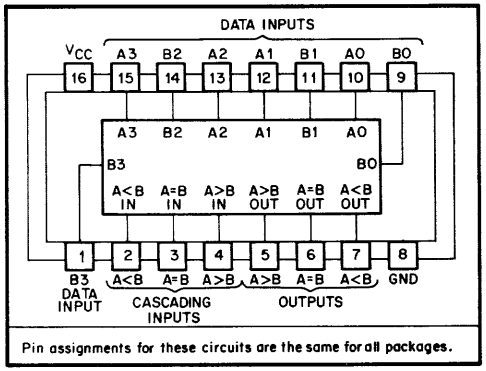
NOTE:
A. Clear overrides load data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

8E-0226

Figure 11-35 74193 IC Illustration (sheet 2)



TOP VIEW



Pin assignments for these circuits are the same for all packages.

8E-0604

Figure 11-36 DEC 7485 IC Illustration

The 7485 IC is used to compare the desired 4-bit sector address with a 4-bit sector address read from the disk cartridge in the RK8-E. This application asserts the A—B output when the two 4-bit addresses are equal.

11.21 DEC 74161 IC

The DEC 74161 IC (Figure 11-37) is a presetable high-speed binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation eliminates output counting spikes normally associated with ripple clock counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock input. To preset of load the counter register, the clock input and the enable must be asserted. The removal of enable allows the counter to be incremented by the clock input.

In the RK8-E, these ICs are cascaded to provide a 12-bit Current Address Register that is preset to an address in memory and incremented during the single cycle data break to select sequential memory locations.

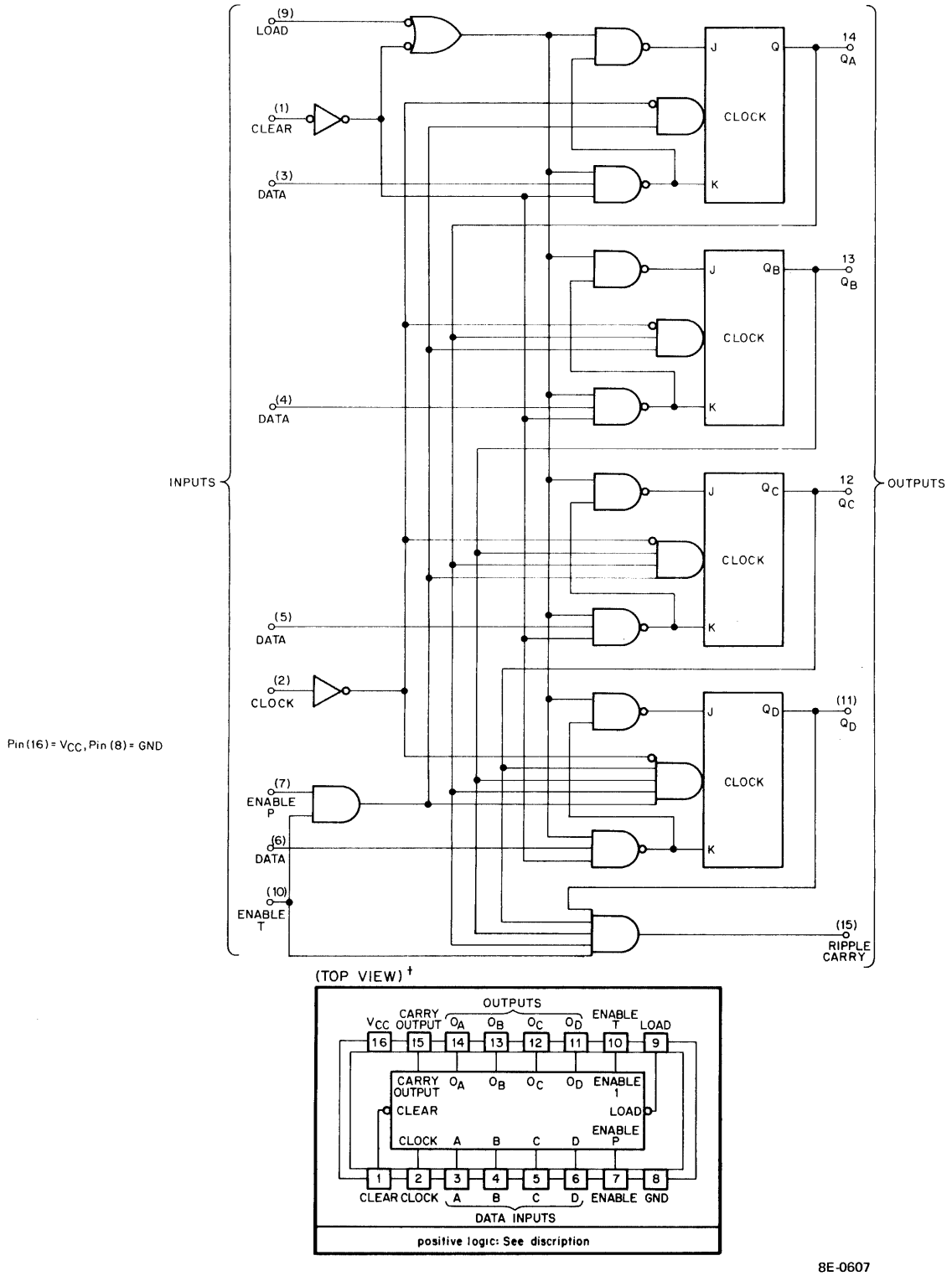
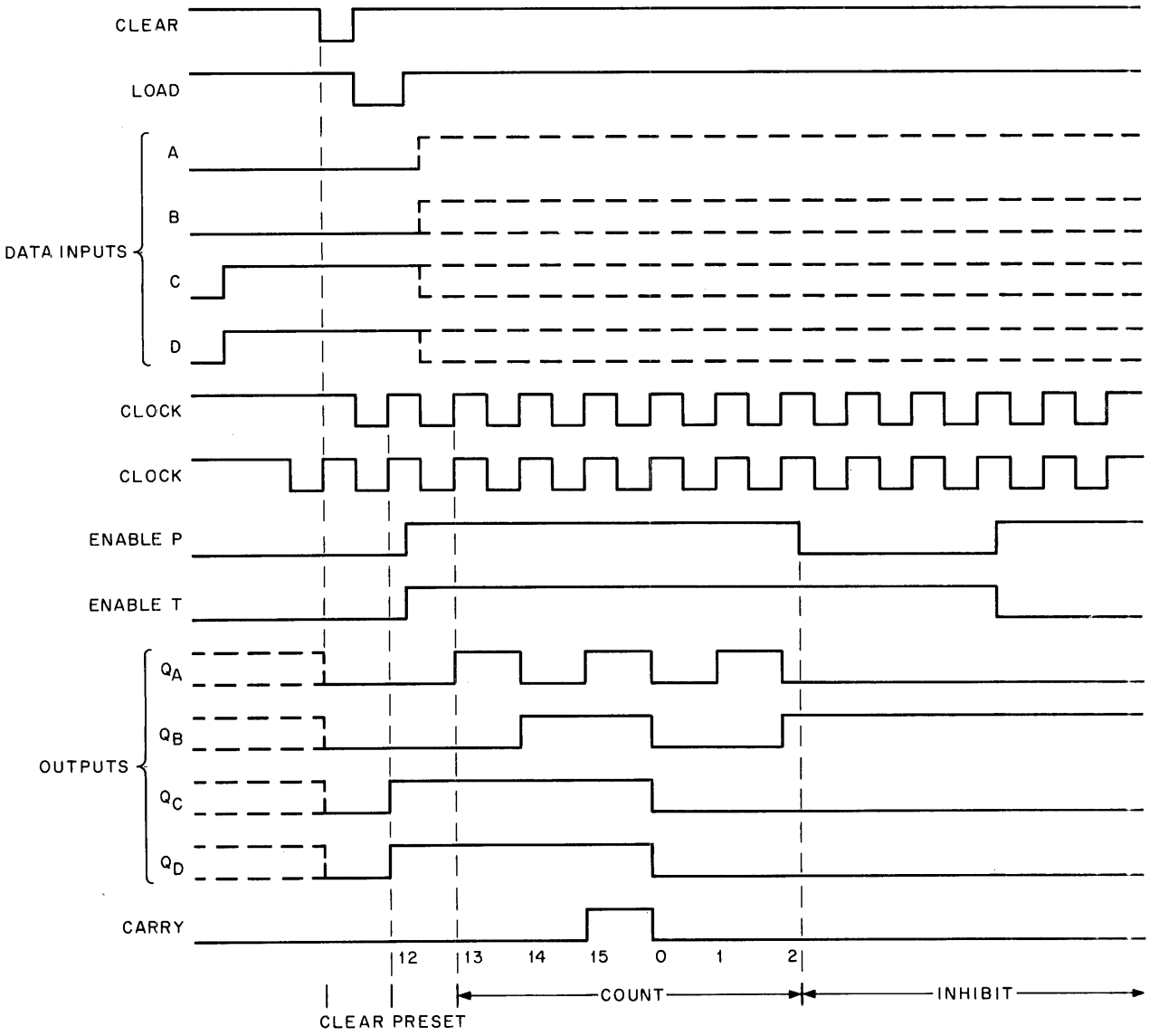


Figure 11-37 DEC 74161 IC Illustration (sheet 1)



The following sequence is illustrated

1. Clear outputs to zero
2. Preset to binary 12
3. Count to 13,14,15,0,1, and 2
4. Inhibit

8E-0603

Figure 11-37 DEC 74161 IC Illustration (sheet 2)

CHAPTER 12
VT8-E HIGH SPEED VIDEO DISPLAY TERMINAL AND CONTROL

SECTION 1 INTRODUCTION

The VT8-E, a video display option for the PDP-8/E, PDP-8/F, and PDP-8/M, consists of a video terminal and three quad modules that plug into the OMNIBUS. The quad modules control the terminal operation and can interface the VT8-E to either an LA30A-P DECwriter or an LS01-E Centronics Line Printer. Up to four VT8-E display options can be used simultaneously with the same computer.

The display terminal comprises a CRT with its associated power supply, deflection circuits, video circuits, and a keyboard with its control logic. The monitor is contained in a desk-top enclosure (Figure 12-1).

Data is transferred from the terminal keyboard to the computer AC Register by program interrupts. Data to be displayed by the monitor is transferred from memory by single cycle data breaks to the VT8-E OMNIBUS control modules. The control modules convert the parallel data to serial video information that is displayed on the viewing screen. The monitor can display both alphanumeric characters and graphic symbols, either alone or in combination.

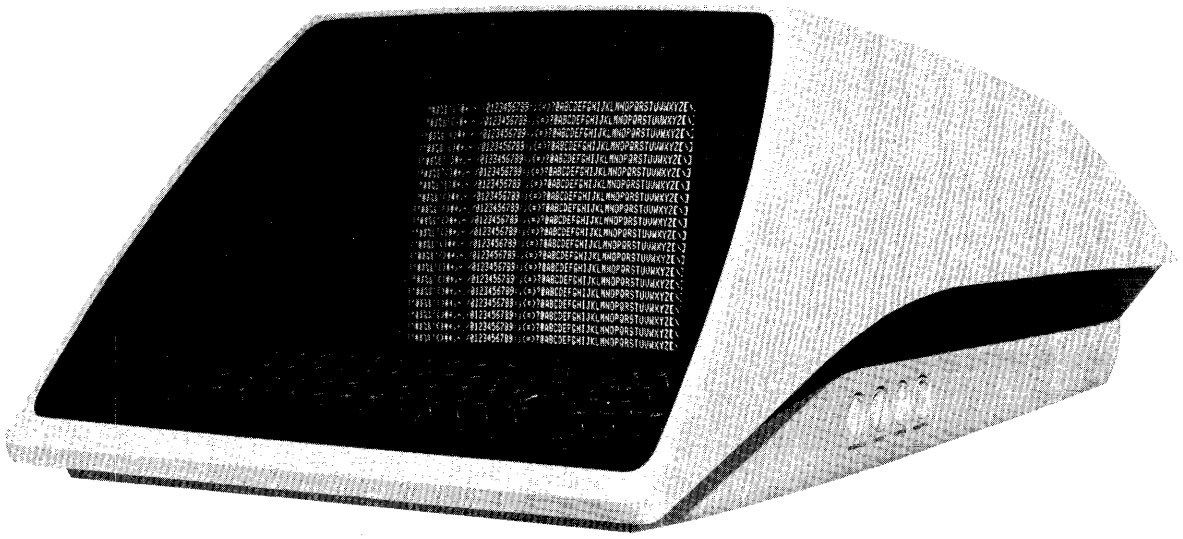


Figure 12-1 VT8-E Display Monitor

Neither the LA30A-P nor the LS01-E Line Printers is discussed here. Details concerning these two printers should be obtained from the respective maintenance manuals. Publications and documents relevant to the VT8-E are:

a. PDP-8/E, PDP-8/F, and PDP-8/M Small Computer Handbook – DEC, 1973

b. PDP-8/E, PDP-8/F, and PDP-8/M Maintenance Manual, Volume 1

c. VT8-E Diagnostic; MAINDEC-08-DHVTB-A (Graphic), MAINDEC-08-DHVTA-A (Alphanumeric)

d. DEC Engineering Drawings, E-CS-M8335-0-1, E-CS-M8336-0-1, and E-CS-M8337-0-1 (interface modules)

e. DEC Engineering Drawing, D-CS-5409917-0-1 (DEC keyboard #2)

f. DEC Engineering Drawings, D-CS-3010326-1-0 (Motorola Raster Display)

12.1 SYSTEM OPERATING SPECIFICATIONS

Operating Temperature Range	5° to 43°C
Operating Humidity Range (without condensation)	10% to 90% (Relative)
Power Requirements (display monitor)	100–130 Vac, 50 or 60 Hz ±5% single phase at 2A 200–260 Vac, 50 or 60 Hz ±5% single phase at 1A
Power Consumption (display monitor)	55W at 115V 65W at 230V

12.1.1 CRT Operating Specifications (Motorola Raster Display)

Screen Size	10-1/8 in. X 7-5/8 in.
Phosphor	P4 (white)
Deflection Type	Magnetic
Deflection Method	Raster Scan
Input Impedance (at VIDEO IN input)	75Ω ± 5%
Video Input Signal	0.9 to 2.2V with separate horizontal and vertical SYNC.
Video Pulse Rise and Fall Time	40 ns (10% to 90% point), measured at cathode with 1.0V p-p input and 30V p-p output.
Video Output Amplitude	30V p-p (minimum), measured at cathode with 1.0V p-p input.
Resolution	Screen Center – 600 lines (minimum) Screen Corners – 400 lines (minimum) (using shrinking raster method)

Horizontal Sweep Frequency	15.6 kHz
Vertical Sweep Frequency	50 or 60 Hz (selectable)
Horizontal Retrace	11 μs (maximum)
Vertical Retrace	21 horizontal lines @ 15.6 kHz
High Voltage	11 kV (minimum) @ 50 μA beam current @ 24 Vdc power supply adjustment
High Voltage Regulation	12 MΩ (maximum), for a beam current change from 50 to 150 μA @ 24 Vdc power supply adjustment.
CRT Refresh Rate	50 or 60 Hz

12.1.2 Visible Display Specifications

Screen Refresh Rate	60 or 50 frames/sec (determined by local line frequency)
Refresh Method	Raster Scan

12.1.2.1 Alphanumeric Mode

Viewing Area	8-1/4 in. (horiz) X 6-1/4 in. (vert) (32 characters/line) 8-1/4 in. X 4-1/4 in. (64 characters/line)
Character Lines	20
Character Size	0.185 in. width 0.220 in. height (32 characters/line)
	0.090 in. width 0.150 in. height (64 characters/line)
Character Spacing	
Horizontal	0.0740 in. (32 characters/line) 0.0370 in. (64 characters/line)
Vertical	0.0946 in. (32 characters/line) 0.0645 in. (64 characters/line)
Character Set	64-character ASCII set (upper case)
Character Generation Method	5 X 7 dot matrix

12.1.2.2 Graphic Mode

Viewing Area	7 in. X 6-1/4 in. (if wired for 32 alphanumeric characters per line)

Viewing Area (Cont)	7 in. X 4-1/2 in. (if wired for 64 alphanumeric characters per line)
Display Lines	200
Flicker-Free Points per Line	189

SECTION 2 INSTALLATION AND ACCEPTANCE TEST

The VT8-E Video Display and Control are installed on site by DEC Field Service personnel. The customer should not attempt to unpack, inspect, install, checkout, or service the equipment.

12.2 UNPACKING

The VT8-E Display Monitor is packed in a specially designed carton to avoid damage during shipment.

NOTE
Carefully examine the VT8-E for damage as it is unpacked. Any damage should be reported immediately.

Unpack the VT8-E Display Monitor as follows:

Step	Procedure
1	Remove the Display Monitor from the shipping container.
2	Remove the polyethylene cover.
3	Remove any tape, etc., from the display monitor cabinet.
4	Remove the display monitor from the shipping skid.
5	Place the display monitor in the desired location.
6	Verify all items listed on the Inventory List shipped with the VT8-E have been received.

12.2.1 Primary Power

The Display Monitor uses a single ac power cable (permanently connected) to connect the site power source to the display monitor. The monitor operates at 110–130 Vac, 50–60 Hz, single phase, or 200–260 Vac, 50–60 Hz, single phase.

Each wire in the ac power cable is color-coded as shown in Table 12-1. The display monitor is normally supplied with a 15A connector. The selected ac service outlet must be capable of at least 2A, 110 Vac, 50 or 60 Hz, or 1A, 200 Vac, 50 or 60 Hz.

Table 12-1
AC Power Cable

Line	Wire Color	Terminal Strip Nomenclature
Frame Ground	Green	Frame Ground
Neutral/Line 2	White	Neutral or Line 2
Line 1	Black	Line 1

12.2.2 VT8-E Installation

Install the VT8-E as follows:

Step	Procedure
1	Ensure PDP-8/E power is off.
2	Ensure the Display Monitor Power Select switch, located on the side of the Display Monitor, is set correctly for the power source (115 Vac or 230 Vac).
3	Use a meter to measure the voltages on the wall receptacle and ensure that the hot, neutral, and ground connections are the same as those on the Display Monitor power connector (Table 12-1).
4	On the M8336 and M8337, ensure the 5 jumpers are installed to select only 64 or 32 characters per line. All jumpers must be installed for the same mode.
5	On the M8335 module ensure the correct device code jumpers are installed. Table 12-2 contains a list of the split lugs which should be connected in each of the 6 groups (A–F) to select one of the 64 possible device codes. Split lug locations (by groups) are shown on D-CS-M8335-0-1 Engineering Drawing cover sheet.
6	On the M8337 and M8335 modules, ensure the jumpers are installed correctly to select the priority assigned to this VT8-E (Table 12-3). Only priorities 9 (highest), 10, and 11 (lowest) may be assigned to the VT8-E. Refer to M8337-0-1 and M8335-0-1 cover sheet for jumper locations.
7	Connect J1 of the 7009042 Cable Assembly to J1 on the M8336 module.
8	Connect J2 of the 7009042 Cable Assembly to J1 on the M8335 module.
9	If a line printer is used, connect the printer cable assembly to J2 on the M8335 module.
10	Install the VT8-E modules on the OMNIBUS as shown in Figure 12-2. Refer to Figure 2-3 in Volume 1 for recommended module installation priorities. The VT8-E is not a memory option. The VT8-E modules must be installed in this order; M8336 Front M8337 Middle M8335 Rear
11	Install H851 Top Connectors as follows (Figure 12-2): *a.* Between M8336H and M8337H *b.* Between M8337E and M8335E *c.* Between M8337F and M8335F
12	Route the 7009042 Cable Assembly to the Display Monitor and connect J3 Winchester Connector to the mating connector on the rear of the console.

13 If a line printer is used, route the printer cable to the line printer and connect it.

NOTE

If more than one VT8-E is installed in one system (up to four may be installed in one system), the second control goes on the OMNIBUS directly behind the first, and the third behind the second, etc. The two controls are interconnected by installing an H851 Top Connector between M8335J of the first control and M8336J of the second control. The controls must be assigned different device codes (Tables 12-2 and 12-3).

14 Turn on PDP-8/E power and run the acceptance test in Paragraph 12.2.4.

Table 12-2
Device Code Select Jumper Installation

Device Code	Group A	Group B	Group C	Group D	Group E	Group F
00	2-3	2-3	2-3	2-3	2-3	2-1
01	2-1	2-3	2-3	2-3	2-3	2-1
02	2-3	2-3	2-3	2-1	2-3	2-1
03	2-1	2-3	2-3	2-1	2-3	2-1
04	2-3	2-3	2-3	2-3	2-1	2-1
05	2-1	2-3	2-3	2-3	2-1	2-1
06	2-3	2-3	2-3	2-1	2-1	2-1
07	2-1	2-3	2-3	2-1	2-1	2-1
10	2-3	2-3	2-1	2-3	2-3	2-1
11	2-1	2-3	2-1	2-3	2-3	2-1
12	2-3	2-3	2-1	2-1	2-3	2-1
13	2-1	2-3	2-1	2-1	2-3	2-1
14	2-3	2-3	2-1	2-3	2-1	2-1
15	2-1	2-3	2-1	2-3	2-1	2-1
16	2-3	2-3	2-1	2-1	2-1	2-1
17	2-1	2-3	2-1	2-1	2-1	2-1
20	2-3	2-1	2-3	2-3	2-3	2-1
21	2-1	2-1	2-3	2-3	2-3	2-1
22	2-3	2-1	2-3	2-1	2-3	2-1
23	2-1	2-1	2-3	2-1	2-3	2-1
24	2-3	2-1	2-3	2-3	2-1	2-1
25	2-1	2-1	2-3	2-3	2-1	2-1
26	2-3	2-1	2-3	2-1	2-1	2-1
27	2-1	2-1	2-3	2-1	2-1	2-1
30	2-3	2-1	2-1	2-3	2-3	2-1
31	2-1	2-1	2-1	2-3	2-3	2-1
32	2-3	2-1	2-1	2-1	2-3	2-1
33	2-1	2-1	2-1	2-1	2-3	2-1
34	2-3	2-1	2-1	2-3	2-1	2-1
35	2-1	2-1	2-1	2-3	2-1	2-1
36	2-3	2-1	2-1	2-1	2-1	2-1

Table 12-2 (Cont)
Device Code Select Jumper Installation

Device Code	Group A	Group B	Group C	Group D	Group E	Group F
37	2-1	2-1	2-1	2-1	2-1	2-1
40	2-3	2-3	2-3	2-3	2-3	2-3
41	2-1	2-3	2-3	2-3	2-3	2-3
42	2-3	2-3	2-3	2-1	2-3	2-3
43	2-1	2-3	2-3	2-1	2-3	2-3
44	2-3	2-3	2-3	2-3	2-1	2-3
45	2-1	2-3	2-3	2-3	2-1	2-3
46	2-3	2-3	2-3	2-1	2-1	2-3
47	2-1	2-3	2-3	2-1	2-1	2-3
50	2-3	2-3	2-1	2-3	2-3	2-3
51	2-1	2-3	2-1	2-3	2-3	2-3
52	2-3	2-3	2-1	2-1	2-3	2-3
53	2-1	2-3	2-1	2-1	2-3	2-3
54	2-3	2-3	2-1	2-3	2-1	2-3
55	2-1	2-3	2-1	2-3	2-1	2-3
56	2-3	2-3	2-1	2-1	2-1	2-3
57	2-1	2-3	2-1	2-1	2-1	2-3
60	2-3	2-1	2-3	2-3	2-3	2-3
61	2-1	2-1	2-3	2-3	2-3	2-3
62	2-3	2-1	2-3	2-1	2-3	2-3
63	2-1	2-1	2-3	2-1	2-3	2-3
64	2-3	2-1	2-3	2-3	2-1	2-3
65	2-1	2-1	2-3	2-3	2-1	2-3
66	2-3	2-1	2-3	2-1	2-1	2-3
67	2-1	2-1	2-3	2-1	2-1	2-3
70	2-3	2-1	2-1	2-3	2-3	2-3
71	2-1	2-1	2-1	2-3	2-3	2-3
72	2-3	2-1	2-1	2-1	2-3	2-3
73	2-1	2-1	2-1	2-1	2-3	2-3
74	2-3	2-1	2-1	2-3	2-1	2-3
75	2-1	2-1	2-1	2-3	2-1	2-3
76	2-3	2-1	2-1	2-1	2-1	2-3
77	2-1	2-1	2-1	2-1	2-1	2-3

Table 12-3
Priority Jumper Installation

Priority	M8337 Install Jumper	M8335 Install Jumpers
9 (highest)	W1	P9 and P10
10	W2	P9′ and P10
11 (lowest)	W3	P9′ and P10′

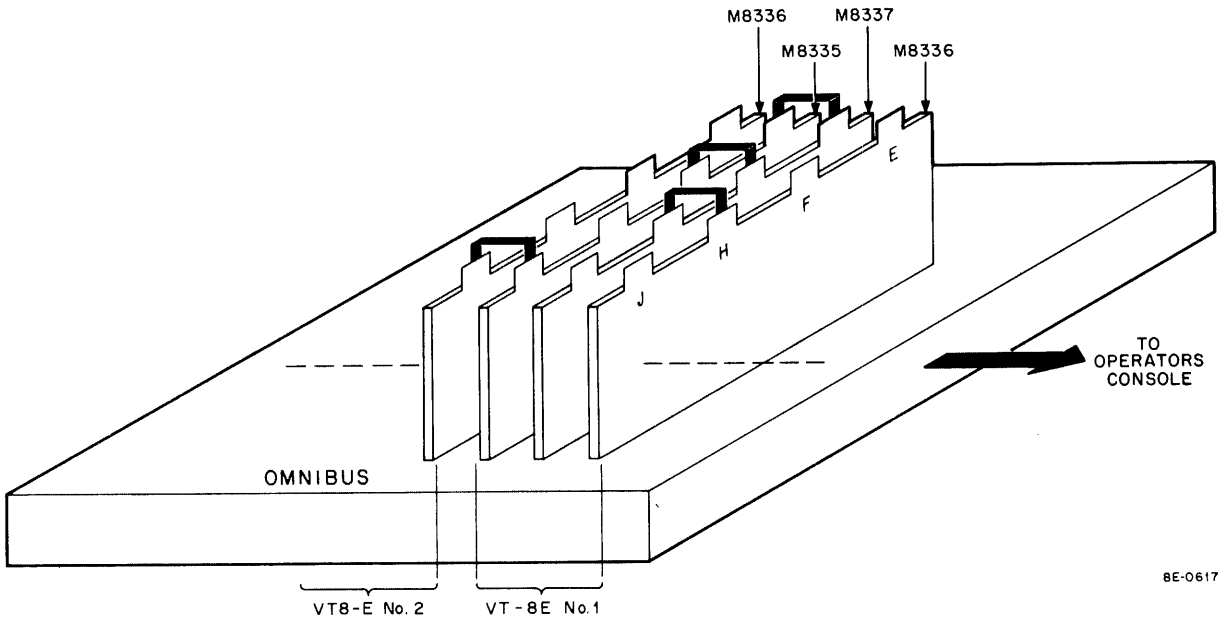


Figure 12-2 VT8-E Module Installation

12.2.3 Acceptance Test

The VT8-E is checked for proper operation by running the two diagnostic programs. Both MAINDECs referenced in the introductory remarks and the A-SP-VT8-E engineering specification give detailed instructions for their performance in the instructions shipped with the paper tapes. If problems arise, refer to the maintenance instructions, both in this manual and in Volume 1.

SECTION 3 OPERATION AND PROGRAMMING

This section provides a functional description of the VT8-E logic, operation and programming information, a list of IOT instructions, and some VT8-E programming examples.

12.3 FUNCTIONAL DESCRIPTION

The functional groups of logic in the VT8-E are described in the following paragraphs (Figure 12-3). Their purpose, location (on what module), and function are provided to familiarize the reader with VT8-E operation. A detailed description of VT8-E logic and timing is given in Chapter 4. Refer to Chapter 9 of the *Small Computer Handbook* – DEC, 1973 for information about data transfers via IOT instructions and data breaks. A detailed block diagram of the VT8-E showing data flow and the interrelationship of the functional groups is in the VT8-E Video Display Control Engineering Drawings.

12.3.1 VT8-E Printer/Keyboard Control Module (M8335)

The functional groups of logic on the M8335 module are discussed in the following paragraphs.

12.3.1.1 MD Bus Gating – Data from the MD lines is applied to the M8335 module by I/O PAUSE if IOT instructions are executed by the program or by MD EN during single cycle data breaks. Single cycle data break is the method used to transfer data between memory and the display control (Paragraph 12.3.4.1).

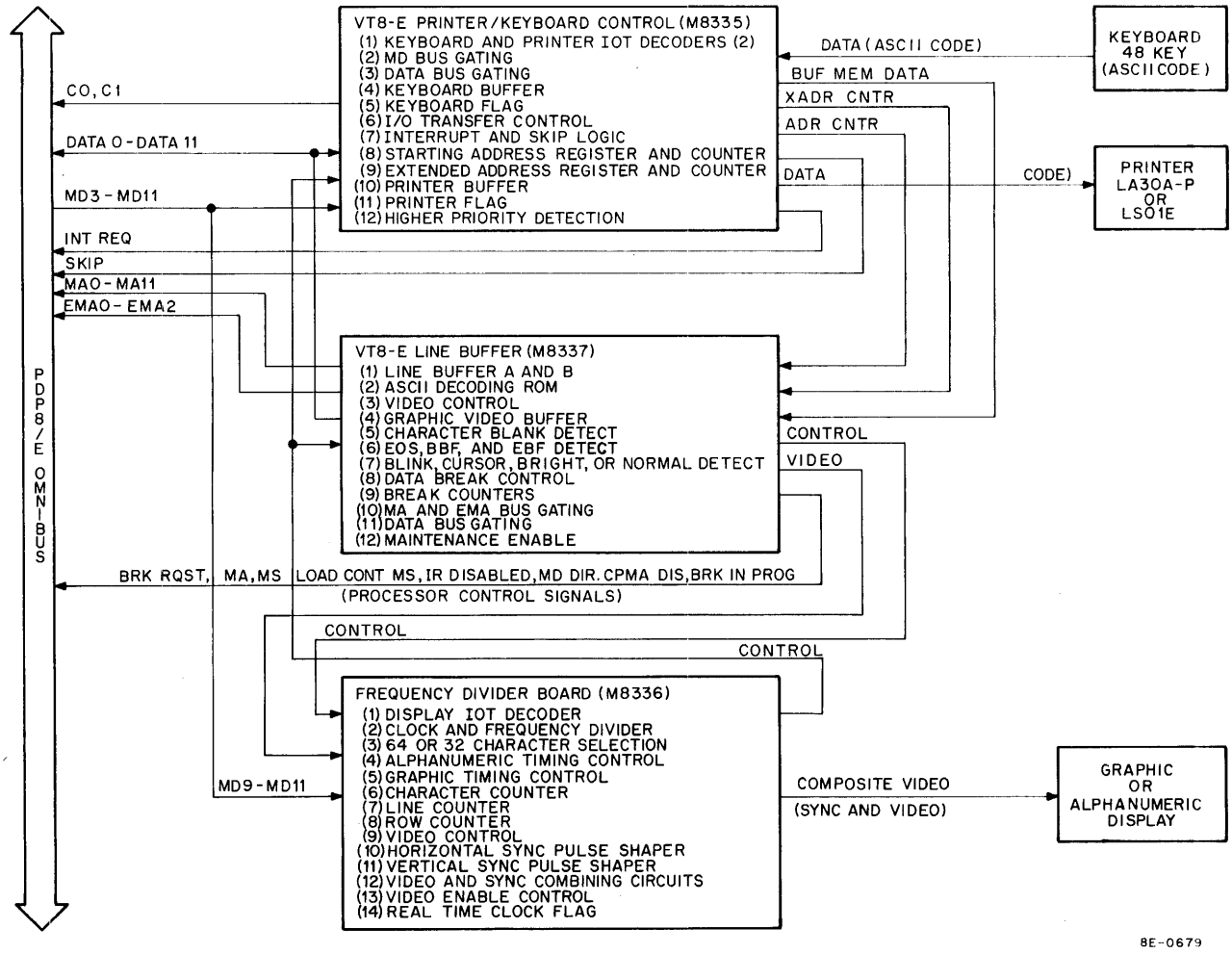


Figure 12-3 VT8-E Block Diagram

12.3.1.2 IOT Decoders – The M8335 module contains two IOT decoders, one for the printer and one for the keyboard. The decoders are assigned different device codes so that the printer IOT decoder is selected when printer IOTs are programmed, and the keyboard IOT decoder is selected when keyboard IOTs are programmed. The keyboard and printer may be assigned any two of the device codes listed in Table 12-2. The device codes assigned to the keyboard and printer must be different from each other and different from the display device code. The IOT decoders decode MD9–MD11 from the MD lines and generate control signals to control keyboard and printer operations; i.e., data transfers. The keyboard and printer instructions are listed in Paragraph 12.3.4.

12.3.1.3 Data Bus Gating – The Data Bus gates are enabled and DATA0–DATA11 are applied to the M8335 logic when the following occur:

a. If the program executes the PNPC or PNLP instructions to load the Printer Buffer.

b. If the program executes a DPLA instruction to load the Starting Address Register or a DPG0 instruction to load the Extended Starting Address Register.

c. During a single cycle data break, DATA 0 – DATA 8, 9, or 10 monitored by the VT8-E during data breaks to determine if the VT8-E has the highest priority for a data break.

12.3.1.4 Keyboard Buffer – The Keyboard Buffer receives a 7-bit ASCII code from the keyboard when one of the keys on the keyboard is pressed. The keyboard also generates a KEYBOARD STROBE which enables the 7-bit ASCII code to be transferred to the buffer and sets the KYBD flag. When the KYBD flag is set, an INT RQST is made if interrupts are enabled, or a SKIP if the DKSF instruction is executed by the program. An INT RQST or SKIP notifies the program that data in the Keyboard Buffer is available to be read into the AC. The program must transfer the data in the buffer to the AC and clear the KYBD flag so that a new 7-bit ASCII character can be transferred from the keyboard to the buffer.

12.3.1.5 I/O Transfer Control – The I/O transfer control logic determines the direction of data flow on the Data Bus and whether the AC is cleared or not. C0 and C1 (the C lines) are asserted by IOT instructions which transfer data to or from the AC.

12.3.1.6 Interrupt and Skip Logic – The interrupt and skip logic allows the program to enable the interrupts and generate an INT RQST when the KYBD and PRINT DONE flags are set or to check the flags using a SKIP instruction, i.e., the DKSF instruction.

12.3.1.7 Interrupt Logic – The keyboard and printer interrupt logic is enabled if bit 11 in the AC is set (1) when the DKIN instruction is executed by the program. If the interrupts are enabled, an INT RQST is made when the KYBD flag is set or the PRINT DONE flag is set. The KYBD flag is set when a keyboard key is pressed, and the PRINT DONE is set when the printer has finished printing a character.

12.3.1.8 Starting Address Register and Counter (SAR) – The Starting Address Register (SAR) is a 12-bit register that is loaded from the AC with the memory address of the first word to be transferred by the single cycle data break facility. The contents of SAR are transferred to the address counter after the DPG0 instruction is executed by the program and the counter is incremented at the end of each data break to select the next sequential memory address. The contents of the counter are applied to the Memory Address lines (MA0–MA11) to address a location in memory.

12.3.1.9 Extended Starting Address Register – The Extended Starting Address Register (XSAR) is loaded from bits 6, 7, and 8 of the AC by the DPG0 instruction. The contents of XSAR are transferred to the XADR COUNTER and used to select a field in memory for data transfers. The XADR COUNTER is incremented when the ADR COUNTER overflows to select the next memory field. At this time the ADR COUNTER starts reading memory locations in the newly selected memory field.

12.3.1.10 Printer Buffer – The Printer Buffer is a 7-bit register that is loaded from the AC by the PNLP instruction. The data from the AC contains a 7-bit ASCII code for a character to be printed. The seven data bits are transferred along with a PRINT STROBE pulse, and when the Print operation is completed, the PRINT DONE flag is set. If interrupts are enabled, an INT RQST is made at this time, or if the flag is checked by the PNSK instruction, the SKIP line is grounded. The program may perform a routine to transfer another character to the printer at this time.

12.3.1.11 PRINT DONE Flag – The PRINT DONE flag is set each time the printer completes a print operation to inform the program that the printer is ready to accept a new character.

12.3.1.12 Higher Priority Detection – The higher priority detection logic monitors the Data Bus to determine if the VT8-E has the highest priority for a data break. If there are any peripherals connected to the OMNIBUS that have a higher priority that the VT8-E, one of the lines on the Data Bus will be low to prevent the VT8-E from doing a data break. As an example, if the peripheral assigned the highest priority wants to do a data break, DATA 0 is asserted (low) and the VT8-E cannot do a data break until DATA 0 goes high at the completion of the other peripheral's data break. When the VT8-E is ready to do a data break, DATA 9 or DATA 10 will be asserted low to prevent peripherals with a lower priority from doing a data break before the VT8-E. As previously discussed, the VT8-E may be assigned one of the three lowest priorities.

12.3.2 VT8-E Line Buffer Module (M8337)

The functional groups of logic located on the VT8-E Line Buffer Module are discussed in the following paragraphs.

12.3.2.1 Line Buffers A and B – Line Buffers A and B provide temporary storage of 32 or 64 words from memory in the Alphanumeric mode or 32 words from memory in the Graphic mode. In the Alphanumeric mode the word from memory (Figure 12-7) selects the visible field, display mode, and character to be displayed. In the Graphic mode, the word from memory (16 words per line) consists of 1s (display a dot) and 0s (do not display a dot) to produce a line on the face of the CRT. The display mode (Alphanumeric or Graphic) is selected by bit 10 (0 → ALPHA and 1 → GRAPHIC) from the AC when the DPG0 instruction is executed by the program.

Each alphanumeric character is displayed on the face of the CRT in a 5 (width) X 7 (height) dot matrix. To display one row of characters (32 or 64 characters), the Display Monitor makes 10 horizontal sweeps across the face of the CRT. The first two scans are used to load the Line Buffers from memory via the Single Cycle Data Break. The third scan addresses a blank ROM location and the remaining seven scans display the alphanumeric data. The first of the seven scans displays the first line of each character in the row of characters to be displayed, the second scan the second line, etc., until seven scans are completed to display a row of characters (32 or 64). When the tenth scan is completed, the program must set up for a new break and initiate a new break cycle to reload the Line Buffers if additional rows of characters (20 maximum) are to be displayed. During the display operation the 7-bit ASCII code (Figure 12-7) is decoded by the ASCII decoding ROMS to generate the video signals to be displayed and the four control bits are decoded to determine the display mode and visible field. A display may be stopped after any number of characters have been displayed, if the display is less than 20 rows, to save computer time. This is done by setting CB1 and CB2 to 1s when the last character is displayed.

In the Graphic mode, data is displayed on the face of the CRT in a 189 (width) X 200 (height) dot matrix. Each line (189 dots) requires 16 12-bit words. The last three bits of the sixteenth word are not used. Each bit of the data word represents a dot or space on the face of the CRT. A logical 1 causes a dot and a logical 0 leaves a space. As an example, 16 words of data containing all 1s displays a row of dots on the face of the CRT. In the Graphic mode, 3200 (200 X 16) words must be defined because there is no way to generate End-of-Screen (EOS). If the full screen is not used, the remainder of the memory locations used should contain all 0s.

12.3.2.2 ASCII Decoding ROMs – The ASCII decoding ROMs decode the 7-bit ASCII code from the Line Buffers and generate a video signal for each line of each character to be displayed. After the start of a horizontal scan, data is shifted out of the Line Buffers to address (the buffer is in a recirculating mode, thus an end-around shift) a ROM character generator location and generate video for one line of the character. ROM character generator locations are addressed seven times (once for each horizontal scan). The video signals generated each time it is addressed are changed by the assertion of signals inside the ROM to change the video pattern and produce the desired character after seven scans. The video out of ROM (VIDEO1–VIDEO5) is applied to the Alphanumeric Video Buffer where it is shifted out to the Video Control logic as five serial video pulses. These pulses will cause dots or spaces to appear on the face of the CRT and after seven scans, an alphanumeric character is formed.

12.3.2.3 Graphic Video Buffer – In the Graphic mode, the contents of the Line Buffer are transferred one word at a time to the Graphic Video Buffer. From the Graphic Video Buffer the 12-bit word is converted to serial video pulses and applied to the Video Control logic. Dots are displayed for data 1s and spaces for data 0s.

12.3.2.4 Character Display Mode Detection Logic – The Character Display mode is determined by CB3 and CB4 (Figure 12-7) of the data word from memory. As shown in Figure 12-7, the character may be displayed in the Normal, Blink, Bold, or Cursor modes. The Mode Detection logic decodes CB3 and CB4 to assert the control signals necessary to select the four modes.

12.3.2.5 Visible Field Detection Logic – The visible field is determined by CB1 and CB2 (Figure 12-7) of the data word. As shown in Figure 12-7, the character may be displayed in the mode selected by CB1 and CB2 (NOP), a

blank field may be ended and the display enabled (EBL), a blank field may be started (BBF) or an End of Screen (EOS) may be selected to end the display. EOS is particularly helpful because it allows smaller displays to be displayed without using the entire core buffer. This saves core buffer space and reduces processor loading.

12.3.2.6 Single Cycle Data Break Control Logic – The single cycle data break control logic is used to force the processor into the Direct Memory Access (DMA) state and transfer data between core memory and the VT8-E Line Buffers via the Memory Data lines. Memory is addressed by the outputs of address and extended address counters, which are applied to the Memory Address lines at the beginning of the break cycle.

12.3.2.7 Processor Control Signals – When the processor is forced into the DMA state, the VT8-E must generate control signals to control the processor. The control signals required to accomplish this are shown in Figure 12-3 and explained in Chapter 9 of the *Small Computer Handbook* – DEC, 1973.

12.3.2.8 Break Counters – The break counters are used to count the words in a data transfer. The counters overflow after 32 words are transferred in the 32 character mode or after 64 words are transferred in the 64 character mode to stop data transfers and release the processor.

12.3.2.9 MA and EMA Bus Gates – The MA and EMA bus gates apply the contents of the address counter and extended address counter to the OMNIBUS MA lines during a data transfer. This allows the selection of a memory field and memory location to be used in a data transfer.

12.3.2.10 Data Bus Gates – The Data Bus gates are enabled when the DPMD instruction is executed by the program to transfer data to the Data Bus. This allows VT8-E registers and buffers to be read into the AC for display or evaluation by the program. To read the Display Buffers and Register with IOT instructions the Maintenance logic must be enabled.

12.3.2.11 Maintenance Enable – The maintenance logic is enabled by the DPSM instruction. This allows the program to read the VT8-E registers and buffers using the maintenance instructions. It also allows data breaks to be taken by the VT8-E at a rate determined by the program.

12.3.2.12 Frequency Divider Board (M8336) – The functional groups of logic on the M8336 module are discussed in the following paragraphs.

12.3.2.13 Display IOT Decoder – The display IOT decoder decodes the display instructions and generates the necessary control signals to set up for data breaks, maintenance operations, and data transfers using IOT instructions. The decoder is enabled when I/O PAUSE is asserted and the device code assigned to the display for this VT8-E is decoded and decodes bits MD9–MD11 of the IOT instruction. At this time, the C lines are asserted to control the direction of the data transfer, INTERNAL I/O is asserted to prevent the processor from performing other IOTs, and the instruction is executed by the VT8-E.

12.3.3 VT8-E Clock and Frequency Divider (M8336)

The VT8-E clock and frequency divider generates the necessary CRT sync pulses and control signals required to display data on the CRT. The timing chain consists of a 21.84 MHz crystal controlled oscillator and a chain of divide-by counters with selected outputs used to generate sync and control signals. Jumpers are provided to allow the selection of 64- or 32-character display control signals. These jumpers allow control signals of different frequencies to be selected for the display of 32 or 64 characters per row. The counters in the timing chain and their function are discussed in detail in Paragraph 12.4.2.2.

12.3.3.1 Real Time Clock Flag – The Real Time Clock flag is set (1) at the start of each vertical retrace. If interrupts are enabled, an interrupt request is made, or if a Skip instruction is being executed by the program, the SKIP bus is grounded and the program will skip an instruction.

12.3.3.2 Video and Sync Combining Circuits – The Video and Sync Combining circuits combine the horizontal and vertical sync with the video pulses from the ROM Character Generator to produce a composite video signal.

12.3.4 IOT Instructions

The following instructions are used to program the VT8-E.

12.3.4.1 Display Instructions – The display instructions assume device code 05 is used. There are 64 possible device codes which can be used (Table 12-2) for the display. The device code for the display, keyboard, and printer must be different (e.g., device code 03 for the keyboard, 04 for the printer, and 05 for the display). If more than one VT8-E is installed in the same system, three new device codes must be selected for the second VT8-E. They must also be different from each other and different from the device codes assigned to other PDP-8/E options installed in the system.

Load Starting Address Register (DPLA)

Octal Code: 6050

Operation: Transfer the contents of the AC to the Starting Address Register (SAR) and clear the AC. The AC must contain the address of the first memory location to be used in a data transfer. The contents of the SAR are transferred to the address counters and then incremented at the end of each single cycle data break. This allows the sequential selection of locations in memory for data transfers.

Load Extended Starting Address (DPGO)

Octal Code: 6051

Operation: Transfer the contents of AC10 and AC11 to the mode select logic, and AC6–AC8 to the Extended Starting Address Register (XSAR). AC10 and AC11 are used to select alphanumeric or graphic mode and enable or disable the interrupt system as follows:

AC10	AC11	
0	0	Alphanumeric Mode, Interrupt Disabled
0	1	Alphanumeric Mode, Interrupt Enabled
1	0	Graphic Mode, Interrupt Disabled
1	1	Graphic Mode, Interrupt Enabled

AC6–AC8 must contain the memory field to be used in a data transfer. The XADR COUNTER is incremented when the ADR COUNTER overflows at the end of each memory field to select the next memory field. The ADR COUNTER selects the first location (0000) in the new memory field. Data transfers may start immediately after this instruction is executed.

STOP the Display (DPSM)

Octal Code: 6052

Operation: Stop the display and inhibit video and VT8-E initiated data breaks. This instruction also transfers AC11 and AC6–AC8 from the AC to the maintenance logic and the Extended Starting Address Register. If AC11 is 1, the Extended Address Register is loaded with the contents of AC6–AC8. If AC11 is 0, the contents of the Starting Address Register are transferred to the address counters and the VT8-E is set up for a maintenance break. The AC must contain the memory field in AC6–AC8 and AC11 must be 1 or 0 to determine which operations are to be done before this instruction is executed.

Maintenance Instruction (DPMB)

Octal Code: 6053

Operation: Transfer the contents of the memory location specified by the Address Counter to the Data Buffer. The Address Counter is incremented by 1 to select the next location in memory.

Maintenance Instruction (DPMD)

Octal Code: 6054

Operation: Jam-transfer the contents of the Data Buffer to the AC. Note that the DPMB and DPMS may be used to transfer data from memory to the Data Buffer and then to the AC where it is displayed. This could aid in troubleshooting the VT8-E.

Maintenance Instruction (DPMS)

Octal Code: 6055

Operation: Transfer the contents of the Extended Address Counter to AC6–AC8 and the state of the SENSE switch into AC0 (Figure 12-4). This allows the program to determine what memory field is selected and determine the condition of the SENSE switch. Bit 0 is a logical 1 when the SENSE switch is on and a logical 0 when the SENSE switch is off. This switch is located on the keyboard and the programmer determines its use and meaning.

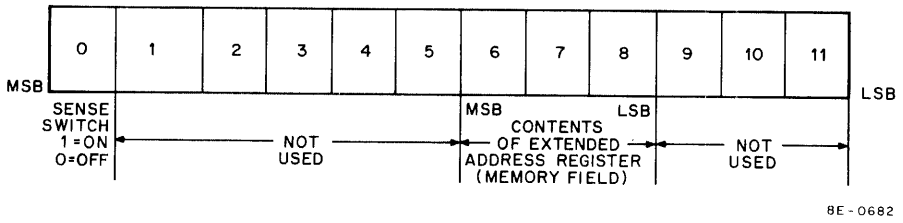


Figure 12-4 Extended Address and Sense Switch Data

Skip On Real Time Clock Flag (DPCL)

Octal Code: 6056

Operation: Skip the next instruction if the Real Time Clock flag is set (1) and clear the flag. Real Time Clock flag is set at the start of each vertical retrace.

Generate A Bell Tone (DPBL)

Octal Code: 6057

Operation: Generate a half-second audible tone for use as a bell. This tone can be heard by the operator and can be used to alert the operator that he must respond; i.e., supply data to the program via the keyboard.

12.3.4.2 Keyboard Instructions – The keyboard instructions assume a device code of 03 has been selected for the keyboard.

Clear Keyboard Flag (DKCF)

Octal Code: 6030

Operation: Clear the Keyboard flag. The Keyboard flag is set when the Keyboard transmitter is ready to transfer data, usually after one of the keyboard keys has been pressed.

Skip on Keyboard Flag (DKSF)

Octal Code: 6031

Operation: Skip the next sequential instruction if Keyboard flag is set. Keyboard flag sets when one of the keyboard keys has been pressed to supply data to the program.

Clear Keyboard Flag and AC (DKCC)

Octal Code: 6032

Operation: Clear the Keyboard flag and the AC.

Logically OR Keyboard Buffer and the AC (DKOB)

Octal Code: 6034

Operation: Logically OR the contents of the Keyboard Buffer with AC5—AC11, deposit the result in AC5—AC11, and transfer a 1 to AC4. AC0—AC03 remain unchanged. When DKOB is combined with the CLA instruction, the contents of the Keyboard Buffer are transferred to AC5—AC11.

Enable Keyboard Printer Interrupt (DKIN)

Octal Code: 6035

Operation: Enable Keyboard Printer interrupt if AC11 = 1 or disable if AC11 = 0. AC11 must be set to 1 or 0 before this instruction is executed by the program.

Read Keyboard Buffer (DKRB)

Octal Code: 6036

Operation: Jam-transfer the contents of the Keyboard Buffer to AC5—AC11 (Figure 12-5), set AC4 to 1, clear AC0—AC3, and clear the Keyboard flag. AC5—AC6 contains a 7-bit ASCII code which represents the key pressed on the keyboard.

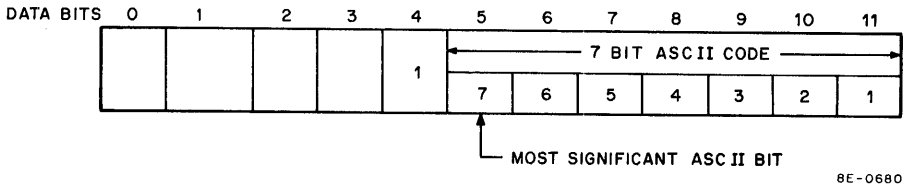


Figure 12-5 Keyboard Data Format

12.3.4.3 Printer Instructions – The following instructions assume a device code of 04 is used for the printer.

Set Printer Flag (PNSF)

Octal Code: 6040

Operation: Set the Printer flag

Skip on Print Done Flag (PNSK)

Octal Code: 6041

Operation: Skip the next sequential instruction if the Print DONE flag is set.

Clear Printer Flag (PNCF)

Octal Code: 6042

Operation: Clear the Printer flag.

NOTE
Octal Code 6043 is not used.

Load Printer Buffer (PNLP)

Octal Code: 6044

Operation: Load the Printer Buffer from AC5–AC11 (Figure 12-6) and Print. AC5–AC11 contains a 7-bit ASCII code which determines the character to be printed.

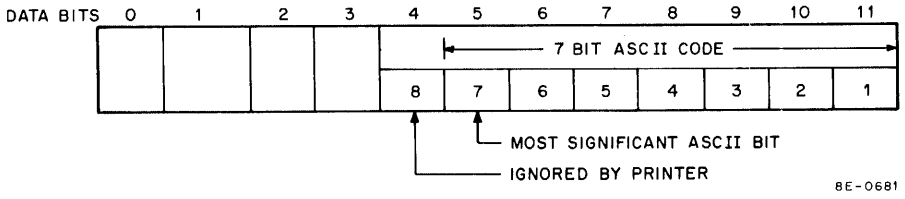


Figure 12-6 Printer Data Format

Skip on Keyboard or Printer Interrupt (PNSI)

Octal Code: 6045

Operation: Skip if the interrupt is enabled and either the Keyboard or Print DONE flag is set.

Load Printer Buffer (PNPC)

Octal Code: 6046

Operation: Load Printer Buffer from AC5—AC11 (Figure 12-6), Clear Print DONE flag, and Print. The 7-bit ASCII code determines the character to be printed.

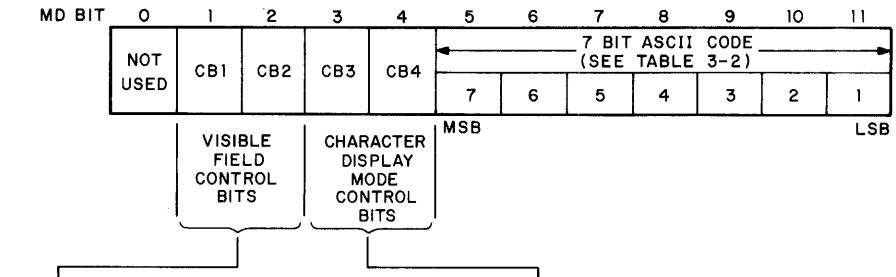
12.3.5 Display Data Format

The two types of data that can be displayed on the VT8-E CRT are alphanumeric and graphic data.

12.3.5.1 Alphanumeric Data Format – Alphanumeric data displayed on the CRT is determined by the 12-bit word (Figure 12-7) transferred from memory during a Single Cycle Data Break. This word determines the visible field, character display mode, and the character to be displayed as shown in Figure 12-6. The VT8-E can display 20 lines of alphanumeric information; 64 normal sized characters or 32 enlarged characters can be displayed on each line.

NOTE

EOS allows termination of the display and LF code 012 allows termination of the current row. Both termination methods save core memory and computer time for display with less than 20 lines.



CB1	CB2	VISIBLE FIELD CONTROL BITS	
0	0	NOP	IF IN VISIBLE FIELD, DISPLAY CHARACTER IN BITS 5-11 ACCORDING TO CB1, CB2.
0	1	EBF	END BLANK FIELD. ENABLE VIDEO STARTING WITH THIS CHARACTER.
1	0	BBF	BEGIN BLANK FIELD. DISABLE VIDEO FOR THIS CHARACTER AND THOSE FOLLOWING. BLANK FIELD CAN BE TERMINATED BY EBF CONTROL CODE.
1	1	EOS	END OF SCREEN. THE PREVIOUS CHARACTER IS THE LAST TO APPEAR ON THE SCREEN. VIDEO AND DATA BREAKS ARE INHIBITED UNTIL THE NEXT VERTICAL RETRACE. THIS ALLOWS ABREVIATED DISPLAY BUFFERS WHEN IT IS NOT DESIRED TO USE THE ENTIRE SCREEN. THIS SAVES CORE BUFFER SPACE AND REDUCES PROCESSOR LOADING.

CB3	CB4	CHARACTER DISPLAY MODE CONTROL BITS	
0	0	NORMAL	DISPLAY THE CHARACTER IN BITS 5-1 AT NORMAL INTENSITY IF IN VISIBLE ZONE.
0	1	BLINK	BLINK THIS CHARACTER AT A 1.9Hz RATE (1.6Hz FOR 50Hz SYSTEMS) IF IN VISIBLE ZONE.
1	0	BOLD	DISPLAY THIS CHARACTER AT INCREASED INTENSITY IF IN VISIBLE ZONE.
1	1	CURSOR	DISPLAY THIS CHARACTER AS A CURSOR IF IN A VISIBLE ZONE. THE CHARACTER AND ITS DOT MATRIX COMPLEMENT ARE DISPLAYED ALTERNATLY AT A 3.7Hz RATE (3.1Hz FOR 50Hz SYSTEMS).

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Figure 12-7 Alphanumeric Display Data Format

12.3.5.2 Graphic Data Format – The VT8-E is capable of displaying graphic information on a 189 (width) X 200 (height) dot matrix. Each dot position corresponds to a bit of a data word in the core buffer. The first word of the buffer defines the first 12 dots on the first row. Bit 0 is the first to be displayed and bit 11 the last. If a bit is set to 1, a dot is displayed and if it is set to 0, no dot is displayed. Sixteen 12-bit words are required to display one line of graphic data. The last 3 bits of the sixteenth word are not used. As an example, 16 words of all 1s (7777) from memory would cause a line of 189 dots to be displayed on the face of the CRT. In the Graphic mode there is no way to terminate the buffer short of 3200 words (200 lines), thus the entire buffer must be defined even if a major portion is blank.

12.3.6 Display Monitor and Keyboard Switches and Controls

12.3.6.1 Display Monitor Switches and Controls – Table 12-4 lists the switches and controls found on the display monitor enclosure.

Table 12-4
Switches and Controls

Control/Switch	Location	Function
CONTRAST Control	Right-hand side	Used to adjust the picture for contrast.
BRIGHTNESS Control	Right-hand side	Used to adjust the CRT brightness (intensity).
VERTICAL Control	Right-hand side	Used to synchronize the raster in the vertical direction.
HORIZONTAL Control	Right-hand side	Used to synchronize the raster in the horizontal direction.
ON/OFF Switch	Keyboard upper-right corner	Applies primary power when in the ON position.
115V/230V	Right-hand side of CRT frame	Selects 115V or 230V as primary power for the display.
AC Circuit Breaker pushbutton	Rear panel	Resets circuit breaker after momentary fault (do not hold in).
SENSE switch	Keyboard lower-right corner	Use determined by the programmer ON = logical 1 OFF = logical 0

12.3.6.2 Keyboard Controls – The basic function of the keyboard is to provide a convenient, on-line method of transmitting ASCII-coded characters to the CPU for processing and, perhaps, display on the VT8-E CRT screen. The keyboard transmits an ASCII code directly to the computer each time a key is pressed, and the computer, in turn, may transmit the character code to the VT8-E control logic. The control logic determines if the received data is to be displayed or used to control the displayed text format.

The keyboard can transmit either full ASCII or a 97-character subset. The selected code is determined by an internal selector switch. With the switch set to position 1, the keyboard transmits the full ASCII character set listed in Table 12-5. With the internal switch set to position 2, the keyboard transmits the 97-character ASCII subset listed in Table 12-6.

The VT8-E Display Monitor does not display lower case alphabetical characters. However, it can receive both upper and lower case characters, which are interpreted and displayed as upper case characters (Table 12-7).

Table 12-5
VT8-E Transmit Codes – Full ASCII Operation

Bit No. 7 6 5 4 3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0 0 0 0			space	0	@	P		p
0 0 0 1			!	1	A	Q	a	q
0 0 1 0			"	2	B	R	b	r
0 0 1 1			#	3	C	S	c	s
0 1 0 0			$	4	D	T	d	t
0 1 0 1			%	5	E	U	e	u
0 1 1 0			&	6	F	V	f	v
0 1 1 1			'	7	G	W	g	w
1 0 0 0	C← (BS)	C→	(	8	H	X	h	x
1 0 0 1	HT		)	9	I	Y	i	y
1 0 1 0	LF	C↑	*	:	J	Z	j	z
1 0 1 1	C↓	ALT	+	;	K	[	k	{
1 1 0 0			,	<	L	\	l	|
1 1 0 1	CR	HOME	-	=	M	]	m	}
1 1 1 0		ERASE LINE	.	>	N	^	n	~
1 1 1 1		ERASE SCREEN	/	?	O	_	o	DEL (rub out)

CTRL

Shifted

Table 12-6
VT8-E Transmit Codes – Half ASCII Operation
(switch in position 2)

Bit No. 7 6 5 / 4 3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 (0) 0	1 1 (0) 1
0 0 0 0			space	0	@	P	@	P
0 0 0 1			!	1	A	Q	A	Q
0 0 1 0			"	2	B	R	B	R
0 0 1 1			#	3	C	S	C	S
0 1 0 0			$	4	D	T	D	T
0 1 0 1			%	5	E	U	E	U
0 1 1 0			&	6	F	V	F	V
0 1 1 1			'	7	G	W	G	W
1 0 0 0	C← (BS)	C→	(	8	H	X	H	X
1 0 0 1	HT		)	9	I	Y	I	Y
1 0 1 0	LF	C↑	*	:	J	Z	J	Z
1 0 1 1	C↓		+	;	K	[	K	[
1 1 0 0			,	<	L	\	L	\
1 1 0 1	CR	HOME	-	=	M	]	M	ALT
1 1 1 0		ERASE LINE	.	>	N	^	N	^
1 1 1 1		ERASE SCREEN	/	?	O	_	O	DEL (rub out)

Shifted

Table 12-7
VT8-E Receiving Codes

Bit No. 7 6 5 4 3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0 0 0 0	@	P	space	0	@	P	space	0
0 0 0 1	A	Q	!	1	A	Q	!	1
0 0 1 0	B	R	"	2	B	R	"	2
0 0 1 1	C	S	#	3	C	S	#	3
0 1 0 0	D	T	$	4	D	T	$	4
0 1 0 1	E	U	Z	5	E	U	%	5
0 1 1 0	F	V	&	6	F	V	&	6
0 1 1 1	G	W	'	7	G	W	'	7
1 0 0 0	H	X	(	8	H	X	(	8
1 0 0 1	I	Y	)	9	I	Y	)	9
1 0 1 0	CR/LF	Z	*	:	J	Z	*	:
1 0 1 1	K	[	+	;	K	[	+	;
1 1 0 0	L	\	,	<	L	\	,	<
1 1 0 1	M	]	-	=	M	]	-	=
1 1 1 0	N	^	.	>	N	^	.	>
1 1 1 1	O	_	/	?	O	_	/	?

12.3.7 Programming Examples

The following VT8-E programming examples are programs that may be used to display alphanumeric or graphic data on the CRT.

12.3.7.1 Graphic Display Program Example – This program displays data from the Switch Register in a 189 X 200 dot matrix. A dot is displayed for those bits on the Switch Register that are set to 1s and a space is displayed for those bits in the Switch Register that are set to 0.

Memory Location	Instruction	Mnemonic			Operation
0200	6007	VTGRPH,	CAF		/CLEAR AND INITIALIZE.
0201	1216		TAD	BUF	/LOAD THE STARTING ADDRESS
0202	6050		DPLA		/OF THE DISPLAY BUFFER INTO THE VT8-E.
0203	1221		TAD	K2	/CODE FOR GRAPHIC
0204	6051		DPGO		/DISPLAY IN GRAPHIC MODE.
0205	1217	VT,	TAD	BUFM1	/SET AUTO INDEX FOR STORING
0206	3010		DCA	10	/THE DATA IN THE SR.
0207	1222		TAD	M6200	/LENGTH OF DISPLAY BUFFER
0210	3220		DCA	COUNT	/SET COUNTER FOR FILLING BUFFER.
0211	7604		LAS		/READ DATA PATTERN FROM THE SR.
0212	3410		DCA I	10	/STORE IN BUFFER
0213	2220		ISZ	COUNT	/BUFFER FILLED.
0214	5211		JMP	.-3	/NO, CONTINUE FILLING IT.
0215	5205		JMP	VT	/RELOAD BUFFER AGAIN.
0216	0400	BUF,	400		/STARTING ADDRESS OF BUFFER.
0217	0377	BUFM1,	400-1		/STARTING ADDRESS OF BUFFER -1.
0220	0000	COUNT,	0		/COUNTER FOR FILLING BUFFER.
0221	0002	K2,	2		/GRAPHIC ENABLE WORD.
0222	1600	M6200,	-6200		/COUNT FOR FILLING BUFFER.
			$		

12.3.7.2 Alphanumeric Display Program Example – This program echos the character typed on the console keyboard on the VT8-E display. The Switch Register is ORed with the character to display the character in the Normal, Blink, Bright, or Cursor mode. The display mode is selected from the Switch Register (Figure 12-7) as follows:

0000	Normal
0200	Blink
0400	Bright
0600	Cursor

Memory Location	Instruction	Mnemonic			Operation
0200	6007	VTALPH,	CAF		/CLEAR AND INITIALIZE.
0201	1233		TAD	BUFM1	/ADDRESS OF BUFFER -1.
0202	3010		DCA	10	/SET AUTO INDEX FOR POSITIONING
					/THE END OF SCREEN CHARACTER.
0203	1233		TAD	BUFM1	/ADDRESS OF BUFFER -1.
0204	3011		DCA	11	/SET AUTO INDEX FOR STORING CHARACTERS.
0205	1235		TAD	EOS	/GET THE END-OF-SCREEN CHARACTER (3000).
0206	3410		DCA I	10	/PUT END OF SCREEN IN DISPLAY BUFFER AREA.
0207	1240		TAD	M2400	/SET COUNTER SO PROGRAM IS RESTARTED
0210	3234		DCA	COUNT	/AFTER A FULL SCREEN IS DISPLAYED.
					/(64 CHARACTER MODE)
0211	1232		TAD	BUF	/LOAD THE STARTING ADDRESS
0212	6050		DPLA		/OF THE DISPLAY BUFFER INTO THE VT8-E.
0213	6051		DPGO		/GO DISPLAY.
0214	6031	INPUT,	KSF		/CHARACTER YET
0215	5214		JMP	.-1	/NO, WAIT.
0216	6036		KRB		/READ THE CHARACTER.
0217	0236		AND	K177	/KEEP ONLY 7 BITS.
0220	7421		MQL		/SAVE IN THE MQ REGISTER.
0221	1235		TAD	EOS	/MOVE THE END-OF-SCREEN
0222	3410		DCA I	10	/CHARACTER UP ONE IN THE BUFFER.
0223	7604		LAS		/READ DISPLAY MODE CONTROL BITS
					/FROM THE SR.
0224	0237		AND	K600	/SAVE ONLY THE CONTROL BITS.
0225	7501		MQA		/"OR" THE CHARACTER WITH THEM.
0226	3411		DCA I	11	/STORE CHARACTER WITH CONTROL BITS.
0227	2234		ISZ	COUNT	/FULL SCREEN (64 CHAR MODE)?
0230	5214		JMP	INPUT	/NO, GET ANOTHER CHARACTER.
0231	5200		JMP	VTALPH	/YES, RESTART THE PROGRAM.
0232	0400	BUF,	400		/STARTING ADDRESS OF BUFFER.
0233	0377	BUFM1,	400-1		/STARTING ADDRESS OF BUFFER -1.
0234	0000	COUNT,	0		/FULL SCREEN COUNTER.
0235	3000	EOS,	3000		/END-OF-SCREEN CHARACTER.
0236	0177	K177,	177		/7 BIT MASK.
0237	0600	K600,	600		/CONTROL BIT MASK.
0240	5400	M2400,	-2400		/LENGTH OF BUFFER.

SECTION 4 DETAILED LOGIC DESCRIPTION

12.4 INTRODUCTION

A simple block diagram of the VT8-E Video Display and Control is shown in Figure 12-8. The interface supplies the monitor with video and sync signals, and an audio tone. The video is either alphanumeric character information or graphic information, or a combination of the two that is made possible by switching the display mode at the screen refresh rate.

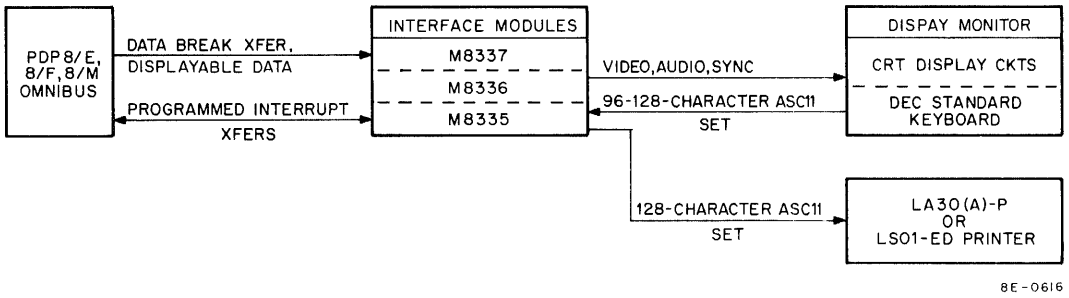


Figure 12-8 VT8-E Functional Block Diagram

The keyboard transfers data directly to the computer's AC Register by program interrupts or flags. Each character code transmitted can either be displayed or used to control the displayed text format. Data transmitted to the system printer is also transferred by program interrupts or flags. When the Interrupt System is disabled, flags are checked by the SKIP instructions.

The logic description is divided into two parts: one part concentrates on the interface logic for both the keyboard/printer and the display, while the second part concentrates on the keyboard and CRT circuits.

12.4.1 Keyboard/Printer Logic

A block diagram of the VT8-E Keyboard/Printer logic is shown in Figure 12-9. Pin assignments for OMNIBUS signals and connector signals can be found on Engineering Drawing E-CS-M8335-0-1.

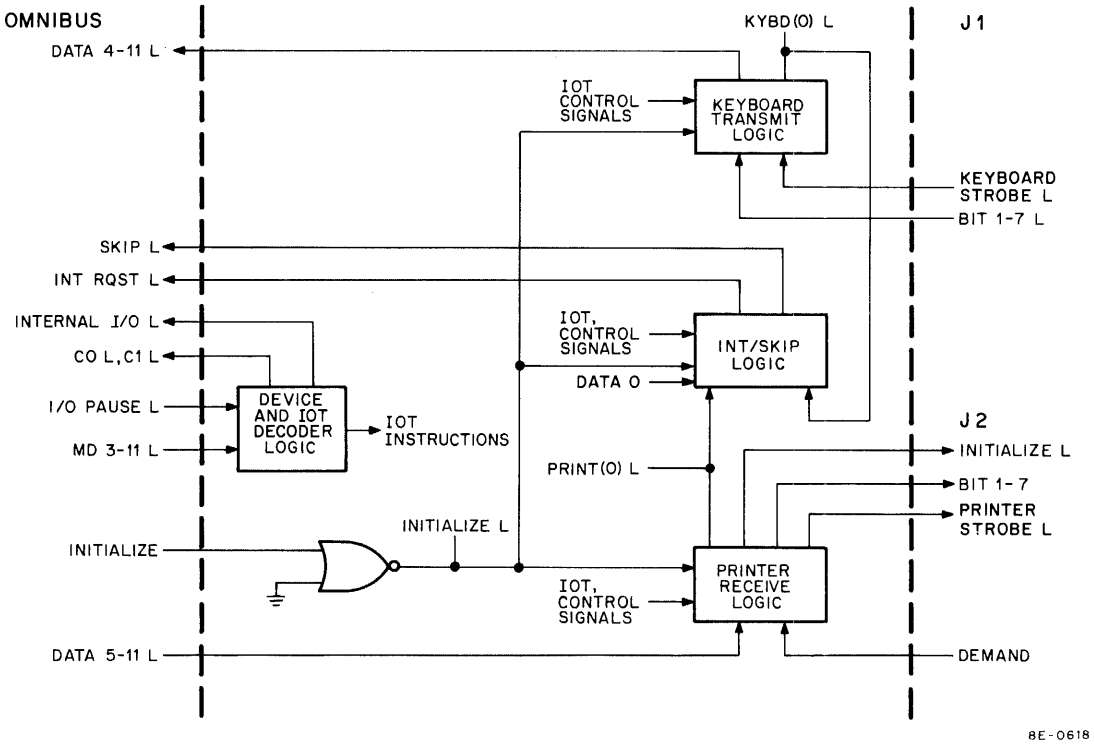


Figure 12-9 Printer/Keyboard Block Diagram

The VT8-E Keyboard/Printer logic has two distinct functions: transfer of data from the CPU AC Register to the Printer Buffer Register and transfer of data from the Keyboard Register to the AC Register. The transfer of data to the Printer Buffer is carried out by the Printer Receive logic. When the printer is able to receive data, it asserts the DEMAND signal. This signal sets the PRNT FLG flip-flop in the Printer Receive logic. The resulting PRNT (0) L signal causes the INT/SKIP logic to assert the OMNIBUS INT RQST L signal, if the VT8-E has been logically connected to the interrupt system. Alternatively, PRNT (0) L can be tested by a program skip instruction in the INT/SKIP logic. In either case, the computer ultimately proceeds to a program subroutine that begins the data transfer. When this subroutine is executed, the information is transferred from the AC Register to the DATA 5–11 lines and clocked into a 7-bit register in the Printer Receive logic. The register outputs are available at J1 as the BIT 1–7 signals. The logic then generates a PRINTER STROBE L signal that clocks the BIT 1–7 data into the Printer Buffer Register, clears the PRNT FLG flip-flop, and causes the printer to negate the DEMAND signal.

The transfer of data from the Keyboard Buffer Register to the AC Register is carried out by the Keyboard Transmit logic. When a keyboard key is pressed, information is applied, via the BIT 1–7 lines, to a 7-bit register in the Keyboard Transmit logic. When the keyboard generates a KEYBOARD STROBE L signal, the information is clocked into the 7-bit register and the KYBD FLG flip-flop is set. The KYBD (0) L signal can be tested in the INT/SKIP logic with a SKIP instruction, or the interrupt system can be used to cause the program to enter an appropriate subroutine. When the subroutine is executed, the information is gated from the register in the Keyboard Transmit logic to lines DATA 5–11 (the logic asserts the DATA 4 L signal separately so that the input character is compatible with the modified-ASCII Teletype code), then to the AC Register. The AC is loaded and, simultaneously, the KYBD FLG flip-flop is cleared.

12.4.1.1 IOT Decoder Logic – The IOT Decoder logic is shown in Figure 12-10, which includes the Video Display Decoding logic for reference. The VT8-E Keyboard/Printer uses 12 IOT instructions, 6 for the keyboard and 6 for the printer. (One of the listed printer IOTs, Skip on Printer or Keyboard Interrupt, apply to both functions and one of the keyboard IOTs, Interrupt Enable/Disable.) More than one keyboard/printer can be interfaced to the PDP-8/E at the same time. The VT8-E (or other control module) associated with each keyboard/printer must be assigned a unique device selection code for both the keyboard and the printer. Therefore, the M8335 module is fabricated with jumpers and solder terminals that allow the user to assign any one of 64 possible device selection codes to both the keyboard and the printer (care should be taken when assigning device selection codes to preclude multiple assignments of the same code). Figure 12-10 illustrates the octal codes and mnemonics that pertain when the VT8-E is manufactured. The octal codes and mnemonics for the instructions are listed in Paragraph 12.3.2. A complete list of device codes and the jumpers required to select each device code is shown in Table 12-2.

12.4.1.2 Printer Receive Logic – The Printer Receive logic is shown in Figure 12-11. Significant signals are related by the timing diagram in Figure 12-12. Refer to both figures when reading the logic description.

The printer routine is initiated by DEMAND changing to the true state, indicating that the printer is ready for another character. This sets the PRNT flag flip-flop. This flip-flop can also be set by the PNSF instruction at TP3 time. If the VT8-E is logically connected to the interrupt system, as this discussion assumes, the PRNT FLG (1) L signal causes the INT/SKIP logic to assert the OMNIBUS INT RQST L signal. The program proceeds to an interrupt servicing routine to determine the identity of the requesting device. The PNSI instruction in the routine causes the program to jump to a VT8-E routine that determines whether the printer or keyboard requested the interrupt (other options are open to the programmer, this is but one example). Ultimately, the VT8-E printer routine executes the PNPC instruction.

During TS2 of the PNPC instruction, information is gated from the AC Register to the DATA lines and remains on the DATA lines through TS3. When PNPC L is decoded in the IOT Decoder logic, it enables NOR gates E25C and E25D (Figure 12-11). NOR gate E25-D asserts the DATA EN signal; both DATA EN A L and DATA EN B L are derived from this signal. The difference between the DATA EN A L and DATA EN B L signals is significant only when considering the Display logic; for the present one must know only that one of these two signals gates lines DATA 9 and DATA 10 to the 7-bit register. The remaining DATA lines are gated to the register flip-flops as shown.

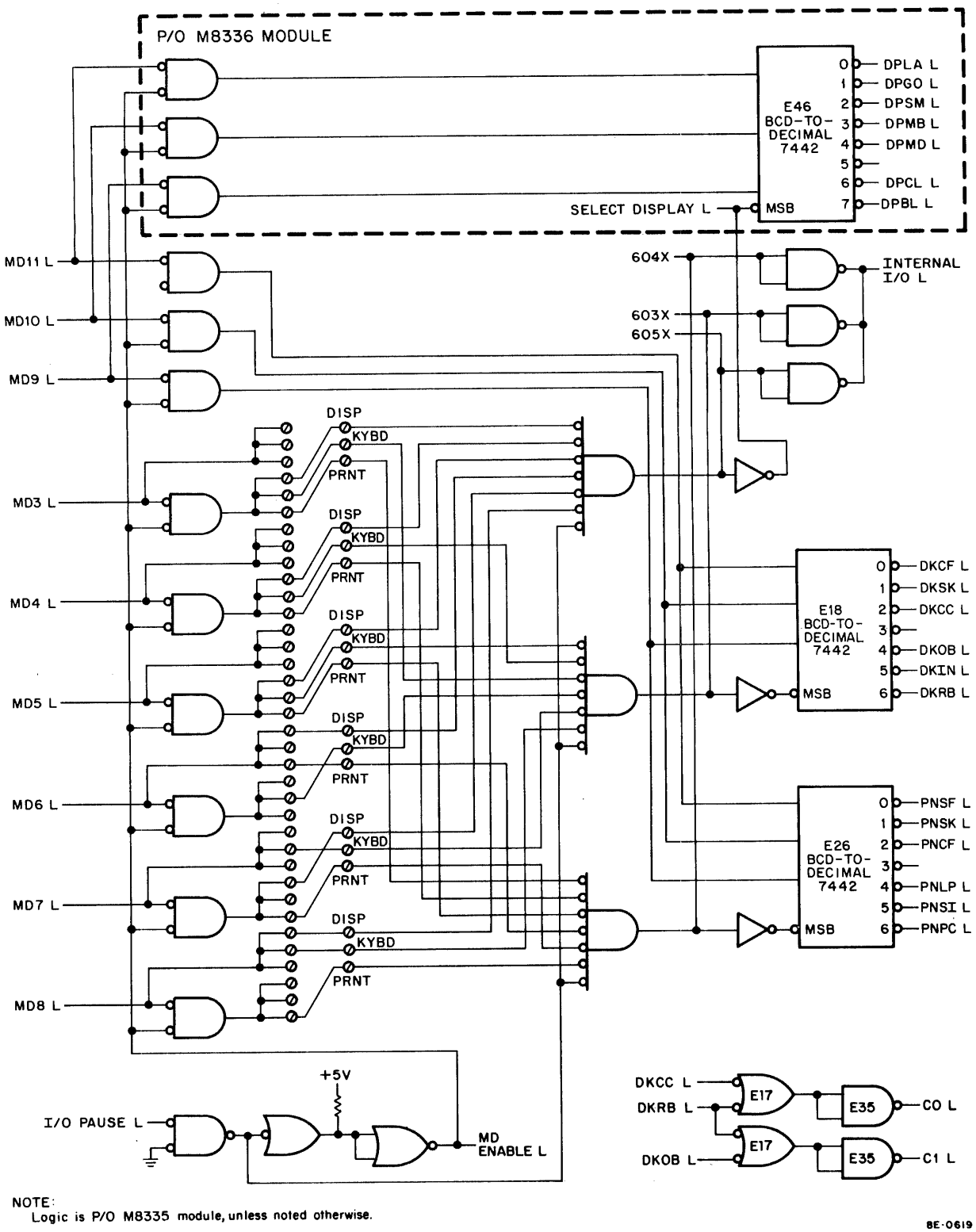


Figure 12-10 IOT Decoder Logic

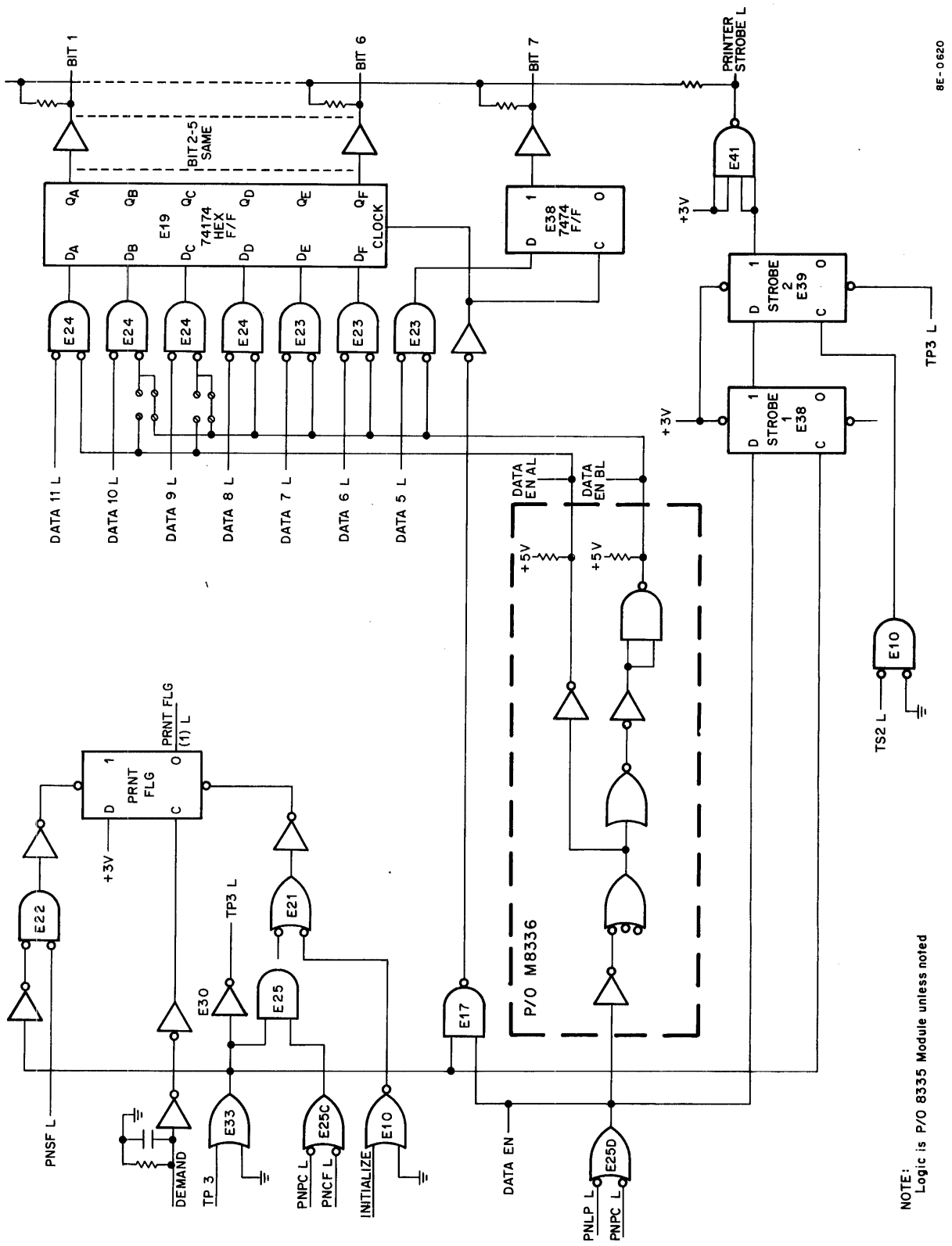
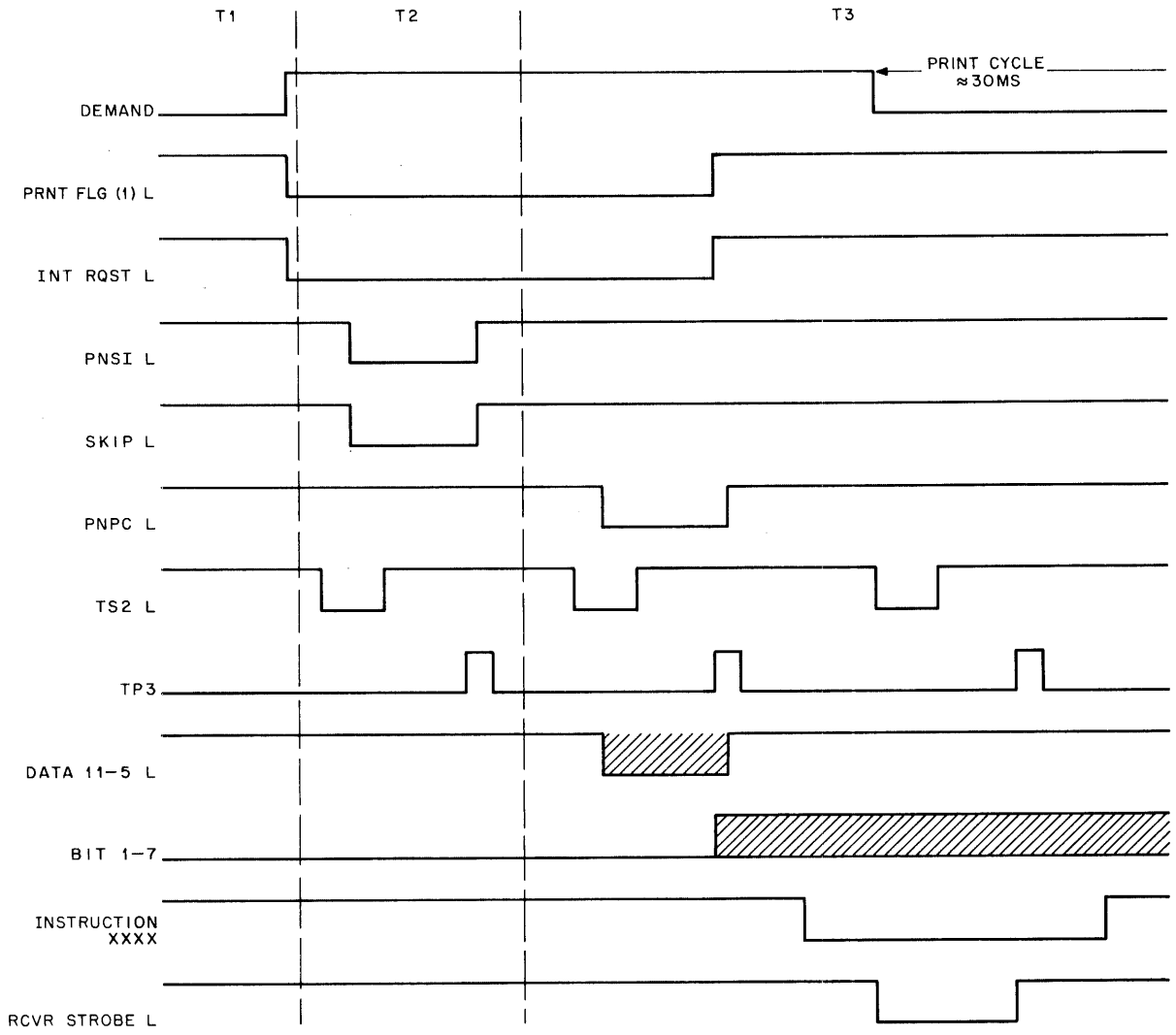


Figure 12-11 Printer Receive Logic

At TP3 time of the instruction, NAND gate E-17 is enabled and the information on the DATA lines is clocked into the 7-bit register. Simultaneously, flip-flop STROBE 1 sets and the PRNT FLG flip-flop is cleared. The register data is applied, via the BIT 1–7 lines, to the Printer Buffer Register. At the beginning of TS2 of the instruction following PNPC, flip-flop STROBE 2 sets and asserts PRINTER STROBE L. This signal loads the Printer Buffer Register and negates the DEMAND signal. Both STROBE 1 and STROBE 2 are cleared by the next TP3. When the print cycle ends approximately 30 ms later, the DEMAND signal is again asserted and a new transfer can be started.



NOTE:
T1, T2 and T3 are distinct time periods.
The amount of time between periods is
a function of program-routine execution time.

8E-0621

Figure 12-12 Printer Receive Logic Timing

12.4.1.3 Keyboard Transmit Logic – The Keyboard Transmit logic is shown in Figure 12-13. Significant signals are related by the timing diagram in Figure 12-14. Refer to both figures when reading the logic description.

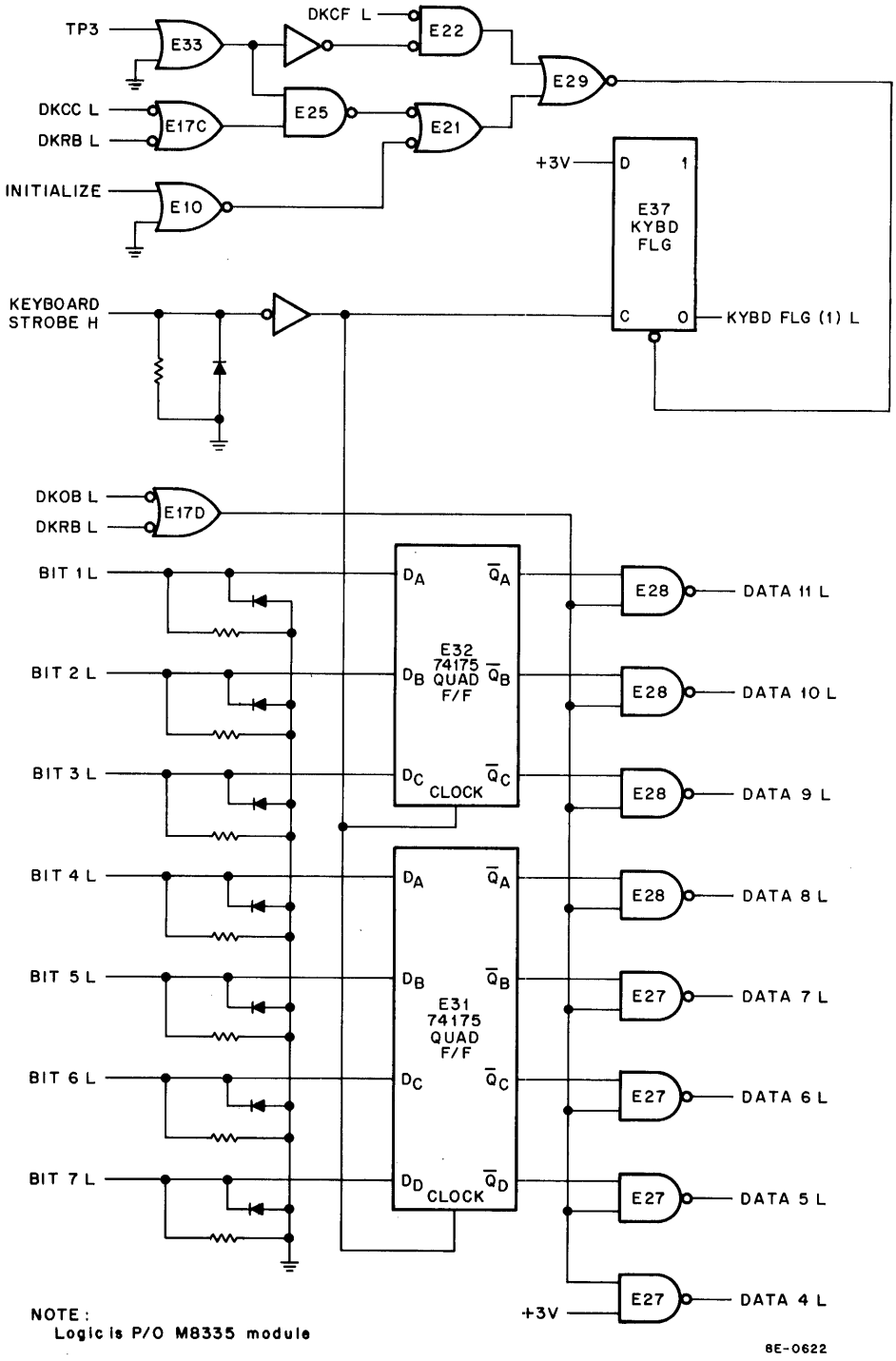


Figure 12-13 Keyboard Transmit Logic

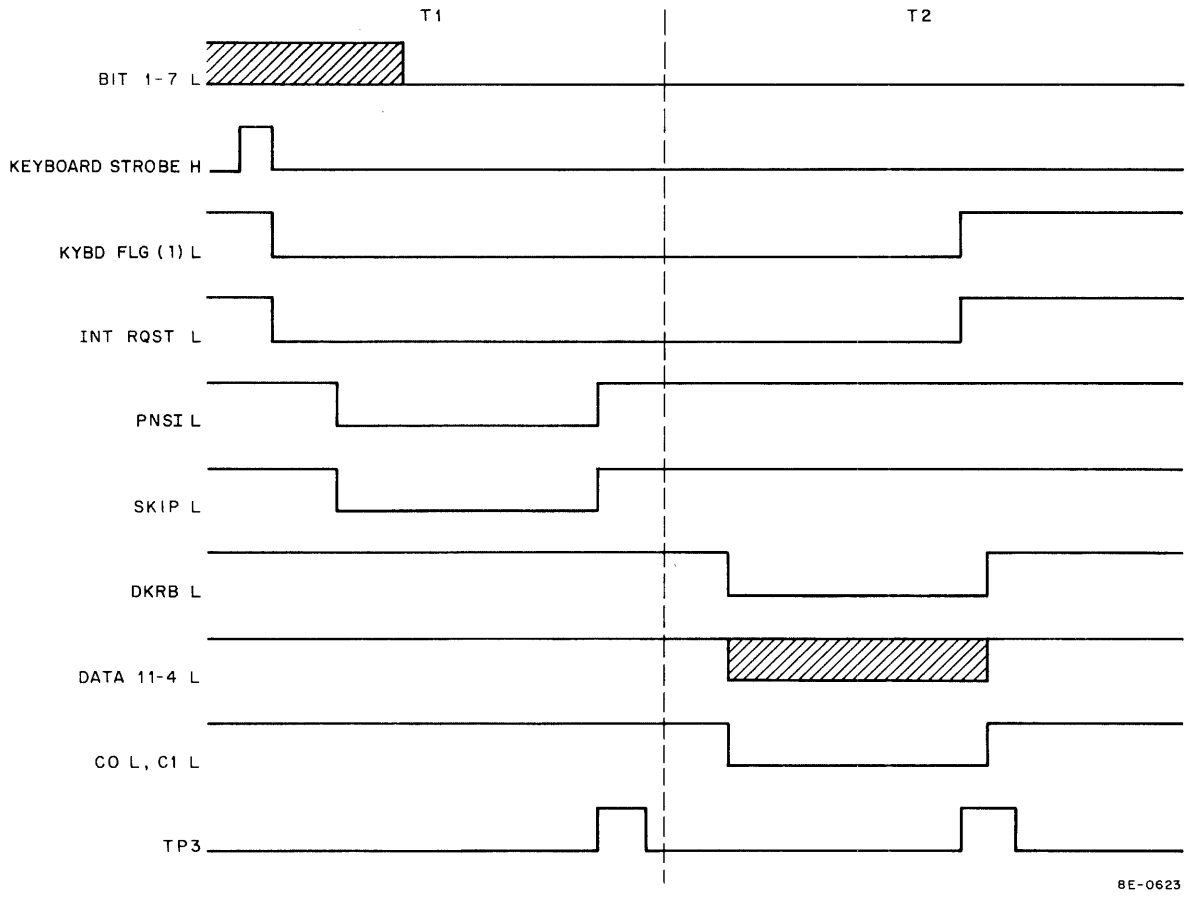


Figure 12-14 Keyboard Transmit Logic Timing

The user initiates the keyboard sequence by pressing a key on the keyboard. The character information is placed on the BIT 1–7 lines. After a period of time that allows the BIT lines to settle, the keyboard generates the KEYBOARD STROBE H signal. The trailing edge of this signal clocks the information into the 7-bit register and sets the KYBD FLG flip-flop. If the VT8-E is logically connected to the interrupt system, as assumed, the KYBD FLG (1) L signal causes the INT/SKIP logic to assert the OMNIBUS INT RQST L signal. The program proceeds to an interrupt servicing routine to determine the identity of the requesting device. The PNSI instruction in the routine causes the program to jump to a VT8-E routine that determines if the printer or keyboard requested the interrupt. Ultimately, the VT8-E keyboard routine executes the DKRB instruction.

When the DKRB instruction is decoded, the IOT Decoder logic generates the DKRB L signal and activates the OMNIBUS C0 and C1 lines. The DKRB L signal enables NOR gates E17C and E17D; the output signal from E17D gates the information from the register outputs to DATA lines 5–11, and also causes NAND gate E27 to assert the DATA 4 L signal. The DATA lines are gated to the AC Register and the information is clocked into the register at TP3 time. Also at TP3, the KYBD FLG flip-flop is cleared, readying the logic for a new data transfer.

12.4.1.4 INT/SKIP Logic – The INT/SKIP logic is shown in Figure 12-15. The PRNT FLG (1) L signal and the KYBD FLG (1) L signal can cause program skips when tested by instructions PNSK and DKSK, respectively. The signals can also be tested by the PNSI instruction, provided the ENA flip-flop, E37, has been set, logically connecting the VT8-E to the interrupt system. When E37 is set, the PNSI L signal enables NAND gate E29, which, in turn, enables NAND gate E34, if either the PRNT FLG (1) L signal or the KYBD FLG (1) L signal is asserted. Simultaneously, NAND gate E13 asserts the INT RQST L signal.

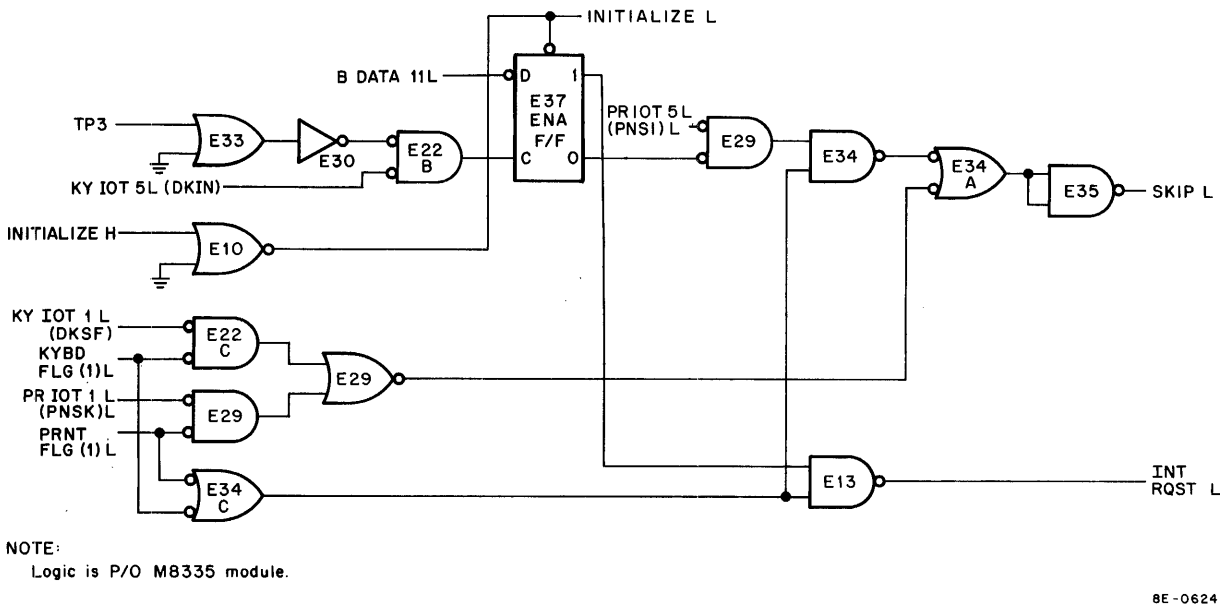


Figure 12-15 Keyboard/Print Interrupt and Skip Logic

The ENA flip-flop is set by the OMNIBUS INIT signal for the PDP-8 family computers. To clear the flip-flop, remove the VT8-E from the interrupt system, load AC11 with logic 0 and then program the DKIN instruction. The logic 0 in AC11 keeps the DATA 11 L signal negated. Thus, the D input of E37 remains high. At TP3 time, NAND gate E22B provides a clock pulse for E37, clearing the flip-flop. E37 can be set at any time with the same instruction merely by loading AC11 with logic 1.

12.4.2 Display Logic

Information displayed by the VT8-E is transferred by data breaks from the PDP-8/E memory. As with all data break devices, the start of the data transfer is under program control. However, the VT8-E is a 1-cycle data break device; consequently, it needs only a starting memory address to carry out the complete data transfer. The starting address, i.e., the memory address of the first data word to be transferred to the VT8-E, is placed in the AC Register by a program TAD instruction. Program IOT instructions gate this address onto the OMNIBUS DATA lines and cause it to be loaded into a starting address register in the VT8-E (Figure 12-16). At the same time, the VT8-E Data Break logic is readied for triggering.

When the CRT sweep is in a specified position, a synchronizing signal is generated by the VT8-E Timing logic. This signal enables the Data Break logic to request a data break and check priority. If no higher priority device has requested a break at this time, the Data Break logic asserts a number of OMNIBUS control signals, enabling direct communication between the interface and memory for one PDP-8/E timing cycle. At the same time, other Data Break logic signals gate the starting address onto the OMNIBUS MA lines. During the data break timing cycle, the data word in the addressed memory location is transferred on the MD lines and loaded into the interface Line Buffer Register. At TP4 time of the timing cycle, the Data Break logic increments the address in the Address Counter. The data word in this new address is transferred during the next data break timing cycle, which might occur immediately after the first (priority is checked during TS4 of each data break cycle; a higher priority device can interrupt the VT8-E data breaks).

After each transfer, the address in the Address Counter is incremented, and the data word in the new address is loaded into the Line Buffer Register. This register holds 32 or 64 data words, depending on the mode (graphic or alphanumeric) or the desired number of alphanumeric characters per line. The Data Break logic counts the number of data breaks; when the specified number of data words has been loaded into the Line Buffer Register, the Data Break logic ceases to request breaks.

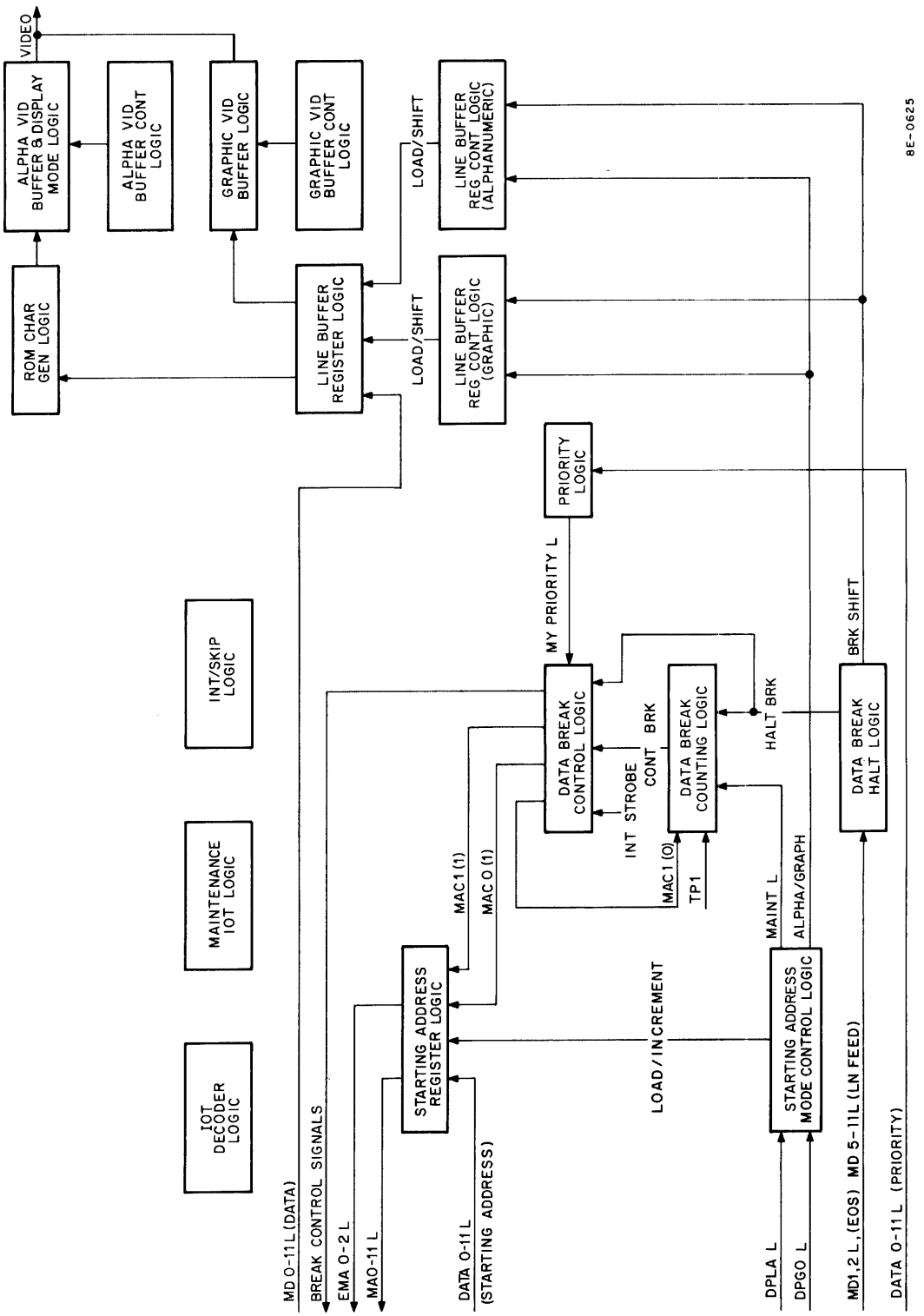


Figure 12-16 Display Logic Block Diagram

If the VT8-E logic has been programmed to display 32 alphanumeric characters per line; for example, each data word in the Line Buffer Register contains: the 7-bit ASCII code representation of an alphanumeric character (bits 5–11); data that controls how the character is displayed (bits 3 and 4); and data that controls the visible field (bits 1 and 2). Because the VT8-E displays only a 64-character set, bits 6–11 of the Line Buffer Register contain sufficient data to display all alphanumeric characters. Characters are formed on the CRT screen when the CRT video circuits selectively intensify points within a 5 X 7 dot matrix. The letter F is illustrated in Figure 12-17. Each horizontal scan line corresponds to one row of the letter. As the sweep scans along a line, video signals selectively intensify points as illustrated (5 video signals in row 1 of the letter F). If 32 alphanumeric characters per line are to be displayed, for example, row 1 of each character is swept out by the same scan line. The next scan line sweeps out row 2 of all 32 characters, and so on until the 7th scan line sweeps out row 7 of the characters, completing the character line.

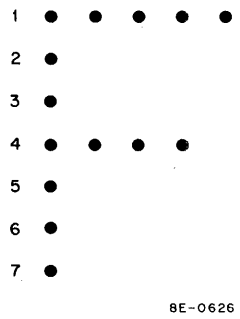


Figure 12-17 Video Presentation for the Letter F

The video signals are generated, indirectly, by a ROM Character Generator. After the start of a horizontal scan line, a 6-bit ASCII character is shifted from the Line Buffer Register (at this time, the register is in the recirculating mode; hence, an end-around shift is performed). The character addresses a ROM Character Generator location. This location contains the video information for one row of the character. For example, assume that the letter F is the first character to be displayed in a particular character line. The 6-bit ASCII representation of the letter F addresses a particular ROM Character Generator location. The information in this location causes row 1 of the letter to be painted during this scan line. The next character to be displayed is shifted from the Line Buffer Register and addresses its unique ROM Character Generator location; the information in the location causes row 1 of this character to be displayed just after character F. Row 1 of all 32 characters is displayed during this scan line.

After the start of the next horizontal scan line, the 6-bit ASCII representation of the letter F is again shifted from the Line Buffer Register. Meanwhile, certain ROM control signals have been asserted so that the addressed location differs from that of the first scan line. This location contains information that causes Row 2 of the letter F to be painted during this scan line. Row 2 of all other characters is displayed during this scan line in similar fashion. Consequently, the Line Buffer Register is shifted 32 times during each scan line; after 7 end-around shifts of the register, a character line has been displayed.

Each character line comprises ten scan lines, rather than the seven just described. The three additional lines occur at the beginning of the character line. During the first two scan lines, the Line Buffer Register is loaded from the OMNIBUS MD lines; during the third scan line, a blank ROM location is addressed. Figure 12-18 represents two character lines as they would appear on the CRT screen. Character line spacing (43% of character height) is provided by the three blank scan lines.

If the VT8-E has been programmed for a graphic display, one line of graphic data is displayed during each horizontal scan line. A line of graphic data is represented by 16 12-bit data words; each bit of a data word represents a dot or a

space on the CRT screen. The Line Buffer Register is loaded with two lines of graphic data by 32 data breaks. As the sweep scans along a line, video signals selectively intensify points to paint the graphic symbol. Although 16 12-bit data words contain 192 bits, only 189 points can be painted by each scan.

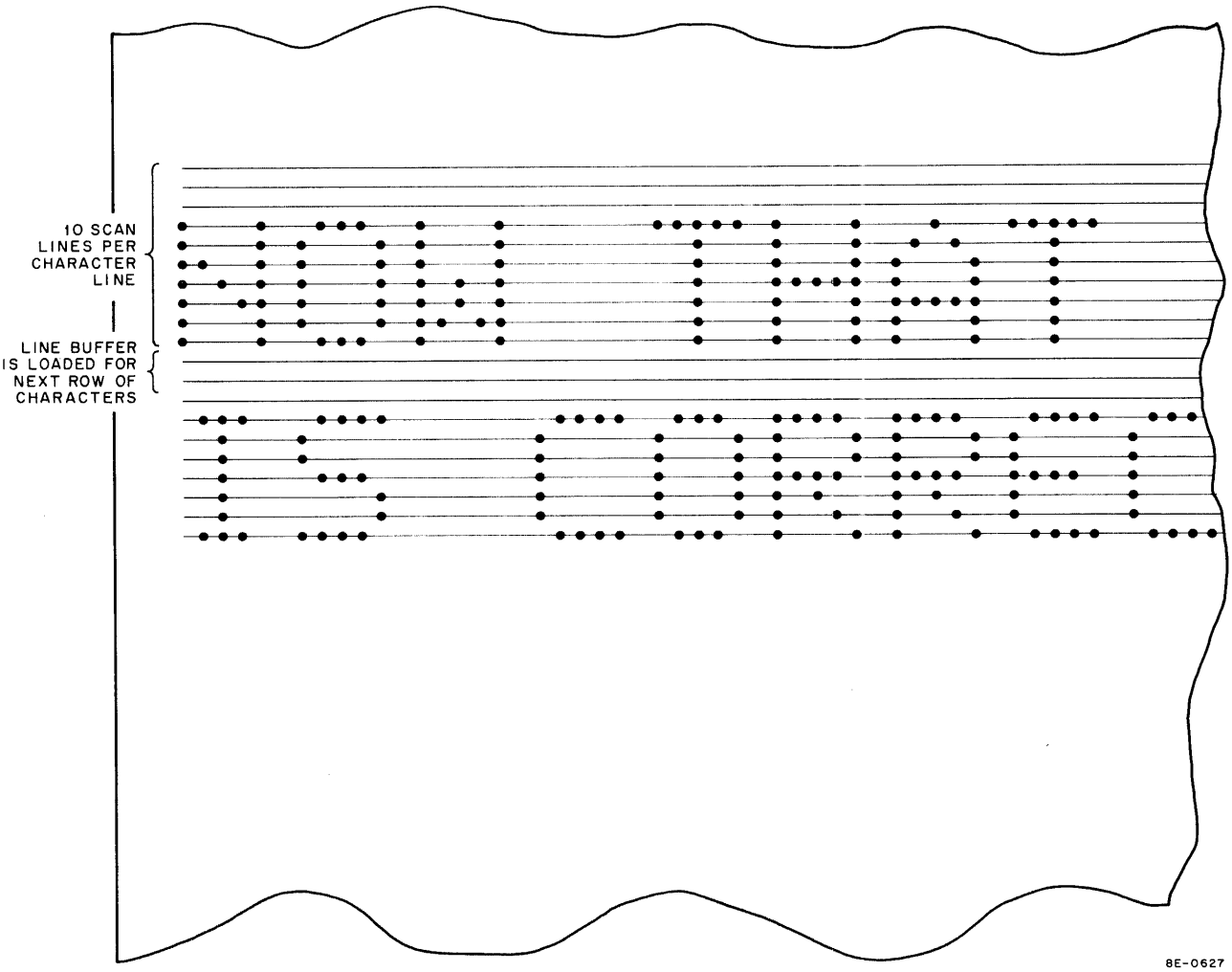


Figure 12-18 Two Alphanumeric Characters Displayed on the CRT

12.4.2.1 VT8-E Timing – The VT8-E Timing logic generates signals that sync the Display logic and the CRT sweep circuits. Figure 12-19 illustrates the CRT vertical and horizontal sweep signals and the VT8-E sync signals.

For 60 Hz operation, the VT8-E timing generates a V SYNC L signal every 16.7 ms. This sync signal causes a vertical retrace, which is carried out in approximately 20 scan lines. A VZONE flip-flop in the timing controls the displayable area in the vertical direction. When the flip-flop is set, the VZONE (1) signal enables a vertical display of 200 scan lines (the horizontal sweep rate is set at 15.6 kHz; a total of 60 scan lines is made non-displayable to remove distortion-prone areas on the CRT screen).

The timing generates an HSYNC signal every 64.1 μs. A HZONE flip-flop in the timing controls the displayable area in the horizontal direction. When the flip-flop is set, the HZONE (1) signal enables graphic or alphanumeric video to be painted in the distortion-free area of the screen (exceptions to this statement are pointed out in the detailed logic discussion).

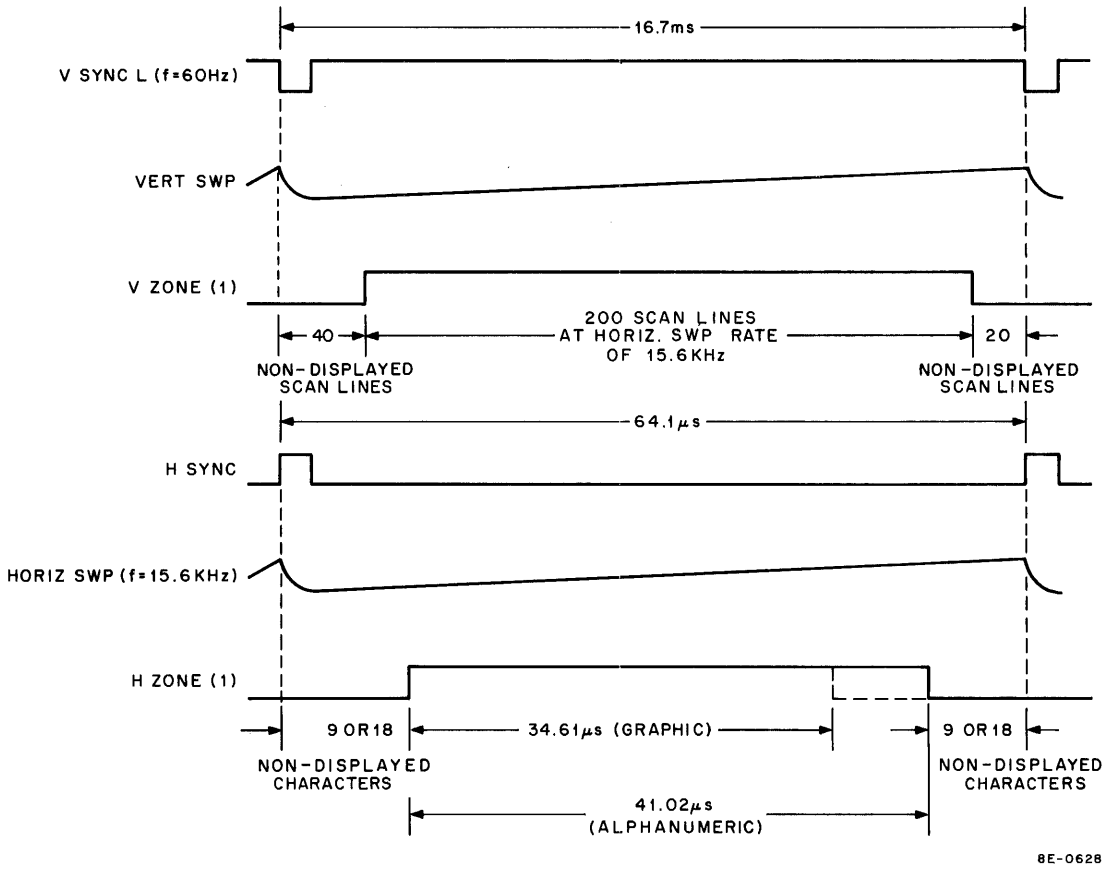
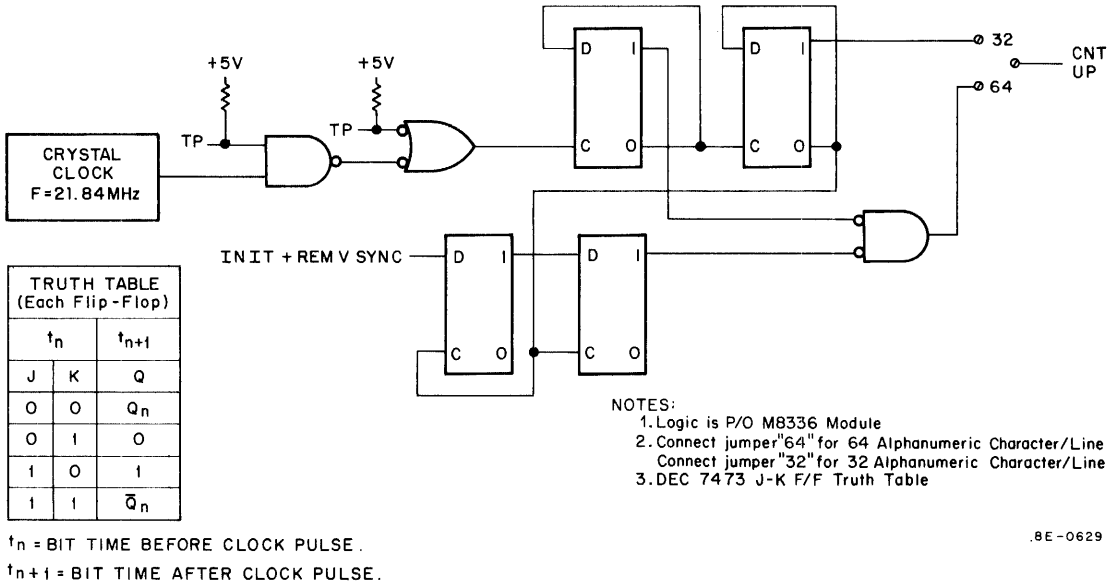


Figure 12-19 Sweep and Sync Signals

The VT8-E timing is such that either 50 or 100 alphanumeric characters could be displayed between HSYNC signals. The HZONE (1) signal reduces the number of characters to either 32 or 64, respectively (an equal number of characters is removed on both sides of the screen). Note that the HZONE (1) signal is of shorter duration for the graphic display. This is explained as follows. Clock pulses of the same basic frequency are used to shift the Alphanumeric Video Buffer Register and the Graphic Video Buffer Register. Seven shift signals are needed to display the rows of the 5 X 7 alphanumeric character matrix (five signals intensify the scan, two signals provide spacing between each character). Thus, 7 X 32, or 224 shift pulses are needed for an entire character line. An entire graphic line needs only 192 shift pulses. Consequently, it seems that the HZONE (1) signal should be reduced by an amount that allows 192 shift pulses to be generated (if the display area is not shortened, an improper display will result). This would mean reducing the graphic displayable area by an amount equal to 32 shift pulses. However, this is not a multiple of seven, which it must be to enable correct alphanumeric display. The closest number that is a multiple of 7 is 35. Thus, the horizontal zone for graphics allows only 189 shift pulses to be produced, cutting off the last 3 data bits in each scan line (note that 28 could not be used because then too many graphic shift pulses would be produced). The pulses are derived from a 5.46 MHz clock (t = 183.15 ns). Therefore, 189 shift pulses require an HZONE (1) signal of only 34.61 μs.

12.4.2.2 VT8-E Timing Logic – The VT8-E Timing logic generates the CRT sync pulses and the interface control signals. All timing and control signals are derived from a crystal-controlled transistor oscillator that produces pulses at a frequency of 21.84 MHz. These pulses are applied to a Clock Pulse Generator, shown in Figure 12-20. The generator divides the basic frequency by 2 and 4, producing well-shaped clock pulses of 10.92 MHz and 5.46 MHz. Two test points are available which allow the oscillator clock to be inhibited and external clocks injected to drive the timing chain.



TRUTH TABLE (Each Flip-Flop)

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

t_n = BIT TIME BEFORE CLOCK PULSE.

t_{n+1} = BIT TIME AFTER CLOCK PULSE.

Figure 12-20 Clock Pulse Generator

The clock pulses selected are applied to a chain of DEC 74161 4-Bit Counters that counts down the pulse frequency to 3.75 Hz (for 60 Hz operation). Selected outputs of the timing chain are gated to produce sync pulses and control signals.

A logic block representation of the DEC 74161 4-Bit Counter Integrated Circuit (IC) is shown in Figure 12-21. This IC, E17, is the first one in the timing chain. Because it is a 4-bit counter, E17 can produce one pulse at its CARRY output for each 16 pulses at its COUNT UP input. However, because the IC can be preset to any count, it can produce a CARRY output for any number of input pulses less than 16. The preset inputs are labeled A through D in Figure 12-21 (A is the LSB). They are wired so that E17 is preset with a count of 1001_2 whenever a signal is applied to the LOAD input and a clock pulse occurs. The CARRY signal is generated when the count is in the 1111_2 state and ENP and ENT are true. A Load signal is generated by the OR gate and E17 is preset to 1001_2. Seven more pulses at the clock input produce another CARRY signal and, again, the counter is preset. Thus, the counter divides by seven. The counter can also be preset by a REMOTE V SYNC IN L signal, enabling the timing to be controlled by some external device. The output of each bit, designated QA through QD (QA is the LSB), is available for gating to generate the sync and control signals.

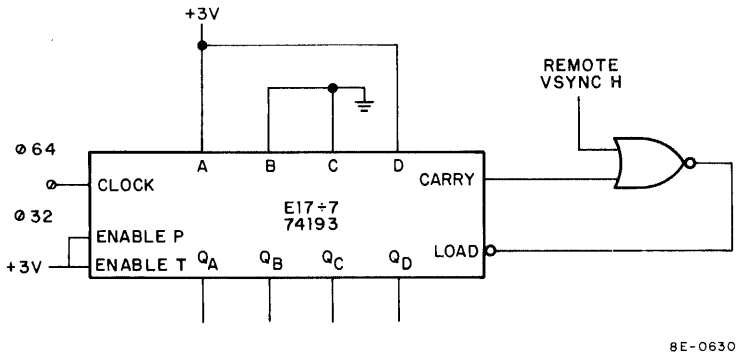
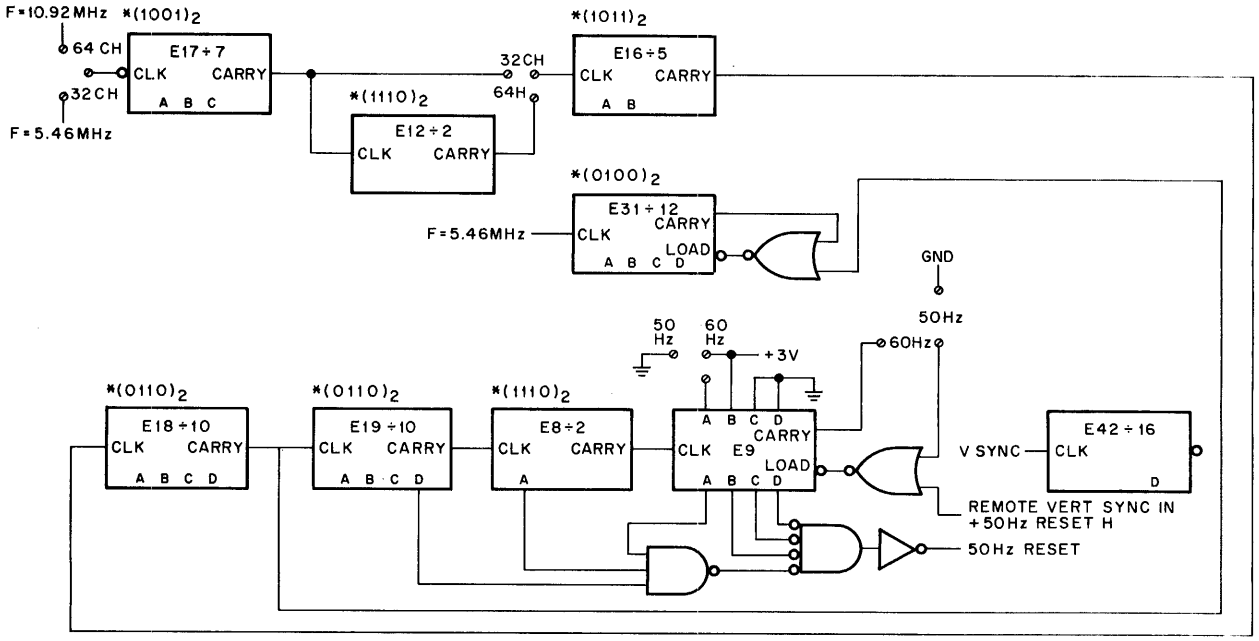


Figure 12-21 4-Bit Counter

Figure 12-22 shows the entire chain of 74161 ICs. Each IC in the figure is represented in shorthand form: i.e., the wiring of the PRESET inputs is not shown, the LOAD input circuits are not shown, and the destination of each output is now shown (only those output bits that are used are indicated on the ICs). The binary designations above each IC block represent the way the preset inputs are wired. For example, E16 is wired thus: PRESET input D is tied to +3V; PRESET input C is grounded; PRESET inputs B and A are tied to +3V. Therefore, E16 is preset with a count of 1011_2 and divides by 5.



*COUNTER IS PRESET TO THIS BINARY VALUE

NOTE:
Logic is P/O M8336 Module

IC OUTPUT FREQUENCY

IC	FREQ. OUTPUT	
	60Hz LINE	50Hz LINE
E17	780KHz(32) 1560KHz(64)	SAME AS 60Hz
E16	156KHz	
E18	15.6KHz	
E19	1.56KHz	
E8	780Hz	
E9	60Hz	50Hz
E42	3.75Hz	3.125Hz

8E-0631

Figure 12-22 VT8-E Timing Chain

Each IC has a NOR gate at its LOAD input, exactly as shown in Figure 12-21; this gate ORs the CARRY output with REMOTE V SYNC and INIT (E17, E12, E16), or with REMOTE V SYNC and 50 Hz RESET (E18, E19, E8, E9). The bit output destinations are shown, in part, only for ICs E19, E8, and E9.

The table in Figure 12-22 indicates the frequency of the CARRY output pulses of each IC. The output frequency from E17 differs for 32 character/line and 64 character/line operation. The bit output signals from E17 determine the alphanumeric character rate, the rate at which characters are painted on the CRT screen. Thus, the rate is twice as fast for 64 character/line operation. E12 divides by two; therefore, the input of E16 is the same for both character rates.

When a 50 Hz line is used, the timing is modified in the last three ICs. For 60 Hz operation, E9 is preset with a count of 0011_2 and its CARRY output provides the LOAD input for E9. E8 and E9, together, divide the output of E19 by 26, producing a CARRY output pulse from E9 at a frequency of 60 Hz. This output is gated elsewhere in the logic to generate the V SYNC L signal that causes a CRT vertical retrace. For 50 Hz operation, the 50 Hz jumpers are connected, and E9 is preset with a count of 0010_2. Furthermore, the LOAD input of E9 is controlled by REMOTE V SYNC IN or 50 Hz RESET H. When E9 attains a count of 001_2 and both E19-D and E8-A are high, E9 is preset and a V SYNC pulse is generated. E8 and E9, together, divide the output of E19 by 31.2, producing pulses having a frequency of 50 Hz. The table shows the output of E9 as 50 Hz (the output is not actually from E9, as for 60 Hz operation, but it is convenient to think of it as so). As for 60 Hz operation, the output is gated to generate the V SYNC L signal.

Note that the REMOTE V SYNC IN or 50 Hz RESET line is activated when E9 is preset; thus, ICs E18, E19, E8, and E9 are preset at the moment of vertical retrace. This active step is not necessary during 60 Hz operation because all ICs automatically overflow to the preset state.

Figure 12-23 shows the logic that generates the horizontal and vertical sync signals, while Figure 12-24 shows the HZONE and VZONE flip-flops and those signals that control the two flip-flops. The timing diagram in Figure 12-25 shows the line timing for both alphanumeric and graphic display. Two hundred of the HZONE (1) signals are generated for each VZONE signal, as shown in Figure 12-19.

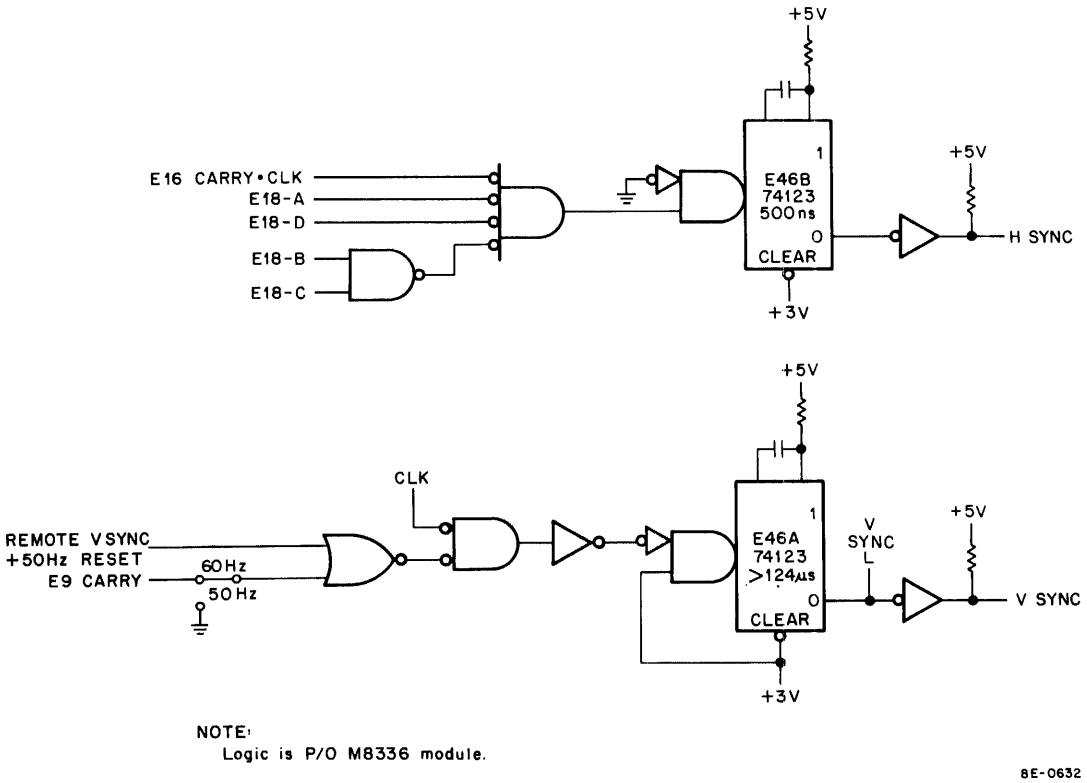


Figure 12-23 Horizontal and Vertical Sync Circuits

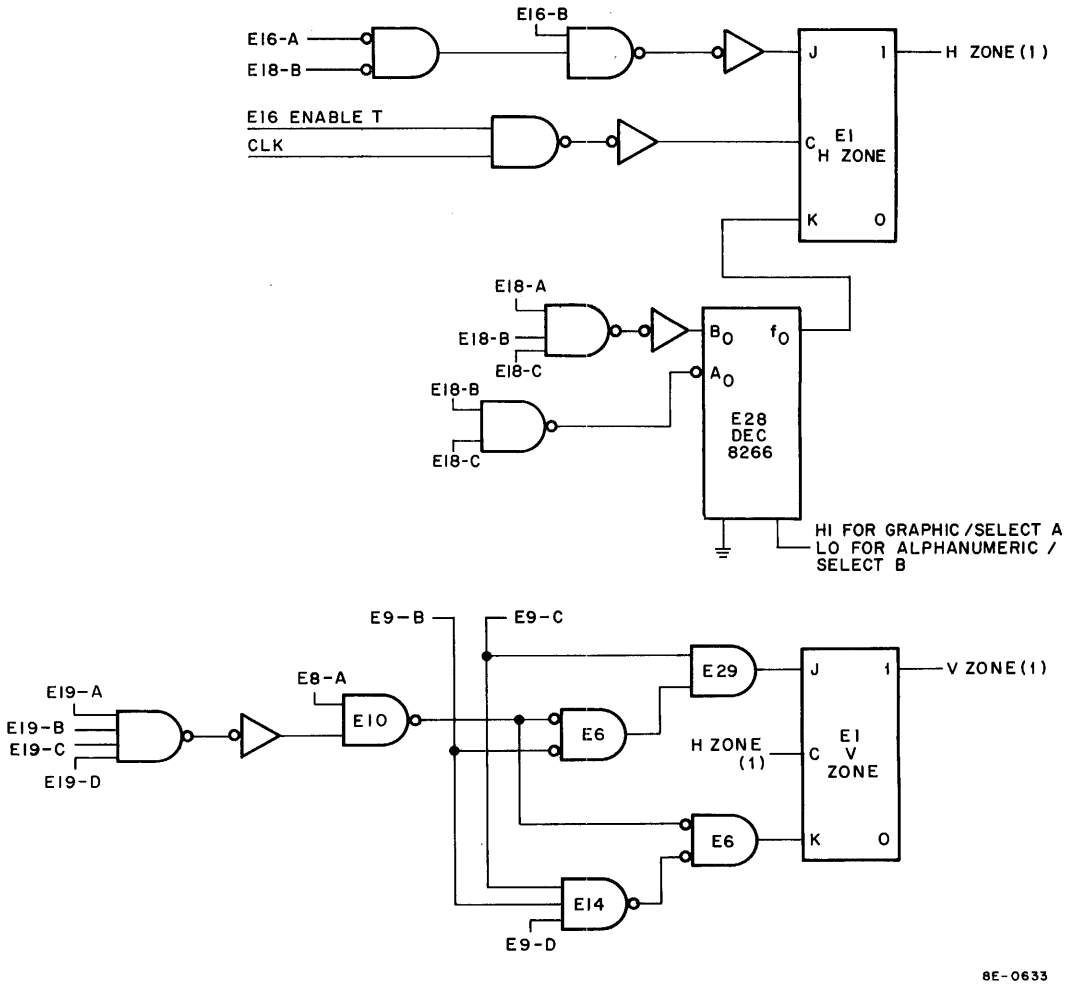


Figure 12-24 Horizontal and Vertical Zone Flip-Flops

12.4.2.3 Starting Address Register Logic – The Starting Address Register logic is shown in Figure 12-26. The logic includes two Starting Address Registers: one is a 12-bit register comprised of two DEC 74174 ICs (hex flip-flop); the other uses three bits of a DEC 74175 IC (quad flip-flop). The Address Counter is comprised of four DEC 74193 ICs (4-bit up-counters) connected in series and is preset from the Buffer Registers.

The control signals that load and clock the Starting Address Registers and the Address Counter are generated by the Starting Address Control logic, shown in Figure 12-27. When the program IOT instruction DPLA is issued, the 12-bit starting address is placed on the DATA lines. The DPLA L signal causes both the DATA EN A L and DATA EN B L signals to be asserted. The starting address is gated through the NAND gates to the DEC 74174 inputs and loaded into the buffer at TP3 time by the LD ST ADD signal.

The extended field must also be identified by the EMA bits. The extended field address bits are placed on lines DATA 6, 7, and 8 by the DPGO IOT instruction. The DPGO L signal causes the DATA EN signals to be asserted, gating the extended address to the DEC 74175 inputs. At TP3 time the XST ADD REG is loaded by the LD XST ADD signal (DPGO).

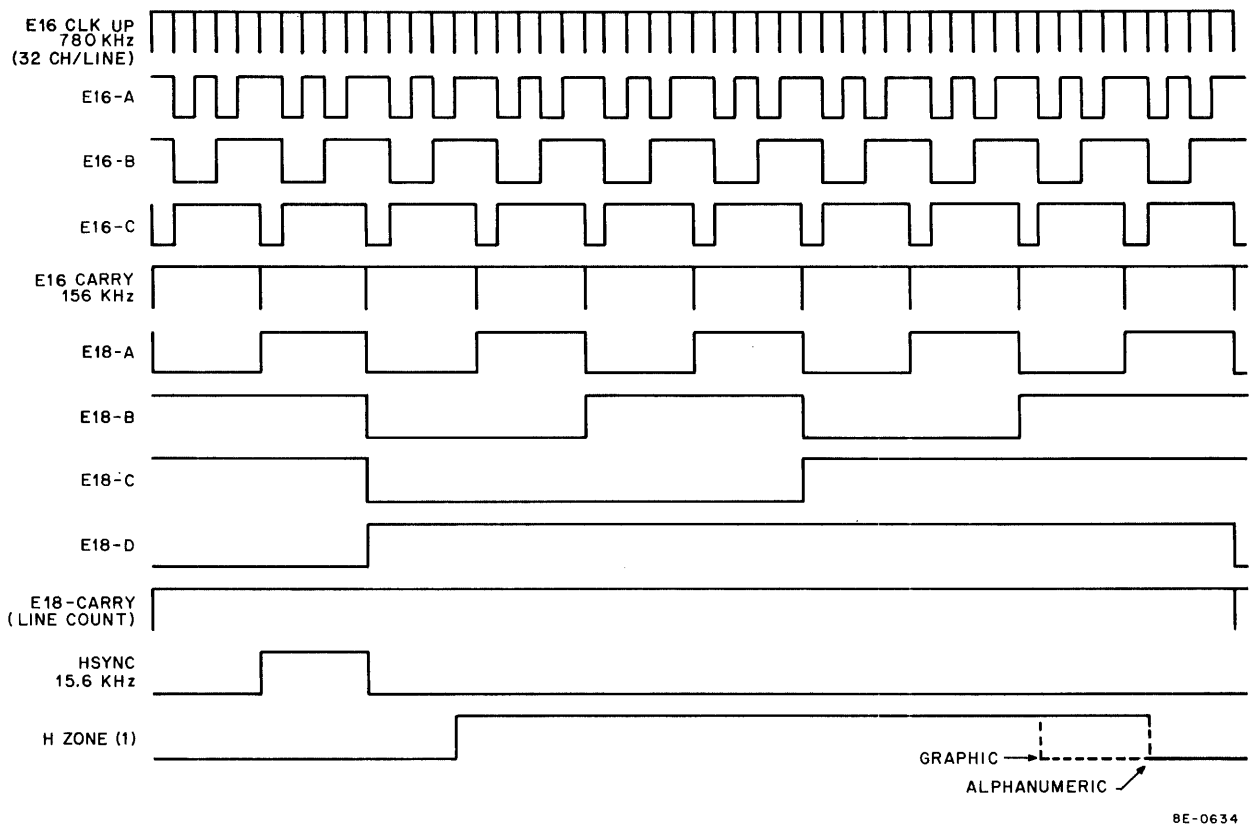
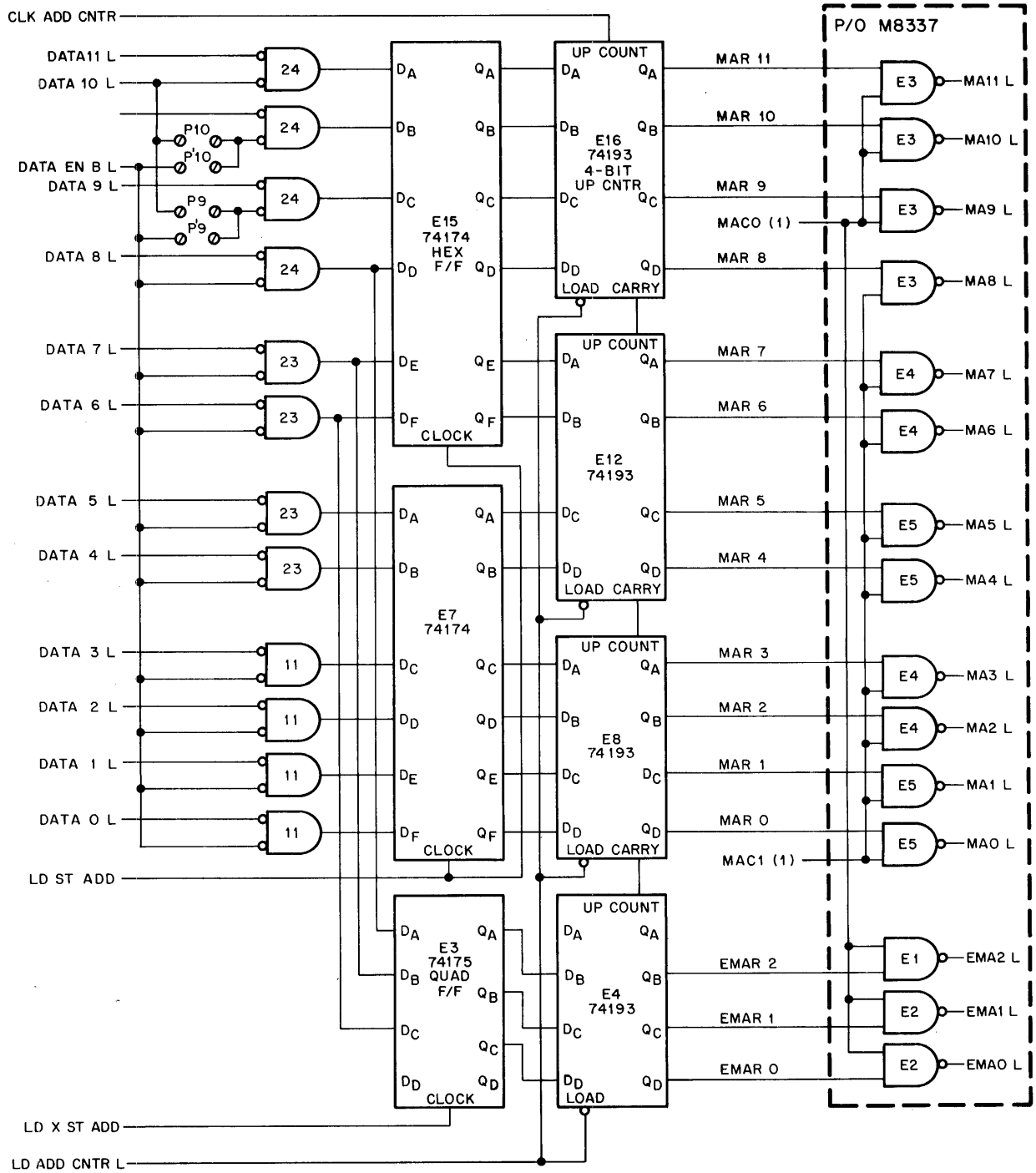


Figure 12-25 Alphanumeric and Graphic Line Timing

The DPGO L signal also clears the MAINT/GO flip-flop (Figure 12-27) at TP3 time, negating the MAINT L signal. This negated signal enables a vertical sweep synchronizing signal, E46(Q), to assert the LD ADD CNTR L signal. This signal loads the starting address (including the extended address) into the 15-bit Address Counter.

At approximately the same time that the Address Counter is loaded, the Data Break Counting logic is readied for triggering. When the sweep is in the specified position, the COUNTING signal is generated, enabling the Data Break Control logic to request a data break. If the VT8-E has highest priority, the MAC0 and MAC1 flip-flops in the Data Break Control logic are set. The MAC0(1) and MAC1(1) signals gate the 15-bit starting address from the Starting Address Register outputs onto the MA0–11 and EMA0–2 lines. At TP1 of the data break timing cycle, the MAC2 flip-flop in the Data Break Control logic is set. The MAC1(1) signal then enables the Starting Address Control logic to assert the CLK ADD CNTR signal at TP4 time of the data break timing cycle. Thus, the address in the Starting Address Register is counted up by one. The next data break timing cycle transfers the data word in the new address to the VT8-E.

12.4.2.4 Data Break Counting Logic – The Data Break Counting logic is shown in Figure 12-28. This logic generates the COUNTING signal that enables the Data Break Control logic to request data breaks. When the PRESET BRK signal is generated, flip-flop E43A is set, asserting the COUNTING signal. The COUNTING signal enables the NBR flip-flop in the Data Break Control logic to be set at INT STROBE time. If the VT8-E has highest priority, data breaks begin. Each TP1 signal of a data break timing cycle causes NAND gate E42 (Figure 12-28) to assert the COUNT BRK signal. This signal is counted by the 4-bit up-counter, E53. When the correct number of data breaks has been performed, flip-flop E43A is cleared via NOR gate E33 and data breaks cease.



NOTE:
Logic is P/O M8335 unless noted.

8E-0635

Figure 12-26 Starting Address Register Logic

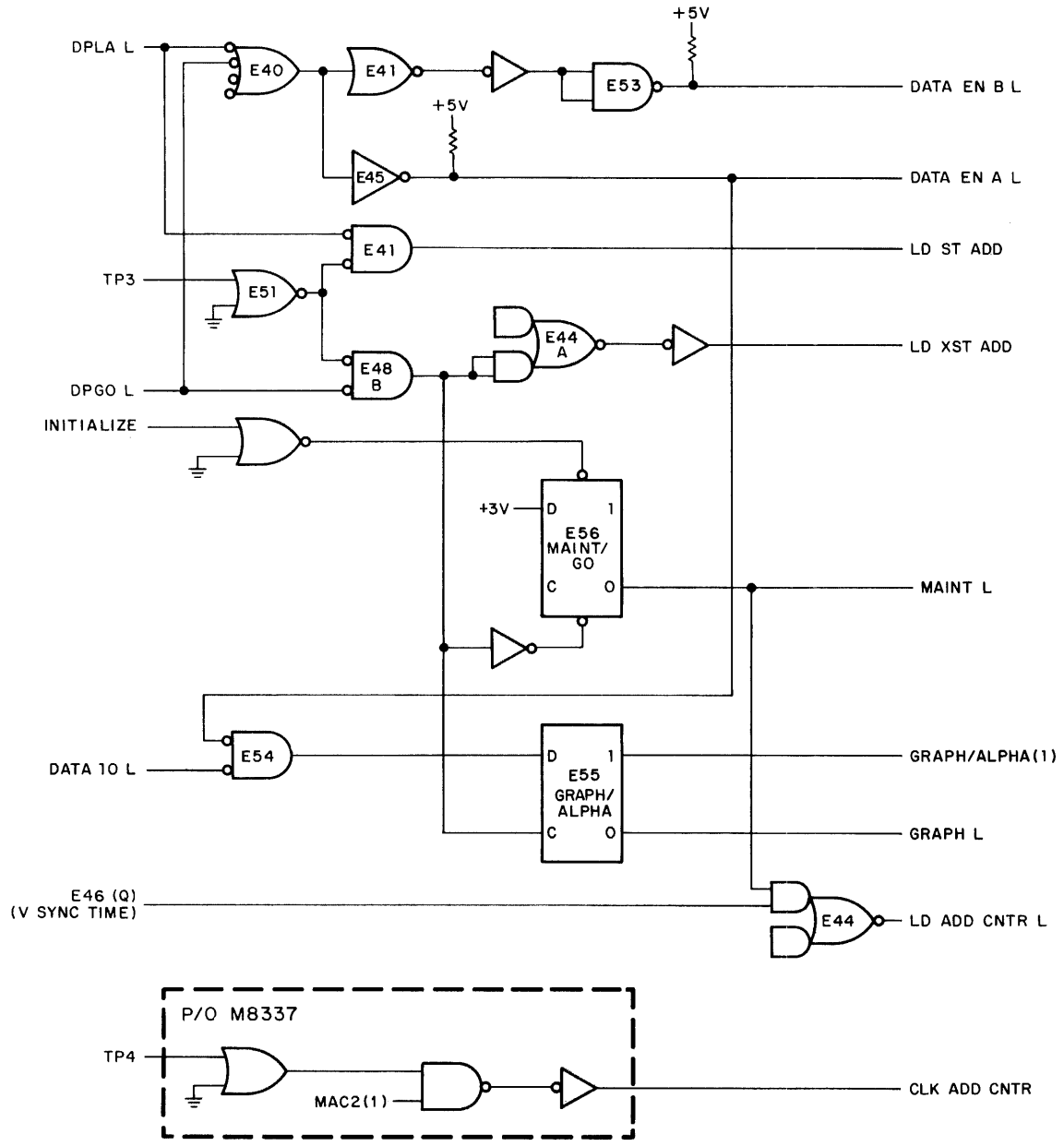


Figure 12-27 Starting Address Register Control Logic

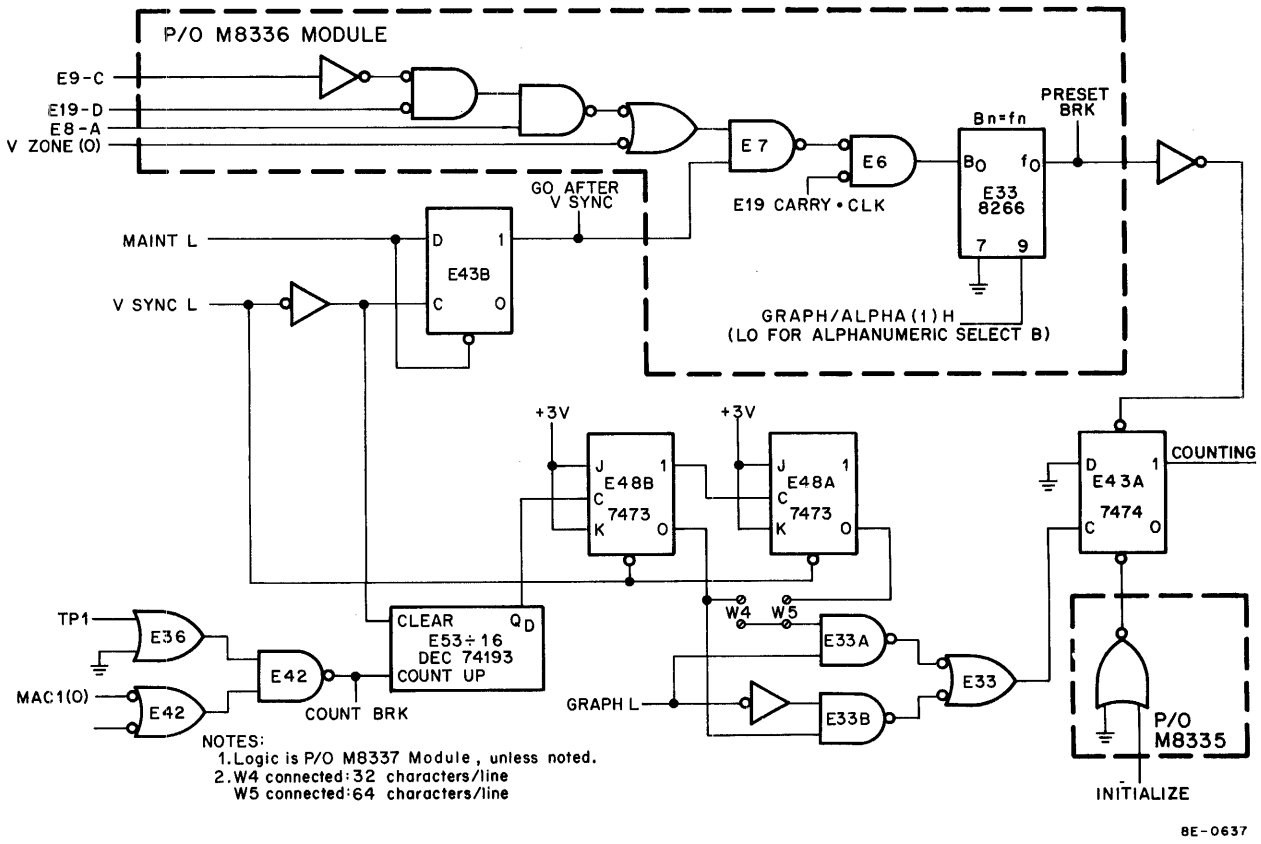


Figure 12-28 Data Break Control Logic

If the logic has been programmed for an alphanumeric display (assume 32 characters/line), 32 data words must be loaded into the Line Buffer Register during two scan lines of the character row. During each of the eight remaining scan lines, the Line Buffer Register is recirculated. Thus, new information is loaded once every ten scan lines and the PRESET BRK signal must be generated only once every ten scan lines.

Note that the logic within the dashed line in Figure 12-28 generates the PRESET BRK signal. The VSYNC L signal prepares this logic for triggering by setting flip-flop E43B, thereby asserting the GO AFTER VSYNC signal (the MAINT L signal is negated by the Starting Address Control logic when a DPGO instruction is issued). VSYNC L also clears the 4-bit up-counter and the two J-K flip-flops. When the VZONE flip-flop is set, NAND gate E7 is enabled. Each E19 CARRY signal that occurs causes PRESET BRK to be generated. Because E19 CARRY occurs once every ten scan lines, the Line Buffer Register is loaded once every ten scan lines, as required.

Figure 12-29 illustrates the timing of the counting network for an alphanumeric display of 32 characters/line. This timing applies to a graphic display, as well, although the GRAPH L signal would be asserted for such a display. If the logic has been programmed for a graphic display, the PRESET BRK signal must be generated differently. Sixteen data words are needed to display one line of graphic data. Thus, the Line Buffer Register can hold two lines of graphic data. Since a line of graphic data is displayed by one scan line, a PRESET BRK signal is required once every two scan lines. The logic in Figure 12-30 is used to generate the Graphic mode PRESET BRK signal. It is similar to the PRESET BRK logic in Figure 12-28. The VSYNC L signal is used in the same way and the data breaks are counted by the counting logic in the same way. The LN CNT signal occurs at the end of each scan line, but the E19-A signal is high for every other scan line. Consequently, the graphic PRESET BRK occurs once every two scan lines.

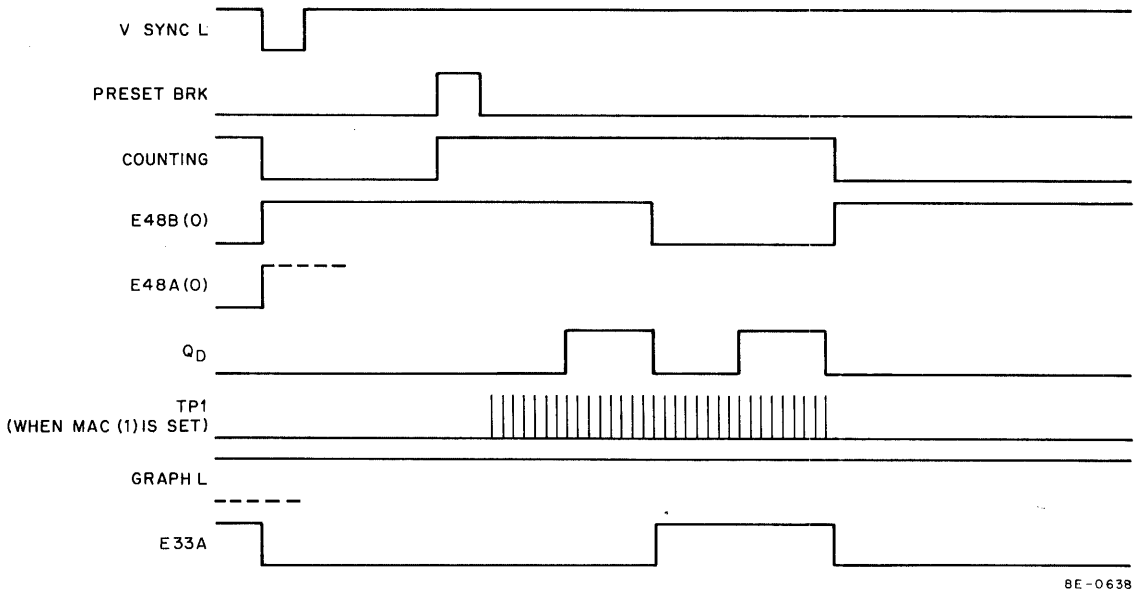


Figure 12-29 Data Break Counting for 32 Characters/Line

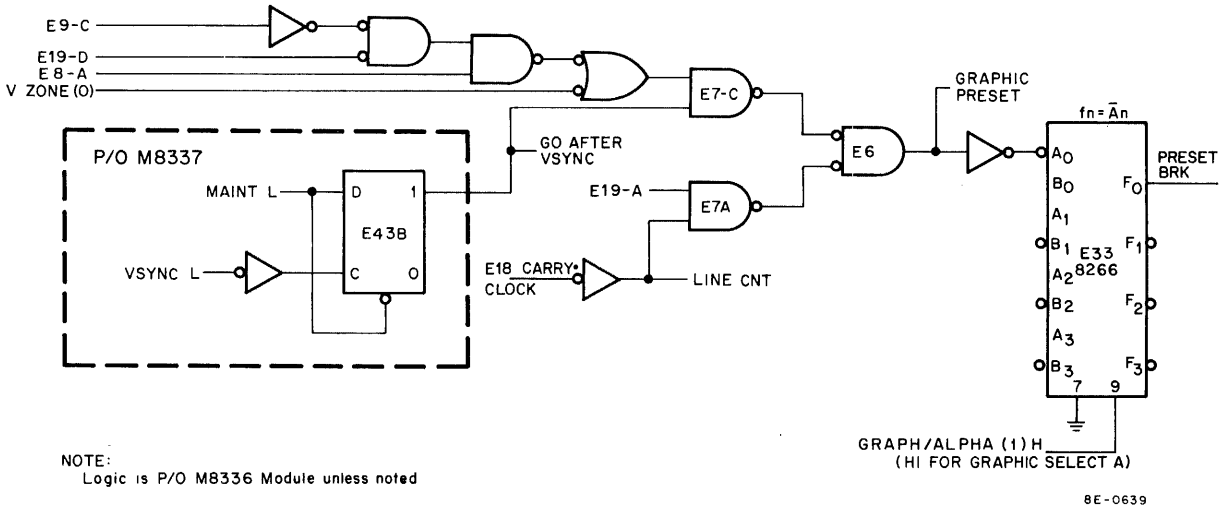


Figure 12-30 PRESET BRK Generation Graphic Mode

12.4.2.5 Data Break Control Logic – The Data Break Control logic is shown in Figure 12-31. When the COUNTING signal is asserted by the Data Break Counting logic, NAND gate E52 is enabled. (MAINT L is negated by the DPGO instruction and HALT BRK L is asserted only for line-feed or end-of-screen.) The NBR flip-flop is set at INT STROBE time, asserting the NBR (1) signal. This signal asserts OMNIBUS signals CPMA DISABLE L and BRK IN PROG L and causes the VT8-E priority to be placed on the DATA lines during TS4. CPMA DISABLE L causes the CPU CPMA Register to be disconnected from the OMNIBUS MA lines, while BRK IN PROG L ensures that only data break devices place priority information on the DATA lines during TS4.

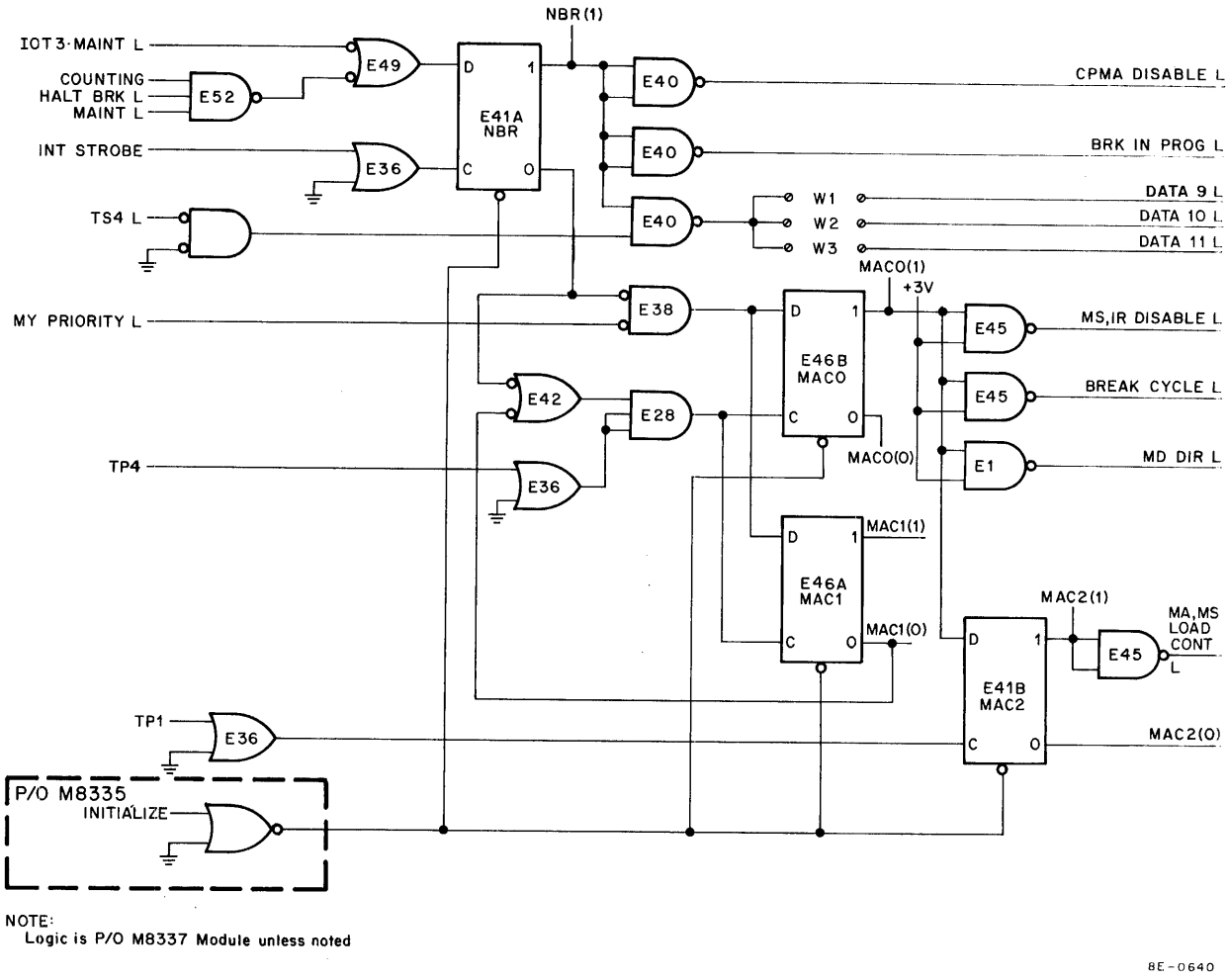


Figure 12-31 Data Break Control Logic

If the VT8- E has highest priority, MY PRIORITY L is asserted by the Priority logic (Figure 12-33). This signal is NANDed with the 0-output of the NBR flip-flop to produce a high logic level at the D-input of both the MAC0 and MAC1 flip-flops; the flip-flops are set at TP4 time via NAND gate E28. The MAC0(1) signal asserts MS, IR DISABLE L, BREAK CYCLE L, and MD DIR L, and enables the MAC2 flip-flop to be set at TP1 time of the data break cycle, thereby asserting MALC L. These OMNIBUS signals complete the CPU takeover process. MS, IR DISABLE L forces the CPU to enter the Direct Memory Access (DMA) state and disables the CPU IR Register. The MALC L signal prevents the CPMA Register from being clocked during the data break operation, while the BRK CYCLE L signal is applied to the programmer's console and can be monitored on the display panel.

The MD DIR L signal is asserted so that the data word transferred during the data break timing cycle is rewritten in the memory location during the write half of the memory timing cycle.

The MAC1(0) signal is applied to NOR gate E42 to ensure that MAC0 and MAC1 can be cleared by TP4 whenever NBR is cleared at INT STROBE time. The MAC1 and MAC2 outputs are used as gating signals elsewhere in the Display logic.

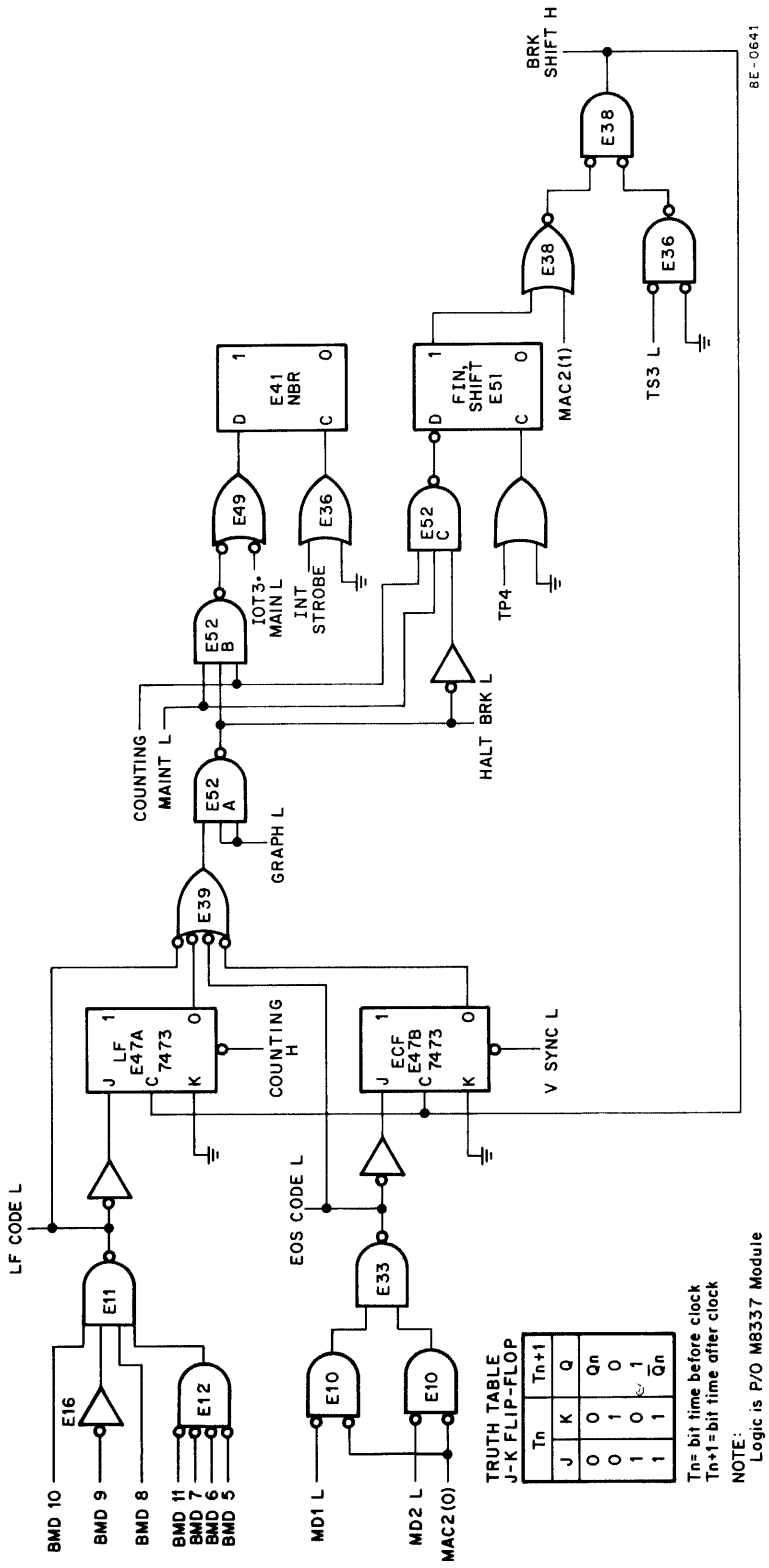


Figure 12-32 Data Break Halt, Line Feed/EOS Logic

12.4.2.6 Data Break Halt, Line Feed, and End-of-Screen Logic – The Data Break Halt, Line Feed, and End-of-Screen logic is shown in Figure 12-32. This logic is used to clear the NBR flip-flop and stop Single Cycle Data Breaks as follows:

a. If the line feed ASCII code (012) is detected on the MD lines, E47A sets. This clears NBR if the counter has not overflowed and the Maintenance mode is not enabled.

b. If the Character Counter overflows when 64 or 32 characters are transferred, counting is negated.

c. If the EOS code is detected (Figure 12-7) and EOS CODE L is asserted.

d. If V SYNC L is asserted at the end of the vertical scan.

If NBR is cleared by EOS CODE or LF CODE before the Character Counters have counted 64 or 32 characters, FIN SHIFT (E51) sets. This allows the counters to continue counting until they overflow (read all 0s) so that they will contain a 0 count when the next data break is initiated. FIN SHIFT also allows BRK SHIFTS to be generated in order to shift the line buffer data into the correct position. FIN SHIFT is clocked at each TP4 time and will clear at the first TP4 time after COUNTING is negated.

IOT3 · MAIN L is used to set NBR to cause one Single Cycle Data Break if the DPMB Maintenance instruction is executed by the program.

12.4.2.7 Priority Logic – The Priority logic is shown in Figure 12-33. Similar logic is contained on all interfaces that connect to the OMNIBUS. Priority is checked during TS4 immediately following the INT STROBE signal that sets the NBR flip-flop.

The VT8-E can have priority 10, 11, or 12. The device having the lowest priority (12) asserts the DATA 11 L signal during TS4. Assume that priority 11 is assigned. This priority causes the VT8-E to assert the DATA 10 L signal during TS4 L (jumper W2 in the Data Break Control logic is connected). Jumpers P10 and P9' must be connected in the Priority logic. Because the DATA EN B L signal is asserted when NBR(1) is high, any data break device with a higher priority can enable one of the NAND gates (the DATA EN A L signal is high throughout the priority check). Thus, MY PRIORITY L is not asserted and VT8-E data breaks do not begin.

If the VT8-E is assigned priority 10, jumpers P10 and P9 are connected. Higher priority devices can assert any of DATA lines 0 through 8, thereby preventing the VT8-E from beginning data breaks. However, any device with a lower priority, 11 or 12, must wait until the VT8-E relinquishes control of the CPU.

12.4.2.8 Line Buffer Register and Control Signal Logic – The Line Buffer Register logic is shown in Figure 12-34. The register comprises four DEC 2518 ICs (hex 32-bit Shift Registers) and is loaded from the MD lines during each data break cycle [MAC2 (0) is asserted low] by control signals generated in the Line Buffer Register Control logic (Figures 12-35 and 12-36).

If 32 alphanumeric characters are to be displayed, Component Registers B1 and B2 are used as a 12 X 32-bit Shift Register that is loaded with the 32 ASCII-coded characters. If 64 characters must be displayed, the A1 and A2 Component Registers are also used as a 12 X 32-bit Shift Register. However, the two 12 X 32-bit registers are loaded alternately, word by word from the MD lines. Consequently, they function together as a 12 X 64-bit Shift Register. If graphic data is displayed, the A and B Registers operate as two independent 12 X 32-bit Shift Registers. While one is displaying two scan lines of data, the other is refreshing for the next two scan lines.

When the LD B L signal, for example, is asserted, the 12 X 32-bit B Register can be loaded from the MD lines. Data gated to the LOAD inputs is shifted by the CLK B signal. When the LD B L signal is negated, the LOAD inputs are disabled; the CLK B signal produces an end-around shift of the data that has been loaded.

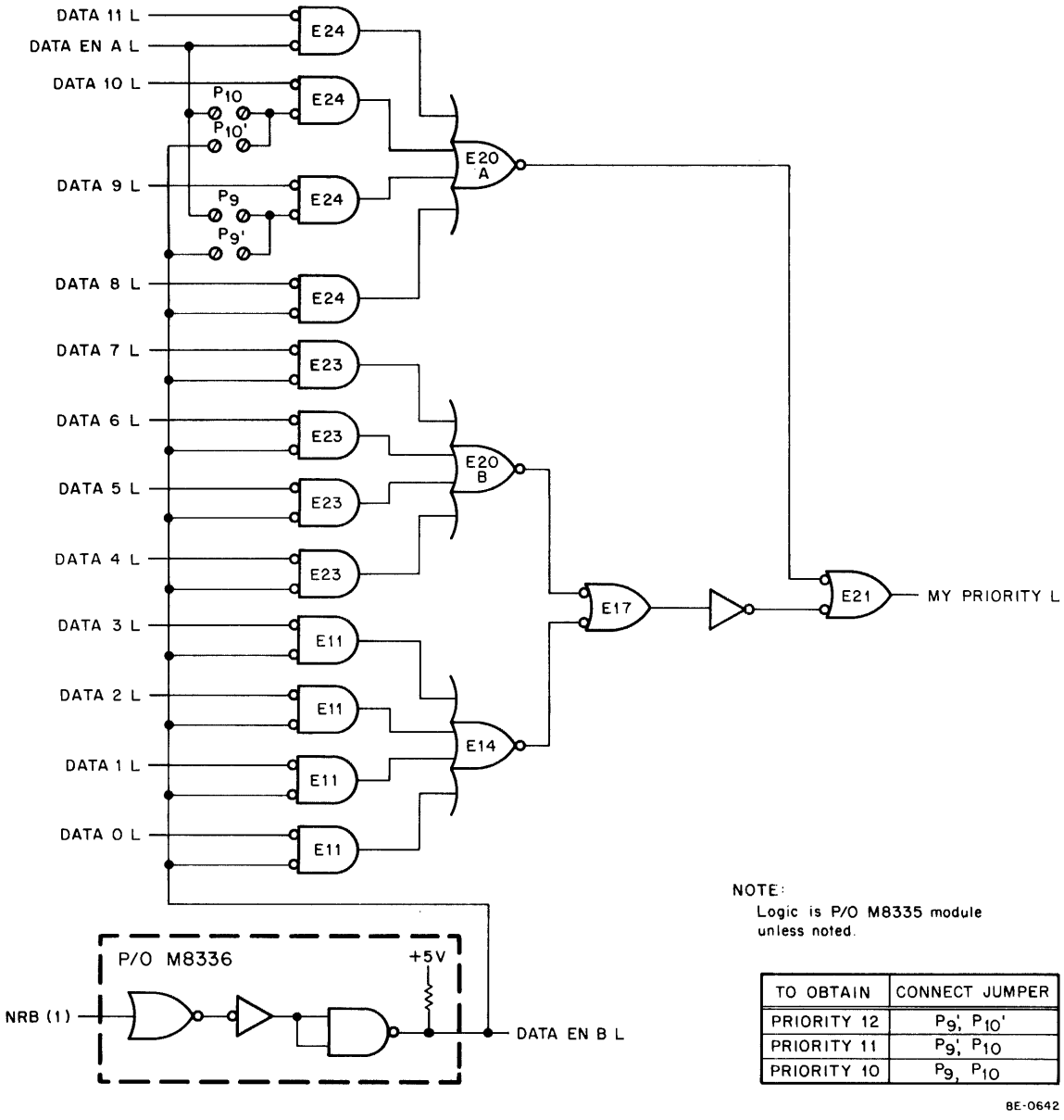


Figure 12-33 Priority Logic

Three DEC 74157 ICs (quad multiplexers) are included in the Line Buffer Register logic. The READ SELECT signal controls the multiplexers, causing either the A_n inputs or the B_n inputs to be gated to the f_n outputs. The outputs are transferred to the Video Buffer logic, alphanumeric or graphic, and converted to serial video information.

Figure 12-37 shows a timing diagram that illustrates how the Line Buffer Register and the multiplexer are controlled when 32 alphanumeric characters are to be displayed. The timing shown is relative; pulse durations, gate widths, etc., may or may not be actual.

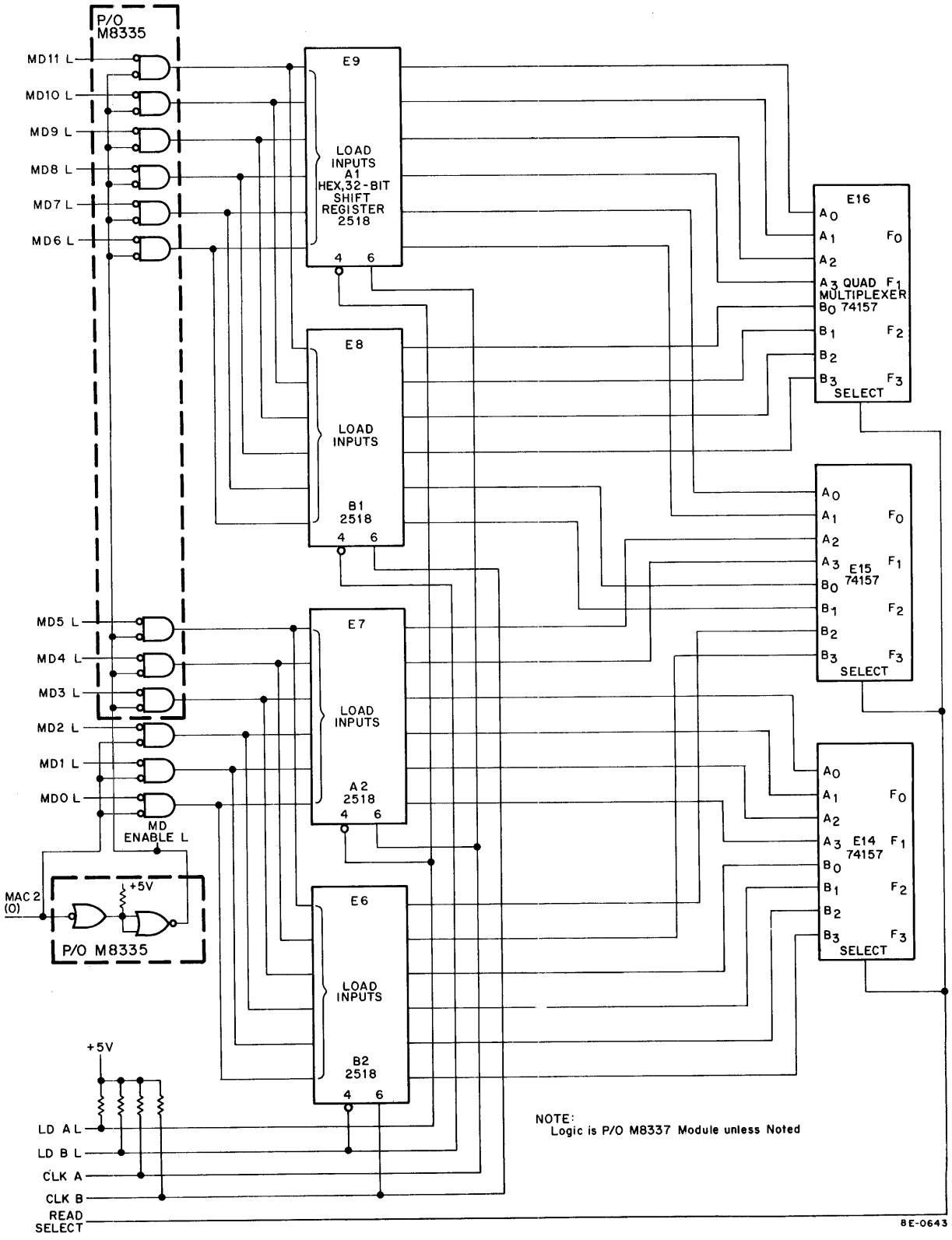


Figure 12-34 Line Buffer Register Logic

The period of time represented as t_1 is that period during which 32 data breaks are being performed (remember that two scan lines are set aside for this purpose). During t_1 the Line Buffer Register must be loaded from the MD lines. The Line Buffer Register Control logic (Figure 12-35) asserts the LD B L signal (the signal E19-D is low throughout t_1, keeping the VIS ZONE L signal high). Each data break cycle causes a data word to be gated to the B Register LOAD inputs. The BRK SHIFT signal that occurs during TS3 L of the break cycle is gated through NAND gate E37A, since the ALPHA CLK ALT is always cleared during a 32 character operation. This causes a CLK B signal to be produced. When 32 data words have been loaded into the register, the COUNTING signal goes low and data breaks cease (COUNTING goes low at TP1 of the break cycle, while BRK SHIFT is asserted during TS3 L).

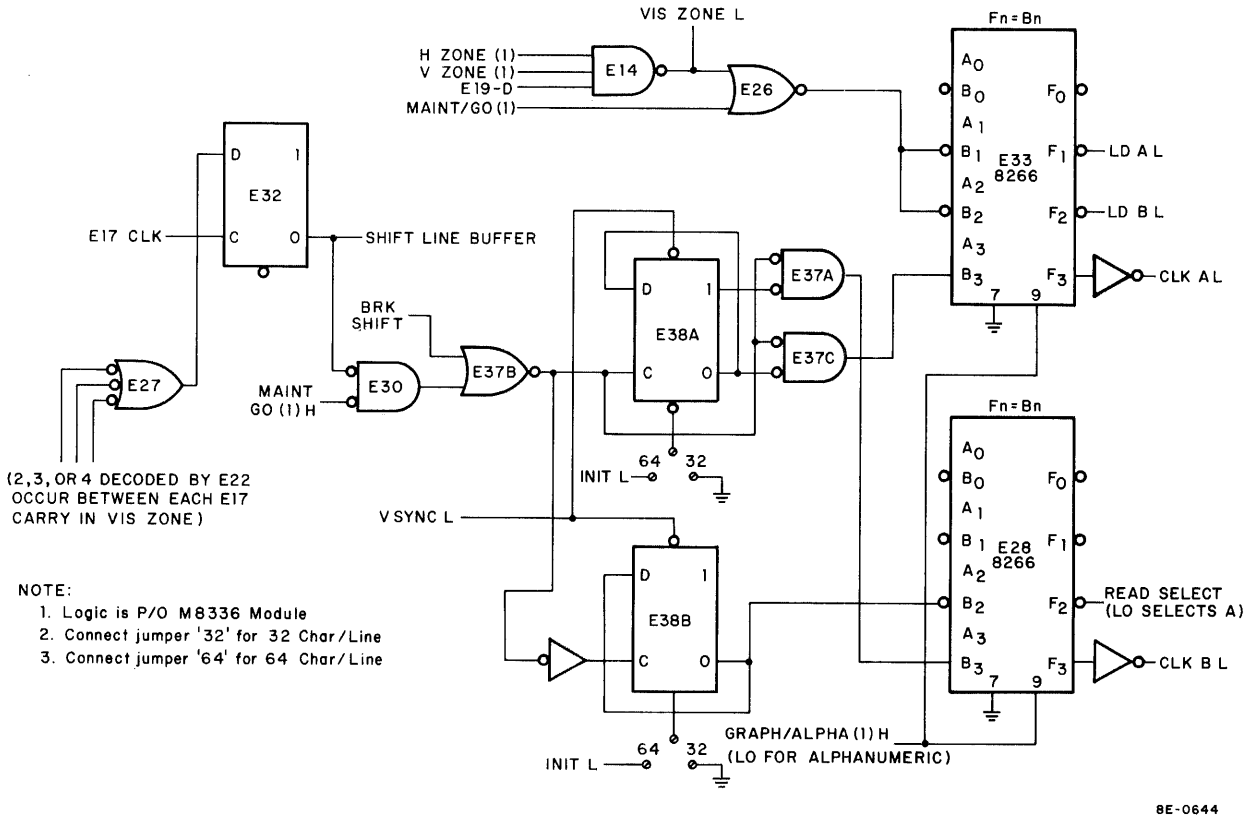


Figure 12-35 Line Buffer Register Control Logic

Throughout each of the next eight scan lines, the Line Buffer Register must be shifted end-around. Period t_2 represents the third scan line and the beginning of the fourth. The VIS ZONE L signal is asserted when HZONE(1) goes high. The LD B L signal is negated, placing the register in the recirculating mode. During the time that VIS ZONE L is low, the VT8-E timing generates 32 SHIFT LINE BUFFER signals. These signals enable NAND gate E37A, thereby generating the CLK B signal. The register is shifted end-around by 32 CLK B signals. (Note that 31 CLK B signals are sufficient to shift all 32 characters through the multiplexer, but 32 are needed for the recirculation.) Each time a character is placed on the register outputs, the multiplexer gates it to the ROM Character logic (only the 6-bit ASCII code, bits 6–11, is gated to the ROM). There it is converted to serial video information for display.

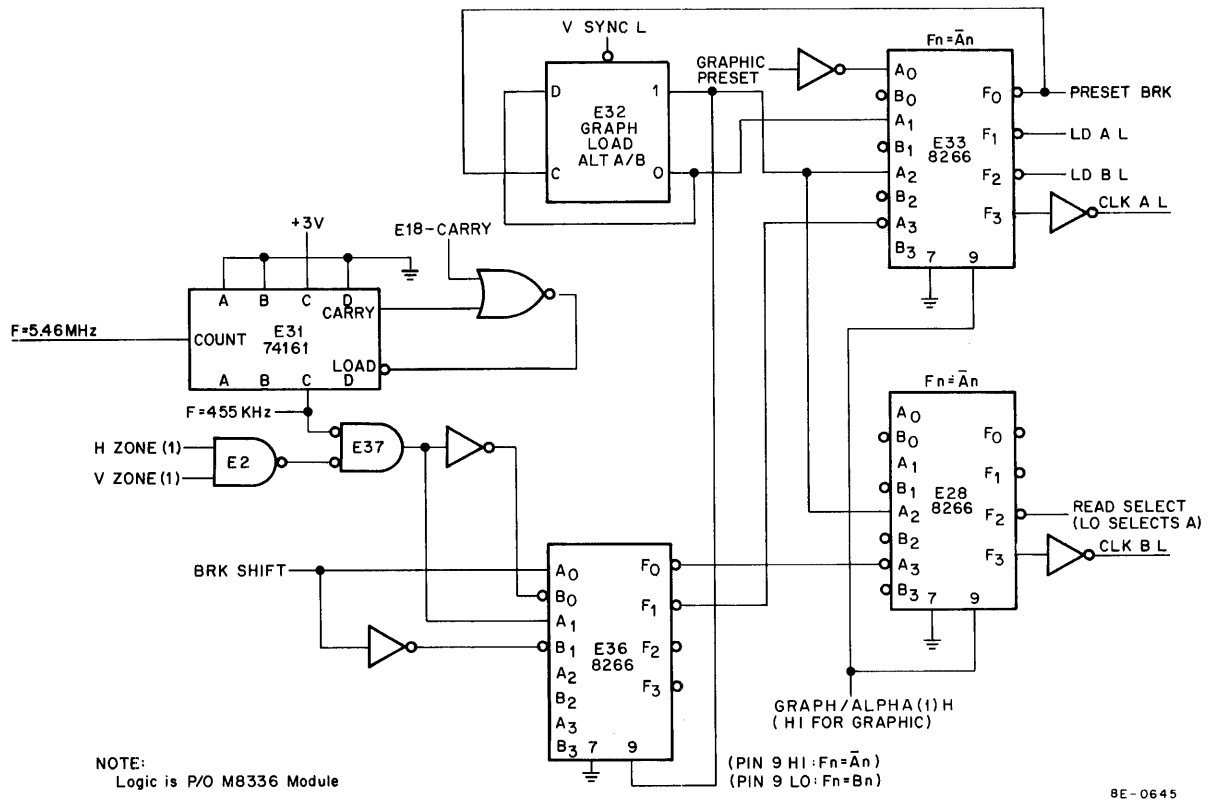


Figure 12-36 Line Buffer Register

The same operation is performed during each succeeding scan line. At the end of the tenth scan line, the character line has been displayed. Another PRESET BRK signal is generated and 32 more characters are loaded into the Line Buffer Register. Note that as these next 32 characters are shifted into the register, the 32 displayed by the just-completed character line are shifted out. Because video is not enabled unless VIS ZONE L is low, there is no danger of these earlier characters being displayed again.

Figure 12-38 shows a timing diagram that illustrates how the Line Buffer Register and the multiplexer are controlled when 64 alphanumeric characters are loaded from the MD lines. Both the A and B Registers are used, providing 64 bits of storage space. As the timing diagram illustrates, the A and B Registers are loaded alternately so that each contains 32 characters when 64 data breaks have been completed. The registers are alternately recirculated during each succeeding scan line (this timing is not shown, but is similar to that of Figure 12-37); when the characters have been displayed, 64 new characters are shifted into the register.

Figure 12-36 shows the logic that controls the Line Buffer Register and the multiplexer during a graphic display. Figure 12-39 shows a timing diagram that illustrates how the graphic data is transferred through the Line Buffer Register logic. Read Select changes every Graphic PRESET which corresponds to every other scan line within the visible zone. When displaying Reg A, CLK A L is generated once for every 12 graphic dot positions that are displayed. This shifts a new word to the output of the Shift Register. The word is then loaded into the Video Buffer after the 12 bits of the previous word have been displayed.

Both the A and B Registers are used when graphic data is displayed. One register is loaded from the MD lines with 32 data words; simultaneously, the information in the other register is displayed.

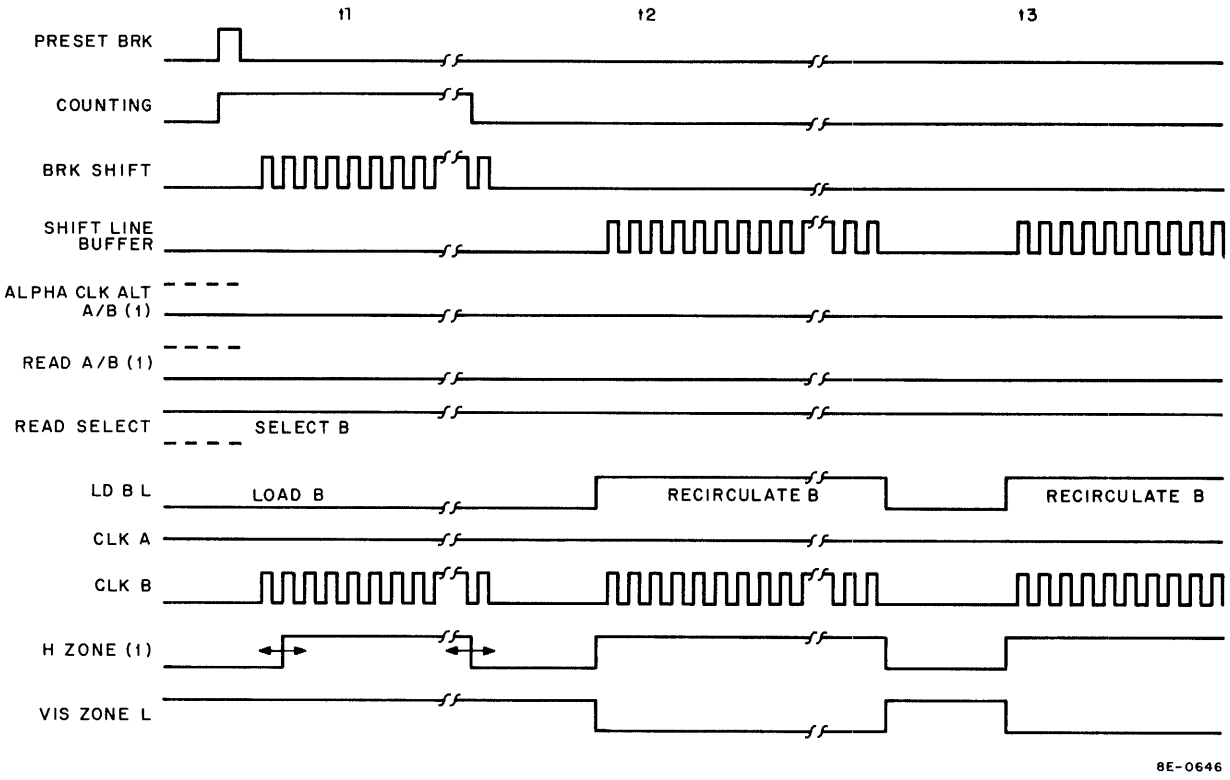


Figure 12-37 Line Buffer Timing for 32 Character Line

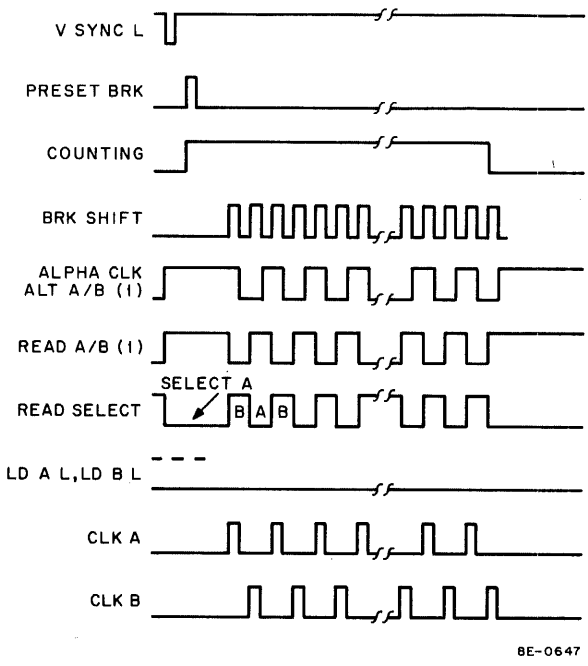


Figure 12-38 Line Buffer Timing for 64 Character Line

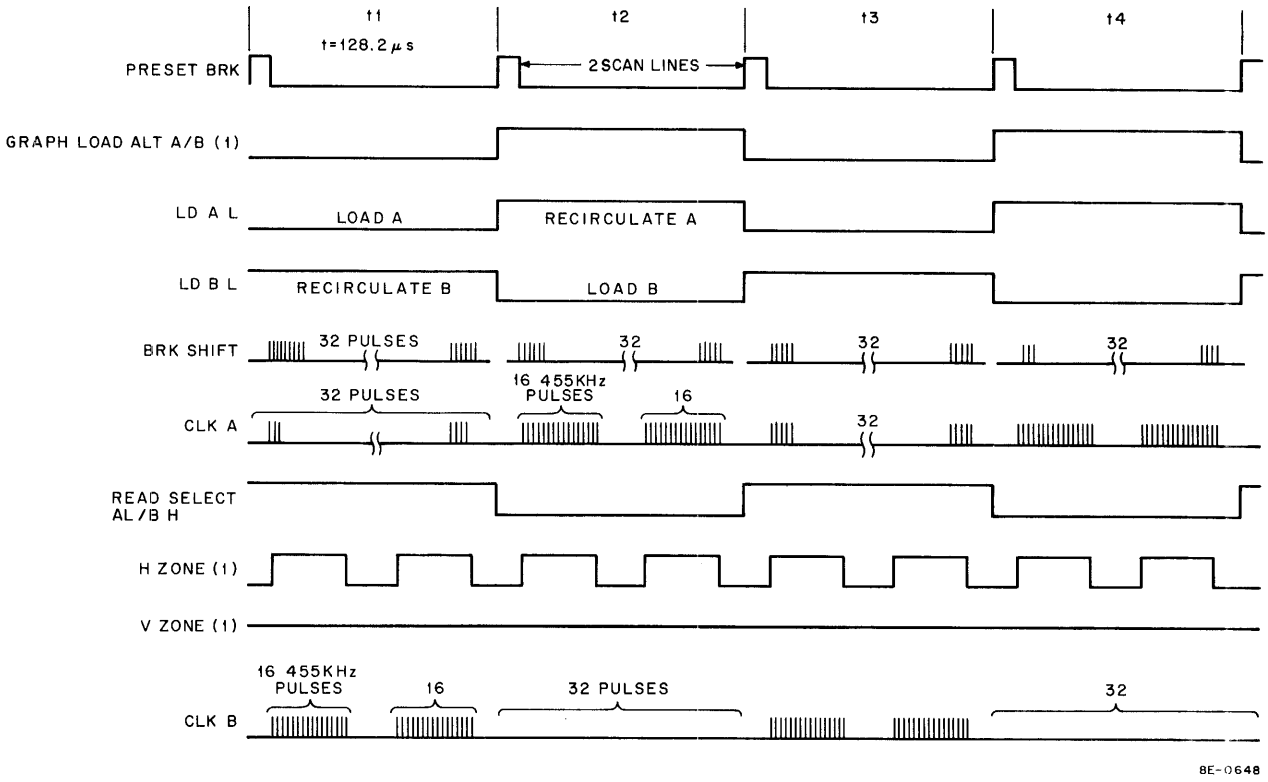


Figure 12-39 Line Buffer Timing

12.4.2.9 ROM Character Generator Logic – The ROM Character Generator logic is shown in Figure 12-40. Included in the figure is a representation of the alphanumeric Video Buffer Register. The major components of the character generator are three 23-XXA2 1024-bit read-only memories; each is organized to provide 256 4-bit word locations. A functional logic diagram of 23-XXA2 is shown in Figure 12-41.

ASCII-coded characters are gated from the Line Buffer Register to each ROM on the six lines designated BIT 6–11. The five most significant bits of the character, bits 6–10, are applied to a 1-of-32 decoder (Figure 12-41). The ROM ROW CNT signals, generated in the VT8-E timing, are applied to 1-of-8 decoders. These three signals select one of 256 4-bit data words. The LSB of the ASCII character, bit 11, is used to gate the 4-bit word out of the ROM to the Video Buffer Register, a DEC 7496 5-bit Shift Register. As Figure 12-40 shows, an odd ASCII character (bit 11 is logic 1) causes the ODD ROM outputs to be selected, while an even character causes the EVEN ROM to be selected. The XTRA ROM provides the necessary fifth bit of the data word and is selected for both even and odd characters.

Remember that ten horizontal scan lines are required to display one character line. During the first two scans, the characters are shifted into the Line Buffer Register. During each of the next eight scans, the Line Buffer Register is recirculated. Bits 6–11 of a character are the same during each scan. The ROM ROW CNT signals change during each scan, cycling through the counts 000_2 to 111_2, where ROM LS ROW CNT is the LSB. Consequently, eight consecutive locations are selected for each ASCII character. The first location is blank, the next seven contain the video information that is ultimately displayed.

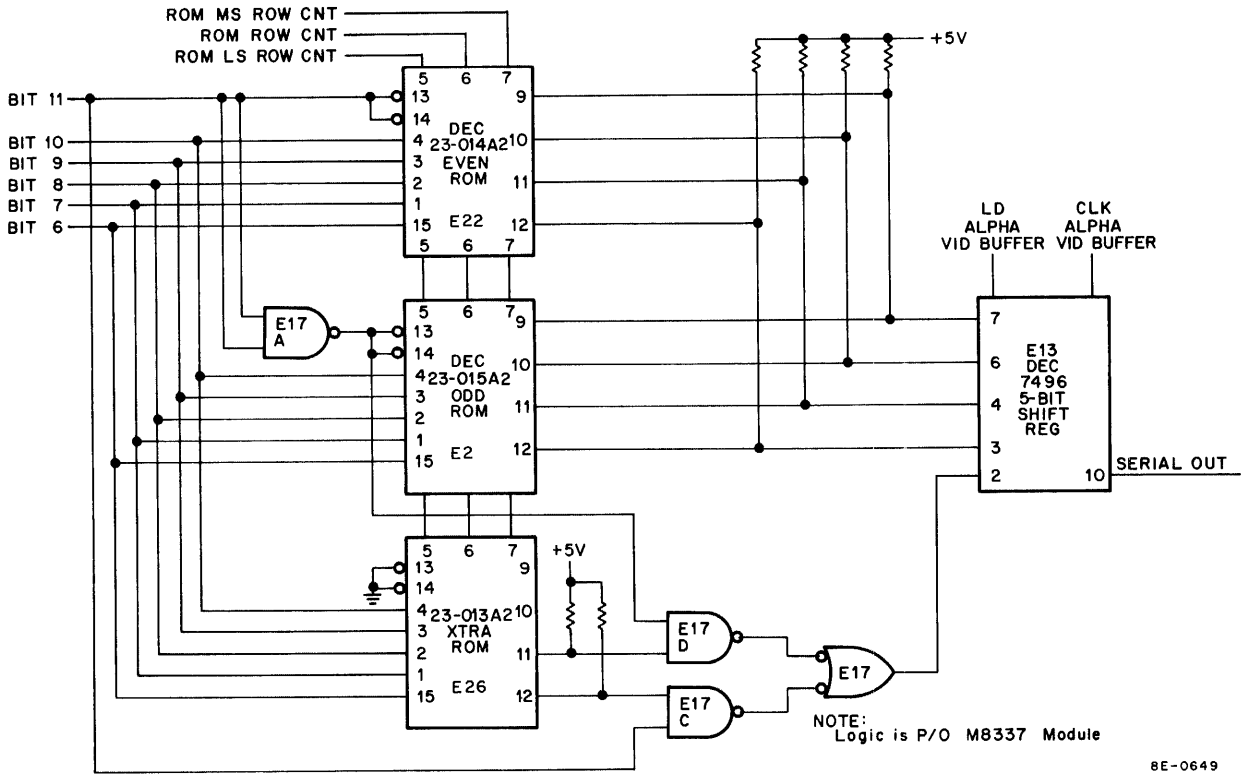


Figure 12-40 ROM Character Generation Logic

Consider the ASCII code for the character H: 001 000 (10_8). Bits 6–10 (001 00) are applied to the 1-of-32 decoder during each scan. During Scan Line 3, the ROM ROW CNT signals are low (000_2). The data in the addressed location is 0000, and no video is displayed. During Scan Line 4, the ROM ROW CNT signals are 001_2. The data in this location is 1000 and is displayed as video. Table 12-8 relates the eight scan lines, the ROM ROW CNT binary representations, and the data in the addressed locations.

The fifth data bit for each scan is taken from the XTRA ROM. Note that only two outputs are available from this ROM. If the character is even, the output at pin 11 is gated to the Video Buffer; if the character is odd, the output at pin 12 is gated. This ROM is addressed exactly as is the EVEN ROM, as indicated in Table 12-9. The fifth data bit for H is taken from pin 11 of the XTRA ROM. The result is shown below.

Scan Line	Data Bits Gated to Video Buffer
3	00000
4	10001
5	10001
6	10001
7	11111
8	10001
9	10001
10	10001

NOTE: The pattern is generated for H.

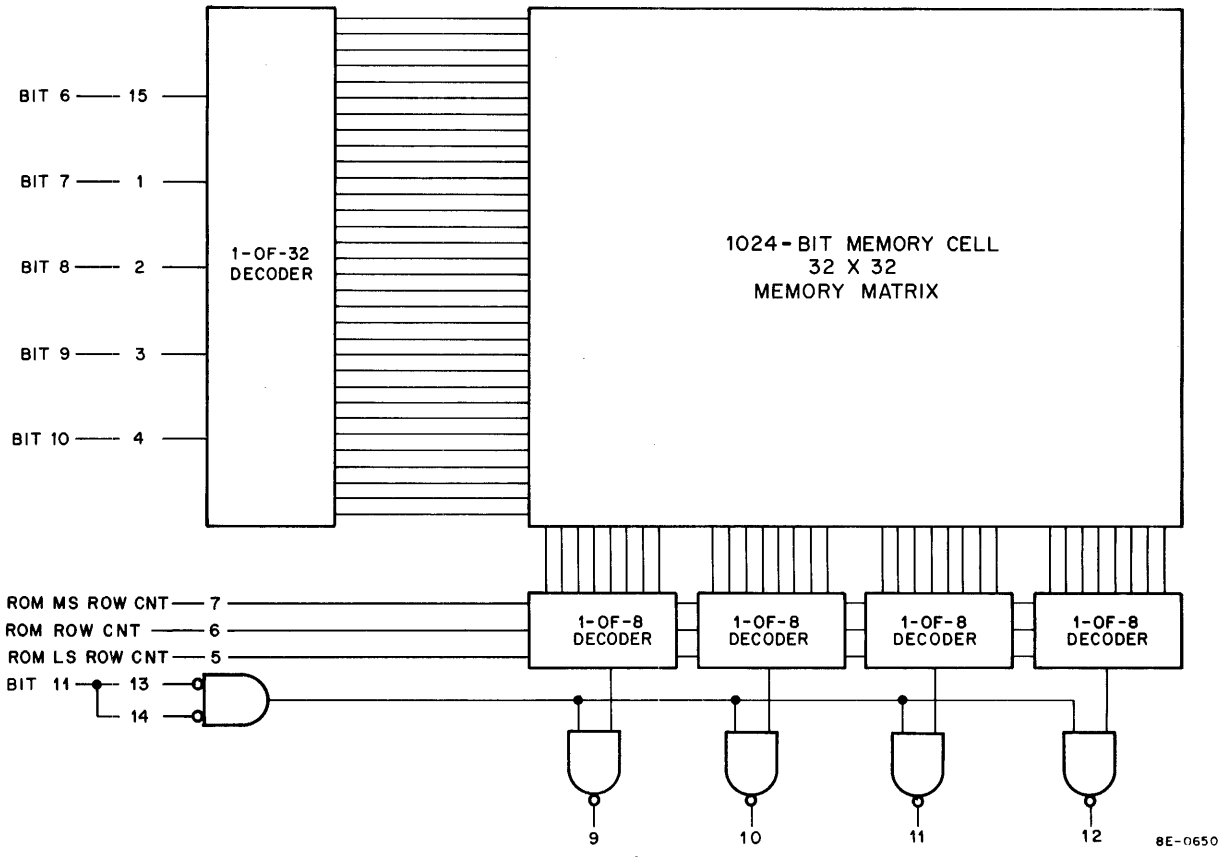


Figure 12-41 ROM Functional Logic Diagram

Table 12-8
Character H, EVEN ROM Data Bits

Scan Line	Bits 6--10	ROM ROW CNT Binary Representation	Data Word in Addressed Location
3	00100	000	0000
4	00100	001	1000
5	00100	010	1000
6	00100	011	1000
7	00100	100	1111
8	00100	101	1000
9	00100	110	1000
10	00100	111	1000

Table 12-9
Character H, XTRA ROM Data Bits

Scan Line	Bits 6–10	ROM ROW CNT Binary Representation	Data Word in Addressed Location
3	00100	000	0000
4	00100	001	0010
5	00100	010	0010
6	00100	011	0010
7	00100	100	0010
8	00100	101	0010
9	00100	110	0010
10	00100	111	0010
			PIN 11 PIN 12

The pattern table for each ROM is included in Appendix A. To locate the pattern for an ASCII character, use the following procedure:

Step	Procedure
1	If the character is even, divide the 6-bit binary representation by 2. The result gives the 6 most significant bits of the location.
2	Find this location in the Octal Location column of the EVEN ROM pattern table (Table A-1) for 4 of the data bits; find the same location in the Octal Location column of the XTRA ROM pattern table (Table A-3) for the fifth data bit. For example: When the binary representation of character T, 010 100 (24_8), is divided by 2, the result is 001 010 (12_8); octal locations 120–127 of the EVEN and XTRA ROMs contain the video information for the character.
3	If the character is odd, take the even binary representation immediately preceding the odd binary representation and divide by 2.
4	Find this location in the ODD and XTRA ROM pattern tables (Tables A-2 and A-3). For example: To find the pattern for character G, 000 111 (07_8), divide 000 110 (06_8) by 2; the result, 000 011 (03_8), identifies locations 030–037 as yielding G.

12.4.2.10 Alphanumeric Video Buffer Control Logic – Figure 12-42 shows the alphanumeric Video Buffer Control logic. The logic generates the signals that allow the Video Buffer to convert the parallel ROM bits to serial alphanumeric video bits. The logic is shown for 32 characters per line; if 64 characters per line are being displayed, the input clock frequency is 10.92 MHz. Figure 12-43 shows a timing diagram for the 32 character per line operation. Refer to both figures when reading the logic description.

The 5.46 MHz signal is gated by the logic to produce the LD ALPHA VIDEO BUFFER and CLK ALPHA VIDEO BUFFER signals. The E17 up-counter provides the necessary gating signals. The A, B, and C outputs of E17 are applied to the DEC 7442 BCD-to-Decimal Decoder, E22. When E22 decodes decimal 2, E26C is enabled and the next clock produces a LD ALPHA VIDEO BUFFER signal. When E22 decodes decimal 3 through 7, E26B is enabled

and 5 clock pulses are gated through to produce CLK ALPHA VIDEO BUFFER. A VID EN signal is also generated when E22 decodes decimal 3 through 7. This signal is asserted through the E28 multiplexer when the VIS ZONE L signal is low (note that the VIS ZONE L must be low for E22 to decode decimal 1 through 7).

Because E17 determines character rate, one LD ALPHA VIDEO BUFFER signal, one VID EN signal, and five CLK ALPHA VID BUFFER signals are generated each time a character is shifted from the Line Buffer Register. Remember that 32 SHIFT LINE BUFFER signals are used to recirculate the Line Buffer Register during each scan. Each SHIFT LINE BUFFER signal generates a CLK B signal that shifts a different character to the ROM Character Generator. The character generator produces five bits that represent the character. A LD ALPHA VIDEO BUFFER signal then parallel loads these bits into the Video Buffer Register.

Five CLK ALPHA VIDEO BUFFER signals shift the data bits out of the buffer to the video logic. The VID EN signal enables the video logic to generate signals for the display. Note that the LD ALPHA VID BUFFER signal, designated A in Figure 12-43, loads the character that is shifted from the Line Buffer Register by the CLK B signal designated A. While this character is being shifted from the Video Buffer, the new 5-bit character is being gated to the buffer inputs. Note, also, that the character horizontal spacing is determined by the gating of the 5.46 MHz signal. The character width is represented by five clock pulses (0.185 inches for 32 characters/line); the horizontal spacing is represented by the two clock pulses in each character period that are not gated (indicated by the dotted-line CLK ALPHA VIDEO BUFFER pulses). Thus, the spacing is 40 percent of the character width, or 0.074 inches.

Figure 12-44 shows the timing of the alphanumeric Video Buffer Control logic for 64 characters per line. The logic is the same as for 32 characters per line operation.

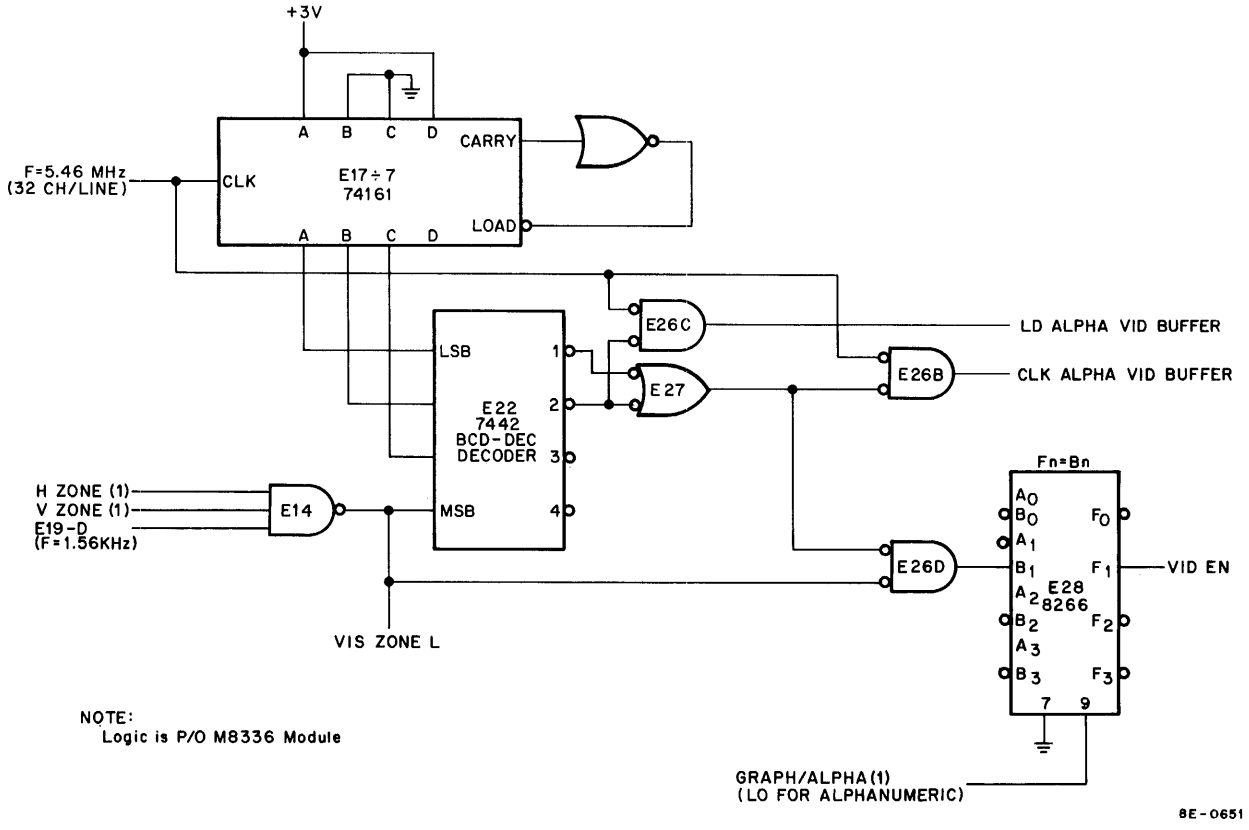


Figure 12-42 Alphanumeric Video Buffer

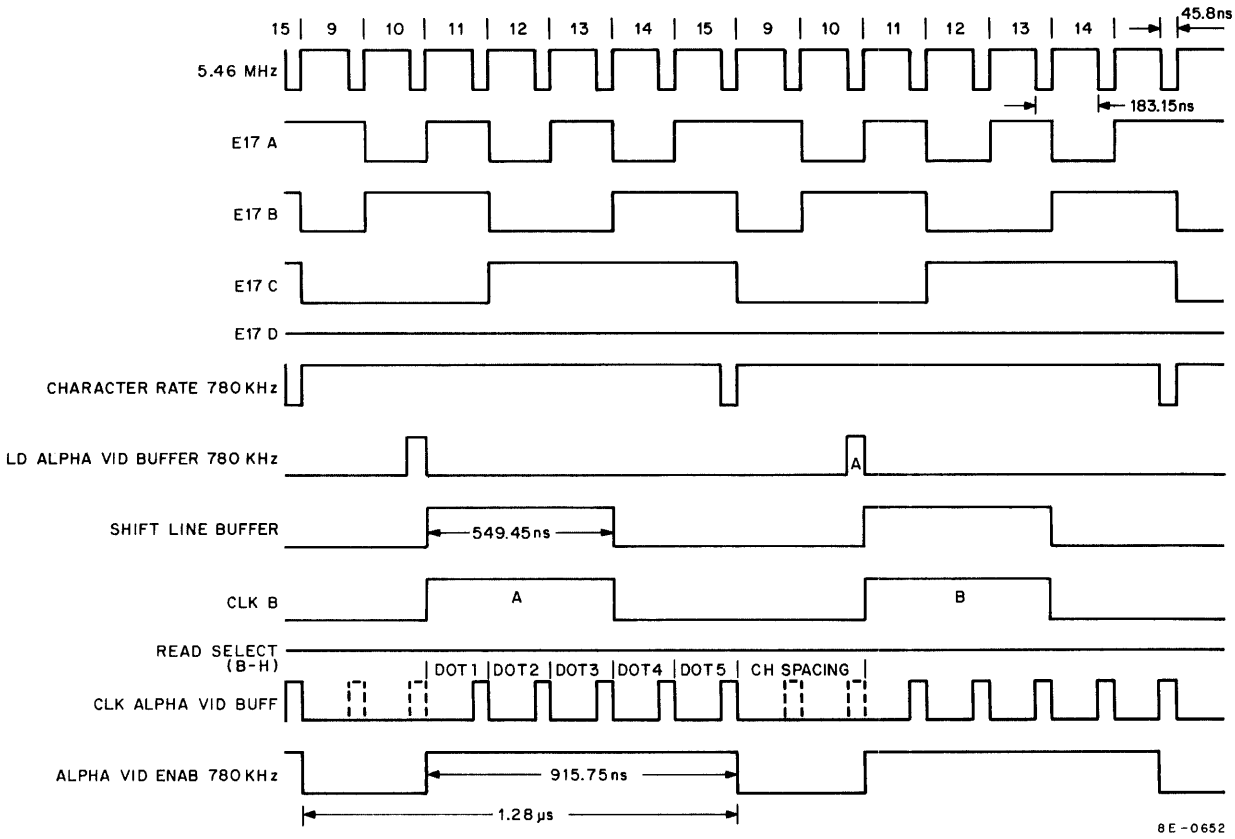


Figure 12-43 Character Timing for a 32 Character Line

12.4.2.11 Graphic Video Buffer and Control Logic – The Graphic Video Buffer and Control logic is shown in Figure 12-45. This logic converts the parallel data in the Line Buffer Register to the serial graphic video signals that are applied to the Display Mode logic.

When a data word is shifted from the Line Buffer Register, it is applied to the Graphic Video Buffer on the lines designated BIT 11–0. The Video Buffer Register comprises three DEC 7595 4-bit Shift Registers that can be parallel loaded and serial shifted. The DEC 74161 counter, E31, counts down the 5.46 MHz clock pulses to produce an LD GRAPH VID BUFFER signal at a frequency of 455 kHz. The derivation of this signal is shown in the timing diagram in Figure 12-46. Graphic Video Buffer is loaded by CLK GRAPH VID BUFFER when LD GRAPH VID BUFFER is true. This occurs every 12 clock pulses.

When the Video Buffer has been loaded, the LD GRAPH VID BUFFER signal goes low. The DEC 7495 Shift Register cannot be shifted while this signal is high. The next eleven CLK GRAPH VID BUFFER signals shift data out of the register (bit 0 is shifted out first). Note that bit 11 is not shifted from the register since only 11 shift pulses are available. Twelve CLK GRAPH VID BUFFER signals are also used to chop graphic video into distinct dots. This occurs at AND gate E28.

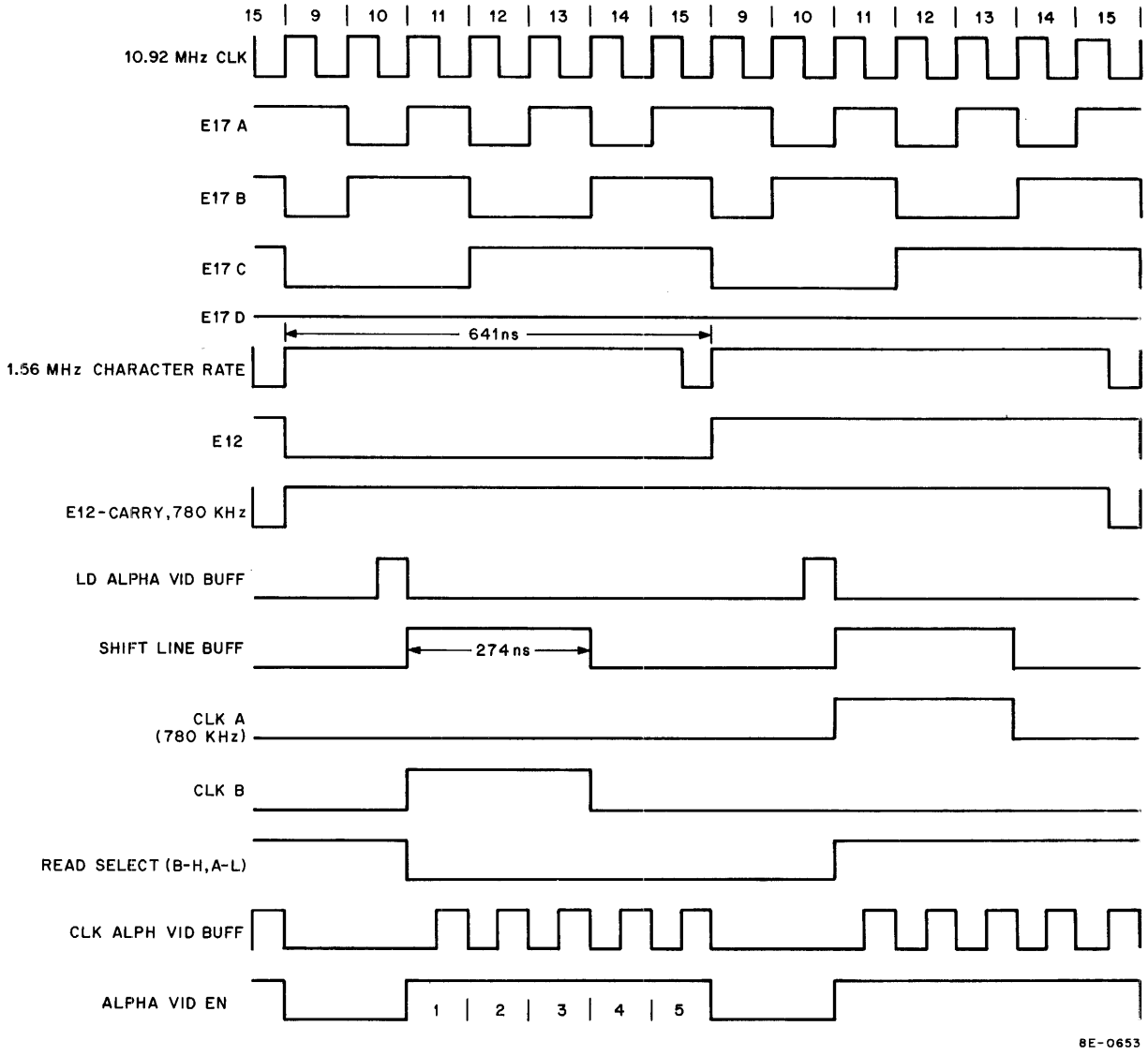


Figure 12-44 Character Timing for a 64 Character Line

12.4.2.12 Visible Field Logic – When an alphanumeric character is to be displayed, the data word transferred to the Line Buffer Register contains not only character information, but also information that controls the visible field and the mode of display. The 12-bit data word is shown in Figure 12-47.

The ASCII-coded character is contained in bits 5–11. Because the VT8-E displays a 64 character set, only bits 6–11 are used to generate character video. Control bits 1 and 2 (referred to as CB1 and CB2) are used to determine the visible field by selectively blanking the video display. Control bits 3 and 4 (referred to as CB3 and CB4) determine how the video is displayed.

Figure 12-48 shows the visible field bits logic. These bits control the visible field as outlined in the table accompanying the logic. When J-K flip-flop E44 is set, the BLANK L signal is asserted and the alphanumeric Video Buffer output is inhibited (Figure 12-50 shows how the BLANK L signal inhibits video). Flip-flop E44 is controlled in an intricate manner that can best be described by a timing diagram. This diagram is shown in Figure 12-49. The timing begins with the start of a character line, represented by the PRESET BRK signal.

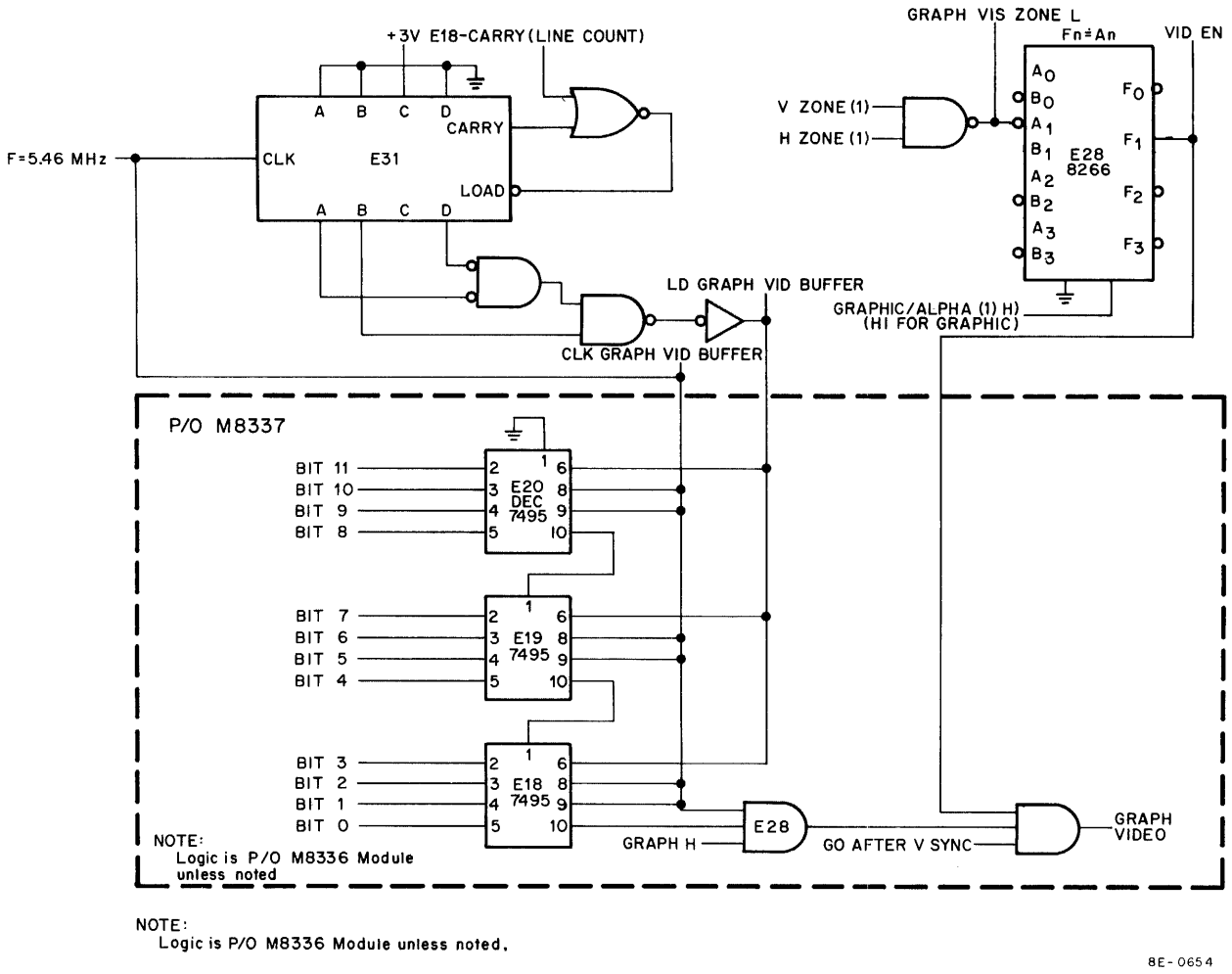


Figure 12-45 Graphic Video Buffer Control Logic

Assume that a character in the previous character line had directed the beginning of a blank field; i.e., CB1 of this character was high, while CB2 was low. When this character was shifted from the Line Buffer Register, the next LD ALPHA VID BUFFER signal to occur sets the J-K flip-flop E50B (Figure 12-47). Each succeeding character is either a NOP direction or another BBF direction (both have the same result in the present situation). At the beginning of the present character line, a PRESET BRK signal and a LINE CNT signal occur simultaneously. The leading edge of the LINE CNT signal clears the E44 flip-flop, while the trailing edge of the PRESET BRK signal sets flip-flop E50A. The next LINE CNT signal sets E44 again, because now E50A is set. All three flip-flops would remain in this state throughout the entire character line and into and through each succeeding character line if no EBF direction were received.

However, if an EBF direction is programmed into a data word, the blank field must be ended at the same point in Scan Lines 3 through 10 (although nothing is displayed in Scan Line 3). Assume that character 16 of the present character line directs an end to the blank field. The LD ALPHA VIDEO BUFFER signal corresponding to character 16 clears flip-flops E44 and E50B. For the rest of Scan Line 3, the BLANK L signal is negated. At the start of the fourth scan line, flip-flop E44 has to be set again to blank the first 15 characters. The LINE CNT signal sets the flip-flop, thereby blanking the first 15 characters of Scan Line 4. Again, the sixteenth character says EBF and clears flip-flop E44 (flip-flop B stays clear throughout). This procedure continues until the character line is completed. The second LINE CNT signal of the next character line clears flip-flop E44, which then remains clear until another BBF or an EOS is directed.

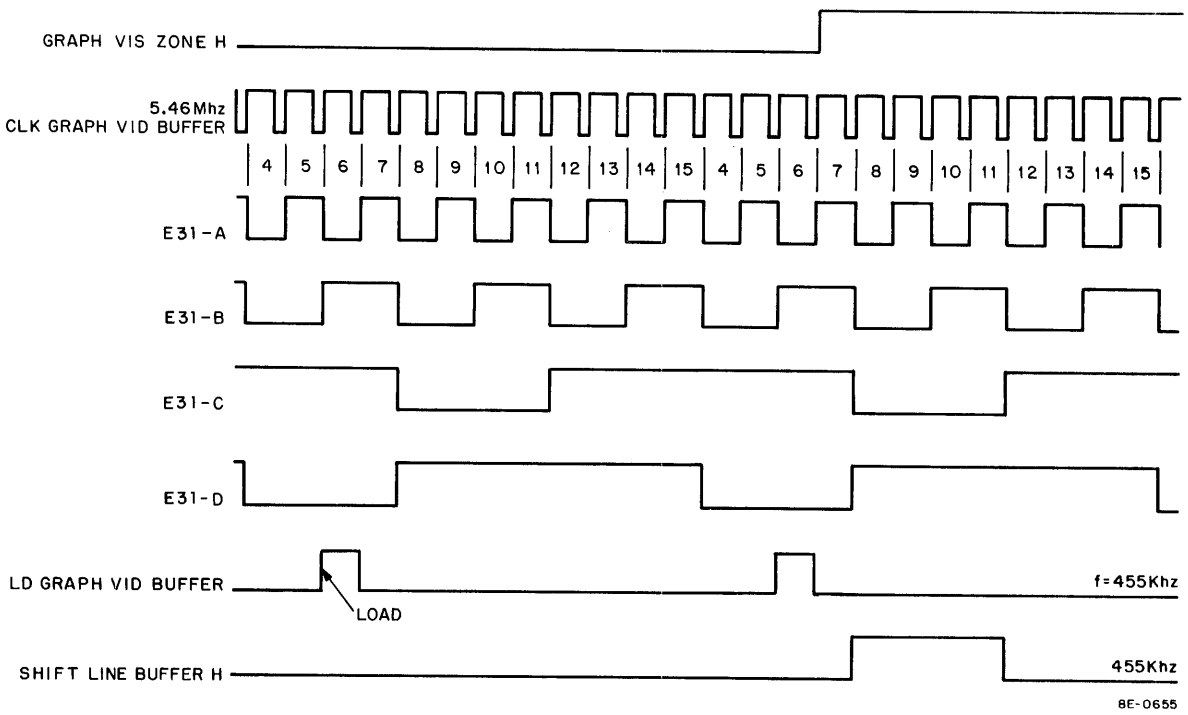


Figure 12-46 Graphic Word Timing

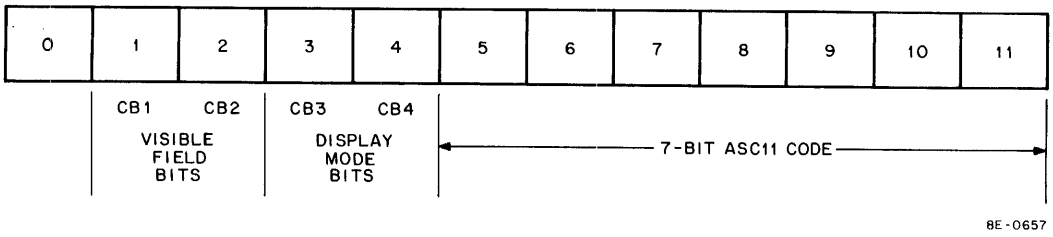
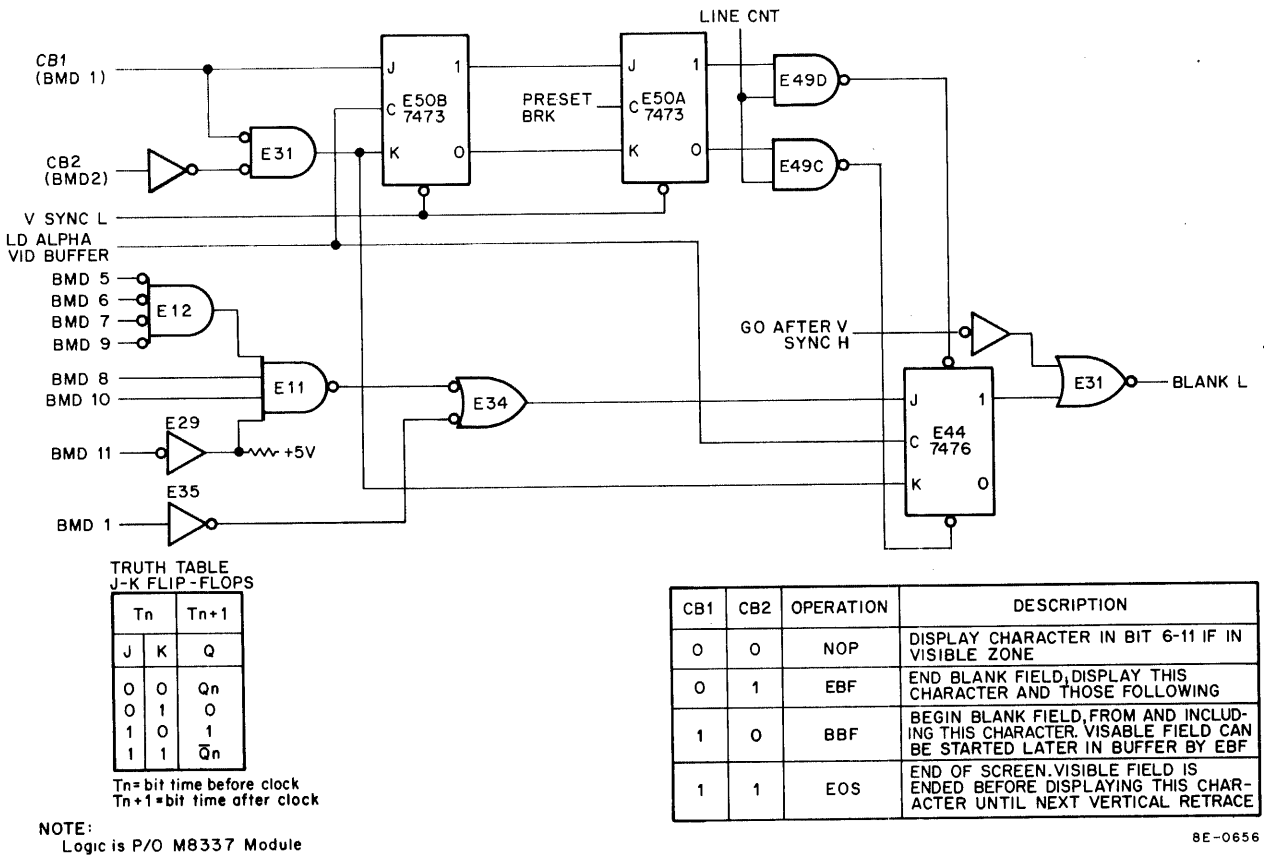


Figure 12-47 12-Bit Data Word Format

When the 7-bit ASCII code for line feed (012) is detected, NAND gate E11 is enabled, putting a high on the J input of flip-flop E44. The LD ALPHA VID BUFFER signal corresponding to the character 012 sets E44, and the rest of the character line is blanked. It would be contradictory to have the EBF control bits set for the line feed character. The K input of E44 should not be a 1 when the LF (012) character is detected.

12.4.2.13 Display Mode Logic – The Display Mode logic is shown in Figure 12-50. These bits determine how the alphanumeric video is displayed, as outlined in the table accompanying the logic.

When the character is to be displayed with normal intensity, the LD ALPHA VID BUFFER signal clears flip-flops E27A and E27B. NAND gate E30B gates the serial output of the alphanumeric Video Buffer Register to NAND gate E39. If the BLANK L signal is not asserted, the asserted ALPHA VID EN signal and the negated GRAPH L signal gate the five data bits to the VIDEO line. If the character is to be displayed at increased intensity, E27A is set, while E27B is cleared. NAND gate E34C is enabled, in addition to E30B. Inverters E29A and E29B have open-collector outputs. For increased intensity, both gates are inactive. Consequently, the VIDEO output is approximately 5V. For normal intensity E29B is active and there is a voltage drop in the neighborhood of 3.5V across the 1 kΩ resistor. Therefore the VIDEO output is approximately 3.5V.



TRUTH TABLE
J-K FLIP-FLOPS

Tn		Tn+1
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Q}n$

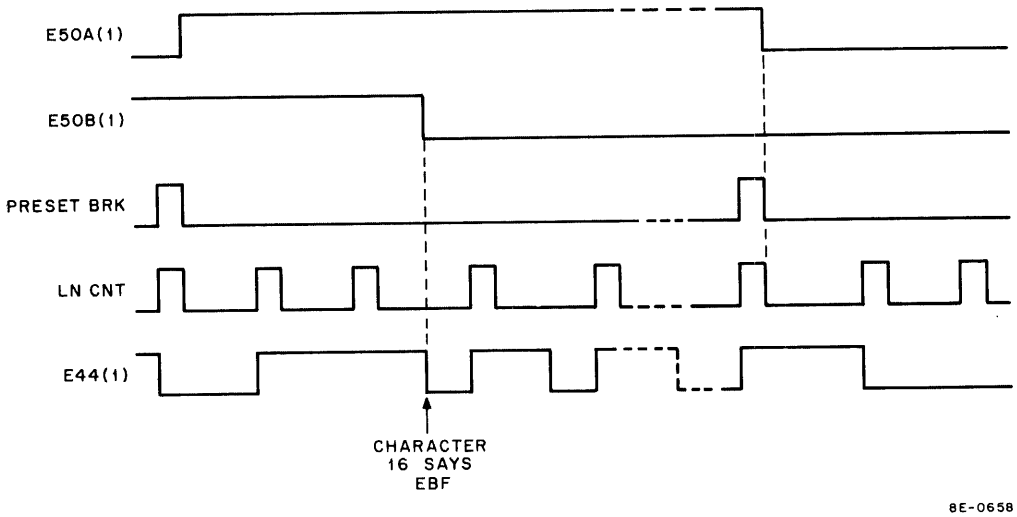
Tn = bit time before clock
Tn+1 = bit time after clock

NOTE:
Logic is P/O M8337 Module

CB1	CB2	OPERATION	DESCRIPTION
0	0	NOP	DISPLAY CHARACTER IN BIT 6-11 IF IN VISIBLE ZONE
0	1	EBF	END BLANK FIELD, DISPLAY THIS CHARACTER AND THOSE FOLLOWING
1	0	BBF	BEGIN BLANK FIELD, FROM AND INCLUDING THIS CHARACTER. VISABLE FIELD CAN BE STARTED LATER IN BUFFER BY EBF
1	1	EOS	END OF SCREEN. VISIBLE FIELD IS ENDED BEFORE DISPLAYING THIS CHARACTER UNTIL NEXT VERTICAL RETRACE

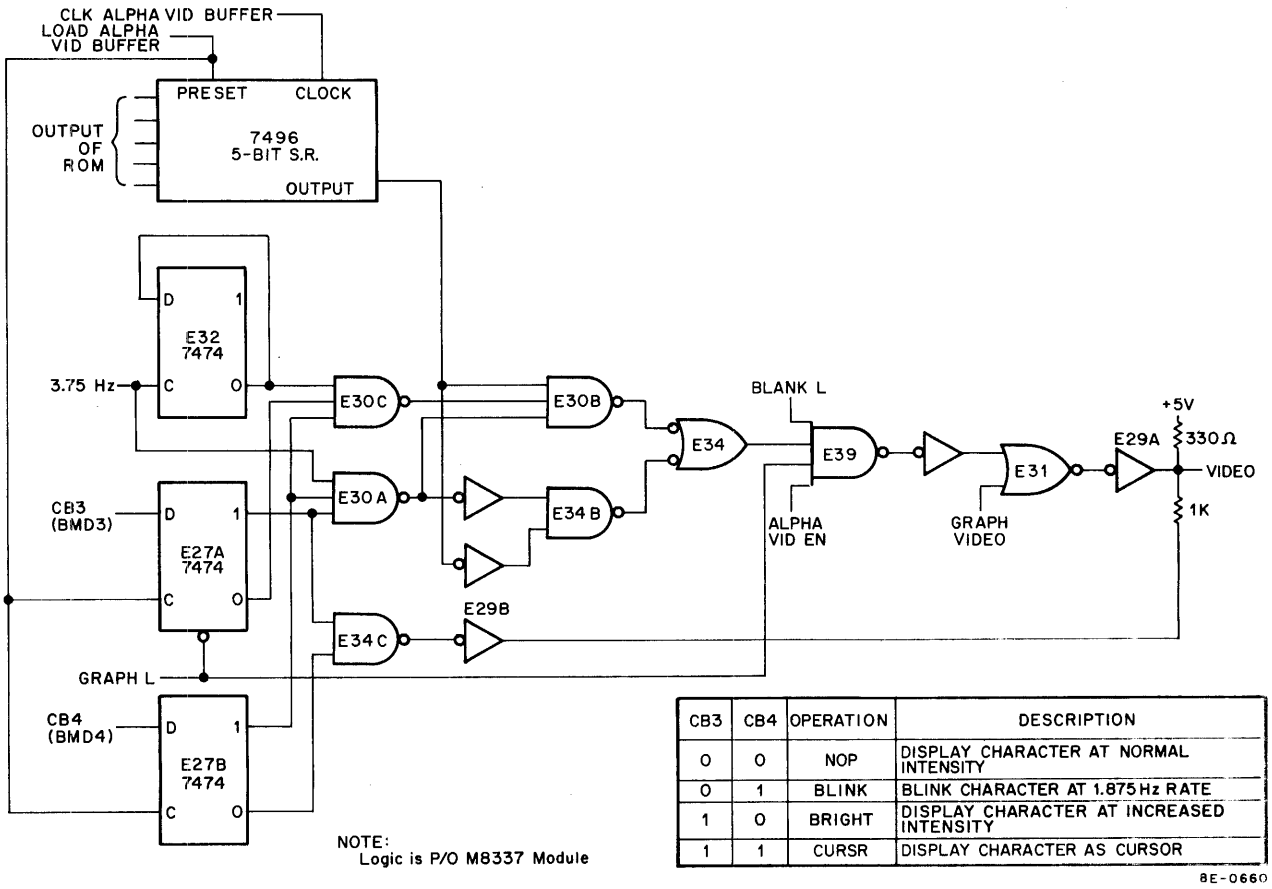
8E-0656

Figure 12-48 Display Control Logic



8E-0658

Figure 12-49 BBF and EBF Timing



CB3	CB4	OPERATION	DESCRIPTION
0	0	NOP	DISPLAY CHARACTER AT NORMAL INTENSITY
0	1	BLINK	BLINK CHARACTER AT 1.875 Hz RATE
1	0	BRIGHT	DISPLAY CHARACTER AT INCREASED INTENSITY
1	1	CURSR	DISPLAY CHARACTER AS CURSOR

Figure 12-50 Display Mode Logic

A character is blinked at a 1.875 Hz rate when CB3 is logic 0 and CB4 is logic 1. The 3.75 Hz signal clocks flip-flop E32. The 0-output of the flip-flop alternately enables and disables NAND gate E30C, resulting in a VIDEO signal that blinks at the desired rate. If CB3 and CB4 are both logic 1, NAND gate E30A is alternately enabled and disabled by the 3.75 Hz signal. NAND gate E30B is enabled by the character bit, while NAND gate E34B is enabled by the character's bit matrix complement. Thus, the character is displayed as a cursor.

12.4.2.14 Maintenance IOT Logic – The Maintenance IOT logic, shown in Figure 12-51, is enabled at TP3 time if the program executes the DPSM instruction to set the MAINT/GO flip-flop (E56). Refer to Paragraph 12.3.4 for a description of the IOT instructions enabled when the VT8-E is in the Maintenance mode. These instructions allow the registers and buffers in the VT8-E to be read into the AC. Data may also be transferred from memory using the DPMB instruction. DPMB sets the BRK RQST flip-flop on the M8337 module and the VT8-E executes one Single Cycle Data Break to transfer data from the memory location determined by the Starting Address Register to the Line Buffer.

12.4.2.15 Display Interrupt and Skip Logic – The Interrupt and Skip logic is shown in Figure 12-52. Interrupts are enabled if bit 11 in the AC is 1 when the DPGO instruction is executed by the program. This sets INT ENA and the VT8-E makes an INT RQST when the Real Time Clock (RTC) flag sets at the start of a vertical retrace and signifies the end of the display frame.

The Skip Bus (SKIP L) is asserted at I/O PAUSE time of the DPCL instruction cycle to cause the program to skip the next sequential instruction. The program may at this time switch modes (Alphanumeric/Graphic) without disturbing the visible presentation.

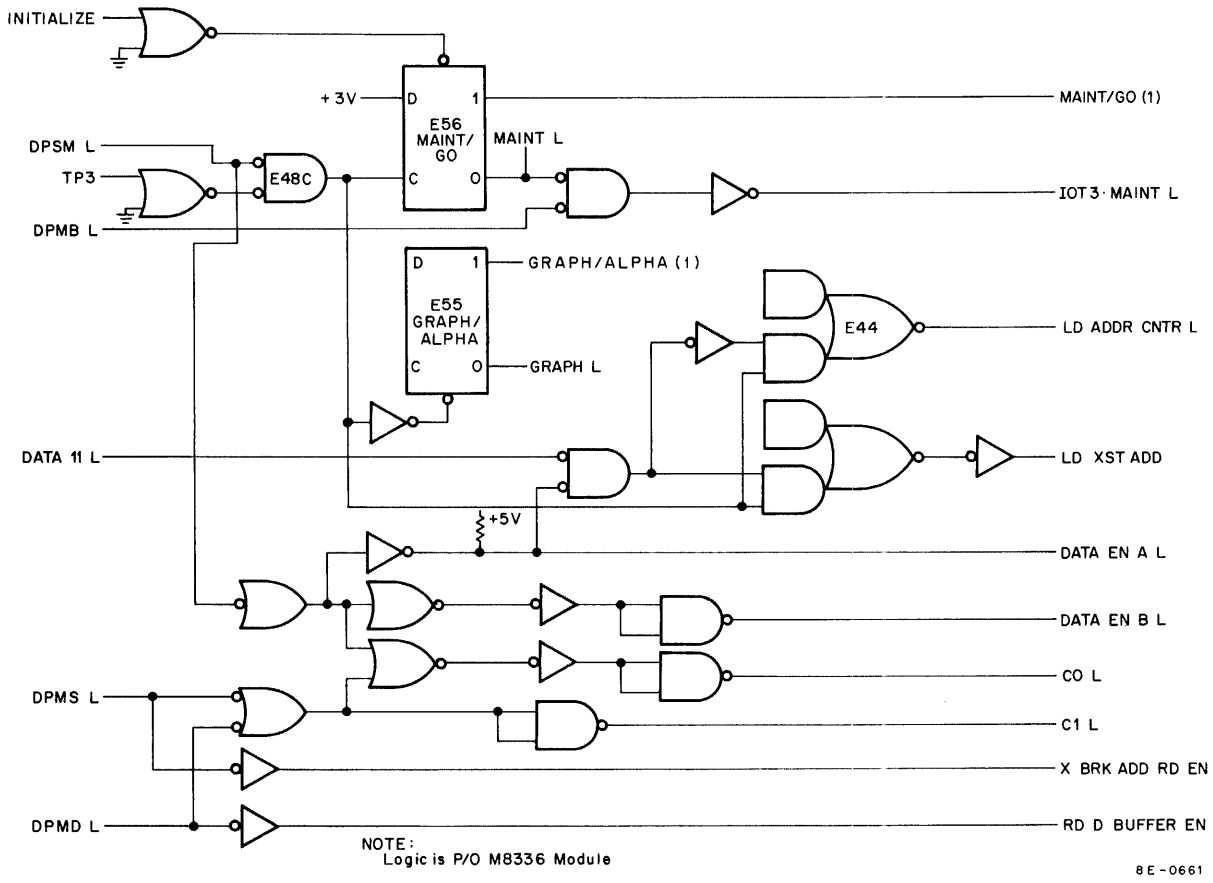


Figure 12-51 Maintenance IOT Logic

12.4.2.16 Bell Logic – The Bell logic is shown in Figure 12-53. BELL EN, a 74123 IC, outputs a 476 ms pulse when the DPBL instruction is executed by the program to enable the 1.56 kHz signal from E11–0 to be applied to the bell. The volume of the tone is adjusted by potentiometer R25 on the M8336 module.

12.5 DISPLAY MONITOR CIRCUITS

12.5.1 Keyboard Logic

The keyboard (Drawing D-CS-3010166-0-0) provides the VT8-E output to the computer. There are 128 ASCII characters or codes that can be generated by the keyboard. A 2-way slide switch is mounted on the Keyboard Logic circuitry board to allow the keyboard to be set for upper/lower case ASCII (128 codes) or lower case ASCII (96 codes) operation. Each key has a variable capacitance that is actuated when the key is pressed, causing an excitation voltage to be applied to one side of the capacitor, generating base drive for the transistor amplifier. A sequential scanning technique is used, employing a MOS integrated circuit that consists of an 8-bit and an 11-bit ring counter (to compose an 8 X 11 matrix), and circuitry to sample the conductance of each transistor amplifier (one per key). As the two (8-bit and 11-bit) registers cycle, the 8-bit counter provides a collector voltage to as many as eleven of the key output amplifiers. Up to eight of the transistor emitters are connected to each of the sensing circuits gated by the 11-bit counter. The two sets of lines that form the 8 X 11 matrix are theoretically capable of sampling up to 88 keys.

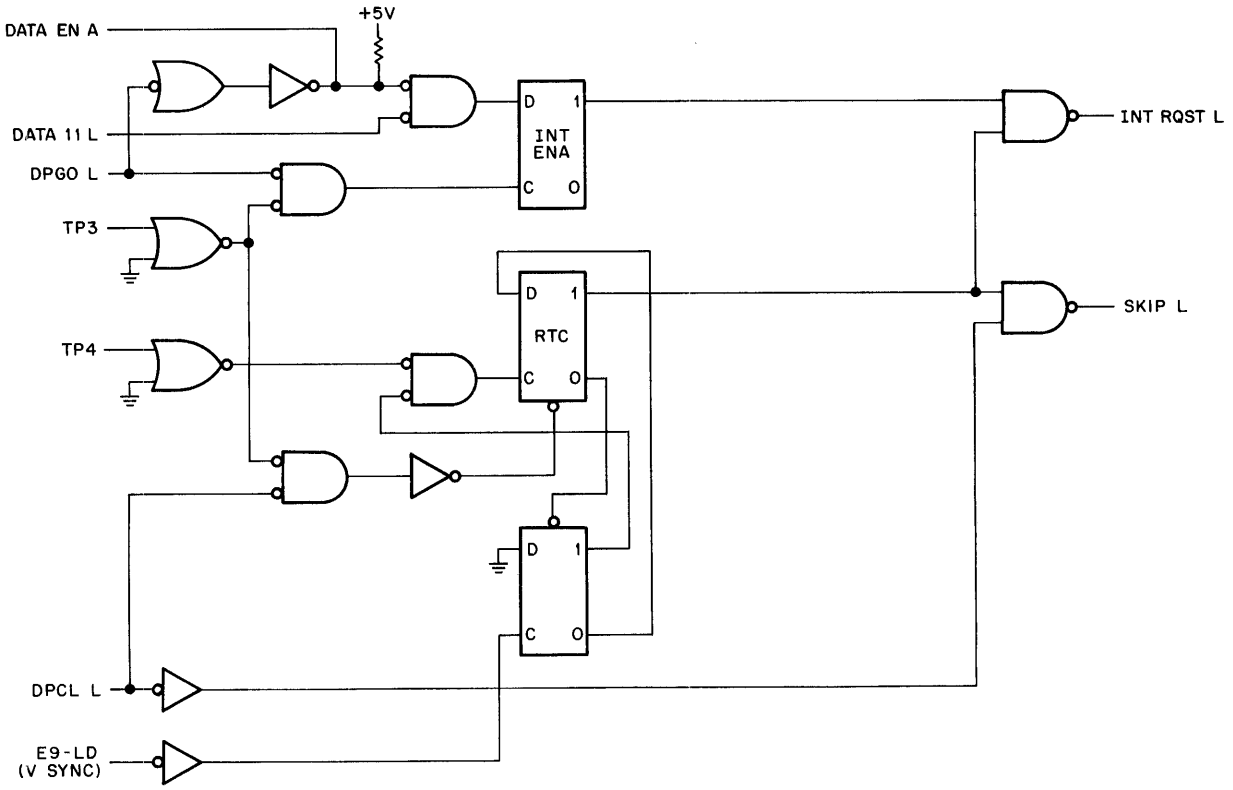


Figure 12-52 Display Interrupt and Skip Logic

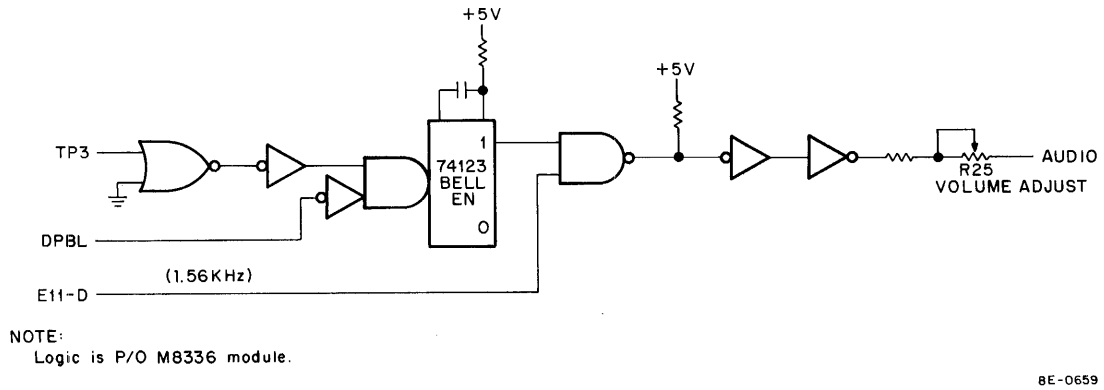


Figure 12-53 Bell Logic

The VT8-E uses the small 8-key keyboard as an extension of the main keyboard to generate cursor control codes to position the cursor and to erase text. The keys used for cursor control or positioning are: cursor up (↑), cursor down (↓), cursor left (←), cursor right (→), and HOME. The erase-to-end-of-line (EOL) and erase-to-end-of-screen (EOS) keys are used in conjunction with the LOCK key. The EOL and EOS codes will not be transmitted unless they are used in conjunction with the LOCK key.

12.5.2 Motorola CRT Display

The following circuit descriptions refer to the detailed circuit schematic of the Motorola CRT Display Module shown in Drawing D-CS-3010326-0-3.

12.5.2.1 Video Amplifier – The Video Amplifier has four stages incorporating devices Q1, Q2, Q3, and Q4. The first stage, Q1, functions as an emitter follower to provide a high impedance input with the 75Ω terminating resistor removed. The high impedance operation permits use of bridging connections to drive a number of monitors from the same signal source. The low output impedance of the first stage permits use of a low resistance contrast control which furnishes flat video response over its entire range without the need for compensation. The collector output of Q1 is used to drive the Sync Separator. C3 provides high frequency roll off to limit the collector output to the band-width required to pass synchronization signals. Q2 is a common emitter stage and is directly coupled to Q4. Q3 and Q4 are connected in a cascade configuration. This common emitter/common base connection greatly reduces the effect of Miller capacity compared with a conventional single transistor video output stage. C6 provides a ground for video at the base of Q3, the grounded base transistor of the video output cascade pair.

The video bias control (R10) is used to set the quiescent collector voltage of Q3, C5, C7, C8, and R15 for high frequency compensation. Restoration of dc voltage is accomplished by setting the video bias control so that sync tips, which are negative-going at the collector of Q3, just go into saturation. Variations in video drive result in variations in the base current of Q2 during sync time due to the low load reflected back when Q3 is saturated. The charge on C4 will thus depend on the amplitude of output collector current during sync time. The result is a clamping action which holds sync tips at the same level despite video signal variations. The Video Amplifier output is direct coupled to the control grid of the CRT. R18 is used to isolate Q3 from transients that may occur as a result of CRT arcing.

12.5.2.2 Sync Separator – The Sync Separator uses a single stage, Q5, to recover sync from the composite video signal. A single-stage Sync Separator is adequate due to the high impedance of the following stages. The video input to the Sync Separator is black positive. C11 is charged by the peak base current that flows when the positive peak of the input takes Q5 to saturation. This charge depends on the peak-to-peak input to Q5 and thus makes the bias for Q5 track the amplitude of the input signal. As a result, Q5 amplifies only the positive peaks of the input signal. The initial bias current through R24 sets the clipping level.

12.5.2.3 Phase Detector – The Phase Detector uses two diodes in a key clamp circuit. Two inputs are required to generate the required output, one from the Sync Separator and one from the horizontal deflection system. The required output must be of the correct polarity and amplitude to correct phase differences between the input sync and the horizontal time base. The horizontal collector pulse is integrated into a sawtooth by R45 and C15. During sync time, both diodes in D7 conduct, shorting C15 to ground.

The sawtooth on C15 is thus clamped to ground at sync time. If the horizontal time base is in phase with the sync, the sync pulse will occur when the sawtooth is passing through its ac axis and the net charge on C15 will be 0 (Figure 12-54). If the horizontal time base is lagging the sync, the sawtooth on C15 will be clamped to ground at a point negative from the ac axis. This will result in a positive dc charge on C16 (Figure 12-54). This is the correct polarity to cause the Horizontal Oscillator to speed up to correct the phase lag.

Likewise, if the horizontal time base is leading the sync, the sawtooth on C15 will be clamped at a point positive from its ac axis, resulting in a negative charge on C15. This is the required polarity to slow the horizontal oscillator (Figure 12-54). R33, C17, C16, and R32 comprise the Phase Detector Filter. The bandpass of this filter is chosen to correct the Horizontal Oscillator phase without ringing or hunting.

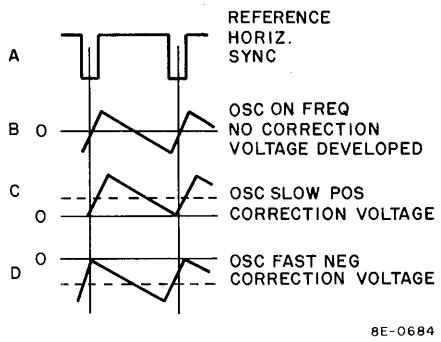


Figure 12-54 CRT Horizontal Oscillator Waveforms

12.5.2.4 Horizontal Oscillator – Q6 is employed in a modified type of Hartley oscillator. The operating frequency of this oscillator is sensitive to its base input voltage. This permits control by the output of the Phase Detector and also by the setting of the horizontal hold control. The horizontal hold range is set by adjusting the core of L1.

12.5.2.5 Pulse Shaper and Horizontal Drive – Q7 is used as a buffer stage between the Horizontal Oscillator and the Horizontal Driver. It provides isolation for the Horizontal Oscillator as well as a low impedance driver for the Horizontal Driver. R38 and C20 form a time constant which shapes the oscillator output to the required duty cycle (approximately 50 percent), to drive the Horizontal Output circuitry. The Horizontal Driver stage, Q8, operates as a switch to drive the Horizontal Output transistor through T1. Because of the low impedance drive and fast switching times furnished by Q7, very little power is dissipated in Q8. C21 and R42 provide damping to suppress ringing of the primary to T1 when Q8 goes into cutoff.

12.5.2.6 Horizontal Output – The secondary of T1 provides the required low drive impedance for Q9. R44 and C24 form a time constant for fast turn-off of the base of Q9. Q9 operates as a switch that, once each horizontal period, connects the supply voltage across the parallel combination of the horizontal deflection yoke and the primary of T2. The required sawtooth of the deflection current through the horizontal yoke is formed by the L-R time constant of the yoke and output transformer primary. The Horizontal Retrace pulse charges C27 through D2 to provide operating voltage for G2 of the CRT. Momentary transients at the collector of Q9, should they occur, are limited to the voltage on C27, since D2 will conduct if the collector voltage exceeds this value.

The damper diode, D1, conducts during the period between retrace and turn-on of Q9. C28 is the retrace tuning capacitor. C29 blocks dc from the deflection yoke. L3 is a magnetically-biased linearity coil that shapes deflection current for optimum trace linearity. L4 is a series width control. C31 and R49, C42 and R68 are damping network components for the linearity and width controls. C43D is charged through D5 developing the video supply voltage.

12.5.2.7 Vertical Oscillator Driver and Output – Sync from the collector of Q5 is integrated by R26 and C35. Q10 and Q11 are connected as a regenerative switch. The series combination of C37 and C38 charges through R58 and D3 until Q10 turns on. This occurs when the emitter of Q10 exceeds its base voltage and causes current to flow into the base of Q11, turning that device on. When Q10 and Q11 conduct, C37 and C38 are discharged to nearly 0. Q10 and Q11 then shut off and the cycle repeats. The setting of the vertical hold control determines the repetition rate of the charge and discharge of C37 and C38. The waveform generated is a positive-going ramp or sawtooth with a fast retrace to 0. D3 provides a small incremental voltage above ground to overcome the forward base-emitter drop of the two following stages. Q12 is an emitter follower used to transform the high impedance drive sawtooth to a low impedance drive for Q13.

T3 matches the collector of Q13 to the vertical yoke. When Q13 is cut off during Vertical Retrace, a high voltage pulse is developed across the primary of T3. To limit this pulse to a safe value a varistor, R81, is connected across

the primary. R66 and C41 provide damping to shape the collector pulse so it may be used for retrace blanking. Since the primary impedance of T3 decreases with current, the degree to which the primary shunts the reflected load impedance varies with collector current. This would result in severe vertical non-linearity unless some compensation is employed.

Resistors R60 and R59 couple the emitter voltage of Q13 to the junction of C37 and C38. Since this path is resistive, the waveform coupled back will be integrated into a parabola by C38. This results in a pre-distortion of the drive sawtooth as shown in Figure 12-55. This is done to compensate for the non-linear charging of C37 and C38 and the changing impedance of the primary of T3. An additional feedback path through R62 and C40 serves to optimize the drive waveshape for best linearity.

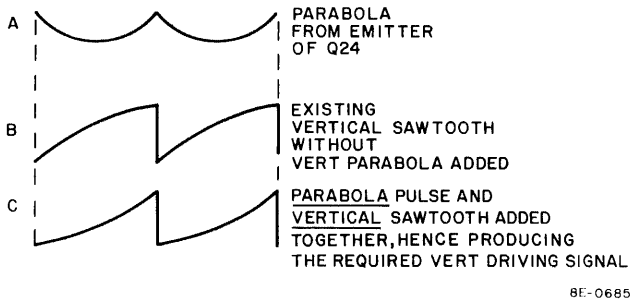


Figure 12-55 CRT Vertical Oscillator Waveforms

12.5.2.8 Retrace Blanking – Both Vertical and Horizontal Retrace blanking are provided by positive pulses applied to the CRT cathode. The collector pulse from the Horizontal Output transistor is placed across R23 through R46. The vertical collector voltage is differentiated by C30 to remove the sawtooth portion of the waveform. The remaining pulse appears across R23. The mixed vertical and horizontal pulses on R23 are coupled to the CRT cathode by C10.

12.5.2.9 Power Supply – The regulated power supply uses a series pass circuit. Q16 is the series pass transistor, Q14 is the driver, and Q15 is the reference amplifier. The output voltage of the regulator appears at the emitter of Q16 and is fed into a voltage divider consisting of R71, R74, and R73. The voltage appearing on the arm of potentiometer R74 is used as an error input to Q15. R74 is thus used as the output voltage adjustment.

Zener diode D13 establishes a reference voltage at the emitter of Q15. R72 establishes the minimum bias current for D13 to ensure proper Zener operation.

The voltage at the arm of R74 is compared with the reference voltage at D13 by Q15. If the voltage at the base of Q15 increases due to an increase in input voltage to the power supply for example, Q15 conducts more current. This decreases the current available to the base of Q14, so Q14 and Q16 conduct less current, resulting in less voltage at the emitter of Q16. In this manner, input voltage changes are reduced by the overall gain of the regulator, which is quite high. R79 reduces the power dissipation in Q16 by carrying some of the supply current. This does not impair regulation over the operating range of the power supply due to the large amount of gain available.

SECTION 5 MAINTENANCE

12.6 INTRODUCTION

VT8-E maintenance theory is directed to the module replacement level. The maintenance effort is divided into two basic categories: preventive maintenance and corrective maintenance.

Preventive maintenance consists of routine periodic checks such as visual inspections, standard maintenance procedures that involve cleaning and lubricating, and diagnostic tests that expose possible weakening conditions to allow corrective action to be taken, eliminating the causative factor(s) of possible failures.

Corrective maintenance consists of isolating the fault or problem and making necessary adjustments and/or replacements when a malfunction occurs. This involves the use of diagnostic routines prepared on paper tape and designed to test the functional units of the system. The procedures and techniques of periodic checking aid in fault isolation. Power requirements can be checked through the checkout procedures for power requirements contained in Paragraph 12.2.2.

12.6.1 Equipment Required

Maintenance procedures for the VT8-E Video Display and Control require the standard equipment (or equivalent), standard hand tools, and test probes listed in Table 12-10.

Table 12-10
Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 620
Oscilloscope	Tektronix	Type 453
X10 Probe	Tektronix	P6010
Recessed Tip	Tektronix	013-0090-00
Diagnostic Self-Test Routines		

12.6.2 Diagnostic Programming

The diagnostic routines, supplied as paper tapes, are used to test the various VT8-E functions and modules. A complete description with instructions is provided with each tape.

12.6.3 Preventive Maintenance

Preventive maintenance consists of tasks performed periodically; its major purpose is to prevent failures caused by minor damage or progressive deterioration due to aging. A preventive maintenance log book should be established and necessary entries made according to a regular schedule. This data, compiled over an extended period of time, can be very useful in anticipating possible component failures resulting in module replacement on a projected module or component reliability basis.

Preventive maintenance tasks consist of mechanical and electrical checks. All maintenance schedules should be established according to the environmental conditions at the particular installation site. Mechanical checks should be performed as often as required to allow the fan and air filter to function efficiently. All other preventive maintenance tasks should be performed on a regular schedule determined by reliability requirements. A recommended schedule is every 600 operating hours or every four months, whichever occurs first.

12.6.3.1 Mechanical Checks – Use the following procedure to perform a mechanical check on the equipment.

Step	Procedure
1	Unplug the VT8-E main power and remove the cover.
2	Clean the exterior with a clean cloth moistened in a mild detergent. Only a very soft cloth should be used to avoid scratching the protective screen used on the face of the CRT.
3	Clean the interior using a vacuum cleaner and ensure that the cabinet air exhaust vents are thoroughly clean and unobstructed to promote adequate cooling. Should the vents become obstructed, premature component failure may occur due to an increase in the VT8-E internal temperature.
4	Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.
5	Inspect the following for mechancial security: jacks, connectors, keyboard, etc. Tighten or replace as required.

12.6.4 Troubleshooting

12.6.4.1 System Troubleshooting – Begin troubleshooting by repeating the operation in which the malfunction was initially observed, using the same program or function. Thoroughly check the program for proper settings and determine if the fault is definitely located in the VT8-E.

If the fault is isolated to the VT8-E, but cannot be immediately localized to a specific logic function, an effort should be made to further isolate the fault to one of the VT8-E modules, e.g., keyboard, M8335 module, CRT module, etc. Some helpful aids during functional analysis are the VT8-E engineering drawings, circuit schematics, timing diagrams, and the applicable VT8-E diagnostic programs.

12.6.4.2 Module Troubleshooting – Once the fault has been isolated to a specific module, carefully remove the suspected module. Inspect the receptacle for wear or damaged contacts. When the operability of the module is verified, repair the faulty module or replace it with a module known to be operating properly and run the last diagnostic program. If the system performs properly, return the system to an operating status and log an entry to record all pertinent data concerning the fault or malfunction. When the individual defective part(s) within a module is located and repaired or replaced, the module should be verified by a validation test.

12.6.4.3 VT8-E Assembly/Disassembly – The following procedures are provided for removal, replacement, and installation of the various VT8-E modular components. Special and cautionary notes contained within the procedures afford special attention and should be adhered to. Only procedures for the removal of the VT8-E modular components are provided; for installation, the procedures should be performed in their reverse order.

12.6.4.3.1 VT8-E Module Boards – The M8335, M8336, or M8337 module boards should be inserted straight into the OMNIBUS, never at an angle. When inserting a module board be certain it is fully seated in the OMNIBUS.

12.6.4.3.2 Cover Removal – The VT8-E cover is secured with four Phillips-head screws. Screw locations are center-front, center-rear, and midway on the two sides. The screws are inserted up through the lower casting and into four cover-retaining brackets. To remove the cover, remove the four retaining screws and lift the cover off.

NOTE

When the cover is removed, the 3-position interlock switch on the left-hand side (viewing from the front) will go from the fully depressed position (ON) to the middle position (OFF) and must be pulled up to the third position (ON).

To install the cover, place the cover back on the lower casing, insert and tighten the four Phillips-head retaining screws. The interlock switch should be in the fully depressed (ON) position.

12.6.4.3.3 VT8-E Keyboards Removal – The VT8-E contains two keyboards, a large teletypewriter-type keyboard, and a small 8-key cursor control keyboard. The small keyboard is secured by four Phillips-head screws that are inserted down through the four corners of the mounting board into the mounting bracket. The large keyboard is secured by four Phillips-head screws that are inserted down through the keyboard mounting bracket. These four screws should not be confused with the smaller and brighter Phillips-head screws that secure the keyboard to the keyboard logic board. The smaller, brighter screws should not be removed.

Use the following procedure to remove the small keyboard:

Step	Procedure
1	Disconnect the ribbon cable from the small keyboard input connector.
2	Remove the four Phillips-head retaining screws from the four corners of the small keyboard mounting board.
3	Slide the keyboard to the left and lift it out.

Use the following procedure to remove the large keyboard:

Step	Procedure
1	Disconnect the 44-pin Berg connector from the keyboard output connector.
2	Remove the four, larger keyboard Phillips-head retaining screws from the keyboard mounting bracket and remove the keyboard

12.6.4.3.4 CRT Removal – The CRT is secured to the VT8-E lower casting with four Phillips-head screws that are inserted through the bottom of the VT8-E and into the bottom four corners of the CRT chassis. Use the following procedure to remove the CRT:

CAUTION

Protective goggles and heavy gloves should be worn when removing and/or carrying the CRT. Never grasp the CRT by the neck, nor chip or scratch any part of the tube.

Step	Procedure
1	Press the interlock switch down to ensure main power is off.
2	Viewing the VT8-E from the front, locate (15-pin and 12-pin) Mate-N-Lok connectors P1 and P2 on the lower right-hand side of the CRT chassis and disconnect both connectors.
3	Locate and remove the four Phillips-head retaining screws on the bottom of the VT8-E, used to secure the CRT chassis to the lower casting. **NOTE** **Upon removal, the CRT should be placed face-down on a soft clean cloth or pad. Under no circumstances should the CRT be grasped by the neck**
4	Lift the CRT out of the lower casing.

APPENDIX A
ROM PATTERN TABLES

Table A-1
ROM Pattern Table
(EVEN ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
0	000	0000	24	030	0000
1	001	0111	25	031	1111
2	002	1000	26	032	1000
3	003	1011	27	033	1000
4	004	1010	28	034	1111
5	005	1011	29	035	1000
6	006	1000	30	036	1000
7	007	0111	31	037	1000
8	010	0000	32	040	0000
9	011	1111	33	041	1000
10	012	1000	34	042	1000
11	013	1000	35	043	1000
12	014	1111	36	044	1111
13	015	1000	37	045	1000
14	016	1000	38	046	1000
15	017	1111	39	047	1000
16	020	0000	40	050	0000
17	021	1110	41	051	0011
18	022	1001	42	052	0001
19	023	1000	43	053	0001
20	024	1000	44	054	0001
21	025	1000	45	055	1001
22	026	1001	46	056	1001
23	027	1110	47	057	0110

Table A-1 (Cont)
ROM Pattern Table
(EVEN ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
48	060	0000	84	124	0010
49	061	1000	85	125	0010
50	062	1000	86	126	0010
51	063	1000	87	127	0010
52	064	1000	88	130	0000
53	065	1000	89	131	1000
54	066	1000	90	132	1000
55	067	1111	91	133	1000
56	070	0000	92	134	1000
57	071	1000	93	135	1000
58	072	1000	94	136	0101
59	073	1100	95	137	0010
60	074	1010	96	140	0000
61	075	1001	97	141	1000
62	076	1000	98	142	1000
63	077	1000	99	143	0101
64	100	0000	100	144	0010
65	101	1111	101	145	0101
66	102	1000	102	146	1000
67	103	1000	103	147	1000
68	104	1111	104	150	0000
69	105	1000	105	151	1111
70	106	1000	106	152	0000
71	107	1000	107	153	0001
72	110	0000	108	154	0010
73	111	1111	109	155	0100
74	112	1000	110	156	1000
75	113	1000	111	157	1111
76	114	1111	112	160	0000
77	115	1001	113	161	0000
78	116	1000	114	162	1000
79	117	1000	115	163	0100
80	120	0000	116	164	0010
81	121	1111	117	165	0001
82	122	0010	118	166	0000
83	123	0010	119	167	0000

Table A-1 (Cont)
ROM Pattern Table
(EVEN ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
120	170	0000	156	234	0100
121	171	0111	157	235	1010
122	172	1000	158	236	1001
123	173	0000	159	237	0110
124	174	0000	160	240	0000
125	175	0000	161	241	0001
126	176	0000	162	242	0010
127	177	0000	163	243	0100
128	200	0000	164	244	0100
129	201	0000	165	245	0100
130	202	0000	166	246	0010
131	203	0000	167	247	0001
132	204	0000	168	250	0000
133	205	0000	169	251	0010
134	206	0000	170	252	1010
135	207	0000	171	253	0111
136	210	0000	172	254	1101
137	211	0101	173	255	0111
138	212	0101	174	256	1010
139	213	0101	175	257	0010
140	214	0000	176	260	0000
141	215	0000	177	261	0000
142	216	0000	178	262	0000
143	217	0000	179	263	0000
144	220	0000	180	264	0000
145	221	0010	181	265	0010
146	222	0111	182	266	0010
147	223	1000	183	267	0100
148	224	0111	184	270	0000
149	225	0000	185	271	0000
150	226	1111	186	272	0000
151	227	0010	187	273	0000
152	230	0000	188	274	0000
153	231	0100	189	275	0000
154	232	1010	190	276	0000
155	233	1010	191	277	0010

Table A-1 (Cont)
ROM Pattern Table
(EVEN ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
192	300	0000	224	340	0000
193	301	0111	225	341	0111
194	302	1000	226	342	1000
195	303	1001	227	343	1000
196	304	1010	228	344	0111
197	305	1100	229	345	1000
198	306	1000	230	346	1000
199	307	0111	231	347	0111
200	310	0000	232	350	0000
201	311	0111	233	351	0000
202	312	1000	234	352	0000
203	313	0000	235	353	0010
204	314	0011	236	354	0000
205	315	0100	237	355	0010
206	316	1000	238	356	0000
207	317	1111	239	357	0000
208	320	0000	240	360	0000
209	321	0001	241	361	0001
210	322	0011	242	362	0010
211	323	0101	243	363	0100
212	324	1001	244	364	1000
213	325	1111	245	365	0100
214	326	0001	246	366	0010
215	327	0001	247	367	0001
216	330	0000	248	370	0000
217	331	0011	249	371	0100
218	332	0100	250	372	0010
219	333	1000	251	373	0001
220	334	1111	252	374	0000
221	335	1000	253	375	0001
222	336	1000	254	376	0010
223	337	0111	255	377	0100

Table A-2
ROM Pattern Table
(ODD ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
0	000	0000	36	044	0010
1	001	0010	37	045	0010
2	002	0101	38	046	0010
3	003	1000	39	047	0111
4	004	1000	40	050	0000
5	005	1111	41	051	1000
6	006	1000	42	052	1001
7	007	1000	43	053	1010
8	010	0000	44	054	1100
9	011	0111	45	055	1010
10	012	1000	46	056	1001
11	013	1000	47	057	1000
12	014	1000	48	060	0000
13	015	1000	49	061	1000
14	016	1000	50	062	1101
15	017	0111	51	063	1010
16	020	0000	52	064	1010
17	021	1111	53	065	1000
18	022	1000	54	066	1000
19	023	1000	55	067	1000
20	024	1111	56	070	0000
21	025	1000	57	071	0111
22	026	1000	58	072	1000
23	027	1111	59	073	1000
24	030	0000	60	074	1000
25	031	0111	61	075	1000
26	032	1000	62	076	1000
27	033	1000	63	077	0111
28	034	1000	64	100	0000
29	035	1011	65	101	0111
30	036	1000	66	102	1000
31	037	0111	67	103	1000
32	040	0000	68	104	1000
33	041	0111	69	105	1010
34	042	0010	70	106	1001
35	043	0010	71	107	0110

Table A-2 (Cont)
ROM Pattern Table
(ODD ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
72	110	0000	108	154	1100
73	111	0111	109	155	1100
74	112	1000	110	156	1100
75	113	1000	111	157	1111
76	114	0111	112	160	0000
77	115	0000	113	161	1111
78	116	1000	114	162	0001
79	117	0111	115	163	0001
80	120	0000	116	164	0001
81	121	1000	117	165	0001
82	122	1000	118	166	0001
83	123	1000	119	167	1111
84	124	1000	120	170	0000
85	125	1000	121	171	0000
86	126	1000	122	172	0000
87	127	0111	123	173	0000
88	130	0000	124	174	0000
89	131	1000	125	175	0000
90	132	1000	126	176	0000
91	133	1000	127	177	1111
92	134	1010	128	200	0000
93	135	1010	129	201	0010
94	136	1101	130	202	0010
95	137	1000	131	203	0010
96	140	0000	132	204	0010
97	141	1000	133	205	0010
98	142	1000	134	206	0000
99	143	0101	135	207	0010
100	144	0010	136	210	0000
101	145	0010	137	211	0101
102	146	0010	138	212	0101
103	147	0010	139	213	1111
104	150	0000	140	214	0101
105	151	1111	141	215	1111
106	152	1100	142	216	0101
107	153	1100	143	217	0101

Table A-2 (Cont)
ROM Pattern Table
(ODD ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
144	220	0000	180	264	1111
145	221	1100	181	265	0000
146	222	1100	182	266	0000
147	223	0001	183	267	0000
148	224	0010	184	270	0000
149	225	0100	185	271	0000
150	226	1001	186	272	0000
151	227	0001	187	273	0001
152	230	0000	188	274	0010
153	231	0010	189	275	0100
154	232	0010	190	276	1000
155	233	0010	191	277	0000
156	234	0000	192	300	0000
157	235	0000	193	301	0010
158	236	0000	194	302	0110
159	237	0000	195	303	0010
160	240	0000	196	304	0010
161	241	0100	197	305	0010
162	242	0010	198	306	0010
163	243	0001	199	307	0111
164	244	0001	200	310	0000
165	245	0001	201	311	1111
166	246	0010	202	312	0000
167	247	0100	203	313	0001
168	250	0000	204	314	0011
169	251	0000	205	315	0000
170	252	0010	206	316	1000
171	253	0010	207	317	0111
172	254	1111	208	320	0000
173	255	0010	209	321	1111
174	256	0010	210	322	1000
175	257	0000	211	323	1111
176	260	0000	212	324	0000
177	261	0000	213	325	0000
178	262	0000	214	326	1000
179	263	0000	215	327	0111

Table A-2 (Cont)
ROM Pattern Table
(ODD ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
216	330	0000	236	354	0000
217	331	1111	237	355	0010
218	332	0000	238	356	0010
219	333	0001	239	357	0100
220	334	0010	240	360	0000
221	335	0100	241	361	0000
222	336	0100	242	362	0000
223	337	0100	243	363	1111
224	340	0000	244	364	0000
225	341	0111	245	365	1111
226	342	1000	246	366	0000
227	343	1000	247	367	0000
228	344	0111	248	370	0000
229	345	0000	249	371	0111
230	346	0001	250	372	1000
231	347	1110	251	373	0001
232	350	0000	252	374	0010
233	351	0000	253	375	0010
234	352	0000	254	376	0000
235	353	0010	255	377	0010

Table A-3
ROM Pattern Table
(XTRA ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
0	000	0000	36	044	0010
1	001	0000	37	045	0010
2	002	0010	38	046	0010
3	003	0011	39	047	0010
4	004	0011	40	050	0000
5	005	0011	41	051	0011
6	006	0001	42	052	0000
7	007	0011	43	053	0000
8	010	0000	44	054	0000
9	011	0000	45	055	0000
10	012	0011	46	056	0000
11	013	0010	47	057	0001
12	014	0000	48	060	0000
13	015	0010	49	061	0001
14	016	0011	50	062	0001
15	017	0000	51	063	0001
16	020	0000	52	064	0001
17	021	0001	53	065	0001
18	022	0000	54	066	0001
19	023	0010	55	067	0011
20	024	0010	56	070	0000
21	025	0010	57	071	0010
22	026	0000	58	072	0011
23	027	0001	59	073	0011
24	030	0000	60	074	0011
25	031	0010	61	075	0011
26	032	0001	62	076	0011
27	033	0000	63	077	0010
28	034	0000	64	100	0000
29	035	0001	65	101	0000
30	036	0001	66	102	0011
31	037	0000	67	103	0011
32	040	0000	68	104	0001
33	041	0010	69	105	0001
34	042	0010	70	106	0000
35	043	0010	71	107	0001

Table A-3 (Cont)
ROM Pattern Table
(XTRA ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
72	110	0000	108	154	0000
73	111	0000	109	155	0000
74	112	0011	110	156	0000
75	113	0010	111	157	0011
76	114	0000	112	160	0000
77	115	0001	113	161	0001
78	116	0011	114	162	0001
79	117	0010	115	163	0001
80	120	0000	116	164	0001
81	121	0011	117	165	0001
82	122	0001	118	166	0011
83	123	0001	119	167	0001
84	124	0001	120	170	0000
85	125	0001	121	171	0000
86	126	0001	122	172	0010
87	127	0000	123	173	0000
88	130	0000	124	174	0000
89	131	0011	125	175	0000
90	132	0011	126	176	0000
91	133	0011	127	177	0001
92	134	0011	128	200	0000
93	135	0011	129	201	0000
94	136	0001	130	202	0000
95	137	0001	131	203	0000
96	140	0000	132	204	0000
97	141	0011	133	205	0000
98	142	0011	134	206	0000
99	143	0000	135	207	0000
100	144	0000	136	210	0000
101	145	0000	137	211	0000
102	146	0010	138	212	0000
103	147	0010	139	213	0001
104	150	0000	140	214	0000
105	151	0011	141	215	0001
106	152	0010	142	216	0000
107	153	0000	143	217	0000

Table A-3 (Cont)
ROM Pattern Table
(XTRA ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
180	264	0001	144	220	0000
181	265	0000	145	221	0000
182	266	0000	146	222	0011
183	267	0000	147	223	0000
184	270	0000	148	224	0000
185	271	0000	149	225	0010
186	272	0001	150	226	0001
187	273	0000	151	227	0001
188	274	0000	152	230	0000
189	275	0000	153	231	0000
190	276	0000	154	232	0000
191	277	0000	155	233	0000
192	300	0000	156	234	0000
193	301	0000	157	235	0010
194	302	0010	158	236	0000
195	303	0010	159	237	0010
196	304	0010	160	240	0000
197	305	0010	161	241	0000
198	306	0010	162	242	0000
199	307	0000	163	243	0000
200	310	0000	164	244	0000
201	311	0001	165	245	0000
202	312	0011	166	246	0000
203	313	0010	167	247	0000
204	314	0000	168	250	0000
205	315	0001	169	251	0000
206	316	0001	170	252	0010
207	317	0010	171	253	0000
208	320	0000	172	254	0011
209	321	0001	173	255	0000
210	322	0000	174	256	0010
211	323	0000	175	257	0000
212	324	0001	176	260	0000
213	325	0011	177	261	0000
214	326	0001	178	262	0000
215	327	0000	179	263	0000

Table A-3 (Cont)
ROM Pattern Table
(XTRA ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
216	330	0000	236	354	0000
217	331	0011	237	355	0000
218	332	0001	238	356	0000
219	333	0000	239	357	0000
220	334	0000	240	360	0000
221	335	0010	241	361	0000
222	336	0010	242	362	0000
223	337	0000	243	363	0001
224	340	0000	244	364	0000
225	341	0000	245	365	0001
226	342	0011	246	366	0000
227	343	0011	247	367	0000
228	344	0001	248	370	0000
229	345	0011	249	371	0000
230	346	0010	250	372	0001
231	347	0000	251	373	0000
232	350	0000	252	374	0010
233	351	0000	253	375	0000
234	352	0000	254	376	0000
235	353	0000	255	377	0000

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