Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-8/I User's Guide

CR8/I

Card Reader System

DEC-8I-H2BB-D

PDP-8/I
CR8/I
CARD READER SYSTEM
USER'S GUIDE

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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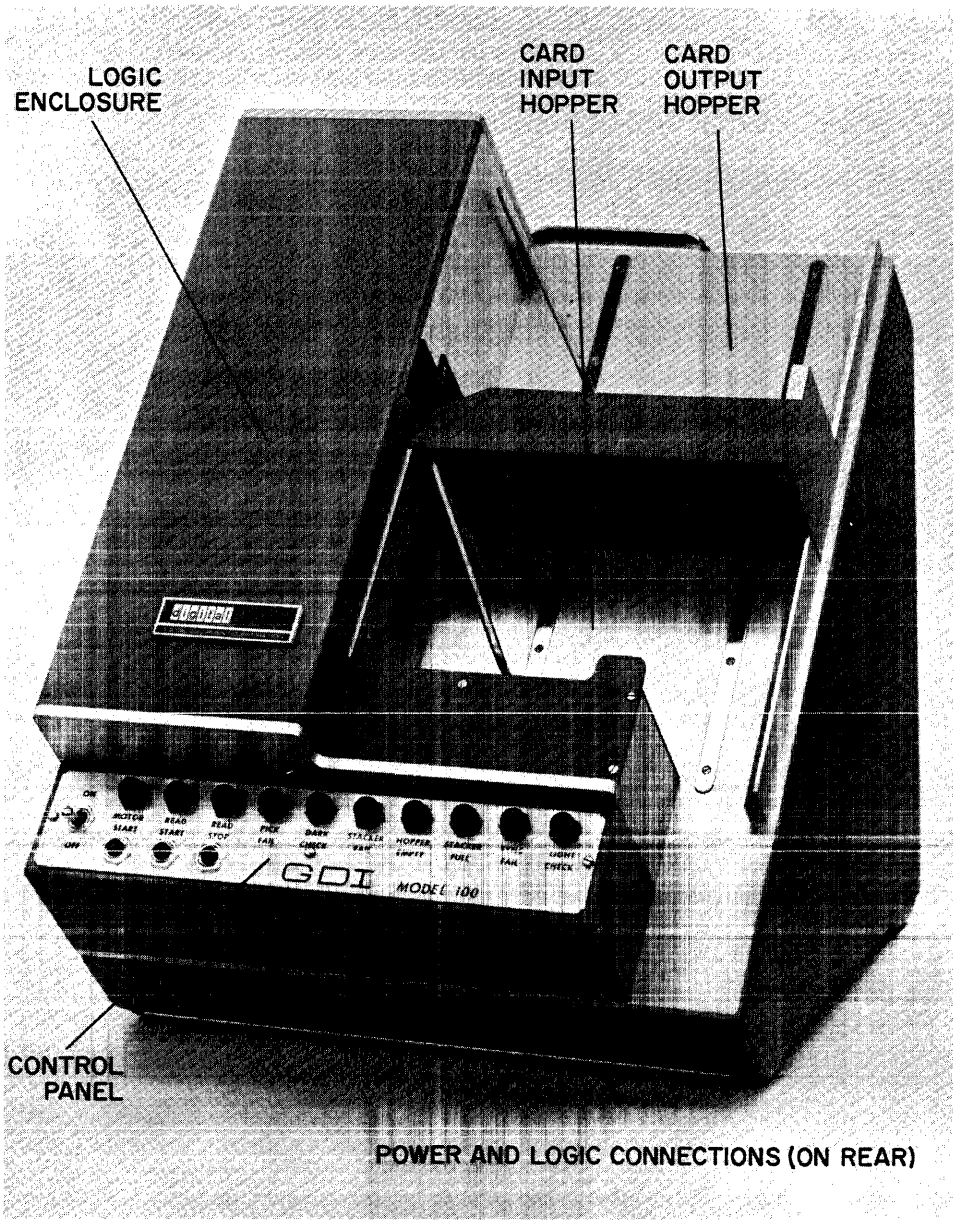
CONTENTS

CONTENTS (Cont)

CARD READER SYSTEM



GDI-100 Card Reader

CHAPTER 1
GENERAL

1.1 GENERAL DESCRIPTION

The DEC CR8/I Card Reader system equips the PDP-8/I computer to accept information from EIA standard data cards. The option is in two parts: the General Design, Inc., (GDI) Model 100 Card Reader, and the DEC CR8/I Control. The control is mounted in the PDP-8/I mainframe and is connected to the GDI-100 by a single cable. The PDP-8/I is prewired to accept this option.

1.1.1 Card Reader

The GDI Model 100 desk-top card reader (frontispiece) consists of a motorized card transport deck, a photoelectric reader, and control and error rejection circuits using IC logic on plug-in boards. Standard data cards are read on program command from the PDP-8/I at rates of up to 200 cards per minute. The card reader is designed to handle even badly mutilated cards without error. The GDI-100 has an internal power supply, and can be tested off-line. The GDI 'Technical Manual, Model 100 Card Reader' gives test and maintenance information.

1.1.2 CR8/I Control

The CR8/I Control logic (Figure 1-1) interconnects the PDP-8/I internal I/O system and the GDI-100. The unit interprets computer IOT instructions to control the card reader, and makes data available through its parallel data register to the computer. The control logic consists of two logic modules (M714 and M716) shown in Figure 1-2.

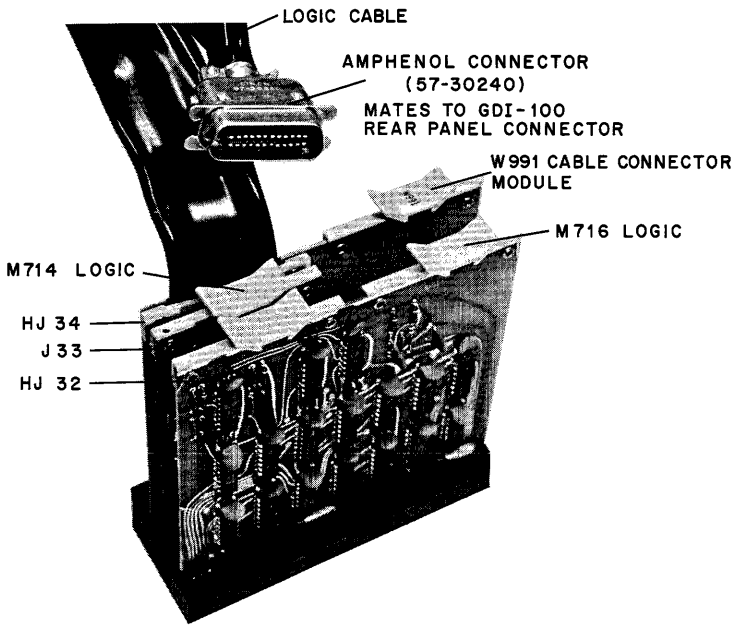
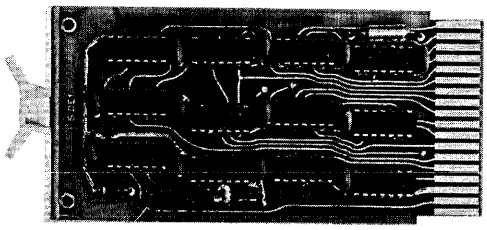
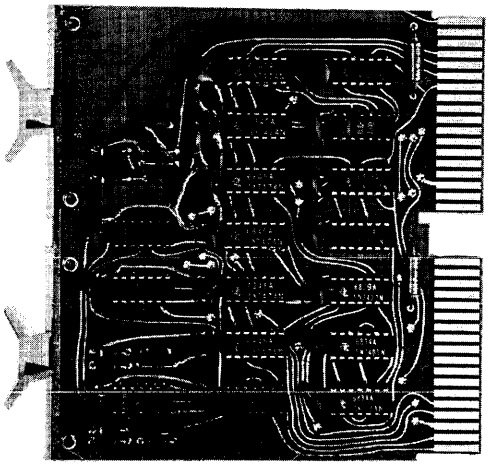


Figure 1-1 CR8/I Control Logic and Cable Assembly



M714 POSITION J33



M716 POSITION HJ32

Figure 1-2 CR8/I Control Logic Modules

1.2 INSTALLATION

The CR8/I Control connects to the GDI-100 by a single cable, as shown in Figure 1-3. This cable terminates in a W991 (double height) module installed in the PDP-8/I. A 24-pin Amphenol connector (57-30240) at the other end attaches to a mating receptacle on the GDI rear panel. The cable is 8 ft long, allowing the GDI to be placed about 5 ft from the computer.

Here is the installation procedure:

a. Unpack the Card Reader option and place the GDI-100 on a sturdy table;

b. Connect the GDI-100 to ac power and test it off-line according to the procedure in Section 4.1;

c. With computer and GDI power off, install the two control modules in their sockets within the computer. The M714 module is in position J33 of the PDP-8/I mainframe, the M716 in position H,J32. Connect the cable from the computer (W991, position H,J34) to the GDI-100;

d. Restore GDI and computer power. The card reader system is now ready for the on-line tests described in Section 4.2.

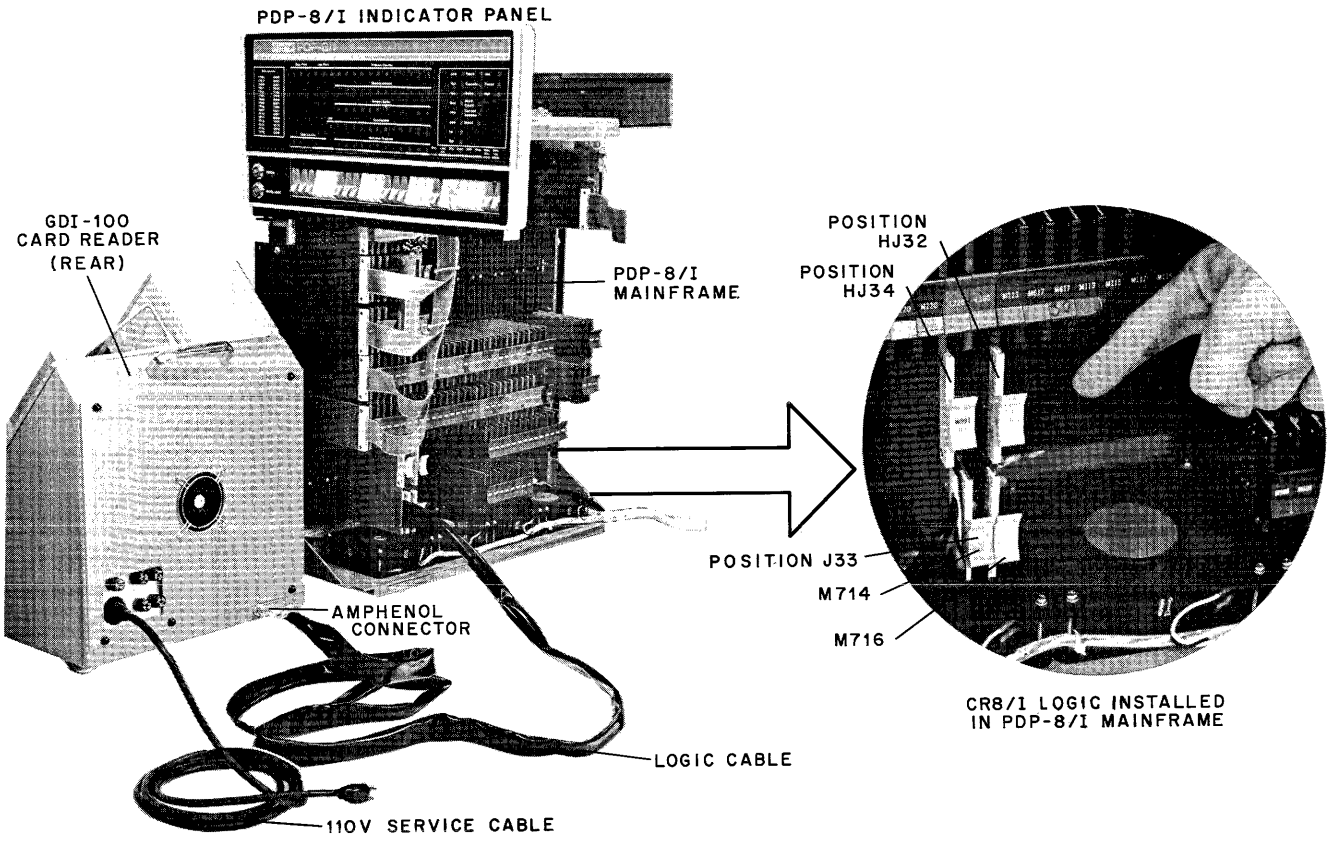


Figure 1-3 CR8/I System Installation

1.3 PHYSICAL AND ELECTRICAL SPECIFICATIONS

GDI-100 Card Reader

Size (h x w x d)	18 x 14 x 18 in.
Weight	47 lb
Temperature Range	15 to 45° C (50 to 105° F)
Power Required	117 ± 10 Vac 60 Hz 1ϕ 300W

Special purchase options are available for 220 Vac or 50 Hz, or both. A 50 Hz conversion kit is available for later changes.

CHAPTER 2
OPERATION PRINCIPLES

2.1 CONTROLS AND INDICATORS

The GDI-100 control panel is shown in Figure 2-1. These controls are discussed in the 'Model 100 Card Reader Technical Manual', Section III. All errors in the card-read operation are sensed and rejected in the GDI-100, and are indicated on this panel. Sections 3.4 and 3.5 of the GDI-100 Technical Manual explain these controls and indicators.

Figure 2-1 GDI-100 Control Panel

2.2 LOGIC SIGNALS

2.2.1 Signal Levels

GDI-100: The card reader uses positive DTμL 930 series integrated circuits. Its logic levels are:

Logic 0 (low) = 0.0 to 0.5V (ground)
Logic 1 (high) = +5.0 ± 0.5V

CR8/I: The control uses standard DEC M-Series module logic levels, compatable with the PDP-8/I computer:

Logic 0 (low) = 0.0 to 0.4V (ground)
Logic 1 (high) = +3.0 ± 0.6V

No level conversion is used, since the GDI-100 and the CR8/I have compatible logic.

2.2.2 Signals

The signals on the cable between the GDI-100 and the CR8/I are:

READ Command	(from CR8/I)
Reader READY	(to CR8/I)
Index Markers (IM)	
Card-In-Reader (CIR)	
DATA (12 Lines)	

These signals appear in the control as shown in the representative logic of Figure 2-2. System timing is shown in Figure 2-3.

READ - The CR8/I Control issues a READ command to the GDI-100 when requested by the PDP-8/I program. READ begins the card-read operation by causing the GDI-100 to pick a card from its input hopper and send it through the read station.

READER READY - When READER READY is true (present), the card reader is ready to read a card. The absence of this signal indicates that the GDI-100 has detected an error in its own operation or in the data card being read. READY false (not present) clears the READ flip-flop. The seven internal GDI trouble signals are indicated on its control panel (Figure 2-1).

INDEX MARKER (IM) - One Index Marker (IM) is generated for each card data column as it is being read. IMs are synchronized with card motion by a serrated sync wheel connected to the GDI motor drive. The GDI uses these pulses to gate each data output from the read station onto its data output lines. Each IM also goes to the CR8/I Control, clearing the data buffer. The same IM delayed (IMD) gates new data into the data buffer 1 μs later, and also sets the DATA READY flip-flop to notify the computer that data is ready for transfer.

CARD-IN-READER (CIR) - This line goes high to indicate a card and clear the READ flip-flop when the leading edge of the card enters the read station, and returns to low when the trailing edge of the card leaves the station. As the CIR goes low, it also sets the CARD DONE flip-flop in the control to notify the program that another card may be read.

DATA - The standard Hollerith data format for EIA standard cards is shown in Table 2-1. A punched hole is read as a data '1'; no hole is a data '0'. Each of the 80 card data columns is checked by a photocell as the card passes the read station. If a hole has been punched in a position, light from an exciter lamp causes the photocell to transmit a data '1'. Twelve parallel lines (one for each photocell zone) go to the control. All the data on a single card are read at each computer read request.

2.3 INSTRUCTION SELECTION

2.3.1 Instruction List

The CR8/I receives its instructions directly from the PDP-8/I internal I/O register. The six control instructions are:

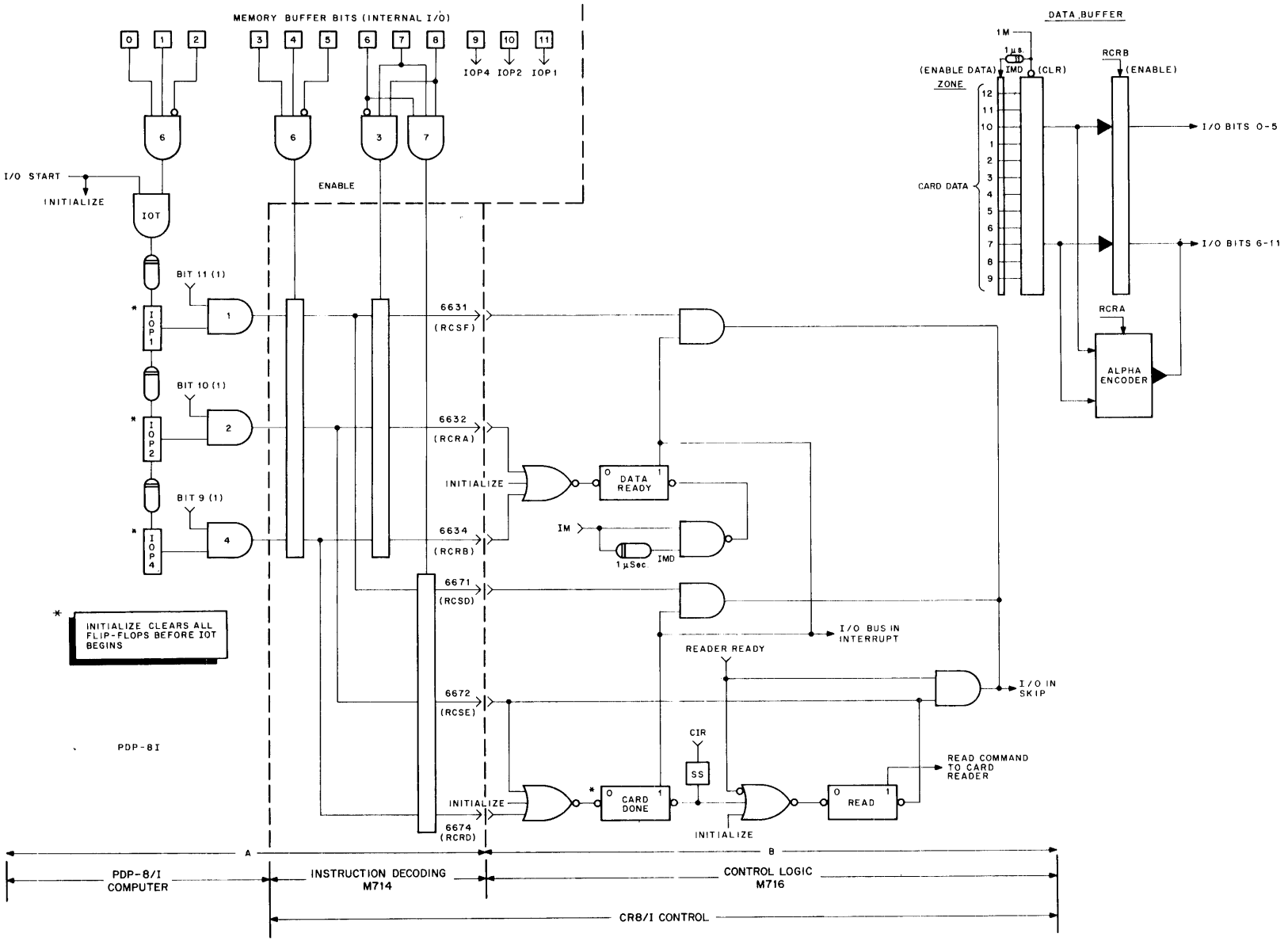


Figure 2-2 CR8/I Representative Control Logic

Mnemonic	Octal Code	Operation	IOP
RCSF	6631	Skip if Data Ready is set	1
RCRA	6632	Read alphanumeric (BCD) data, clear the Data Ready	2
RCRB	6634	Read binary data and clear the Data Ready	4
RCSD	6671	Skip if CARD DONE is set	1
RCSE	6672	Set READ (to advance a card) clear CARD DONE, skip if reader READY (NOT READY if false)	2
RCRD	6674	Clear CARD DONE	4

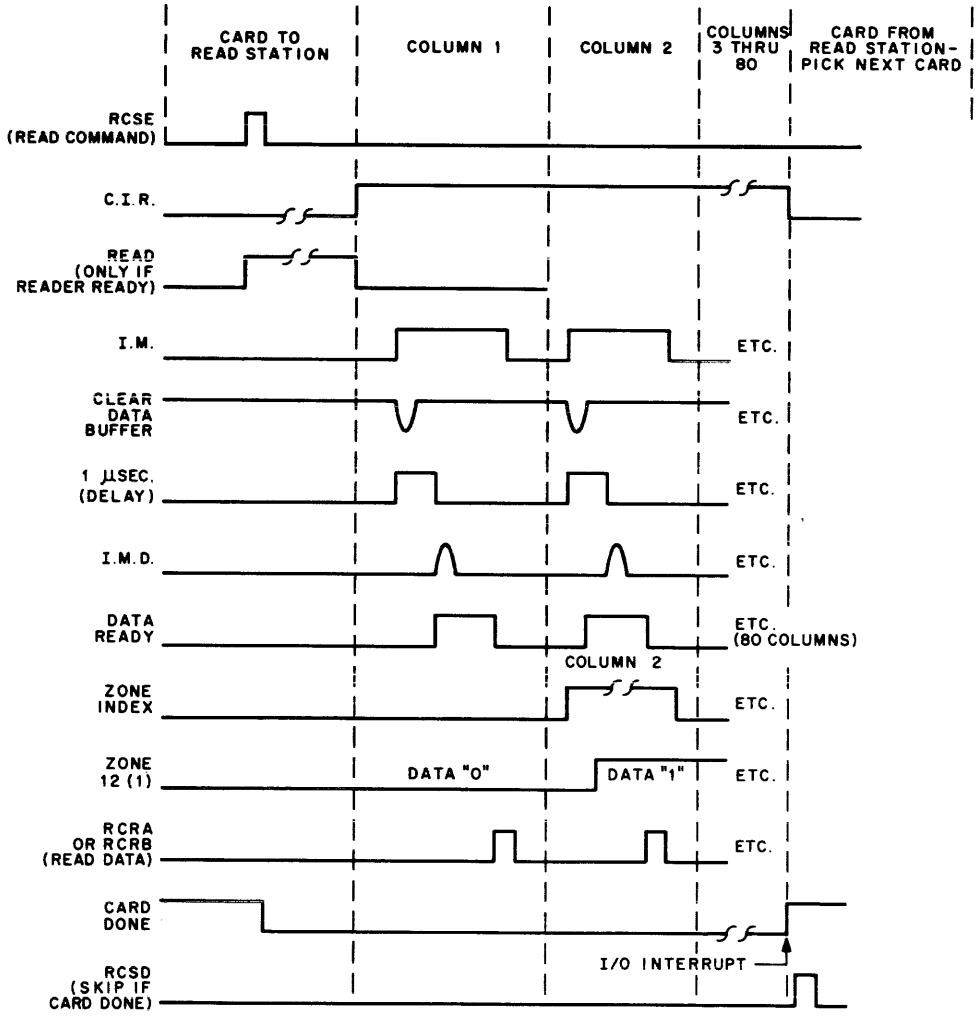


Figure 2-3 CR8/I Card Reader System Timing

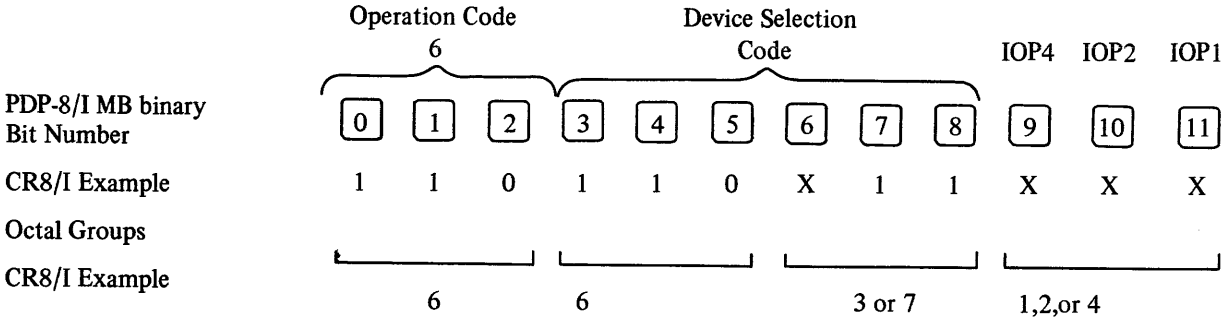
Table 2-1
Card Reader Data Code

Card Code		Internal		Card Code		Internal	
Zone	Num.	Code	Character	Zone	Num.	Code	Character
–	–	00 0000	Blank	11	0	11 0000	Invalid
12	8-2	11 1010	¢	11	1	10 0001	J
12	8-3	11 1011	.	11	2	10 0010	K
12	8-4	11 1100	)	11	3	10 0011	L
12	8-5	11 1101	]	11	4	10 0100	M
12	8-6	11 1110	<	11	5	10 0101	N
12	8-7	11 1111	←	11	6	10 0110	O
12	–	11 0000	+	11	7	10 0111	P
11	8-2	10 1010	!	11	8	10 1000	Q
11	8-3	10 1011	$	11	9	10 1001	R
11	8-4	10 1100	*	0	8-2	01 1010	;
11	8-5	10 1101	[	0	2	01 0010	S
11	8-6	10 1110	>	0	3	01 0011	T
11	8-7	10 1111	&	0	4	01 0100	U
11	–	10 0000	–	0	5	01 0101	V
0	1	01 0001	/	0	6	01 0110	W
0	8-3	01 1011	,	0	7	01 0111	X
0	8-4	01 1100	(	0	8	01 1000	Y
0	8-5	01 1101	"	0	9	01 1001	Z
0	8-6	01 1110	#	–	0	01 0000	0
0	8-7	01 1111	%	–	1	00 0001	1
–	8-2	00 1010	Invalid	–	2	00 0010	2
–	8-3	00 1011	=	–	3	00 0011	3
–	8-4	00 1100	@	–	4	00 0100	4
–	8-5	00 1101	↑	–	5	00 0101	5
–	8-6	00 1110	,	–	6	00 0110	6
–	8-7	00 1111	\	–	7	00 0111	7
12	0	11 0000	Invalid	–	8	00 1000	8
12	1	11 0001	A	–	9	00 1001	9
12	2	11 0010	B				
12	3	11 0011	C				
12	4	11 0100	D				
12	5	11 0101	E				
12	6	11 0110	F				
12	7	11 0111	G				
12	8	11 1000	H				
12	9	11 1001	I				

2.3.2 Octal Code

The four digit octal code is in this format:

IOT Instruction Bit Assignments



(X indicates that this bit may change)

2.3.3 IOP Selection

Figure 2-2 shows how IOP instructions are translated into control signals. The first and last (octal) instruction numbers are decoded by the basic computer. When the first number is a six, IOT operation is begun when the computer START switch is depressed. The signal INITIALIZE is also generated to prepare the logic for its initial operation. The IOT 'chain' generates IOP pulses 1, 2, and 4 in a delayed sequence. The last octal number (MB bits 9, 10, and 11) selects the IOP pulse which is to be allowed to pass through the computer internal I/O bus. Only one IOP pulse is allowed for each instruction. (Thus, the last octal number is always 1, 2, or 4 except for testing.)

The middle two octal numbers are the I/O device select code. The CR8/I 'device' has been assigned 63_8 and 67_8.

CHAPTER 3
PROGRAM OPERATION

3.1 CARD FEED CYCLE

When READY is true, the PDP-8/I may request a card pick by generating an RCSE instruction (6672_8). This command generates a READ command, and also an I/O skip.

In response to the READ command, the card reader picks a card from the input hopper and propels it through the photoelectric read station and into the output hopper. As the trailing edge of each card leaves the read station, the end of signal CIR sets the CARD DONE flag, which generates an I/O interrupt.

When RCSD (6671_8) is generated, CARD DONE will produce an I/O skip to inform the program that another card may be requested.

3.2 READ DATA CYCLE

After a card read cycle begins, one IM is generated in the card reader at each of the 80 data columns on a card, to enable data outputs from the card reader. Each IM also clears the control data buffer and 1 μs later, a delayed IM (IMD) enables data from the card reader to load the buffer.

At the same time the register is loaded, the DATA READY flag is generated. This flag causes an I/O interrupt, and on RCSF (6631_8), causes a skip to a card data reading subroutine.

Card data is read by either an RCRA (6632_8) or RCRB (6634_8). RCRB gates all 12 binary bits in the data register to the computer I/O bus. An alphanumeric encoder also has access to the data register, and on an RCRA, discharges the 12 reassembled bits on the I/O bus as bits 6 through 11, only. (Bits 0 through 5 are discarded.)

3.3 READ LAST CARD CYCLE

When the card reader senses an empty input hopper at the same time as a CIR, READY becomes false. RCSE instructions are now inhibited from generating an I/O skip (and from transmitting any further READ commands to the card reader).

CHAPTER 4
TESTING AND MAINTENANCE

4.1 GDI CARD READER OFF-LINE TESTING

(Refer to Section 3.5 of the GDI Technical Manual for a discussion of reader error detection.)

Before starting test procedure, be sure to turn the PDP-8/I off or disconnect the CR8/I control cable.

a. Adjust the read assembly only if necessary, according to the GDI Technical Manual, Section 6-12, page 6-5.

b. Be sure that the photo exciter lamp is clean and that its illumination is centered on the gate.

c. Place 400 cards with alternating columns of all 0s and all 1s data in the card hopper and press MOTOR START and READ START to cycle the cards.

d. Check proper operation of the picker, read station, stacker, and HOPPER EMPTY and STACKER FULL switches. Also check the pulleys in the rear of the unit for smooth operation. If STACKER FULL indicates with less than 400 cards in the output hopper, adjust the microswitch.

e. Repeat Steps c and d five times.

f. Place 400 cards with all 0s pattern in the reader and check the time needed to cycle all cards; it should be 120 seconds or less.

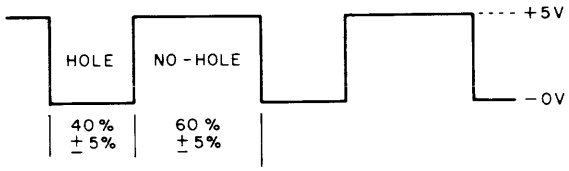
g. Check these pulse widths on reader logic card 4008, in location A-3 (GDI Technical Manual, pages 7-5 and 8-3):

Test Point	60 Hz	50 Hz
TP1	80 ms	66 ms
TP2	180 ms	150 ms
TP3	20 ms	20 ms

Correct waveforms for these signals are shown in the GDI Manual, page 5-30.

h. Check synchronization between TP1 (on reader logic card 4008) and the timing disk pulse. Four TP1 timing pulses are generated for each timing disk pulse. (Refer to GDI Technical Manual, Drawing No. B-4015.)

i. Refer to the GDI Technical Manual schematic 4003. Place the 400 cards with alternating 0s and 1s in the hopper. With the cards cycling, check the waveform of each of the 12 amplified data bits; it should be:



j. To check for PICK FAIL detection - with no cards in the input hopper press the HOPPER EMPTY microswitch down so that the HOPPER EMPTY indicator is not lit; then press MOTOR START and READ START. The reader should make two successive pick attempts and then indicate PICK FAIL.

k. To check for DARK CHECK - DARK CHECK senses whether both leading and trailing columns (0 and 81) of each card indicate no data (are dark). Make a hole anywhere in column 0 of one card, and in column 81 of another. When either card is read, the reader should stop and indicate a DARK CHECK. The "0-card" should stop in the read station and the "81-card" should be stacked in the output hopper.

l. To test STACKER FAIL detection - Place four cards in the input hopper. Hold the stacker gate down and start the card reader. After three cards are cycled, the reader should indicate a STACKER FAIL. One card should remain in the input hopper.

m. To test STACKER FULL - Put 410 cards in the input hopper and depress MOTOR START and READ START. STACKER FULL should indicate when between 405 and 410 cards have been stacked.

n. To test LIGHT CHECK - This signal is a logical OR of two error conditions. The first occurs when any one of the reader photodiodes indicates a dark condition between card passes. This condition is simulated by placing a card in the input hopper, depressing MOTOR START, and inserting a piece of paper between the read lamp and the photodiodes. The reader should stop and indicate a LIGHT CHECK. The second condition occurs when any photodiode indicates a dark condition just after a card should have exited the read station (i.e., at fictitious column '84'). For the second test, make a card which is several columns longer than standard size and try to read it. A LIGHT CHECK should again indicate.

4.2 CR8/I SYSTEM ON-LINE TESTING

The GDI-100 and the CR8/I Control are tested as a functional unit by DEC diagnostic program MAINDEC-08-D20A, which includes two special 80-card test decks, one with binary, the other with alphanumeric data.

4.3 LIFE TEST

Using the Data Test section of MAINDEC-08-D20A, the card reader option should perform 50 consecutive passes of either diagnostic card deck, with no errors.

4.4 DEC ACCEPTANCE TEST

Each card reader system must pass this acceptance test:

a. Card Reader Off-Line Check, steps f, g, h, and i;

b. On-Line Check which consists of Life Test in Section 4.3.

4.5 CUSTOMER ACCEPTANCE TEST

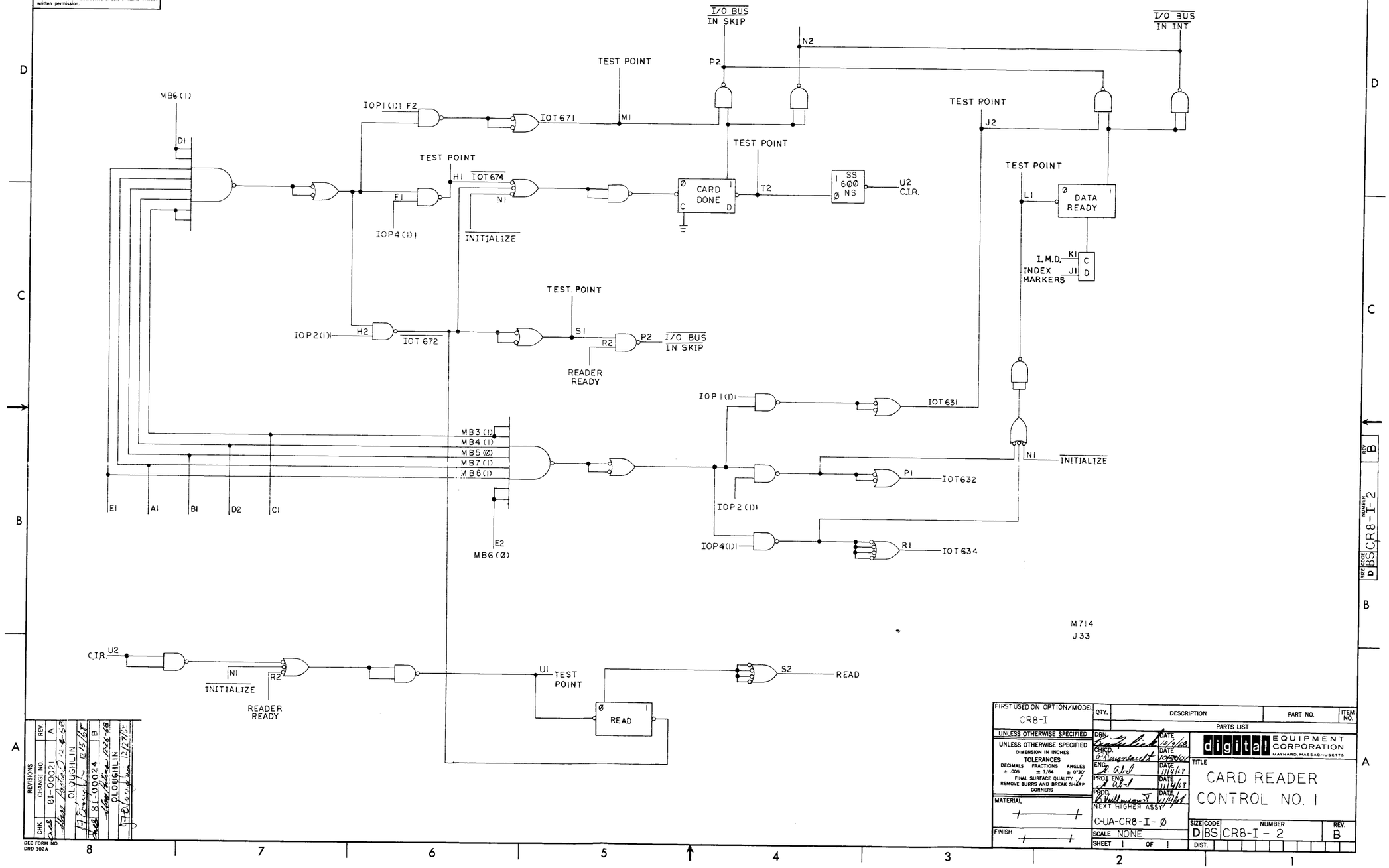
The card reader system must pass the MAINDEC-08-D20A diagnostic test program.

4.6 CR8/I SYSTEM ON-LINE TROUBLESHOOTING

Before you troubleshoot the card reader system, be sure the GDI-100 is operating properly off-line. Then reconnect the CR8/I control cable to the GDI when system power is off. Refer to the system timing in Figure 2-3.

4.6.1 Test Equipment Required

400 cards punched with alternate columns of all 0 and all 1 data;
An oscilloscope with two probes and one sync cable;
MAINDEC-08-D20A diagnostic program for the CR8/I Card Reader System;
Cable block and circuit schematics (Figures 4-1, 4-2, 4-3, 4-4 and 4-5)

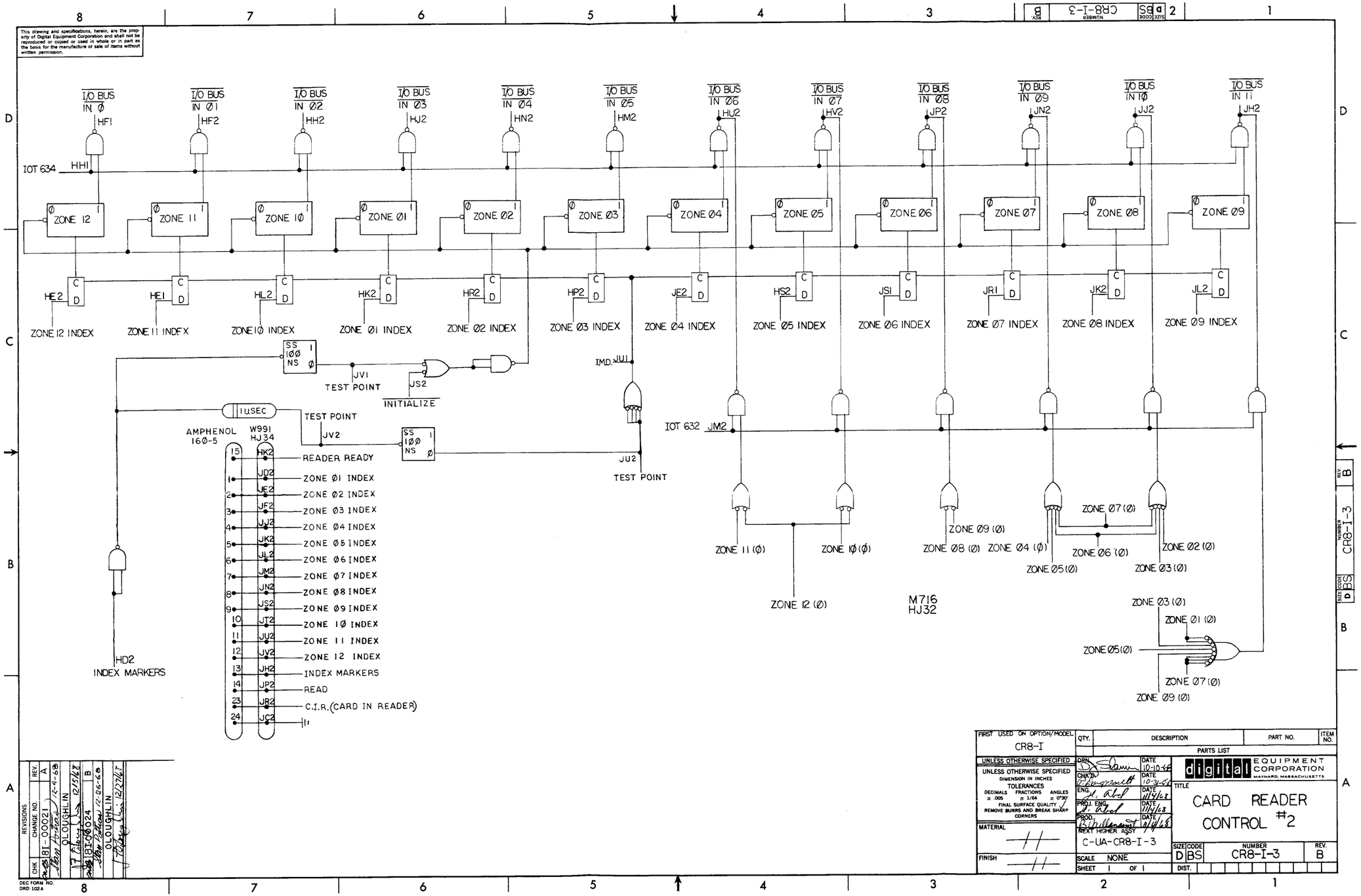


REVISIONS			
CHK	CHANGE NO.	REV.	
Dick	81-00021	A	
Alan Peters	12-8-68		
OLYMPHLIN			
H Crosby	12/5/68		
Fred	81-00024	B	
Alan Peters	12-26-68		
OLYMPHLIN	12/27/68		
Fred Wilson			

DEC FORM NO. DRD 102A

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
CR8-I		PARTS LIST		
UNLESS OTHERWISE SPECIFIED	DRN. Fred Lek	DATE 10/1/68	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	CHK'D. C.J.	DATE 10/30/68	TITLE CARD READER CONTROL NO. 1	
	ENG. M. Abel	DATE 11/4/68		
	PROJ. ENG. M. Abel	DATE 11/4/68		
MATERIAL	PROD. R. Vallancourt	DATE 11/14/68		
	NEXT HIGHER ASSY C-UA-CR8-I-Ø		SIZE D CODE BS NUMBER CR8-I-2 REV. B	
FINISH	SCALE NONE			
	SHEET 1 OF 1		DIST.	

Figure 4-1 CR8/I Logic Schematic (M714)



REVISIONS	REV.	CHANGE NO.	CHK.	
	A	81-00021		12-4-68
		OLOUGHLIN		12/5/68
	B	83-00024		12-26-68
		OLOUGHLIN		12/27/68

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
CR8-I		PARTS LIST		

UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. — DATE 10-10-68
CHK'D — DATE 10-31-68
ENG. — DATE 11/4/68
PROJ. ENG. — DATE 11/4/68
PROD. — DATE 12/4/68
NEXT HIGHER ASSY C-UA-CR8-I-3
SCALE NONE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
CARD READER CONTROL #2

SIZE	CODE	NUMBER	REV.
D	BS	CR8-I-3	B

DIST.

DEC FORM NO. DRD 102A

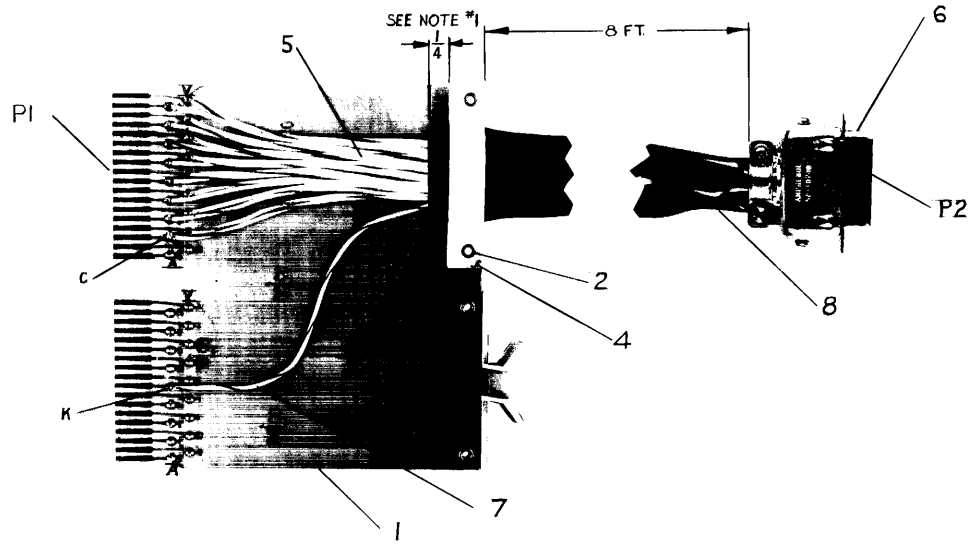
Figure 4-2 CR8/I Logic Schematic (M716)

WIRE TABLE

ITEM NO.	AWG	DESCRIPTION COLOR	CONNECTIONS FROM	CONNECTIONS TO
5	22	BLK & WHT	P1-C	P2-24
		BRN & WHT	P1-D	P2-1
		RED & WHT	P1-E	P2-2
		ORN & WHT	P1-F	P2-3
		YEL & WHT	P1-H	P2-13
		GRN & WHT	P1-J	P2-4
		BLU & WHT	P1-K	P2-5
5	22	VIO & WHT	P1-L	P2-6
5	22	GRY & WHT	P1-M	P2-7
		WHT	P1-N	P2-8
		BLK & WHT	P1-P	P2-14
		BRN & WHT	P1-R	P2-23
		RED & WHT	P1-S	P2-9
		ORN & WHT	P1-T	P2-10
		YEL & WHT	P1-U	P2-11
5		GRN & WHT	P1-V	P2-12
7	22	BLU & WHT	P1-K	P2-15

NOTES:

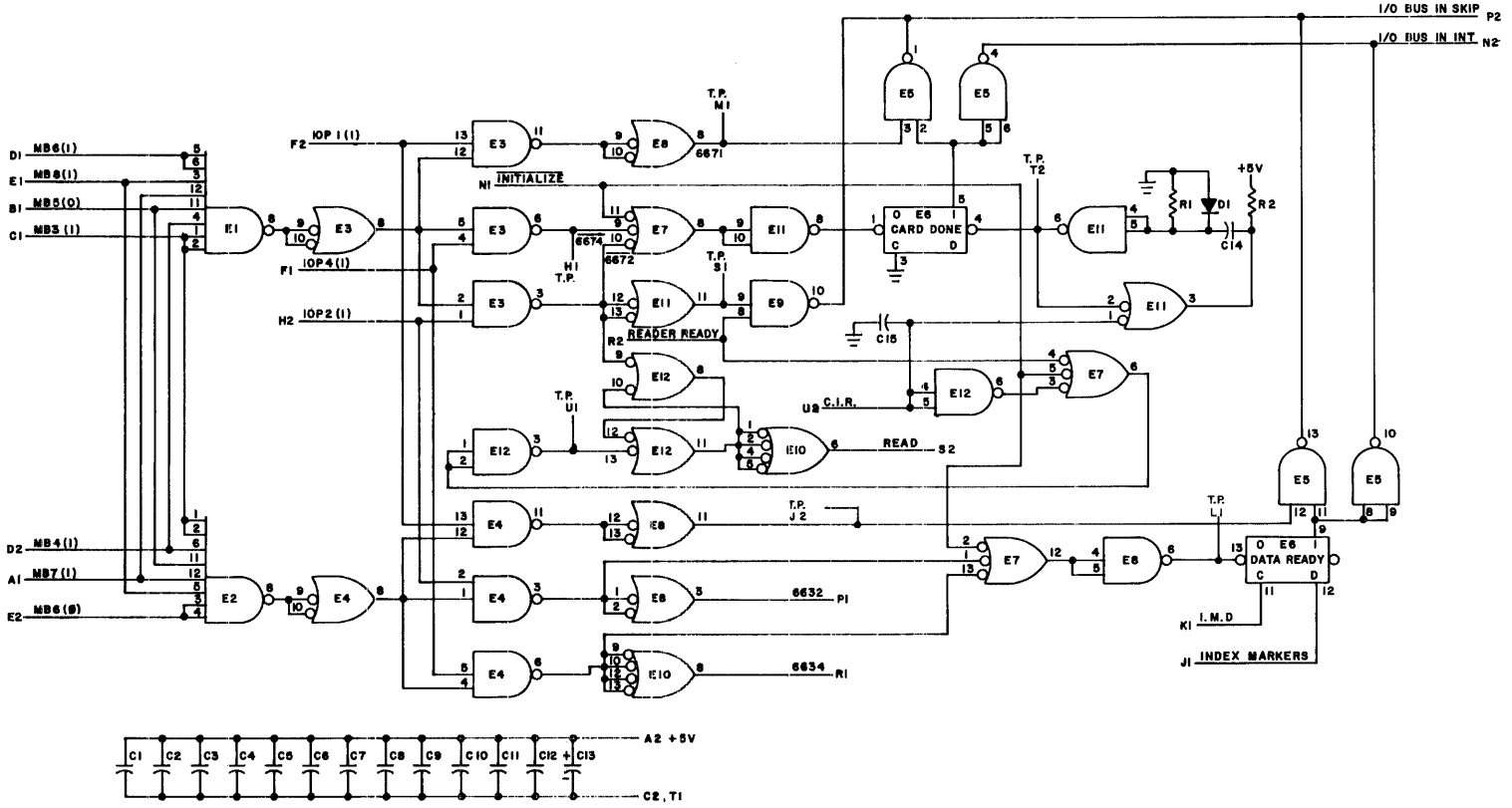
1 THE SLEEVING ITEM #8 SHALL EXTEND AT LEAST $\frac{1}{4}$ INCH BEYOND THE FASTENING CLAMP #4.



QTY.	DESCRIPTION	PART NO.	ITEM NO.
A/R	SLEEVING (BLACK)	91-07247	8
A/R	#22 AWG WIRE STRD WHT/BLU	91-07400-7	7
1	PLUG, AMP #57-30240	1203466	6
A/R	CABLE, RIBBON - 20 COND.	91-07575	5
1	CABLE CLAMP (WHT)	1202704	4
2	EYELETS #GS-4-7 (STIMPSON)	90-06732	2
1	BLANK MODULE	W991	1

PARTS LIST

Figure 4-3 CR8/I Cable Assembly

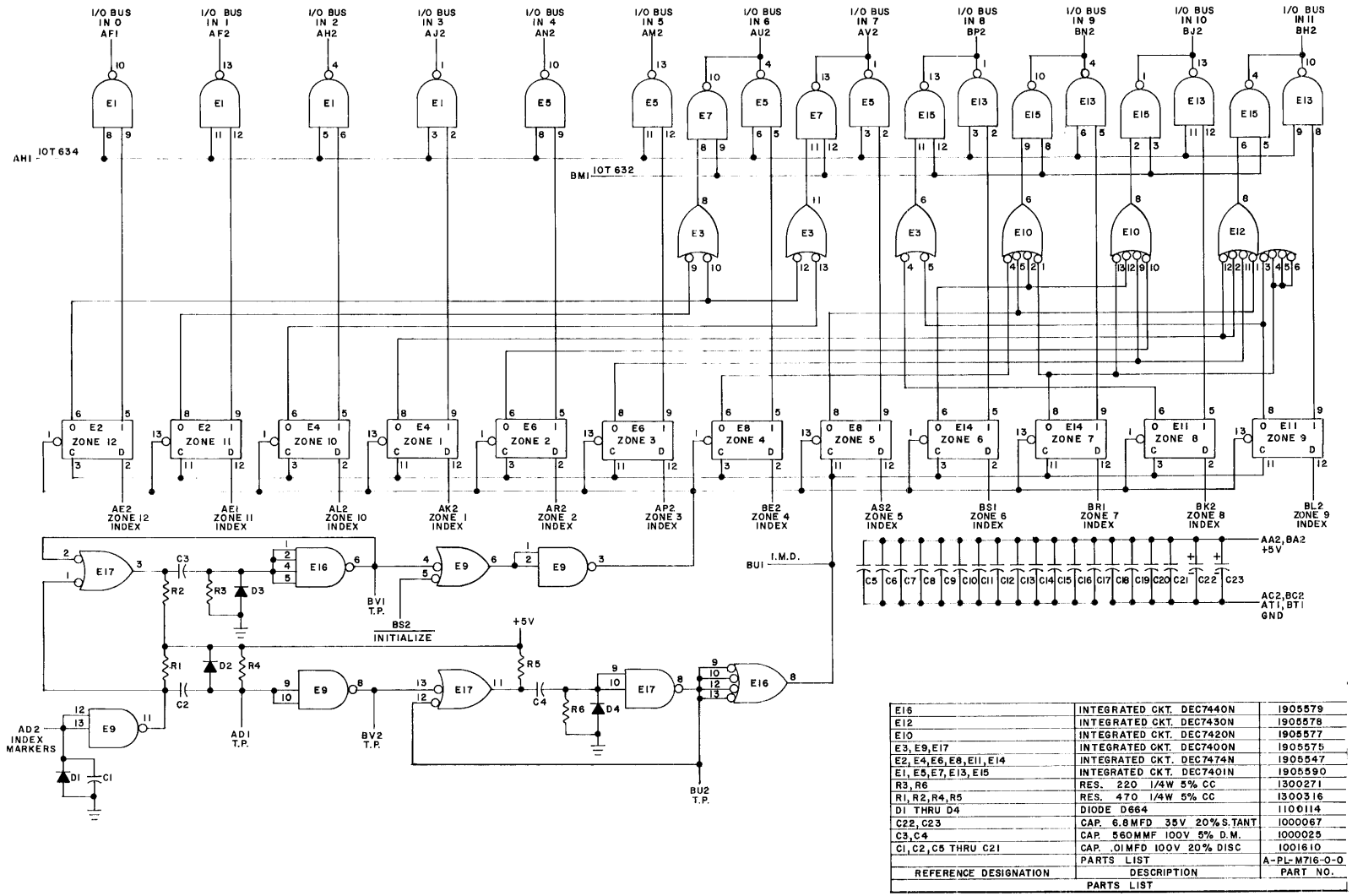


NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-M714-0-0
C1 THRU C12	CAP. .01MFD 100V 20% DISC	1001610
C13	CAP. 6.8MFD 35V 20% S.TANT	1000067
C14, C15	CAP. .005MFD 50V 20% D.CER.	1001765
D1	DIODE D664	1100114
R1	RES. 220 1/4W 5% CC	1300271
R2	RES. 470 1/4W 5% CC	1300316
E1, E2	INTEGRATED CKT. DEC7430N	1905578
E3,E4,E6,E11,E12	INTEGRATED CKT. DEC7400N	1905575
E5, E9	INTEGRATED CKT. DEC7401N	1905590
E8	INTEGRATED CKT. DEC7474N	1905547
E7	INTEGRATED CKT. DEC7410N	1905576
E10	INTEGRATED CKT. DEC7440N	1905579

PARTS LIST

Figure 4-4 M714 Module, Circuit Schematic



REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-M716-0-0
E16	INTEGRATED CKT. DEC7440N	1905579
E12	INTEGRATED CKT. DEC7430N	1905578
E10	INTEGRATED CKT. DEC7420N	1905577
E3, E9, E17	INTEGRATED CKT. DEC7400N	1905575
E2, E4, E6, E8, E11, E14	INTEGRATED CKT. DEC7474N	1905547
E1, E5, E7, E13, E15	INTEGRATED CKT. DEC7401N	1905590
R3, R6	RES. 220 1/4W 5% CC	1300271
R1, R2, R4, R5	RES. 470 1/4W 5% CC	1300316
D1 THRU D4	DIODE D664	1100114
C22, C23	CAP. 6.8MFD 35V 20% S. TANT	1000067
C3, C4	CAP. 560MMF 100V 5% D.M.	1000025
C1, C2, C5 THRU C21	CAP. .01MFD 100V 20% DISC	1001610

PARTS LIST

Figure 4-5 M716 Module, Circuit Schematic

4.6.2 Test Procedure

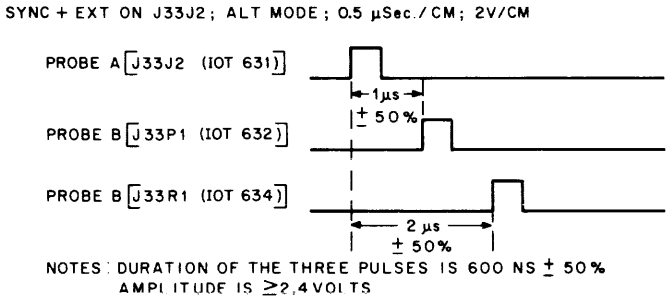
To check instructions 6631, 6632, and 6634:

a. Run this program:

Address	Instruction
7000	6637 (microinstructions 6631, 6632, and 6634 combined)
7001	5200 (jump to address 7000)
7002	7402 (halt; something is wrong)

This program should never halt; if it does, check INITIALIZE.

b. Check these signals:

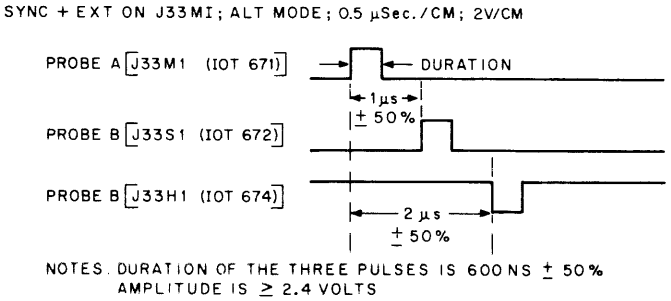


To check instructions 6671, 6672, and 6674:

a. Run this program:

Address	Instruction
7000	6677 (microinstructions 6671, 6672 and 6674 combined)
7001	5200 (jump to address 7000)
7002	7402 (halt; something is wrong)

b. Check these signals:



To check READY with machine ready: The GDI-100 should be ready to read, with MOTOR START and READ START indicators lit, and all others dark. Two cards of any pattern are placed in the input hopper.

a. Run this program:

Address	Instruction
7000	6672 (skip if reader is ready; advance one card)
7001	7402 (halt; something is wrong)
7002	7402 (halt; system OK)

One card should be fed through the reader, leaving MA = 7002 and MB = 7402.

To check READY with machine not ready: The GDI-100 should indicate READ STOP, and have two cards of any pattern in the input hopper. The remaining indicators do not apply to this test.

a. Run the same program as above. No cards should be fed through the reader, leaving MA = 7001 and MB = 7402.

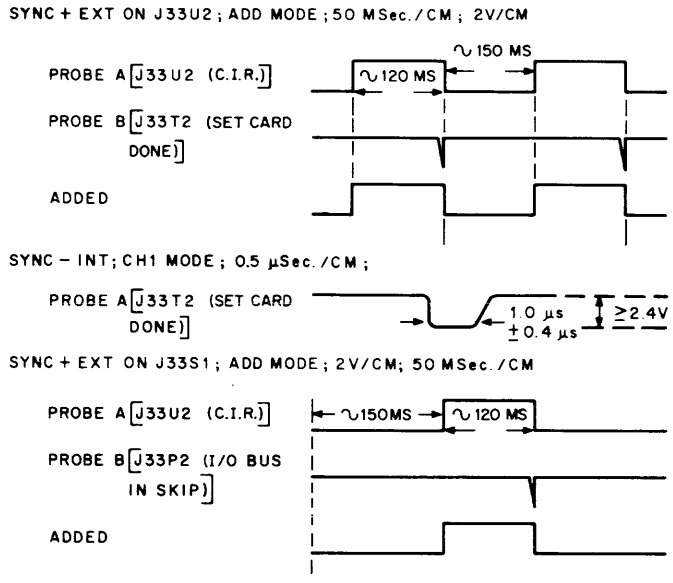
To check CARD DONE circuits:

a. Load the 400-card test deck into the input hopper and prepare the GDI-100 to read.

b. Run this program:

Address	Instruction
7000	6672 (skip if card reader is ready; advance one card)
7001	7402 (halt at end of deck)
7002	6671 (skip on CARD DONE flag)
7003	5202 (jump to address 7002, to look for CARD DONE)
7004	5200 (jump to address 7000, to read another card)

c. Check these signals:

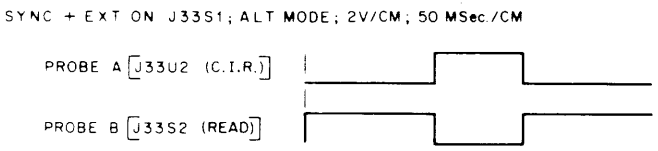


To check the READ command:

a. Load the input hopper with the 400-card test deck.

b. Run the same program as above.

c. Check these signals:



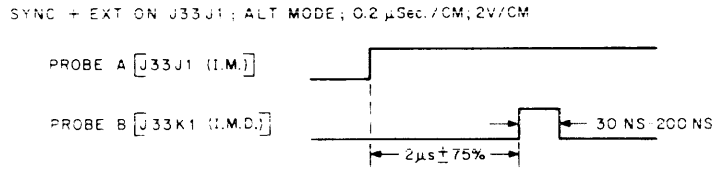
To check the DATA READY flag:

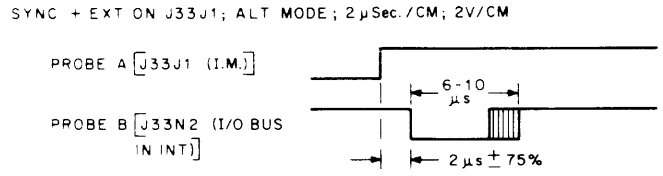
a. Load the PDP-8/I with the MAINDEC-08-D20A diagnostic program.

b. Load the input hopper with the 400-card test deck.

c. Load address 0700 and start the computer. (Addresses 0700 to 0715 are the test.)

d. Check these signals:



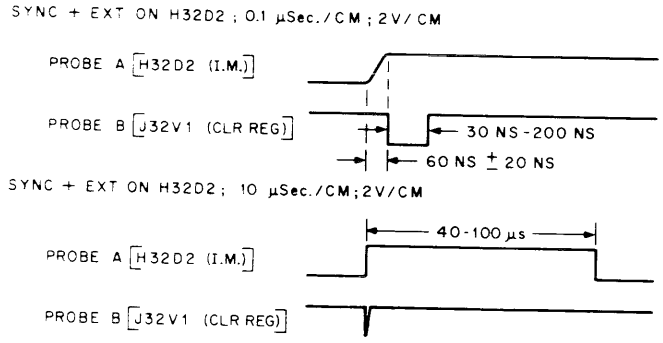


To check the Clear Register pulse: (One should occur at the leading edge of each IM.)

a. Load the 400-card test deck.

b. Load address 0700 and start the computer.

c. Check these signals:

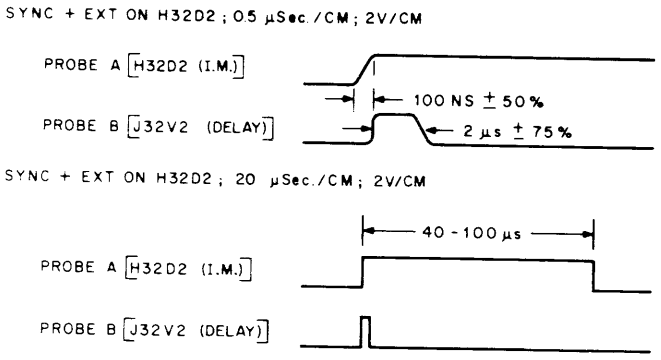


To check the delay circuit:

a. Load the 400-card test deck.

b. Load address 0700 and start the computer.

c. Check these signals:

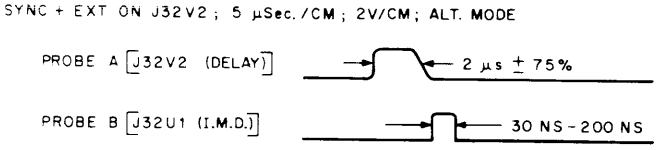


To check IMD (IM delayed): (This clock pulse should occur at the trailing edge of the delay signal.)

a. Load the 400-card test deck.

b. Load address 0700 and start the computer.

c. Check these signals:

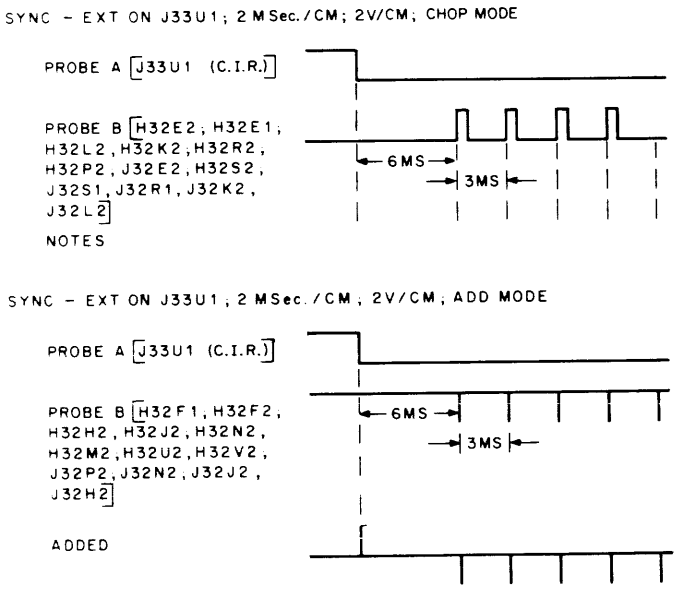


To check the CR8/I data register (binary bits):

a. Load the 400-card test deck.

b. Load address 0700 and start the computer.

c. Check these signals:



4.7 MAINTENANCE

GDI-100: Periodic maintenance is required for the card reader. Refer to the GDI 'Technical Manual, Model 100 Card Reader', Section VII.

CR8/I: The Card Reader Control logic is simple and straightforward. You should be able to locate any trouble quickly by using the troubleshooting test procedures in Section 4.6.

If you locate a defective module, replace it with one from spares and return the defect to DEC for repair or replacement.

For emergency servicing, or where spare logic boards are not available, integrated circuit chips can be replaced with standard commerical ICs.

Use Texas Instrument series prefixed 'SN'. (DEC 7400N is equivalent to T.I. number SN 7400 N, etc.)

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