DEC-8I-HR2A-D

PDP-8/I

MAINTENANCE MANUAL

OPTION DESCRIPTIONS
AND
ENGINEERING DRAWINGS

VOLUME II

1st Printing October 1968
2nd Printing (Rev) May 1969
3rd Printing July 1969
4th Printing (Rev) May 1970

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INTRODUCTION

This volume contains three parts: Functional Descriptions of Options, Engineering Drawings, and Appendices. The part containing the Functional Descriptions is supplemented by the below listed separate publications.

Title	Number
BB08 General Purpose Bus Interface Option	DEC-08-HIZA-D
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PART I

OPTION DESCRIPTIONS

LIST OF FUNCTIONAL DESCRIPTIONS

ASR33 Teletype

Data Break

MC8/I, MM8/I Extended Memory

MP8/I Memory Parity Option

VC8/I Oscilloscope Display Option

VP8/I Incremental Plotter Option

KW8/I Real-Time Clock Option

FUNCTIONAL DESCRIPTION OF OPTIONS

ASR33
TELETYPE
OPTION

FUNCTIONAL DESCRIPTION

ASR33
TELETYPE

INTRODUCTION

The Model ASR33 Teletype unit is provided as standard equipment with the PDP-8/I. The unit serves as a keyboard and perforated-tape reader input, and as a page-printer and tape-punch output for the computer. The unit is described in Teletype Corporation bulletins 273B and 1184B.

The Teletype unit is modified as follows, to permit operation with the PDP-8/I.

a. The WRU (who are you) pawl is removed for the teletype mechanism. In network communications operation, this pawl is triggered to respond to the WRU command received from a transmitting station. When triggered, the pawl causes a "here is" code to be generated and transmitted, identifying the unit to the interrogating station.

b. A cable from main frame location J12 is connected between the teletype control, and the teletype unit. This signal cable connects to a terminal block within the teletype stand. A relay is added and connections are made to a tape reader advance magnet. These connections enable tape motion while the control assembles a character, and disable the magnet when a character begins a serial transfer. The teletype conversion requires little time to complete, and does not permanently limit any normal use of the ASR33.

The control logic, which consists of three integrated-circuit modules located within the processor main frame, assembles or disassembles serial information for the teletype unit for parallel transfer to, or from, the PDP-8/I processor accumulator.

The control logic contains the flags which enact a program interrupt, or an instruction skip based upon the availability of the teletype unit, thus controlling the information transfer between the Teletype and the processor as a function of the program.

Teletype-control logic adjustments, and ASR33 maintenance are described in Chapter 5 of this manual.

Operation

The teletype control logic can be considered as two separate and independent devices: the teletype receiver, and the transmitter. The teletype receiver (drawing BS-8I-0-11), performs a "read" operation in which an asynchronous serial data word from the teletype keyboard or reader, is assembled by the receiver (M706) for a parallel transfer to the accumulator.

The teletype transmitter (drawing BS-8I-0-12) performs a "print/punch" operation in which a parallel data transfer from the accumulator to the transmitter logic (M707) occurs. The logic converts the parallel word to a serial word, and sends it to the teletype unit to be decoded and punched on paper tape, or printed.

Certain program instructions are used to initiate the transfer of the assembled parallel data to the accumulator in the "read" operation, and the loading of the parallel data from the accumulator into the transmitter logic in the "print/punch" operation. These instructions are decoded as IOT instructions by the processor and generate IOP pulses. Bits 0 through 2 of these instructions contain the octal code 6, indicating an input/output (IOT) instruction. Bits 3 through 8 of the instruction provide a 6-bit octal code

(I/O address code) sensed by the teletype control logic to allow control of the transmitter and receiver operations. This I/O address code is 03_8 for the teletype receiver, and 04_8 for the teletype transmitter. A 6-input NAND gate in both the receiver and transmitter logic senses the coding, and allows the IOP pulses to perform the following functions.

(03) IOP1 - generates $\overline{\text{TTI SKIP}}$ if the keyboard flag is set.
(03) IOP2 - Clears the keyboard flag, clears accumulator, and starts reader if the reader switch is ENABLED.
(03) IOP4 - transfers (reads) the assembled parallel word through the positive internal bus to the AC.
(04) IOP1 - generates $\overline{\text{TTO SKIP}}$ if the teleprinter flag is set.
(04) IOP2 - Clears the teleprinter flag.
(04) IOP4 - Loads the parallel word into the TT0-TT7 buffer and initiates the release of the serial word to the teletype unit.

Signals used by the teletype unit are standard 11-unit-code serial current pulses consisting of marks (bias current), and spaces (no current). The marks correspond to binary 1s; the spaces correspond to binary 0s. Each 11-unit teletype character consists of three sections: a 1-unit start bit, eight 1-unit character bits (ASCII code), and two 1-unit stop bits. The start bit (a space) indicates the beginning of a character and allows synchronization between the control logic and the serial word. The eight data bits represent the actual binary data. Following the start bit, the data bits are assembled, or disassembled with the least significant bit first. The two stop bits (marks) allow the computer and teletype to resynchronize.

LOGIC DESCRIPTION

The following paragraphs describe the read and print/punch cycles, and the program instruction set for teletype operation.

Read Cycle - Figure 1 shows the sequence of events that occur when a serial word from the teletype unit is assembled in the receiver. The receiver circuitry is shown on engineering drawing BS-8I-0-11.

The clock (drawing BS-8I-0-12) is free-running, producing TTI CLOCK pulses at 880 Hz. The clock is common to both the receiver and transmitter functions; however, the clock frequencies needed for these units differ.

When the computer is turned on, or the Start key is depressed, the processor INITIALIZE level is generated. INITIALIZE clears the IN ACTIVE flip-flop, the SPIKE DETECTOR flip-flop, and generates KCC to clear the KEYBOARD FLAG and set the READER RUN flip-flop (drawing BS-8I-0-11). Clearing the IN ACTIVE flip-flop generates the $\overline{\text{START ENABLE}}$ level. This level, combined with the start bit at the output of the Schmitt trigger (ST), which is produced by the Teletype Distributor by program control allows a TTI CLOCK pulse to generate $\overline{\text{PRESET}}$. The $\overline{\text{PRESET}}$ pulse allows the serial data from the teletype to synchronize with the receiver logic in the following manner.

$\overline{\text{PRESET}}$ sets the IN ACTIVE flip-flop and each TTI register flip-flop to a binary 1, and clears the READER RUN flip-flop. With READER RUN cleared, a relay in the tape reader is energized to release the tape-feed latch, stopping tape motion only when the beginning of a character has been sensed, and before sensing of the next character begins. In addition, the SPIKE DETECTOR flip-flop is set to sample the line 1/2 unit after the start bit is received. If the start bit is not present at this time, the IN ACTIVE flip-flop clears and awaits another $\overline{\text{PRESET}}$ signal. This eliminates noise on the start bit that is less than 1/2 unit. If the start bit is still present, i.e., no false start due to noise, TTI SHIFT pulses are generated and the start bit is loaded (a binary 0) into TTI 0. The shift pulses are synchronized to occur during the middle of each serial bit time. As Figure 6-1 illustrates, each succeeding

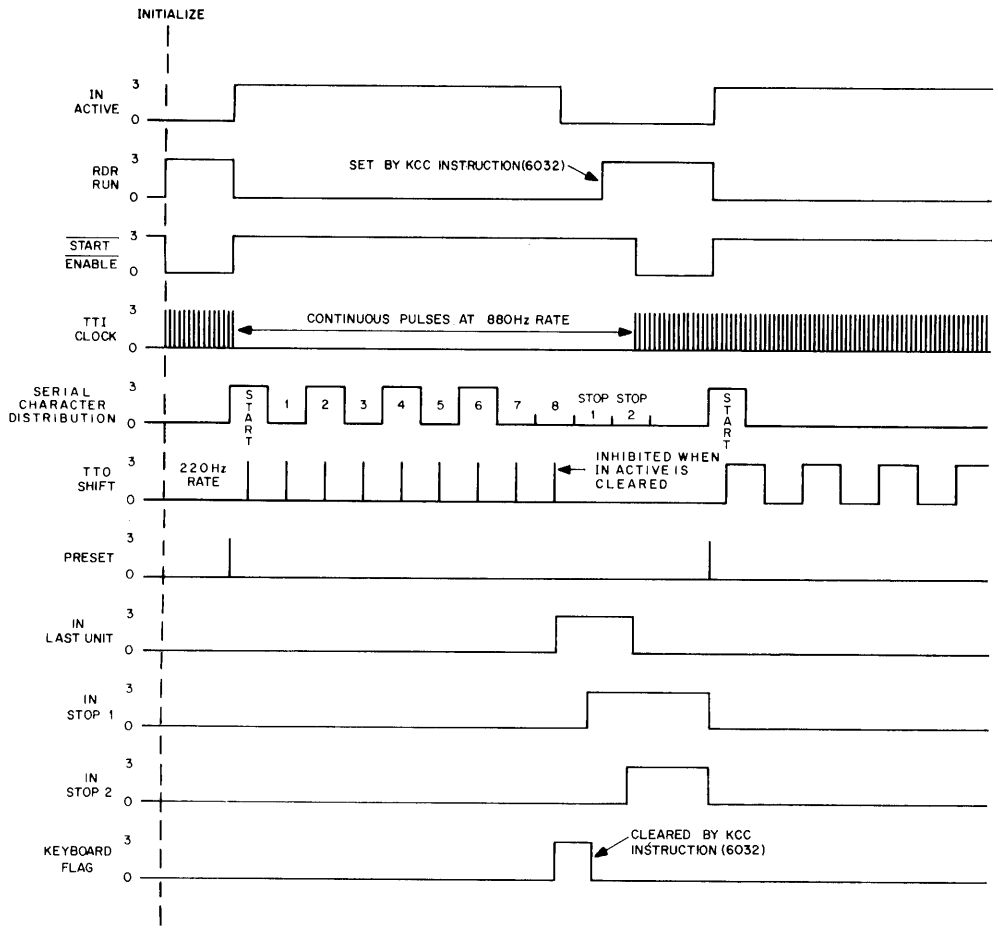


Figure 1 Teletype Read Cycle Timing Diagram

TTI SHIFT pulse loads the character bits into the receiver serial shift register. When the start bit is shifted into TTI 7, the next TTI SHIFT pulse produced sets the IN LAST UNIT and KEYBOARD FLAG flip-flops. Setting of IN LAST UNIT clears the IN ACTIVE flip-flop, disabling further TTI SHIFT pulses. When cleared, IN ACTIVE allows the CLOCK SCALE 2 pulses to set the IN STOP 1 and IN STOP 2 flip-flops which count out the stop time. IN STOP 2 when set, clears the IN LAST UNIT flip-flop, allowing $\overline{\text{START ENABLE}}$ to produce $\overline{\text{PRESET}}$ when the start bit of the next character appears at the output of the Schmitt trigger (ST).

When the KEYBOARD FLAG flip-flop is set, $\overline{\text{TT INT}}$ (drawing BS-8I-0-12) is generated. $\overline{\text{TT INT}}$ generates INT RQST (BS-8I-0-10) in the processor. If the program interrupt facility is enabled, INT RQST indicates to the PDP-8/I that a device is requesting service. The program then enters a "search" subroutine to determine which device issued the interrupt. This is accomplished by executing a series of "flag-checking" skip instructions. When the KEYBOARD FLAG sensing instruction KSF (6031) is performed, and the flag is raised, $\overline{\text{TT SKIP}}$ (Drawing BS-8I-0-12) is generated producing I/O SKIP (Drawing BS-8I-0-10) in the processor. IO SKIP forces the processor program counter to increment by one, thus the next instruction is skipped. A service routine for the teletype receiver is entered when the skip occurs. In this routine, the KEYBOARD FLAG is cleared, READER RUN is set to release a new serial word to the receiver, and the previously assembled word is sent, in parallel, to the processor.

Print/Punch cycle - Figure 2 illustrates the sequence of events that occur when a parallel word from the accumulator is loaded into the transmitter logic, and disassembled into serial word format for use by the teletype unit. The transmitter logic is shown on engineering drawing BS-8I-0-12.

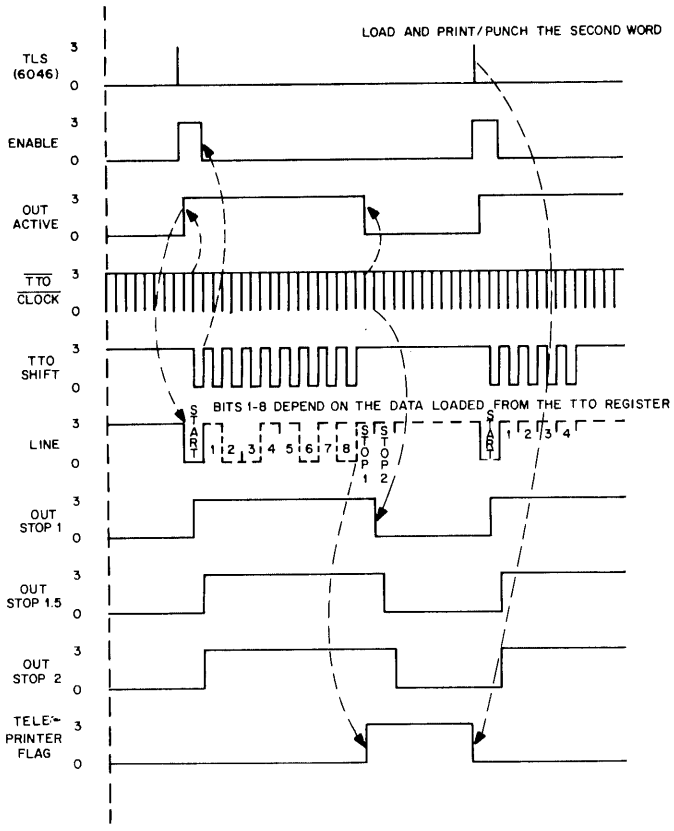


Figure 2 Print/Punch Cycle Timing Diagram

When the computer is turned on, or whenever the Start key is pressed, the processor INITIALIZE level is generated. This level clears the ENABLE, OUTACTIVE, TELEPRINTER FLAG, and TTO register flip-flops. Execution of the program instruction TLS (6046) generates TTO SELECT in the transmitter logic, and IOP1 and IOP2 in the processor. IOP4 and TTO SELECT combine in the transmitter logic to load the parallel word (accumulator bits AC04 through AC11) into the TTO register, and set the ENABLE flip-flop. IOP2 and TTO SELECT are combined to clear the TELEPRINTER FLAG.

After the data is loaded into the TTO register, TTO SHIFT pulses are generated, and the serial shift commences. TTO SHIFT pulses are produced through the complementing action of the FREQUENCY DIVIDE flip-flop which is clocked at a 220 Hz rate by $\overline{\text{TTO CLOCK}}$. Synchronization is provided by using both of these clocks as indicated in Figure 2, and described below.

When the first $\overline{\text{TTO CLOCK}}$ pulse following the setting of ENABLE occurs, the following events take place: the OUT ACTIVE flip-flop is set, the start bit is placed on the line to the PRINT SELECTOR MAGNET DRIVER (PSM line), and OUT STOP 1 is set (discussed later). Alternate $\overline{\text{TTO CLOCK}}$ pulses produce a TTI SHIFT pulse which shifts the data word bit-by-bit into the LINE flip-flop. The first TTI SHIFT pulse clears the ENABLE flip-flop. As data is shifted onto the PSM line, binary 0s are shifted into the TTO register through ENABLE. When the parallel-to-serial conversion has completed, an 8-input NAND gate senses all zeroes in the TTO register, and its output $\overline{\text{TTO} = 0}$ allows OUT ACTIVE to clear with the next TTO CLOCK pulse. In addition, $\overline{\text{TTO} = 0}$ enables the TELEPRINTER FLAG to set with the next (and last) TTO SHIFT pulse. When OUT ACTIVE is cleared, TTI SHIFT is disabled, and the two 1-unit stop bit times are counted out by the OUT STOP register. The first $\overline{\text{TTO CLOCK}}$ pulse occuring after OUT ACTIVE was cleared, clears the OUT STOP 1 flip-flop. The OUT STOP 1.5 and the OUT STOP 2 flip-flops are cleared by the next two consecutive pulses. If another TLS instruction has been issued (print/punch another character), the operation commences with the occurrence of the first $\overline{\text{TTO CLOCK}}$ pulse after OUT STOP 2 is cleared. For the print/punch operation with the ASR33, a 2-unit stop time period is required because of the inherent electro-mechanical delay time in the teletype unit.

When the TELEPRINTER FLAG is set, $\overline{\text{TT INT}}$ (drawing BS-8I-0-12) is generated. $\overline{\text{TT INT}}$ produces INT RQST (drawing BS-8I-0-10) in the processor. If the program interrupt facility is

enabled, INT RQST indicates that a device is requesting service. The program then enters a "search" subroutine to determine which device issued the interrupt. This is accomplished by executing a series of "flag-check" skip instructions. When the TELEPRINTER FLAG sensing instruction TSF (6041) is performed and the flag is raised, $\overline{\text{TT SKIP}}$ (Drawing BS-8I-0-12) is generated producing I/O SKIP (Drawing BS-8I-0-10) in the processor. I/O SKIP forces the program counter to increment by one, thus the next instruction is skipped. A service routine for the teletype transmitter is entered when the skip occurs. For the transmitter service, a new character is transferred to the transmitter to be printed or punched by the teletype unit.

Teletype Instruction Description

Table 1 contains descriptions of the teletype keyboard/reader and the teleprinter/punch instructions.

Table 1
Teletype Instruction Descriptions

Mnemonic	Octal Code	Description
KSF	6031	Generates IOP1 to sense the status of the KEYBOARD FLAG. When the flag is set, the next sequential program instruction is skipped. This indicates that the assembled word is ready for transfer to the accumulator.
KCC	6032	Generates IOP2 to clear the KEYBOARD FLAG and set READER RUN. In addition, TT AC CLEAR is generated to clear the accumulator.
KRS	6034	Generates IOP4 to transfer the assembled word in parallel to the accumulator through the major register bus. The KEYBOARD FLAG is not cleared.
KRB	6036	Generates IOP2 and IOP4 to perform the functions of the KCC and KRS commands during a single computer cycle. The KEYBOARD FLAG is cleared.
TSF	6041	Generates IOP1 to sense the status of the TELEPRINTER FLAG. When the flag is set, the next sequential program instruction is skipped. This indicates that the print/punch operation has completed.

Table 1 (Cont)
Teletype Instruction Descriptions

Mnemonic	Octal Code	Description
TCF	6042	Generates IOP2 to clear the TELEPRINTER FLAG.
TPC	6044	Generates IOP4 to load the parallel word into the transmitter register, initiating the print/punch operation.
TLS	6046	Generates both IOP2 and IOP4 to combine the functions of the TCF and TPC instructions in one computer cycle.

DATA BREAK
FUNCTIONAL DESCRIPTION

DATA BREAK

INTRODUCTION

Peripheral equipment connected to the data break facility can cause a temporary suspension in the program in progress to transfer information with the computer core memory, via the MB. One I/O device can be connected directly to the data break facility or up to seven devices can be connected to it through the Type DM01 Data Multiplexer. This cycle stealing mode of operation provides a high-speed transfer of individual words or blocks of information at core memory addresses specified by the I/O device. Since program execution is not involved in these transfers, the program counter, accumulator, and instruction register are not disturbed or involved in these transfers. The program is merely suspended at the conclusion of an instruction execution, and the data break is entered to perform the transfer, then the Fetch state is entered to continue the main program.

Data breaks are of two basic types: single-cycle and three-cycle. In a single-cycle data break, registers in the device (or device interface) specify the core memory address of each transfer and count the number of transfers to determine the end of data blocks. In the three-cycle data breaks two computer core memory locations perform these functions, simplifying the device interface by omitting two hardware registers.

The computer receives the following signals from the device during a data break (these input/output signals can be changed to positive "bus" logic as described in Chapter 1).

Signal	-3V	0V
Break Request	No break request	Break Request
Cycle Select	One-cycle break	Three-Cycle break
Transfer Direction	Data into PDP-8/I	Data out of PDP-8/I
Increment CA inhibit	CA incremented	CA not incremented
Increment MB(pulse)	MB not incremented	MB incremented
Address (12 bits)	Binary 0	Binary 1
Data (12 bits)	Binary 0	Binary 1

The computer sends the following signals to the device during a data break.

Signal	Characteristics
Data (12 bits)	-3V = binary 0, 0V = binary 1
Address Accepted	.35 - .45 μs negative pulse beginning at TP4 of a break cycle.
WC Overflow	-3V level change occurring at TP2 time of the WC state and lasting for one machine cycle.
Buffered Break	-3V when in Break state.

To initiate a data break, an I/O device must supply four signals simultaneously to the data break facility. These signals are the Break Request signal, which sets the BRK SYNC flip-flop in the major state generator to control entry into the data break states. (Word Count for a three-cycle data break or Break for a single-cycle data break); a Transfer Direction signal, supplied to the MB control element to allow data to be strobed into the MB from the peripheral equipment and to inhibit reading from core memory; a cycle select signal which controls gating in the major state generator to determine if the one-cycle or three-cycle data break is to be selected; and a core memory address of the transfer which is supplied to the input of the MA. When the break request is made, the data break replaces entry into the Fetch state of an instruction. Therefore the data break is entered at the conclusion of the Execute state of most memory reference instructions and at the conclusion of a Fetch state of augmented instruction. Having established the data break, each machine cycle is a Word Count, Current Address, or Break cycle until all data transfers have taken place, as indicated by removal of the break request signal by the peripheral equipment.

More exactly, the break request signal enables the BRK SYNC flip-flop. At TP1 time, the BRK SYNC flip-flop is set if the break request has been received, and is cleared otherwise.

At TP4 time of each machine cycle, the major state generator is set to establish the state for the cycle. At this time, the status of the BRK SYNC flip-flop is sampled and, if in the 1 state, the Word Count or Break state is set into the major state generator and a data break commences.

Therefore, to initiate a data break, the break request must be at ground potential for at least 500 ns preceding TP1 of the cycle preceding the data break cycle. A break request signal should be supplied to the computer when the address, data, transfer direction, and cycle select signals are supplied to the computer.

When a data break occurs, the address designated by the device is loaded into the MA at TP4 time of the last cycle of the current instruction, and the major state generator is set to the Word Count state if the cycle select signal is at ground, or is set to the Break state if this signal is at -3V. The program is delayed for the duration of the data break, commencing in the following cycle. A break request is granted only after completion of the current instruction as specified in the following conditions:

a. At the end of the Fetch cycle of an OPR or IOT instruction, or a directly addressed JMP instruction
b. At the end of the Defer cycle of an indirectly addressed JMP instruction
c. At the end of the Execute cycle of a JMS, DCA, ISZ, TAD, or AND instruction

At the beginning of the Word Count cycle of a three-cycle data break or the Break cycle of a one-cycle data break, the address supplied to the input of the MA is strobed into the MA and the computer supplies an address accepted signal to the device. Entry into the Break cycle is indicated to the peripheral equipment by a buffered break signal and by an address accepted signal that can be used to enable gates in the device to perform tasks associated with the transfers. The address accepted signal is the most convenient control to be used by I/O equipment to disable the break request signal, since this signal must be removed at TP4 time to prevent continuance of the data break into the next cycle. If the transfer direction signal establishes the direction as out of the computer, the content of the core memory register at the address specified is transferred into the MB and is immediately available for strobing by the peripheral equipment. If the transfer direction signal specifies a data direction into the PDP-8/I, reading from core memory is inhibited and data is transferred into the MB from peripheral equipment.

The status of the BRK SYNC flip-flop is sensed at the beginning of a Break cycle to determine

if an additional Break cycle is required. If a break request signal has been received since TP4, the Break state is maintained in the major state generator; if the break request signal has not been received by this time; the Fetch state is set into the major state generator to continue the program. The break request signal should be removed by the end of the address accepted signal if additional Break cycles are not required.

SINGLE-CYCLE DATA BREAK

One-cycle breaks transfer a data word into computer core memory from a device, transfer a data word into a device from core memory, or increment the content of a device-specified core memory location. In each of these types of data break, one computer cycle is stolen from the program by each transfer; break cycles occur singly (interleaved with the program steps) or continuously (as in a block transfer), depending upon the timing of the break request signal at rates of up to 660 kHz.

During the memory-strobe portion of the Break cycle, the content of the addressed cell is read into the MB, if the transfer direction is out of the computer (into the I/O device). If the transfer direction is into the computer, generation of the Memory Strobe pulse is inhibited so that the MB (cleared during the previous cycle) remains cleared. Information is transferred from the output data register of the I/O device into the MB and is written into core memory during TS3 and TS4 times of the Break cycle. In an outward transfer, the write operation restores the original content of the address cell to memory.

If there is a further break request, another Break cycle is initiated. If there is no break request, the content of the PC is transferred into the MA, the IR is cleared, and the major state generator is set to Fetch. The program then executes the next instruction.

The increment MB facility is useful for counting iterations or events by means of a data break, so that the PC and AC are not disturbed. Within one Break cycle of 1.5 μs, a word is fetched from a device-specified core memory location, is incremented by one, and is restored to the same memory location. The increment MB signal-input must be supplied to the computer only during a Break cycle in which the direction of transfer is out of the PDP-8/I. These restrictions can be met by a simple AND gate in the device; an increment MB signal is generated only when an event occurs, the buffered break signal from the computer is present, and the transfer direction signal supplied to the computer is at ground potential.

THREE-CYCLE DATA BREAK

The three-cycle data break provides an economical method of controlling the transfer of data between the computer core memory and fast peripheral devices. Transfer rates in excess of 200 kHz are possible using this feature of the PDP-8/I.

The three-cycle data break differs from the one-cycle break in that a ground-level cycle select signal is supplied so that when the data break conditions are fulfilled the program is suspended and the Word Count state is entered. The Word Count state is entered to increment the fixed core memory location containing the word count. The device requesting the break supplies this address as in the one-cycle break, except that this is a fixed address supplied by wired ground and -3V signals rather than from a register.

Following the Word Count state a current address state occurs in which the location following the word count address (bit 11 = 1 after + 1 => MA) is read, incremented by one, restored to memory, and loaded into the MA to be used as the transfer address. Then the normal Break state is entered to effect the transfer between the device and the computer memory cell specified by the MA.

Word Count State

When this state is entered, the contents of the core memory address specified by the external device plus 1 is loaded into the MB at TP2 time. The word count, established previously by instructions, is the 2's complement negative number equal to the required number of transfers. If the word becomes 0 when incremented, the computer generates a WC overflow signal and supplies it to the device. During TS3 and TS4 times, the incremented word count is rewritten in memory, the content of the MA is incremented by 1, to establish the next location as the address for the following memory cycle, and the major state generator is set to the current address state.

Current Address State

Operations during the second cycle of the three-cycle data break depend upon the condition of the increment CA inhibit (+1 → CA inhibit) signal supplied to the computer from the I/O device. At TP2 time, the MB is loaded with either the contents of the memory cell following the word count (current address register) or the incremented contents of the current address register (i.e., if CA inhibit is at ground, the contents are loaded; if CA inhibit is at -3V, the incremented contents are loaded). The current address register may be incremented to advance the address of the transfer to the next sequential location. During TS3 and TS4 times, the content of the MB is rewritten into core memory, the address word in the MB is transferred into the MA to designate the address to be used in the succeeding memory cycle, and the major state generator is set to Break state.

Break State

The actual transfer of data between the external device and the core memory, through the MB, occurs during the Break state as during a single-cycle data break, except that the address is determined by the current content of the MA rather than directly by the device.

LOGIC DESCRIPTION

The data break facility allows I/O devices to transfer information directly with the PDP-8/I core memory on a cycle-stealing basis. Up to seven devices can connect to the data break facility through the optional Data Multiplexer Type DM01. The data break is particularly well-suited for devices which transfer large amounts of information in block form.

Peripheral I/O equipment operating at high speeds can transfer information with the computer through the data break facility more efficiently than through programmed means. The combined maximum transfer rate of the data break facility is over 7.8 million bits per second. Information flow to effect a data break transfer with an I/O device appears in Figure 1.

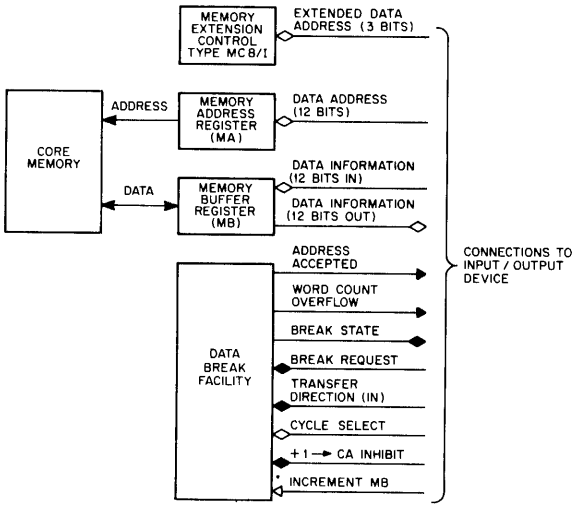


Figure 1 Data Break Transfer Interface Block Diagram

In contrast to programmed operations, the data break facilities permit an external device to control information transfers. Therefore, data-break device interfaces require more control logic circuits, and are more costly than programmed-transfer interfaces.

Data breaks are of two basic types: single-cycle and three-cycle. In a single-cycle data break, registers in the device (or device interface) specify the core memory address of each transfer and count the number of transfers to determine the end of data blocks. In the three-cycle data break, two computer core memory locations perform these functions, simplifying the device interface by omitting two hardware registers.

In general terms, to initiate a data break transfer of information, the interface control must do the following.

a. Specify the affected address in core memory.

b. Provide the data word by establishing the proper logic levels at the computer interface (assuming an input data transfer), or provide readin gates and storage for the word (assuming an output data transfer).

c. Provide a logical signal to indicate direction of data word transfer.

d. Provide a logical signal to indicate single-cycle or three-cycle break operation.

e. Request a data break by supplying a proper signal to the computer data break facility.

Single-Cycle Data Breaks

Single-cycle breaks are used for input data transfers to the computer, output data transfers from the computer, and memory increment data breaks. Memory increment is a special output data break in which the content of a memory address is read, incremented by one, and rewritten at the same address. It is useful for counting iterations or external events without disturbing the computer program counter (PC) or AC registers.

Input Data Transfers

Figure 2 illustrates timing of an input transfer data break. The address to be affected in core

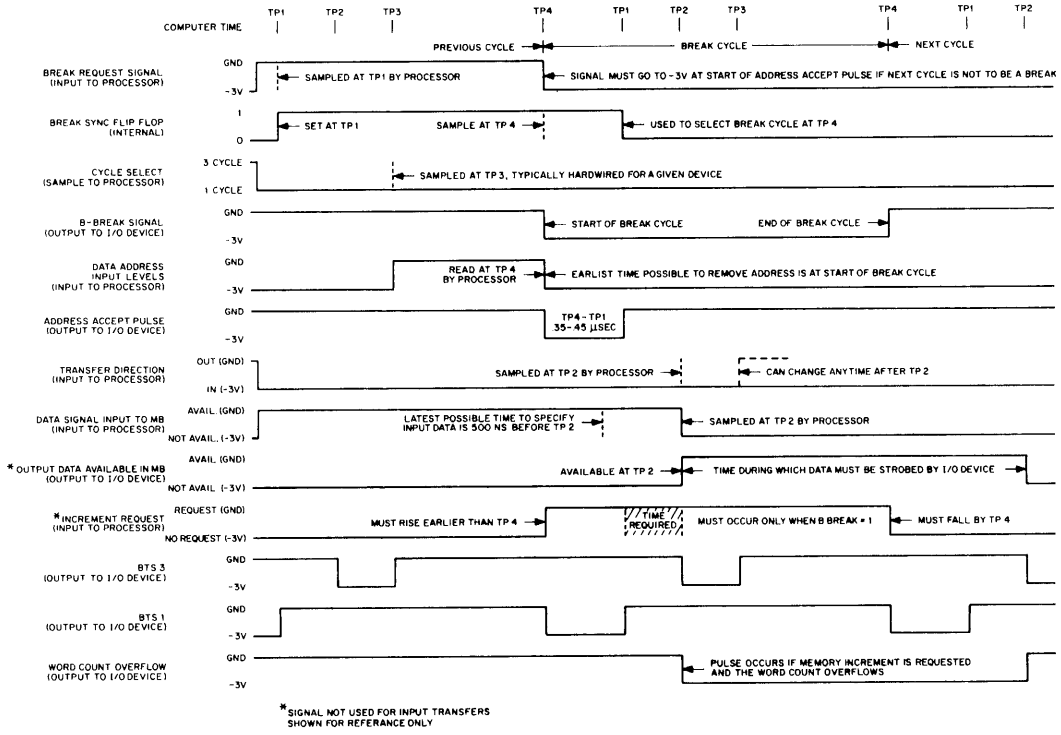


Figure 2 Single-Cycle Data Break Input Transfer Timing Diagram

is normally provided in the device interface in the form of a 12-bit flip-flop register (data break address register) which has been preset by the interface control by programmed transfer from the computer.

External registers and control flip-flops supplying information and control signals to the data break facility and other PDP-8/I interface elements are shown in Figure 3. The input buffer register (IB in Figure 3) holds the 12-bit data word to be written into the computer core memory location specified by the address contained in the address register (AR in Figure 3).

Appropriate output terminals of these registers are connected to the computer to supply ground potential to designate binary 1s. Since most devices that transfer data through the data break facility are designed to use either single-cycle or three-cycle breaks, but not both, the cycle select signal can usually be supplied from a stable source (such as a ground connection or a -3V clamped load resistor) rather than from a bistable device as shown in Figure 3.

Other portions of the device interface, not shown in Figure 3, establish the data word in the input buffer register, set the address into the address register, set the direction flip-flop to indicate an input data transfer, and control the break request flip-flop. These operations can be performed simultaneously or sequentially, but all transients should occur before the data break request is made. Note that the device interface need supply only static levels to the computer, minimizing the synchronizing logic circuits necessary in the device interface.

When the data break request arrives, the computer completes the current instruction, generat-

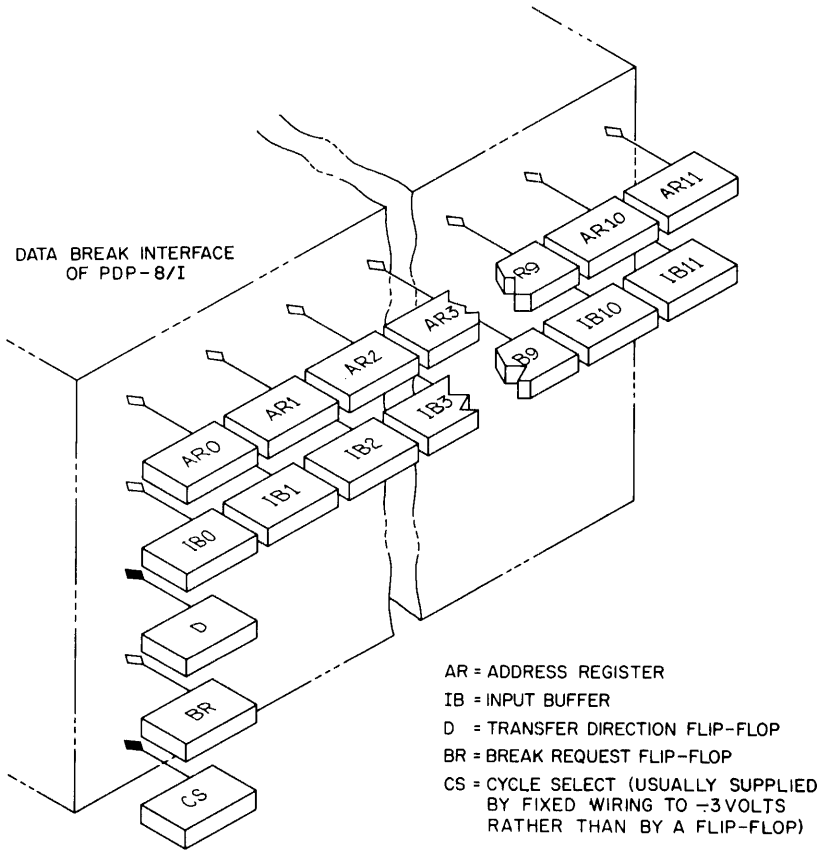


Figure 3 Device Interface Logic for Single-Cycle Data Break Input Transfer

es an address accepted pulse (at TP4 time of the cycle preceding the data break) to acknowledge receipt of the request, then enters the Break state to effect the transfer. The address accepted pulse can be used in the device interface to clear the break request flip-flop, increment the content of the address register, etc. If the break request signal is removed before TP1 time of the data break cycle, the computer performs the transfer in one 1.5 μs cycle and returns to programmed operation.

Output Data Transfers

Timing of operations occurring in a single-cycle output data break is shown in Figure 4. Basic logic circuits for the device interface used in this type of transfer are shown in Figure 5. Address and control signal generators are similar to those discussed previously for input data transfers, except that the transfer direction signal must be at ground potential to specify the output transfer of computer information. An output data register (OB in Figure 5) is usually required in the device interface to receive the computer information. The device, and not the PDP-8/I, controls strobing of data into this register. The device must supply strobe pulses for all data transfers out of the computer (programmed or data break) since circuit configuration and timing characteristics differ in each device.

When the data break request arrives, the computer completes the current instruction and generates an address accepted pulse as in input data break transfers. At TP4 time the address supplied to the PDP-8/I is loaded into the MA, the Break state is entered, and the MB is cleared. Not more than 450 ns after TP4 (at TP2 time), the content of the device-specified core memory address is read and available in the MB. (This word is automatically rewritten at the same address during the last half of the Break cycle and is available for programmed operations when the data break is finished.) Data bit signals are available as static levels of ground potential for binary 1s and -3V for binary 0s.

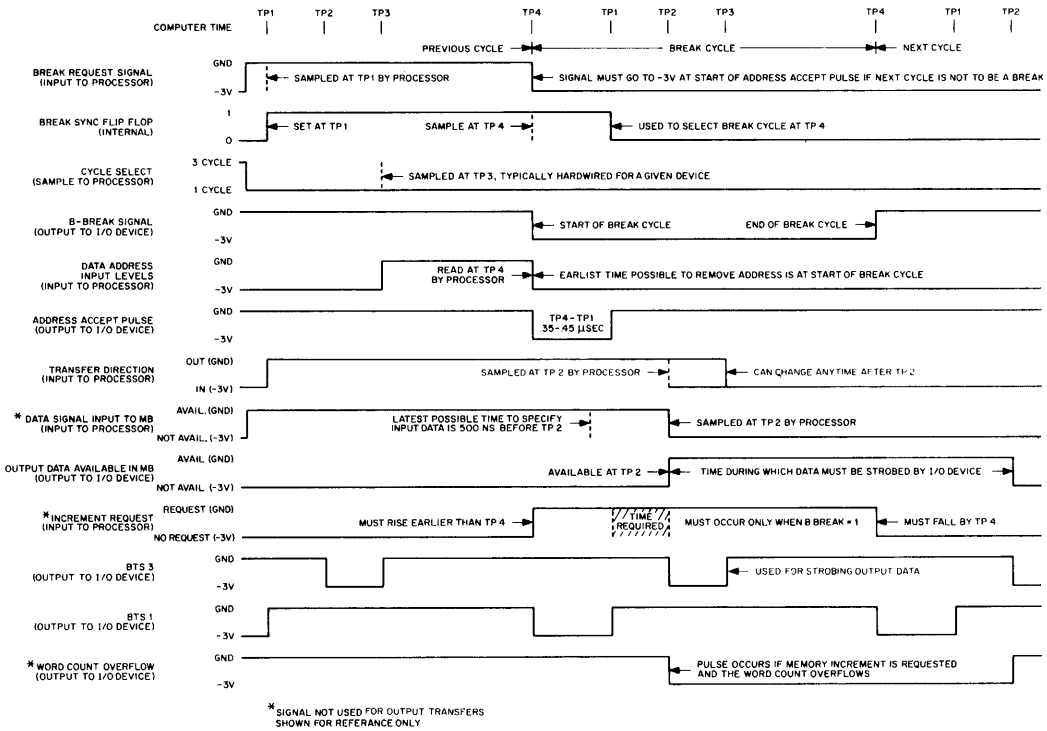


Figure 4 Single-Cycle Data Break Output Transfer Timing Diagram

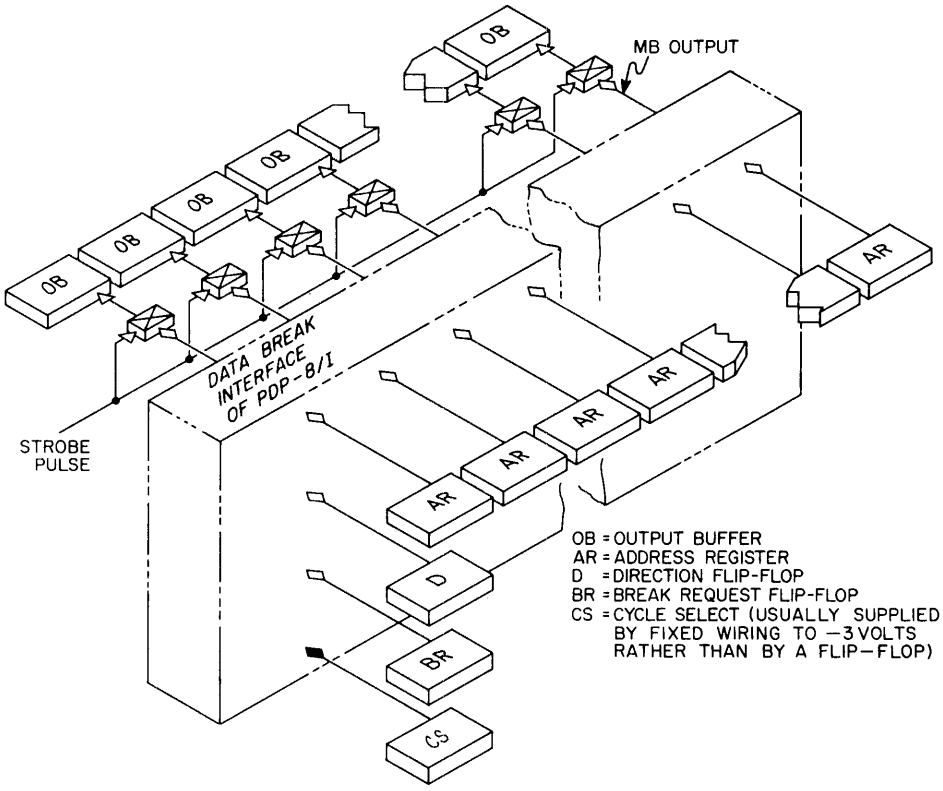


Figure 5 Device Interface Logic for Single-Cycle Data Break Output Transfer

The MB is cleared at TP2 time of each computer cycle, so the data word is available in the MB for approximately 1.5 μs to be strobed by the device interface.

Generation of the strobe pulse by the device interface can be synchronized with computer timing through use of timing pulses BTS1 or BTS3, which are available at the computer interface. In addition to a timing pulse (delayed or used directly from the computer), generation of this strobe pulse should be gated by condition signals that occur only during the Break cycle of an output transfer. Figure 6 shows typical logic circuits to effect an output data transfer. In this example, the B Break signal and an inverted transfer direction signal are combined in a diode NAND gate to condition a diode-capacitor-diode gate. A buffered BTS1 pulse triggers the DCD gate to produce the strobe pulse. The BTS1 pulse determines the timing of the transfer in this example, since the input of the output buffer register has DCD gates. Conventional DCD gates require a minimum setup time of 400 ns, which is adequately provided between the time when data is available in the MB and TS1 time.

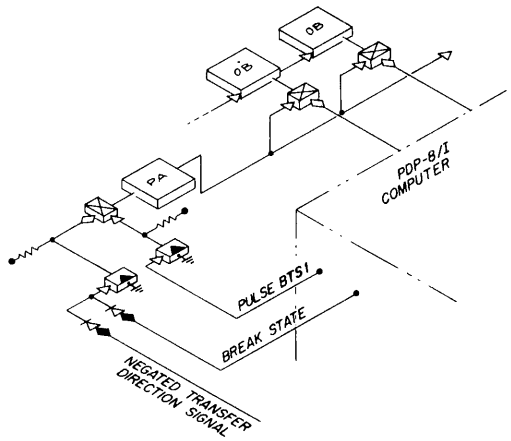


Figure 6 Device Interface for Strobing Output Data

By careful design of the input and output gating, one register can serve as both the input and the output buffer register. Most DEC options using the data break facility have only one data-buffer register with appropriate gating to allow it to serve as an output buffer when the transfer direction signal is at ground potential or as an input buffer when the transfer direction signal is -3V.

Memory Increment

In this type of data break, the content of core memory at a device-specified address is read into the MB, is incremented by one, and is rewritten at the same address within one 1.5 μs cycle. This feature is particularly useful in building a histogram of a series of measurements, such as in pulse-height analysis applications. For example, in a computer-controlled experiment that counts the number of times each value of a parameter is measured, a data break can be requested for each measurement, and the measured value can be used as the core memory address to be incremented (counted).

Signal interface for a memory increment data break is similar to an output transfer data break except that the device interface generates an increment MB signal and does not generate a strobe pulse (no data transfer occurs between the PDP-8/I and the device). Timing of memory increment operations appear in Figure 7, and an example of the logic circuits used by a device interface appears in Figure 8.

An interface for a device using memory increment data breaks must supply twelve data address signals, a transfer direction signal, a cycle select signal, and a break request signal to the computer data break facility as in an output transfer data break. In addition, a ground potential increment MB signal must be provided at least 250 ns before TP2 time of the Break cycle. This signal can be generated in the device interface by AND-combining the B break computer output signal, the output transfer condition of the transfer direction signal, and the condition signal in the device that indicates that an increment operation should take place. When the computer receives this increment MB signal,

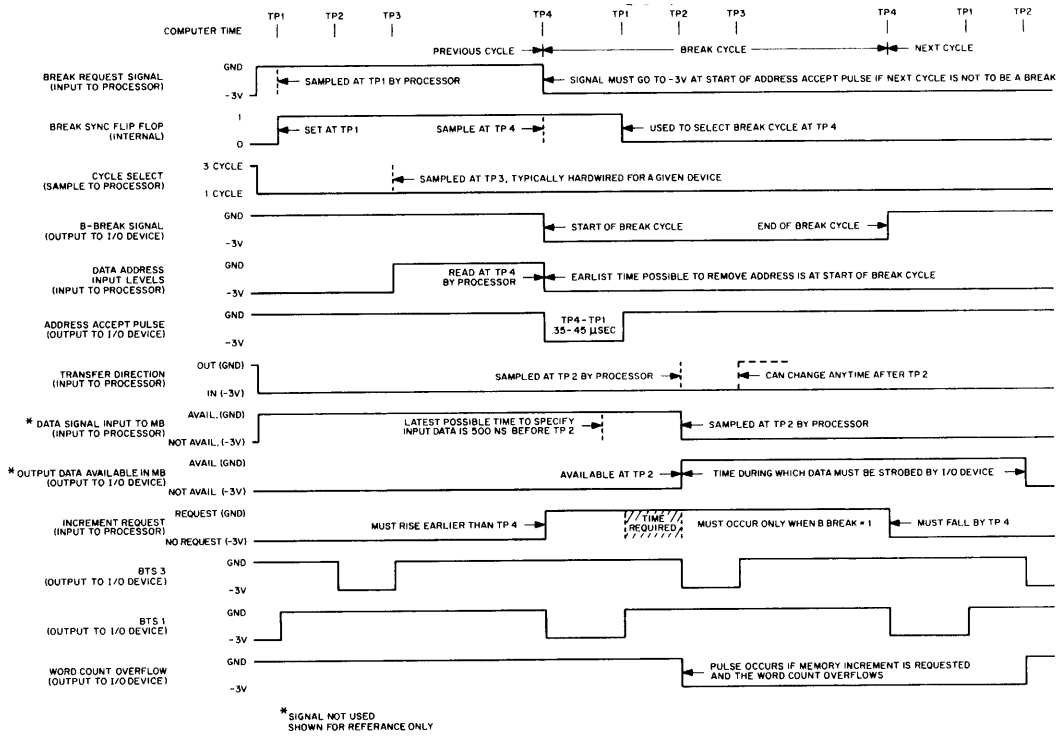


Figure 7 Memory Increment Data Break Timing Diagram

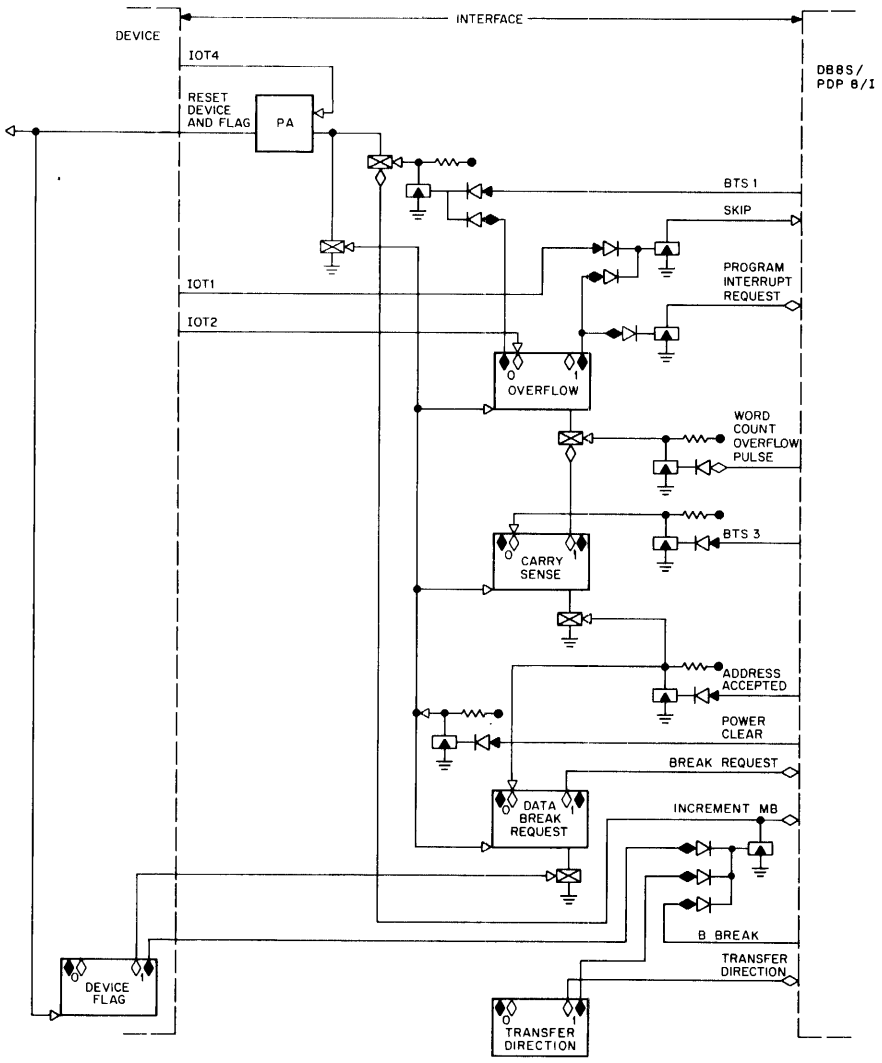


Figure 8 Device Interface Logic for Memory Increment Data Break

it forces the MB control element to generate a count MB pulse at TP2 time to increment the content of the MB.

The device interface logic shown in Figure 8, samples the word count overflow signal to determine if word count overflowed when the data word was incremented. If overflow occurs, this logic requests a program interrupt to allow the program to take some appropriate action, such as incrementing a core memory for numbers above 4096, stopping the test to compile the data gathered to the current point in the operation, reinitializing the addressing, etc. The logic in Figure 8 uses the select code of programmed data transfer operation to skip on the overflow condition to determine the cause of a program interrupt, to clear the overflow flip-flop, and to clear the device flag. Note that the devices that use data break transfers almost always use programmed data transfers to start and stop operation of the device, to initialize registers, etc., and do not rely on data break facilities alone to control their operations.

Three-Cycle Data Breaks

Timing of input or output three-cycle data breaks is shown in Figure 9. The three-cycle break uses the block transfer control circuits of the

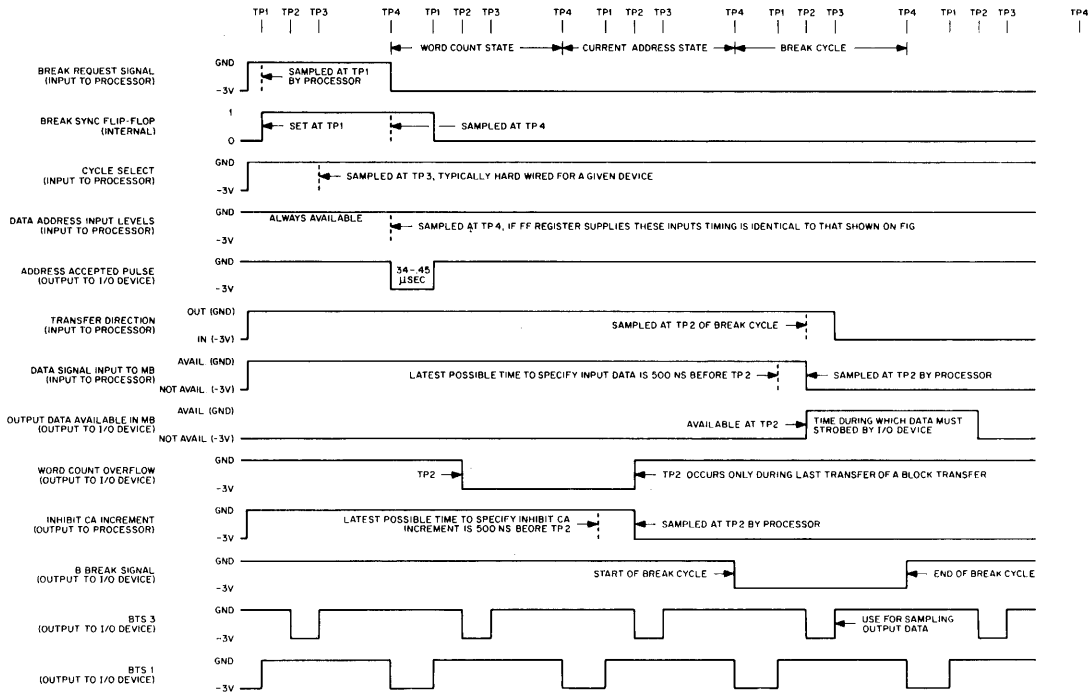


Figure 9 Three-Cycle Data Break Timing Diagram

computer. The block transfer control provides an economical method of controlling the flow of data at high speeds between PDP-8/I core memory and fast peripheral devices, e.g., drum disk, magnetic tape and line printers, allowing transfer rates in excess of 200 kc.

The three-cycle data break facility provides separate current address and word count registers in core memory for the connected device, thus eliminating the necessity for flip-flop registers in the device control. When several devices are connected to this facility, each is assigned a different set of core locations for word count and current address, allowing interlaced operations of all devices as long as their combined rate does not exceed 200 kc. The device specifies the location of these registers in core memory, thus the software remains the same regardless of other equipment that may be connected to the machine. Since these registers are located in standard memory, they may be loaded and unloaded directly without the use of IOT pulses. In a procedure where a device requests to transfer data to or from core memory, the three-cycle data break facility performs the following sequence of operations:

a. An address is read from the device to indicate the location of the word count register. This address is always the same for a given device; thus it can be wired in and does not require a flip-flop register.

b. The content of the specified address is read from memory and 1 is added to it before rewriting. If the content of this register becomes 0 as a result of the addition, a WC overflow pulse will be transmitted to the device. To transfer a block of N words, this register is loaded with -N during programmed initialization of the device. After the block has been fully transferred this pulse is generated to signify completion of the operation.

c. The next sequential location is read from memory as the current address register. Although the content of this register is normally

incremented before being rewritten, an increment CA inhibit (+1 → CA inhibit) signal from the device may inhibit incrementation. To transfer a block of data beginning at location A, this register is program initialized by loading with A-1.

d. The content of the previously read current address is transferred to the MA to serve as the address for the data transfer. This transfer may go in either direction in a manner identical to the single-cycle data break system.

The three-cycle data break facility uses many of the gates and transfer paths of the single-cycle data break system, but does not preclude the use of standard data break devices. Any combination of three-cycle and single-cycle data break devices can be used in one system, as long as a multiplexer channel is available for each. Two additional control lines are provided with the three-cycle data break. These are:

a. Word Count Overflow. A level change from GND to -3V, from TP2 to TP2, is transmitted to the device when the word count becomes equal to zero.

b. Increment CA Inhibit. When ground potential, this device-supplied signal inhibits incrementation of the current address word.

In summary, the three-cycle data break is entered similarly to the single-cycle data break, with the exception of supplying a ground-level cycle select signal to allow entry of the WC (Word Count) state to increment the fixed core-memory location containing the word count. The device requesting the break supplies this address as in the one-cycle data break, except that this address is fixed and can be supplied by wired ground and -3V signals, rather than from a register. The sole restriction on this address is that it must be an even number (bit 11 = 0). Following the WC state a CA (Current Address) state is entered in which the core memory location following the WC address (bit 11 = 1 after PC + 1 = >PC) is read, incremented by one, restored to memory, and used as the transfer address (by MB = >MA). Then the normal B (Break) state is entered to effect the transfer.

MC8/I MM8/I
EXTENDED MEMORY OPTION
FUNCTIONAL DESCRIPTION

MC8/I MM8/I EXTENDED MEMORY

INTRODUCTION

Additional capacity can be added to the standard PDP-8/I 4K core memory in 4096-word increments. The addition of seven 4K fields, plus the standard memory, yields the maximum storage capacity of 32,768 words. Figure 1 illustrates the extended-memory organization. As shown in this block diagram, the PDP-8/I main frame contains: the standard memory (field 0); and MC8/I which is the first memory extension (field 1) and the memory selection control (D-BS-MC8I-0-1) for all eight memory extensions.

Local memory timing for both field 0 and field 1 is provided by the basic memory.

MM8I's provide external memory expansion with common local memory timing control for every two 4096 word segments. This control, and associated read/write and addressing techniques (D-BS-MC8I-0-2 through 4), does not differ from that of the basic PDP-8/L as discussed in Chapter 4.

A discussion of extended memory control follows.

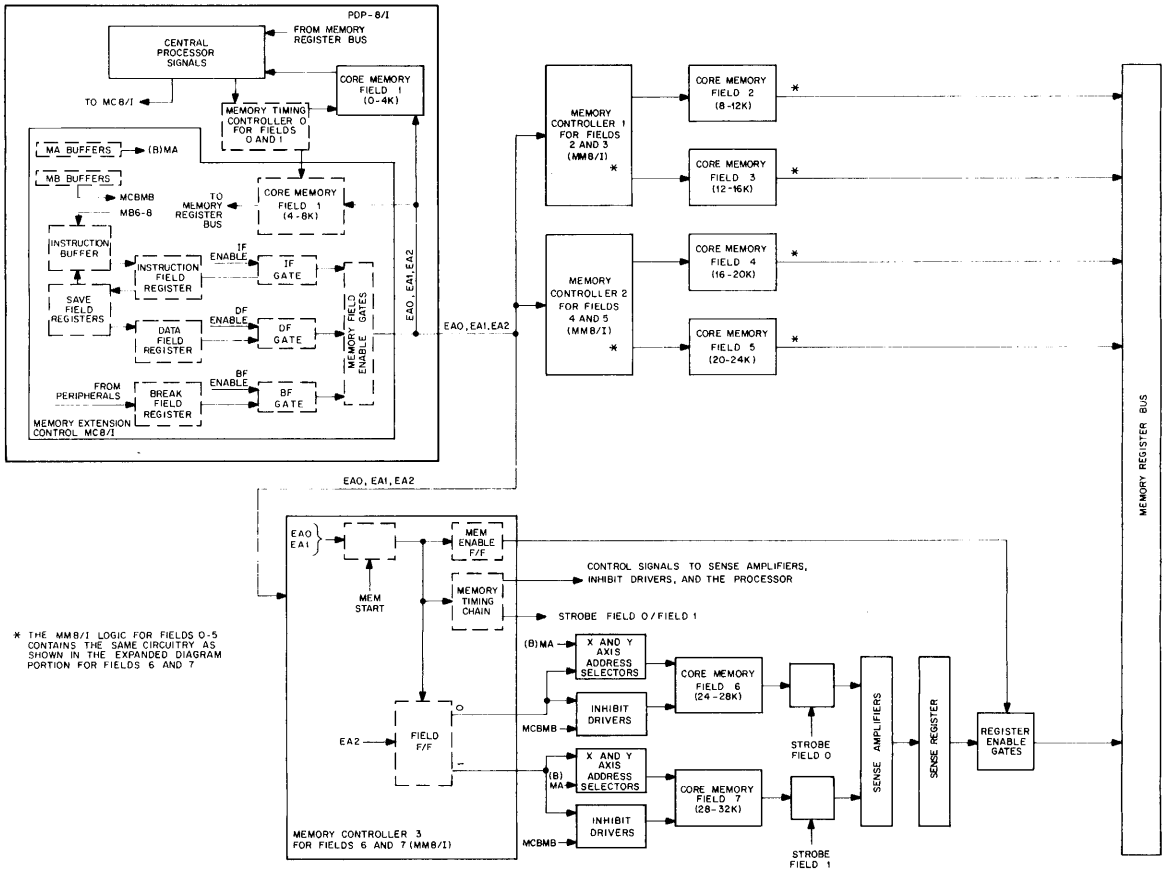


Figure 1 Extended Memory Block Diagram

LOGIC DESCRIPTION

Instruction Field Register

This 3-bit register determines the memory field to be used for storage and retrieval of program-instructions. The IF register may be loaded from either the IF switch register (IFSR) or the instruction buffer (IB) register. All program-executed transfers to the IF enter from the IB. The content of the IFSR, however, is loaded directly into the IF, and the IB, under manual control of the LOAD ADD key. When a JMP or JMS instruction is executed, the content of IB, is transferred to the IF.

When an interrupt occurs, the contents of the IF are transferred to the save field register (SF). At the end of the interrupt subroutine the contents of the SF are restored to the IF through the IB by execution of the RMF instruction.

When the CIF instruction is executed (refer to extended memory instruction descriptions in this chapter) the contents of MB06 through MB08 are transferred to the IB; the contents of the BI are transferred to the IF at the execution of a JMP or JMS instruction. During the time between the CIF instruction and the JMP or JMS, program interrupts are inhibited.

Data Field Register (DF)

This 3-bit register determines the field to be used for data storage and retrieval. The DF can be loaded from three discrete sources: MB06 through MB08, the Save Field, and the Data Field switch register (DFSR).

Initially, the DF is loaded manually from the DFSR by actuating LOAD ADD. While the program is running, a CDF (change data field) instruction can be used to alter the content of the DF to permit selection of a different field of memory. Bits 06, 07, and 08 of the CDF instruction contain the desired field address. Once loaded, the content of the DF remains unchanged until altered either manually by LOAD ADD through the DFSR, or under program control by a CDF instruction.

During a program-interrupt operation the content of the DF is automatically stored in the Save Field register and restored to the DF upon completion of the interrupt subroutine by the RMF instruction.

Instruction Buffer Register (IB)

This 3-bit register provides input buffering for data transfers made into IF under program control. Manual transfers from IFSR are made directly into IF and, simultaneously, into IB. This transfer of data into both registers is necessary to prevent inadvertent changing of the content of IF. (The output of IB is loaded into IF at the execution time of every JMP or JMS instruction.)

Transfers into IB are made under program control during the execution of CIF (change instruction field) and RMF (restore memory field) instructions. The content of IF, however, remains unchanged until the execution of the next JMS or JMP instruction strobes the output of IB into IF.

Save Field Register (SF)

This 6-bit register provides temporary storage, during a program interrupt, for the contents of both IF and DF. This is necessary to permit IF and DF to be cleared so the program interrupt subroutine starts in field 0. At the conclusion of the interrupt subroutine, an RMF instruction loads the contents of SF0-2 into IB for subsequent transfer into IF, and the content of SF3-5 into DF. The last instruction in the subroutine (JMP I 0) completes the transfer from IB to IF.

Break Field Register (BF)

This 3-bit register determines the field to be used for storage and retrieval for data transfers from I/O devices using the data break facility.

The BF is loaded from the EXT DATA ADD 0, 1, and 2 lines by TP3 of the cycle before a data break is initiated. Each device puts its own field address on the EXT DATA ADD 0, 1, and 2 when it requests a break.

Field Selection (EA0, EA1, EA2)

As Figure 1 illustrates, the MC8/I Memory Extension Control contains gating that allows access to all memory fields. The gate outputs EA0, EA1, and EA2 (drawing BS-MC8I-0-1; sheet 1), taken collectively, form a code that selects one of the memory fields. The EA0 and EA1 levels enable one of the four memory controllers (each of which controls two memories). The EA0 and EA1 configurations are: 00 (for fields 0 and 1), 01 (for fields 2 and 3), 10 (for fields 4 and 5) and 11 (for fields 6 and 7). The third enable level (EA2) specifies which of the two memory fields within the group indicated by EA0 and EA1 is selected. Table 1 clarifies the field select coding, and the distinction between the enable levels.

Table 1
Field Select Codes

EA0	EA1	Memory Controller Selected (EA0 and EA1)	EA2	Field Selected
0	0	0	0	0
0	0		1	1
0	1	1	0	2
0	1		1	3
1	0	2	0	4
1	0		1	5
1	1	3	0	6
1	1		1	7

The memory field enable gates may be activated from one of three sources: the IF register, the DF register, or the BF register. The IF register is gated to the EA0, EA1, and EA2 levels at all times except during a break cycle or an indirectly referenced data handling instruction. The data handling instructions are AND, TAD, ISZ, and DCA. In addition, when the Start, Exam, or Dep key is actuated, the IF register is gated to EA0, EA1, and EA2 to generate the memory field select code. The DF register is gated to the extended addressing bits when any indirectly-addressed memory-reference instruction other than JMP or JMS is executed (AND, TAD, ISZ or DCA). The BF decoder allows the BF to generate the memory field select code during a break cycle.

Interrupt Inhibit

The interrupt inhibit (drawing BS-MC8I-0-1; sheet 2) logic disables the INT OK (drawing BS-8I-0-7) level in the processor from the time a CIF instruction is decoded, until a JMP or JMS command finishes the CIF command. This prevents honoring of an interrupt before the field is changed. Interrupt synchronization is restored after the IF is loaded from the IB, allowing further program interrupts to occur.

EXTENDED MEMORY INSTRUCTION DESCRIPTIONS

The following paragraphs describe the instruction set necessary to control program execution with the extended memory option.

Change Data Field (CDF)

This instruction contains the octal code 62N1, where N is the octal number of the field to which control is changing. The CDF command is used prior to storing or retrieving data with any indirectly-addressed memory-reference instruction other than JMP or JMS. This instruction is generated by combining the MEM EXT level (62), the contents of MB06 through MB08 (N), and MB11 (1), with the EXT GO signal (drawing BS-MC8I-0-1, sheet 2).

Change Instruction Field (CIF)

This instruction contains the octal code 62N2, where N is the octal number of the field to

which the program is changing. The CIF command is executed prior to a JMP or JMS instruction. The 62N2 instruction allows MB06 through MB08(N) to be loaded into the IB by combining these bits with MEM EXT (62), and MB10 (Drawing BS-MC8I-0-1, sheet 2). The IB is loaded by EXT GO and the conditions MB09 = 0, MB10 = 1, MB11 = 0. The IB is then transferred to the IF when the next JMP or JMS command is executed.

Restore Memory Field (RMF)

This instruction (octal code 6244) restores the contents of the SF to the DF and IB registers. The conclusion of an interrupt subroutine (JMP I 0) loads the IF from the IB. SF ENABLE (Drawing BS-MC8I-0-1, sheet 2) allows bits SF3 through SF5 to be loaded into the DF. The contents of the IB are transferred to the IF by executing a JMP or JMS instruction.

Read Interrupt Buffer (RIB)

The purpose of this instruction is to allow storing that same field in memory if the power failure option is installed. This instruction (octal code 6234) reads the contents of the 6-bit SF register into the AC on the $\overline{ME}$6 through $\overline{ME11}$ lines (Drawing BS-MC8I-0-1, sheet 2). These lines activate the INPUT BUS 06 through 11 lines in the processor.

Execution of the RIB command generates $\overline{MEM\ EXT\ I/O\ ENABLE}$ (Drawing BS-MC8I-0-1, sheet 2), and MEM EXT AC LOAD ENABLE which produce AC LOAD and IO ENABLE in the processor. IO ENABLE allows INPUT BUS 6 through 11 lines to load into the AC when AC LOAD is generated.

Read Data Field (RDF)

This instruction (octal code 6214) reads the contents of DF0 through DF2 onto the ME6 through ME8 lines. The data is transferred to accumulator bits AC06 through AC08 in the same manner as with the RIB instruction.

Read Instruction Field (RIF)

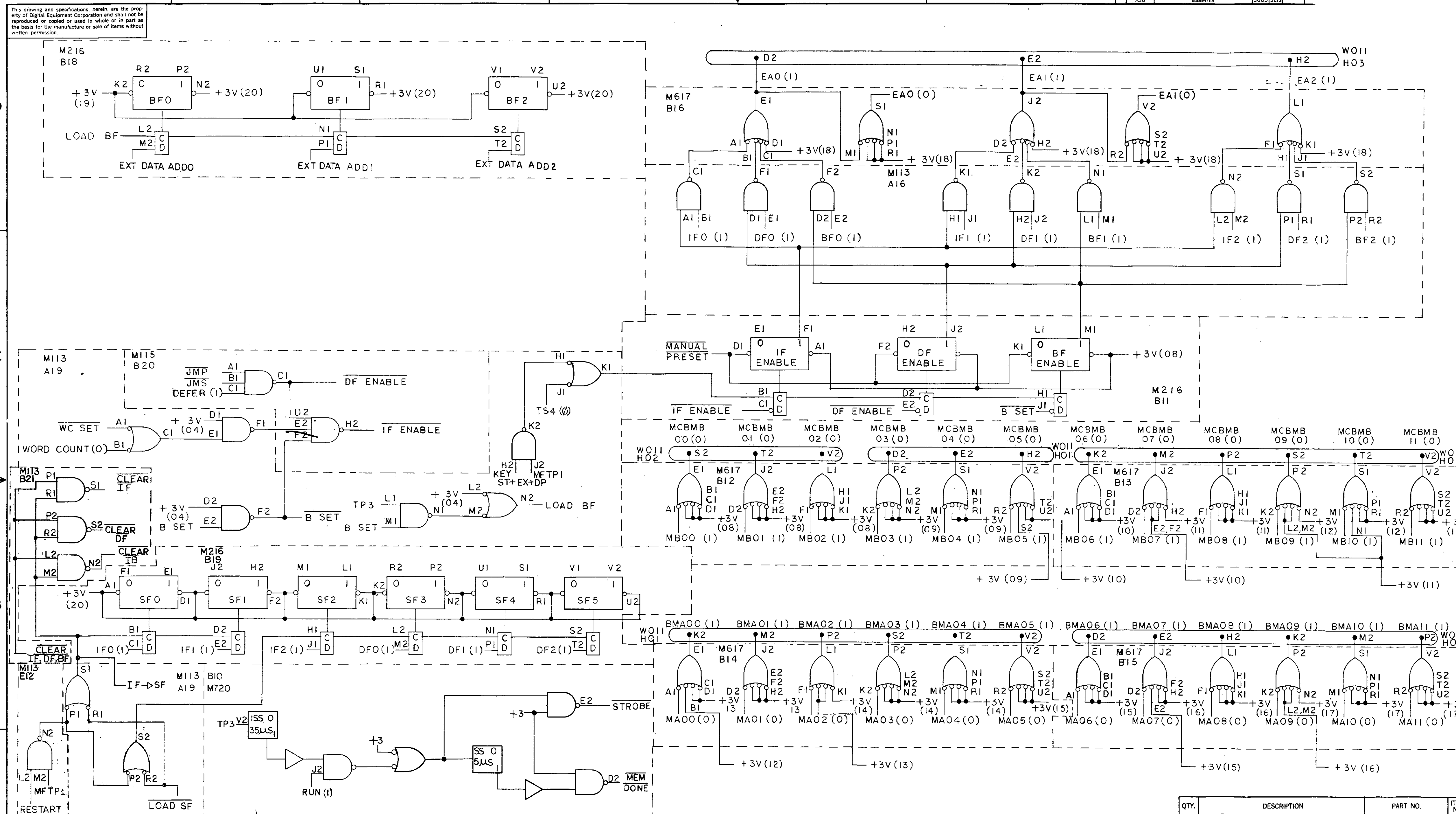
This instruction (octal code 6224) reads the contents of IF0 through IF2 onto the $\overline{ME}$9 through $\overline{ME11}$ lines. The data is transferred through the INPUT BUS 06 through 08 to bits AC06 through AC08 in the same manner as with the RIB and RDF instructions.

ENGINEERING DRAWINGS

The following drawings pertaining to the MC8/I, MM8/I are included in this section.

Drawing Number	Title	Revision
D-BS-MC8I-0-1	Memory Extension Control	S
D-BS-MC8I-0-2	Inhibit Drivers	C
D-BS-MC8I-0-3	X Axis Selection	C
D-BS-MC8I-0-4	Y Axis Selection	C
D-MU-MM8I-0-1	Not Available	B
D-BS-MM8I-A-1	Memory Control	M
D-BS-MM8I-A-2	Sense Amplifiers and Inhibit Drivers	C
D-BS-MM8I-A-3	X Axis Selection, Field 0	B
D-BS-MM8I-A-4	Y Axis Selection, Field 0	D
D-BS-MM8I-B-1	Inhibit Drivers, Field 1	C
D-BS-MM8I-B-2	X Axis Selection, Field 1	B
D-BS-MM8I-B-3	Y Axis Selection, Field 1	B
B-CS-G020-0-1	Sense Amplifier	H
B-CS-G021-0-1	Sense Amplifier	H
B-CS-G221-0-1	Memory Selector	D
B-CS-G228-0-1	Inhibit Driver	E
B-CS-G229-0-1	Not Available	-
B-CS-G624-0-1	Resistor Board	D
B-CS-G805-0-1	Negative Regulator	F

Drawing Number	Title	Revision
C-CS-G826-0-1	Regulator Control	L
B-CS-M113-0-1	10 2-Input NAND Gates	C
B-CS-M115-0-1	8 3-Input NAND Gates	C
B-CS-M216-0-1	Six Flip-Flops	B
B-CS-M310-0-1	Delay Line	D
B-CS-M360-0-1	Variable Delay	B
B-CS-M617-0-1	6 4-Input NOR Buffers	B
B-CS-M720-0-1	Memory Detection	A


M216
B18
BF0
BF1
BF2
LOAD BF
EXT DATA ADD0
EXT DATA ADD1
EXT DATA ADD2
M617
B16
EA0 (1)
EA0 (0)
EA1 (1)
EA1 (0)
EA2 (1)
M113
A16
IF0 (1)
DF0 (1)
BF0 (1)
IF1 (1)
DF1 (1)
BF1 (1)
IF2 (1)
DF2 (1)
BF2 (1)
W011
H03
MANUAL PRESET
IF ENABLE
DF ENABLE
BF ENABLE
B SET
M216
B11
M113
A19
M115
B20
JMP
JMS
DEFER (1)
WC SET
WORD COUNT (0)
TS4
KEY ST+EX+DP
MFTP1
CLEAR IF
CLEAR DF
CLEAR IB
LOAD BF
M216
B19
SF0
SF1
SF2
SF3
SF4
SF5
CLEAR IF, DF, BF
IF→SF
M113
B10
M720
TP3
ISS 0 35μS
SS 0 5μS
RUN (1)
STROBE
MEM DONE
RESTART
LOAD SF
MCBMB 00 (0)
MCBMB 01 (0)
MCBMB 02 (0)
MCBMB 03 (0)
MCBMB 04 (0)
MCBMB 05 (0)
MCBMB 06 (0)
MCBMB 07 (0)
MCBMB 08 (0)
MCBMB 09 (0)
MCBMB 10 (0)
MCBMB 11 (0)
W011 H02
W011 H01
M617 B12
M617 B13
MB00 (1)
MB01 (1)
MB02 (1)
MB03 (1)
MB04 (1)
MB05 (1)
MB06 (1)
MB07 (1)
MB08 (1)
MB09 (1)
MB10 (1)
MB11 (1)
BMA00 (1)
BMA01 (1)
BMA02 (1)
BMA03 (1)
BMA04 (1)
BMA05 (1)
BMA06 (1)
BMA07 (1)
BMA08 (1)
BMA09 (1)
BMA10 (1)
BMA11 (1)
W011 HG1
M617 B14
M617 B15
MA00 (0)
MA01 (0)
MA02 (0)
MA03 (0)
MA04 (0)
MA05 (0)
MA06 (0)
MA07 (0)
MA08 (0)
MA09 (0)
MA10 (0)
MA11 (0)

NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS, PER DEC. STD 054

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

		DATE
DRN.	R. E. Bernier	1 MAR 67
CHK'D.		9-21-67
ENG.	E. de Castro	10-10-67
PROJ. ENG.	E. de Castro	10-1-67
PROD.		8-21-67

FIRST USED ON E-UA-8I-0-0

SCALE
SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
MEMORY EXTENSION CONTROL

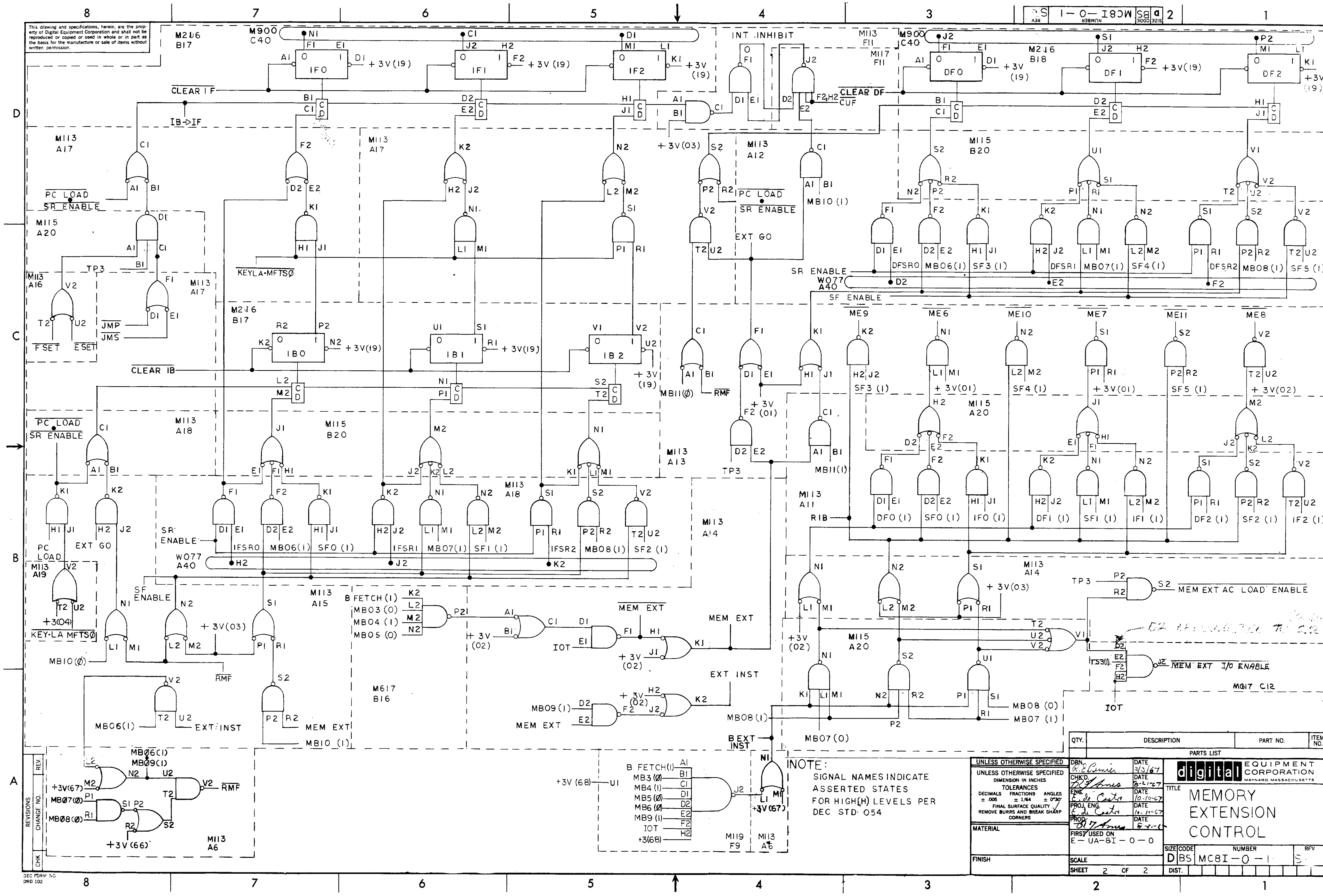
SIZE D CODE BS NUMBER MC8I-0-1 REV S

DIST.

REVISIONS

FORM NO 102

I-EM7


MEMORY EXTENSION CONTROL
NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH(H) LEVELS PER DEC STD 054
DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
FIRST USED ON
E - UA-8I - 0 - 0
D BS MC8I - 0 - 1
SHEET 2 OF 2
PARTS LIST
QTY. DESCRIPTION PART NO. ITEM NO.
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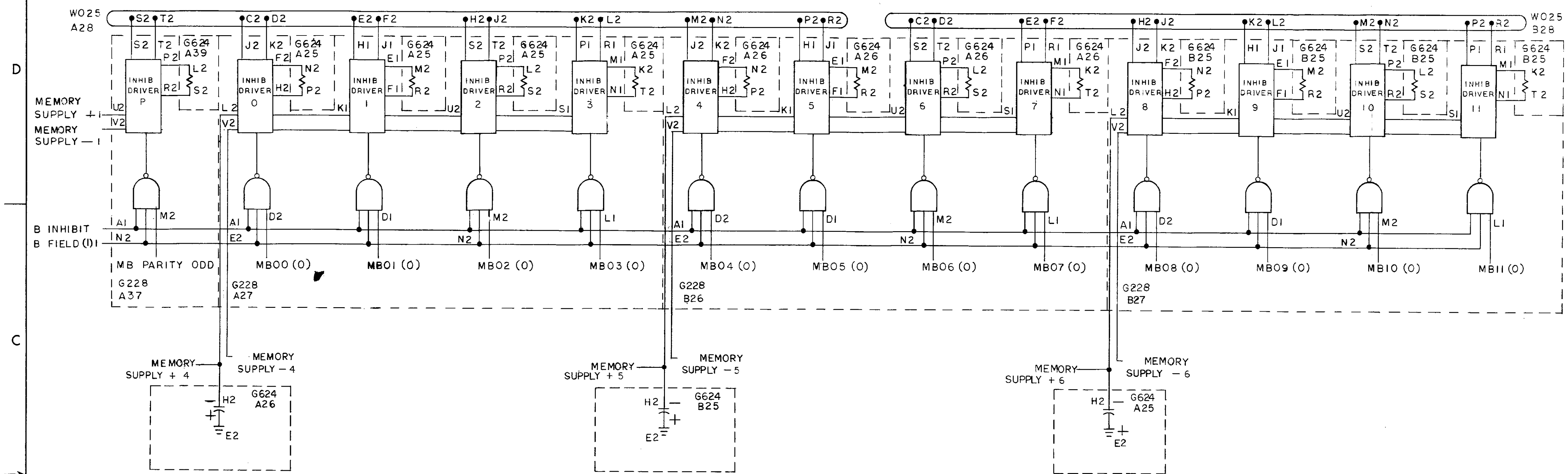
CLEAR IF
IB→IF
INT. INHIBIT
CLEAR DF
CUF
CLEAR IB
PC LOAD
SR ENABLE
KEY-LA MFTSØ
JMP
JMS
F SET
E SET
EXT GO
SF ENABLE
W077 A40
RMF
MEM EXT
EXT INST
IOT
B FETCH (1)
MEM EXT AC LOAD ENABLE
MEM EXT I/O ENABLE
IF0
IF1
IF2
DF0
DF1
DF2
IB0
IB1
IB2
ME9
ME6
ME10
ME7
ME11
ME8



NOTES:
1. DRAWING DEPICTS MC8I-B
2. FOR MC8I-A REMOVE G228 IN LOCATION A37
3. SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054

REV.	CHANGE NO.	CHK
A	ECO #4	
B	EC-0002	
C	8I-00015	

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

DRN: R. Bernier DATE 2/8/67
CHK'D DATE 8-1-67
ENG. DATE 10-10-67
PROJ. ENG. DATE 10-10-67
PROD. DATE 8-21-67
FIRST USED ON E-UA-8I-0-0

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
INHIBIT DRIVERS

SIZE	CODE	NUMBER	REV
D	BS	MC8I-0-2	C

SCALE
SHEET 1 OF 1
DIST.

DEC FORM NO DRD 102

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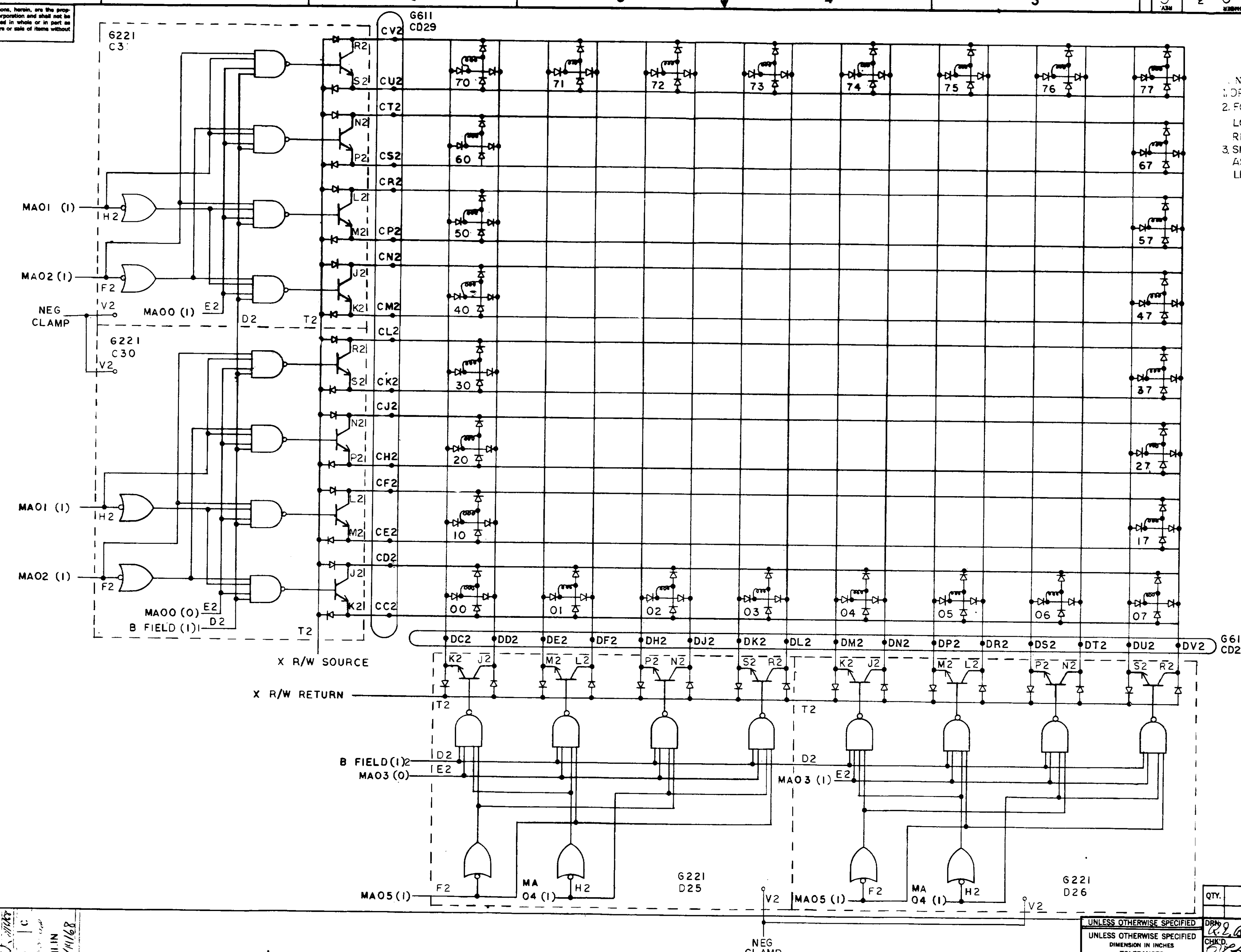

NOTES:

1. DRAWING DEPICTS MC8[illegible]-A
2. FOR MC8[illegible]-B, G6[illegible] IN LOCATION CD29 IS REPLACED WITH A G612
3. SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. R. E. Berner DATE 2/7/67
CHK'D. DATE 9-21-67
ENG. E. de Castro DATE 10-10-67
PROJ. ENG. E. de Castro DATE 10-10-67
PROD. DATE 8-2-67
FIRST USED ON E—UA—8I—0—0
SCALE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
X AXIS SELECTION

SIZE D CODE BS NUMBER MC8I-0-3 REV. C

DEC FORM NO DRD 102

I-EM13

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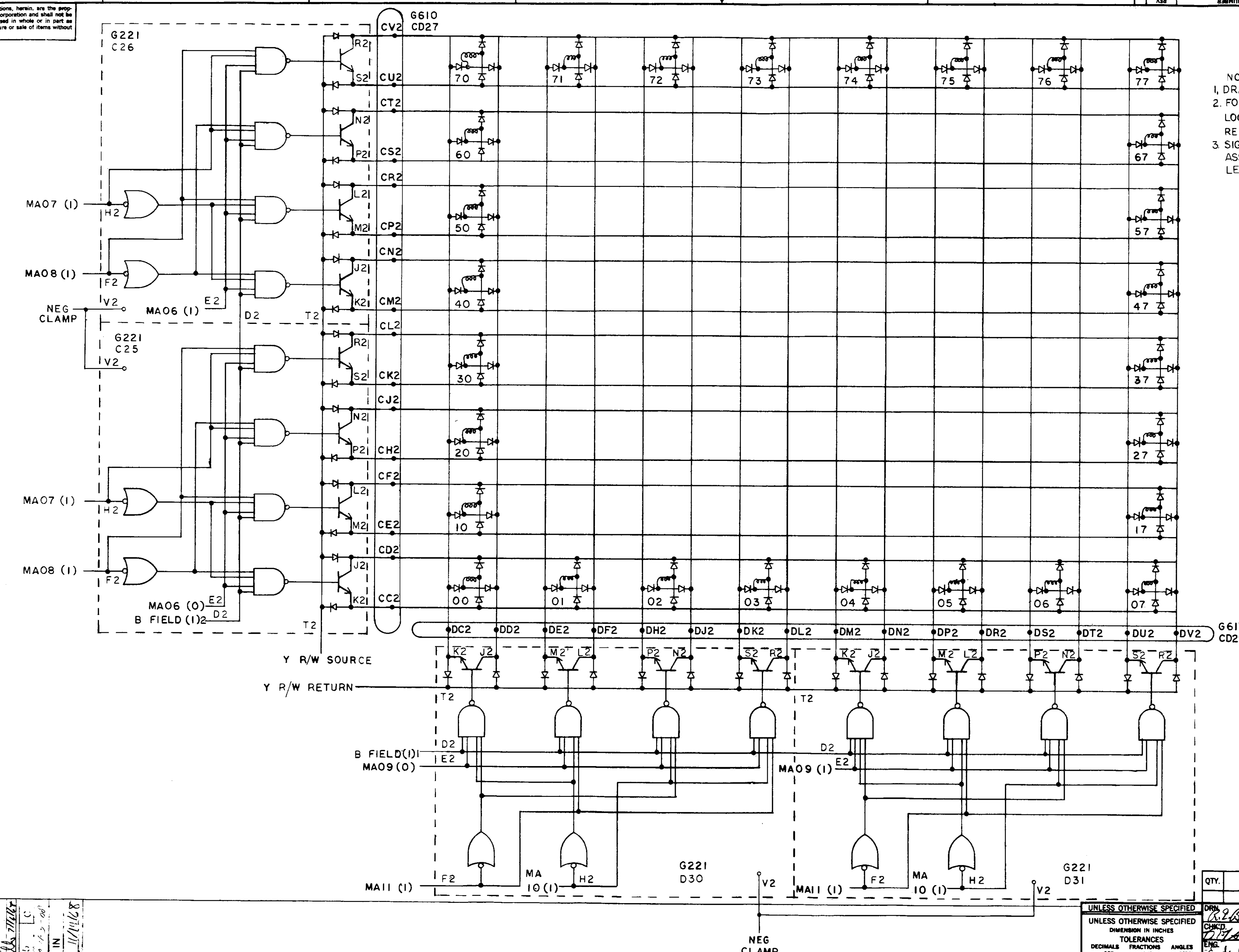


NOTES:
1. DRAWING DEPICTS MC8I-A
2. FOR MC8I-B, G6II IN LOCATION CD29'S REPLACED WITH A G612
3. SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. R.E. Berner DATE 2/1/67
CHKD. DATE 8-21-67
ENG. E. de Castro DATE 10-11-67
PROJ. ENG. E. de Castro DATE 10-10-67
PROD. DATE 8-21-67
FIRST USED ON E-UA-8I-0-0

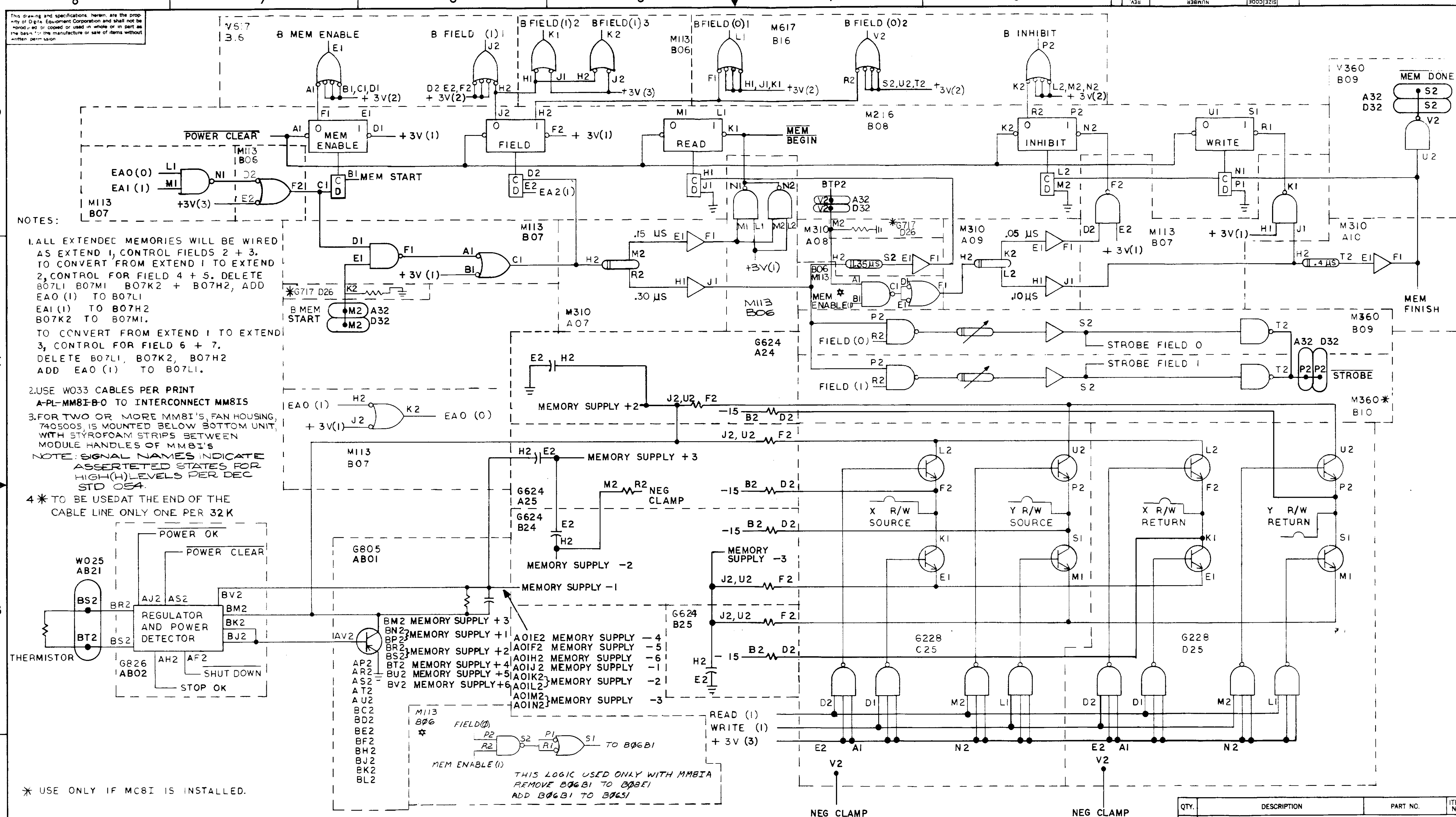
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
Y AXIS SELECTION

SIZE D CODE BS NUMBER MC8I-0-4 REV. C
SCALE
SHEET 1 OF 1
DIST.

REVISIONS: REV. A, B, C — CHANGE NO. E.C.O. #4 ...

DEC FORM NO DRO 102



NOTES:

1. ALL EXTENDEC MEMORIES WILL BE WIRED AS EXTEND 1, CONTROL FIELDS 2 + 3.
TO CONVERT FROM EXTEND 1 TO EXTEND 2, CONTROL FOR FIELD 4 + 5. DELETE B07L1 B07M1 B07K2 + B07H2, ADD
EA0 (1) TO B07L1
EA1 (1) TO B07H2
B07K2 TO B07M1.
TO CONVERT FROM EXTEND 1 TO EXTEND 3, CONTROL FOR FIELD 6 + 7.
DELETE B07L1, B07K2, B07H2
ADD EA0 (1) TO B07L1.
2. USE W033 CABLES PER PRINT A-PL-MM8I-B-0 TO INTERCONNECT MM8IS
3. FOR TWO OR MORE MM8I'S, FAN HOUSING, 7405005, IS MOUNTED BELOW BOTTOM UNIT, WITH STYROFOAM STRIPS BETWEEN MODULE HANDLES OF MM8I'S

NOTE: SIGNAL NAMES INDICATE ASSERTETED STATES FOR HIGH(H) LEVELS PER DEC STD 054.

4 ✳ TO BE USEDAT THE END OF THE CABLE LINE ONLY ONE PER 32K

✳ USE ONLY IF MC8I IS INSTALLED.

REV.	CHANGE NO.
A	8
B	
C	18
D	MM8I 00002
E	MM8IA-00004
F	00006
H	MM8I-00007
J	MM8IA 00008
K	00011
L	00012
M	MM8IA-00013

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

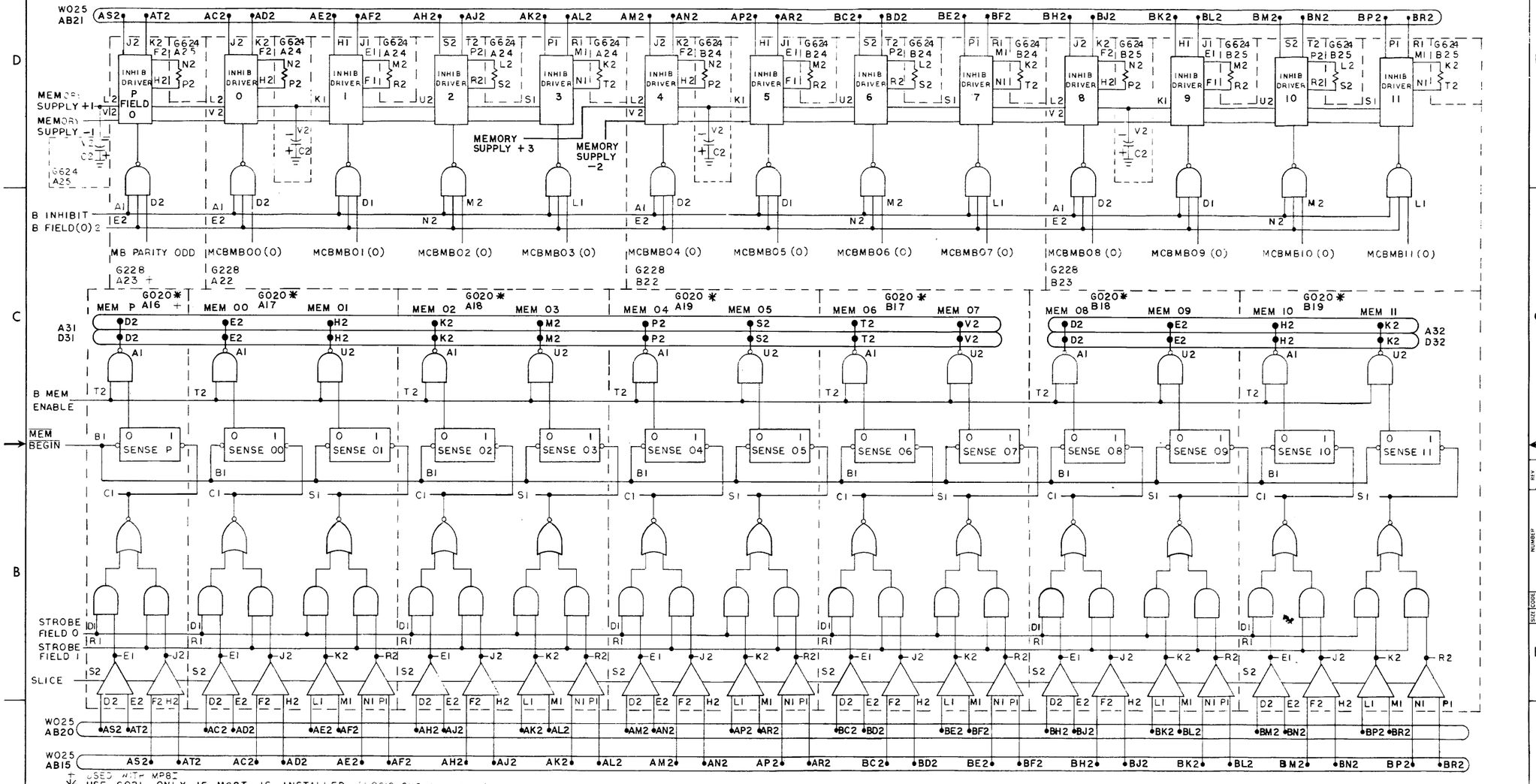
DRN DATE 10/3/67
CHK'D. DATE 11-22-67
ENG. DATE 11-29-67
PROJ. ENG. DATE 11-29-67
PROD. DATE 11-29-67
FIRST USED ON C-UA-MM8I -0-0
SCALE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
MEMORY CONTROL

SIZE D CODE BS NUMBER MM8I — A — 1 REV. M

DEC FORM NO DRD 102



NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH(H) LEVELS PER DEC STD 054

REVISIONS	REV	CHK	CHANGE NO
	A		
	B		
	C		
	D		

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY / REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

DRN		DATE 11-7-67
CHK'D		DATE 11-22-67
ENG		DATE 11-1-67
PROJ. ENG.		DATE 11-15-67
PROD.		DATE 11-25-67

FIRST USED ON: C-UA-MM8I-0-0
SCALE
SHEET 1 OF 1

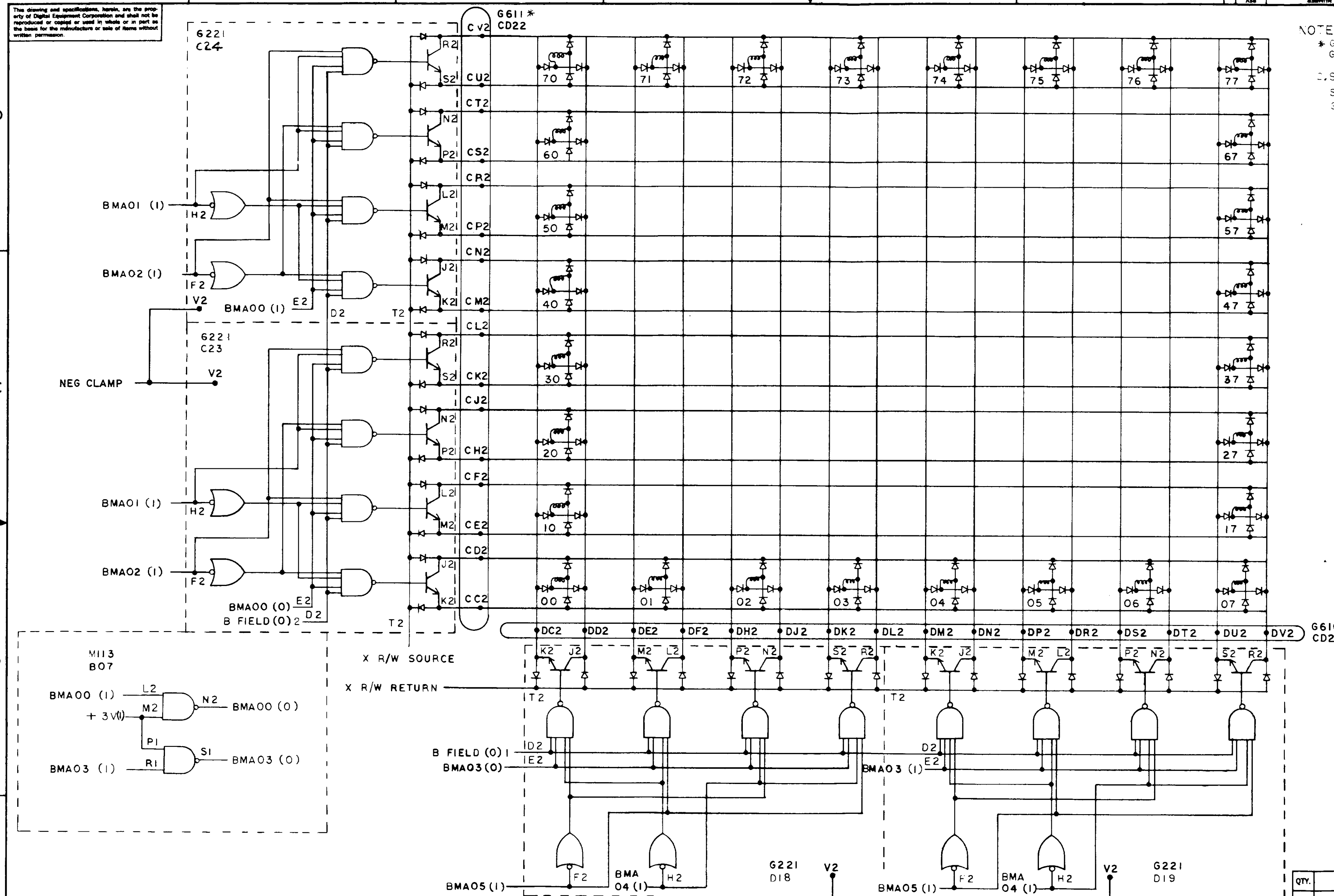
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: SENSE AMPS & INHIBIT DRIVERS

SIZE	CODE	NUMBER	REV.
D	BS	MM8I-A-2	E

DIST.

DEC FORM NO DRD 102



NOTE

* G6 ... LOCATION CD22 REPLACE WITH G6 2 IF MP8I IS INSTALLED.

2. SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 034

NEG CLAMP

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DIGITAL EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE
X AXIS SELECTION FIELD 0

FIRST USED ON C-UA-MM8I -0-0

SIZE D CODE BS NUMBER MM8I — A — 3 REV.

SHEET 1 OF 1

DEC FORM NO DRD 102

G610 CD20

G221 C19

A32 D32 — T2 T2 — MB PARITY ODD

BMA07 (1) — H2

BMA08 (1) — F2

BMA06 (1) E2 D2 T2

V2

6221 C18

NEG CLAMP — V2

BMA07 (1) — H2

BMA08 (1) — F2

BMA06 (0) E2 D2 T2

B FIELD(0) I

Y R/W SOURCE

Y R/W RETURN

CV2 CU2 CT2 CS2 CR2 CP2 CN2 CM2 CL2 CK2 CJ2 CH2 CF2 CE2 CD2 CC2

70 71 72 73 74 75 76 77
60 67
50 57
40 47
30 37
20 27
10 17
00 01 02 03 04 05 06 07

DC2 DD2 DE2 DF2 DH2 DJ2 DK2 DL2 DM2 DN2 DP2 DR2 DS2 DT2 DU2 DV2

G611 * CD22

M113 B07

BMA 06 (1) — P2 R2 + 3V(1) — S2 — BMA 06 (0)

BMA 09 (1) — T2 U2 — V2 — BMA 09 (0)

NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH(H) LEVELS PER DEC STD 054

B FIELD(0) I D2 E2 — BMA09 (0)

BMA09 (1) D2 E2

BMA11 (1) — F2 — BMA 10 (1) H2

G221 D23 — V2 — NEG CLAMP

BMA11 (1) — F2 — BMA 10 (1) H2

V2 — G221 D24

A28 D28
- D2 D2 — MCBMB 03 (0)
- E2 E2 — MCBMB 04 (0)
- H2 H2 — MCBMB 05 (0)
- K2 K2 — BMA 00 (1)
- M2 M2 — BMA 01 (1)
- P2 P2 — BMA 02 (1)
- S2 S2 — BMA 03 (1)
- T2 T2 — BMA 04 (1)
- V2 V2 — BMA 05 (1)

A29 D29
- D2 D2 — BMA 06 (1)
- E2 E2 — BMA 07 (1)
- H2 H2 — BMA 08 (1)
- K2 K2 — BMA 09 (1)
- M2 M2 — BMA 10 (1)
- P2 P2 — BMA 11 (1)
- S2 S2 — MCBMB 00 (0)
- T2 T2 — MCBMB 01 (0)
- V2 V2 — MCBMB02 (0)

A30 D30
- D2 D2 — EA0 (1)
- E2 E2 — EA1 (1)
- H2 H2 — EA2 (1)
- K2 K2 — MCBMB 06 (0)
- M2 M2 — MCBMB 07 (0)
- P2 P2 — MCBMB 08 (0)
- S2 S2 — MCBMB 09 (0)
- T2 T2 — MCBMB 10 (0)
- V2 V2 — MCBMB 11(0)

NOTE
* C61 IN LOCATION G022 REPLACE WITH G612 IF MP8I IS INSTALLED

REVISIONS	REV	CHK	CHANGE NO
	A		00006

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

		DATE
DSN		1-22-67
CHK'D		1-22-67
ENG		1-24-67
PROJ ENG		1-24-67
PROD		1-24-67

FIRST USED ON C-UA-MM8I-0-0

SCALE

SHEET 1 OF 1

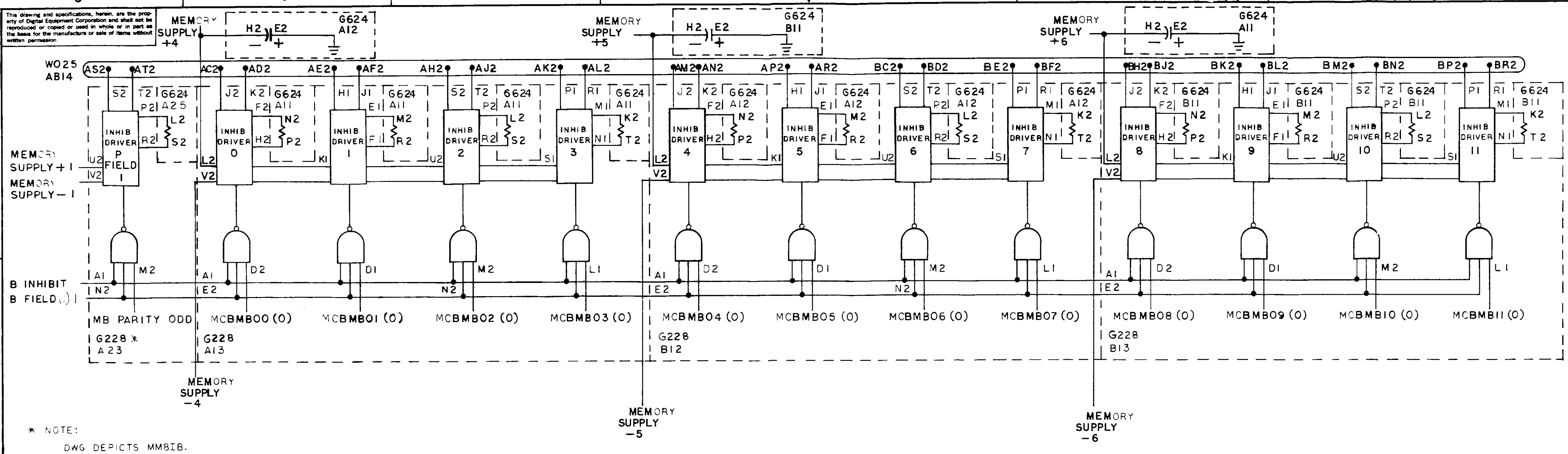
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
Y AXIS SELECTION FIELD 0

SIZE	CODE	NUMBER	REV.
D	BS	MM8I — A —4	D

DIST.

DEC FORM NO DRD 102



* NOTE:

DWG DEPICTS MM8IB.
FOR MM8IB WITHOUT PARITY
REMOVE G228 IN LOCATION A23.

SIGNAL NAMES INDICATE
ASSERTED STATES FOR
HIGH (H) LEVELS PER DEC
STD 054

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: INHIBIT DRIVERS FIELD 1

FIRST USED ON: C-UA-MM8I-0-0

SIZE D CODE BS NUMBER MM8I — B — REV C

SHEET 1 OF 1

I-EM25

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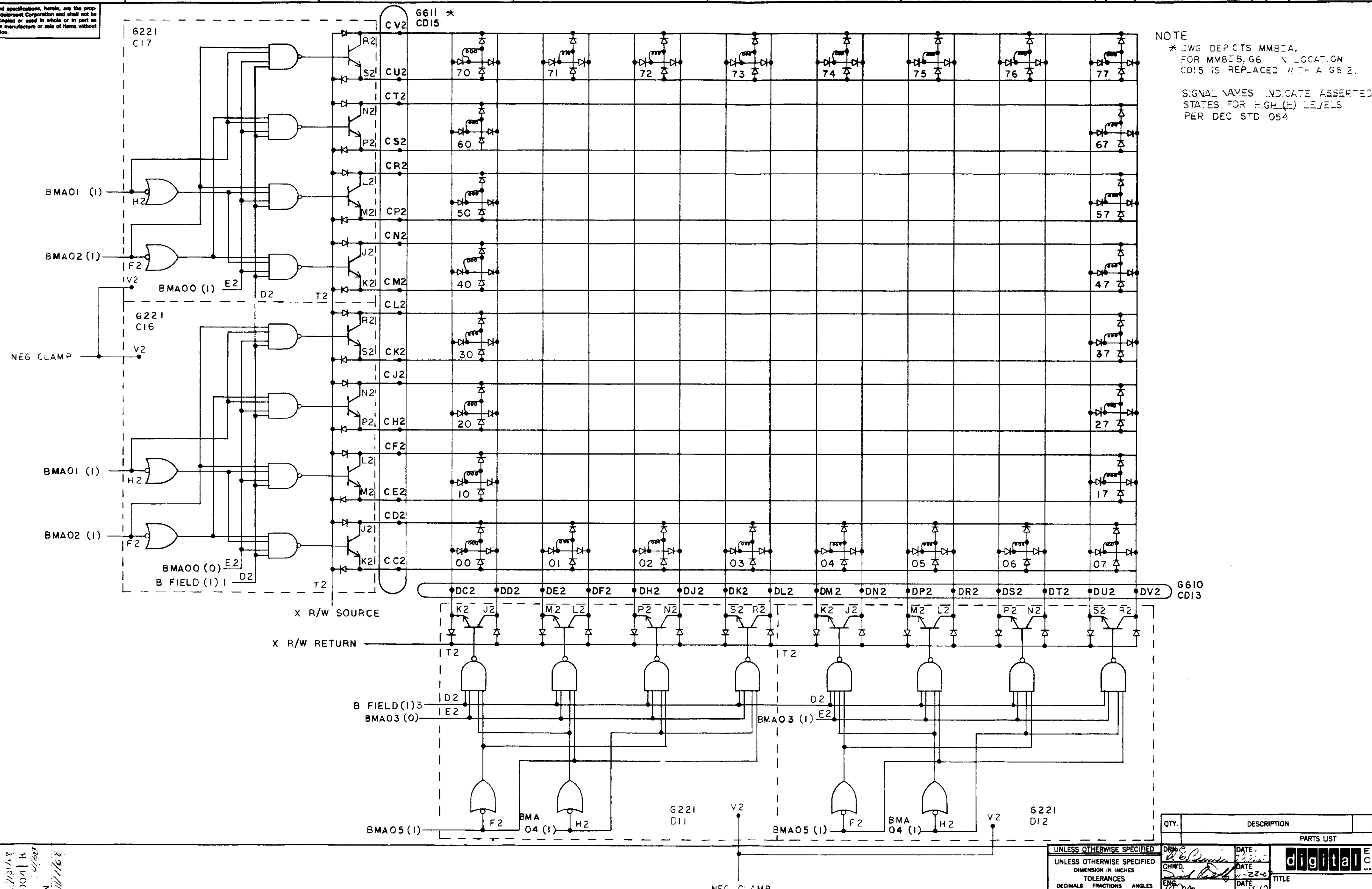


NOTE
* DWG DEPICTS MM8IA.
FOR MM8IB, G611 IN LOCATION CD15 IS REPLACED WITH A G612.

SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054

REV	CHANGE NO	CHK
A	MM8I 00001 7-30-68	
B	MM8IA 00001 11/16/68	

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

FIRST USED ON C-UA-MM8I-0-0

SCALE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

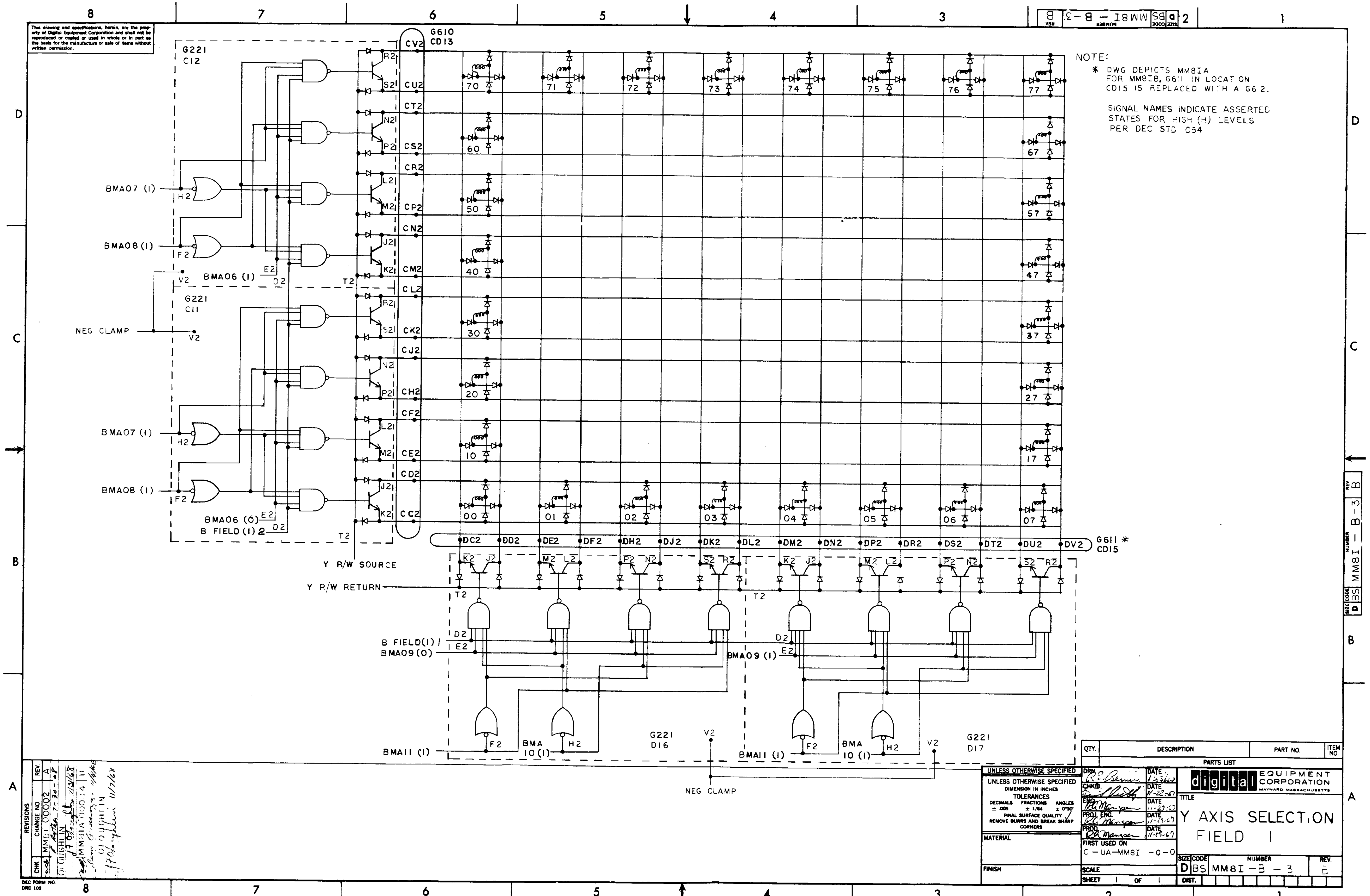
TITLE
X AXIS SELECTION
FIELD 1

SIZE D CODE BS NUMBER MM8I — B — 2 REV. B

QTY. | DESCRIPTION | PART NO. | ITEM NO.
PARTS LIST

DEC FORM NO DRO 02

I-EM27



QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

FIRST USED ON C-UA-MM8I-0-0

digital EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS

TITLE: Y AXIS SELECTION FIELD 1

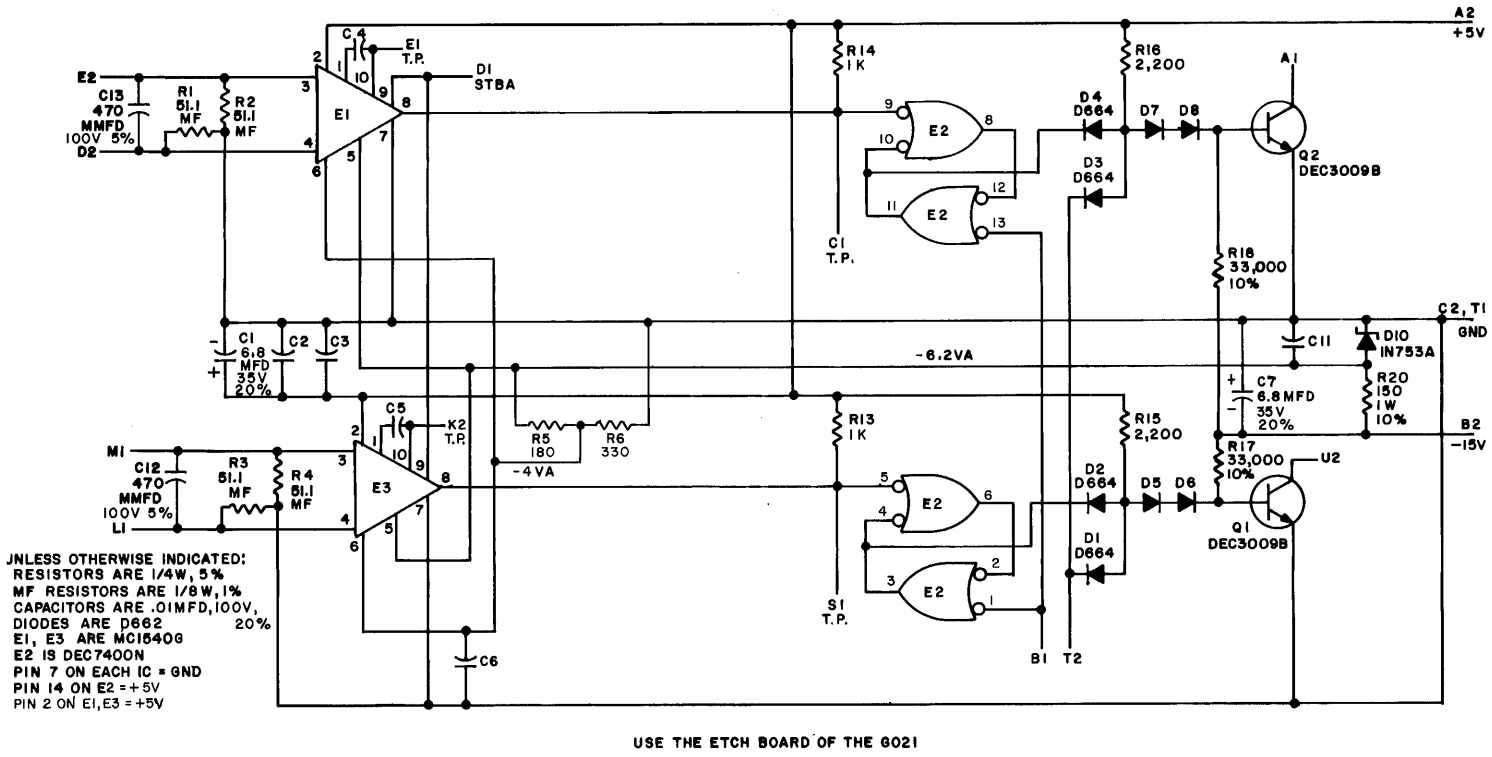
SIZE D CODE BS NUMBER MM8I-B-3 REV. B

SCALE

SHEET 1 OF 1

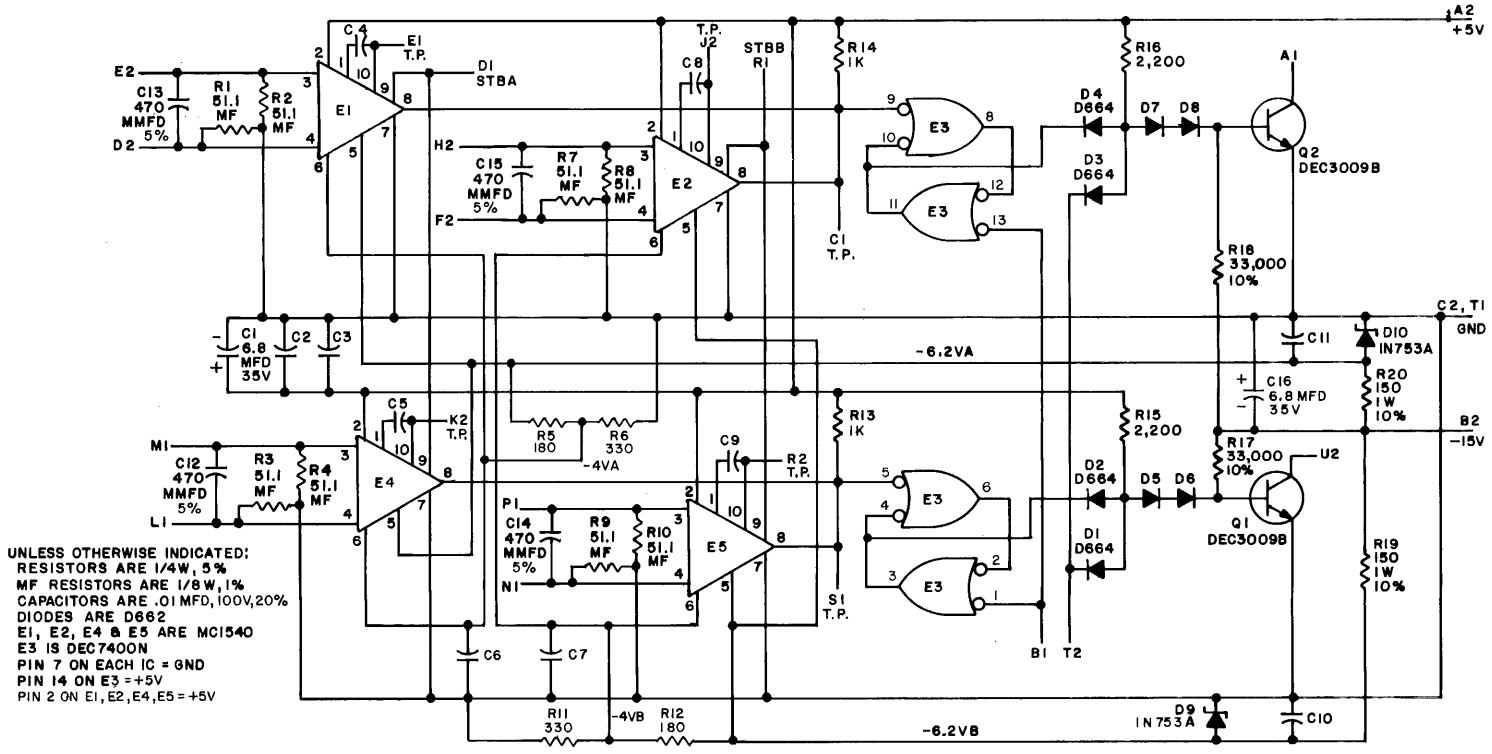
DEC FORM NO DRG 102

I-EM29

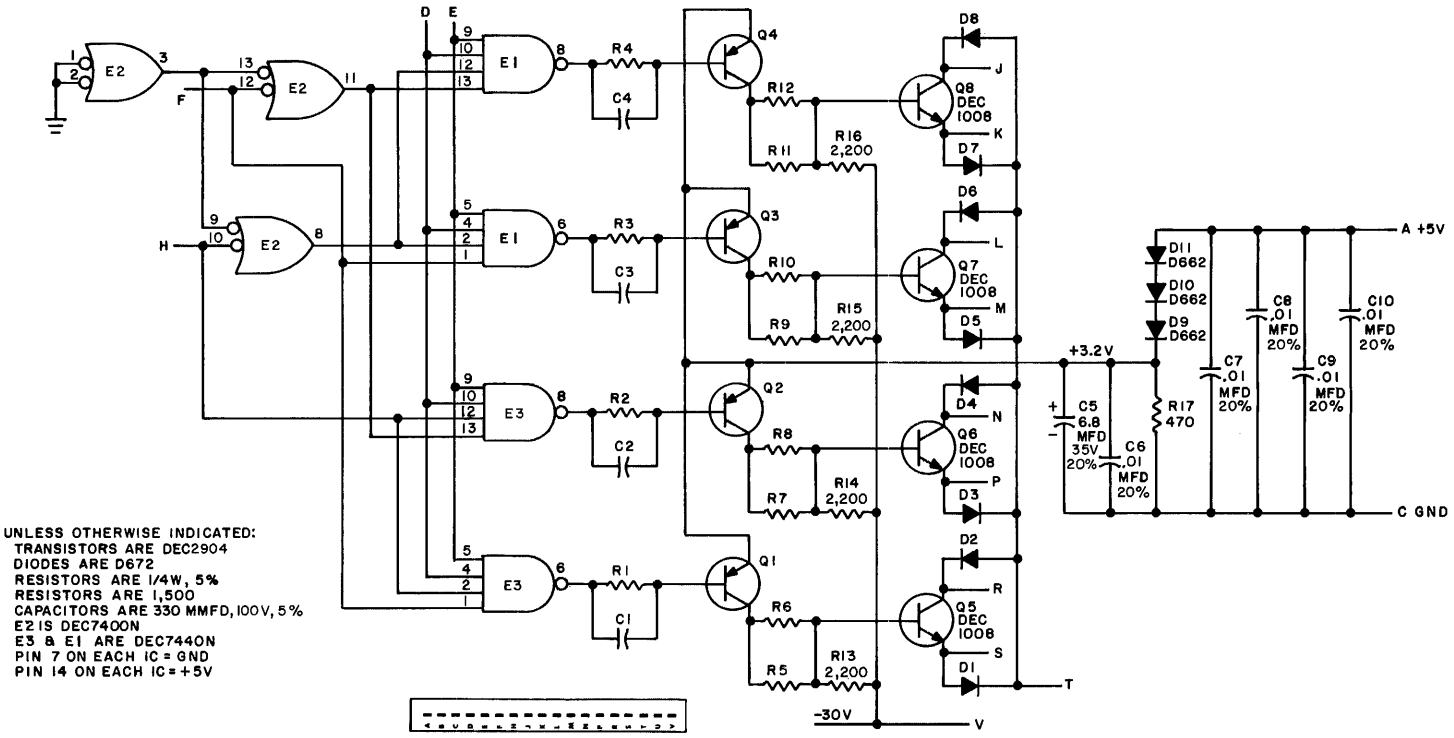


USE THE ETCH BOARD OF THE G021

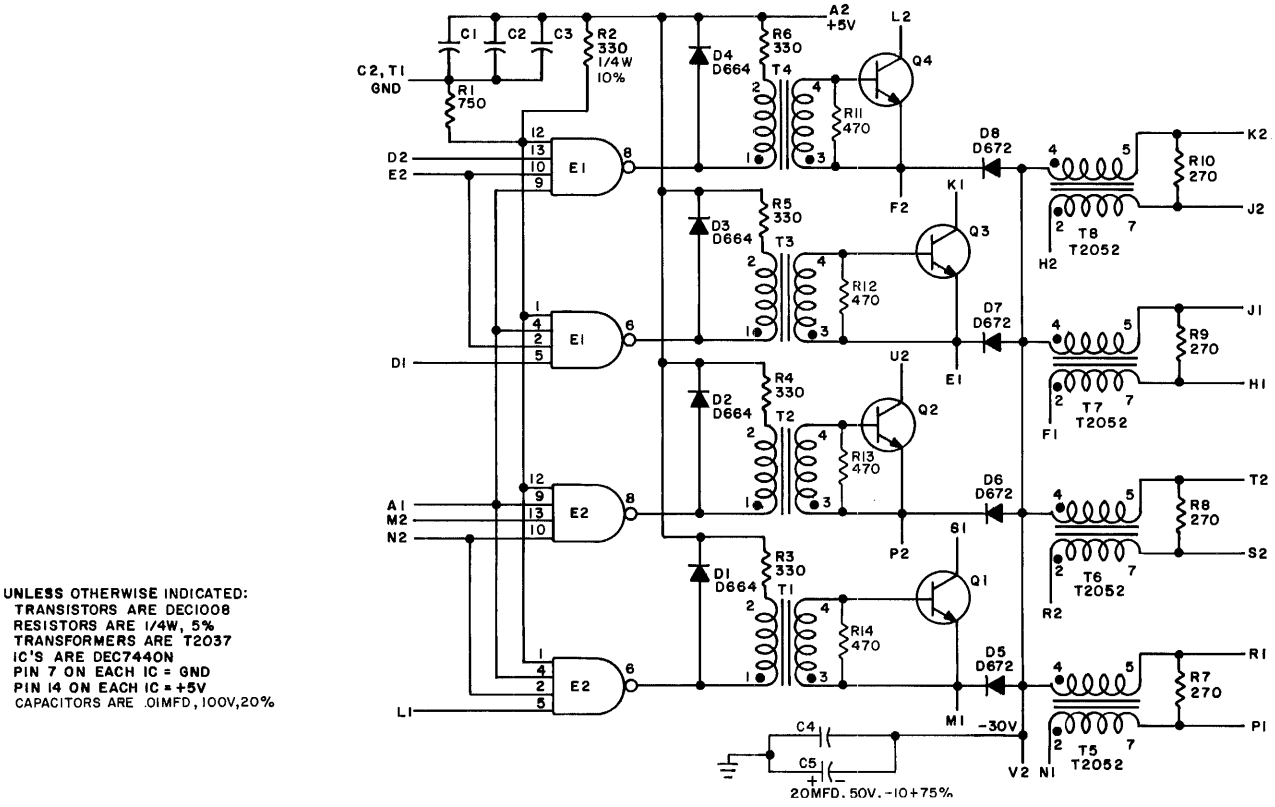
B-CS-G020-0-1 Sense Amplifier



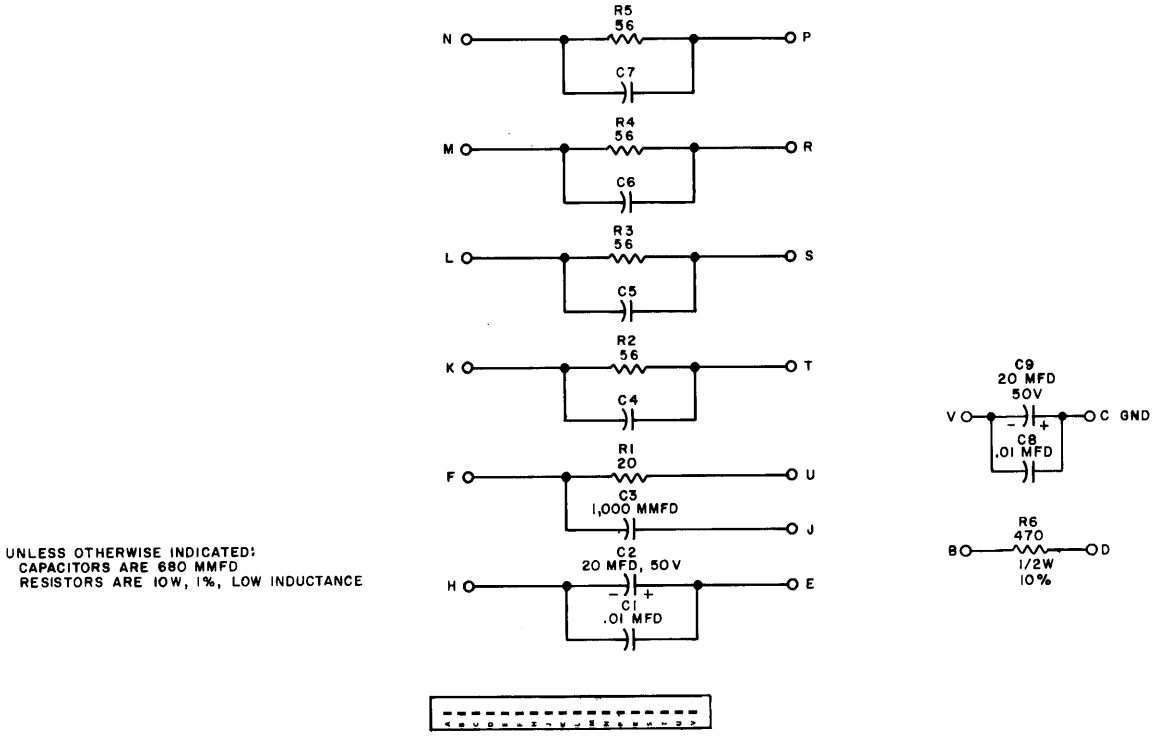
B-CS-G021-0-1 Sense Amplifier



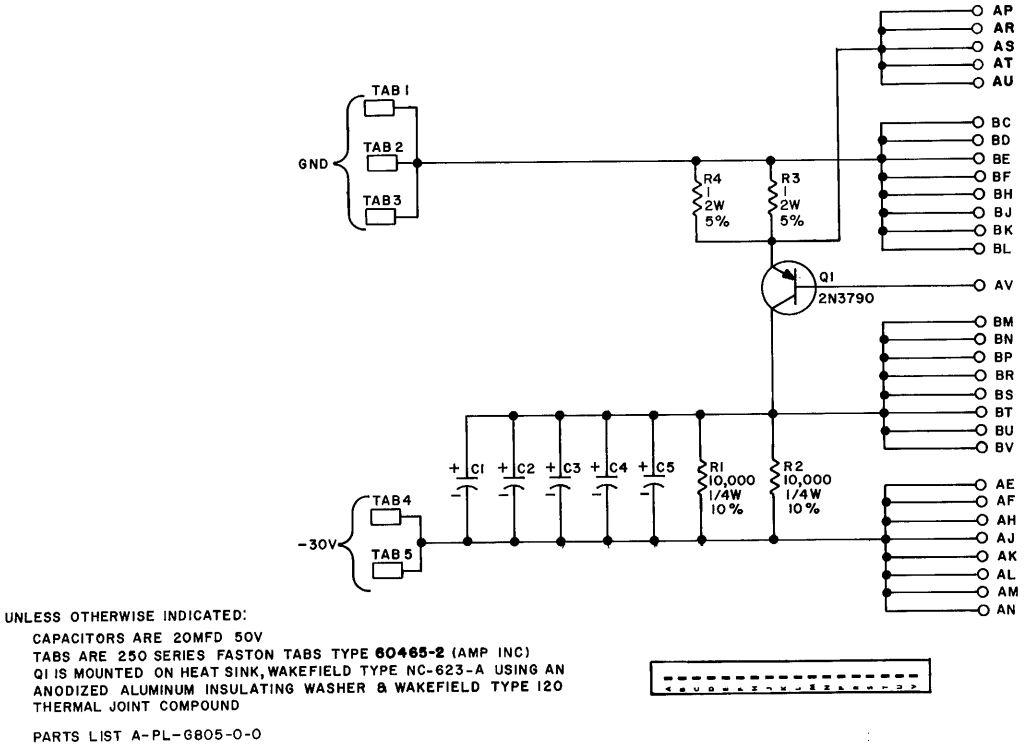
B-CS-G221-0-1 Memory Selector



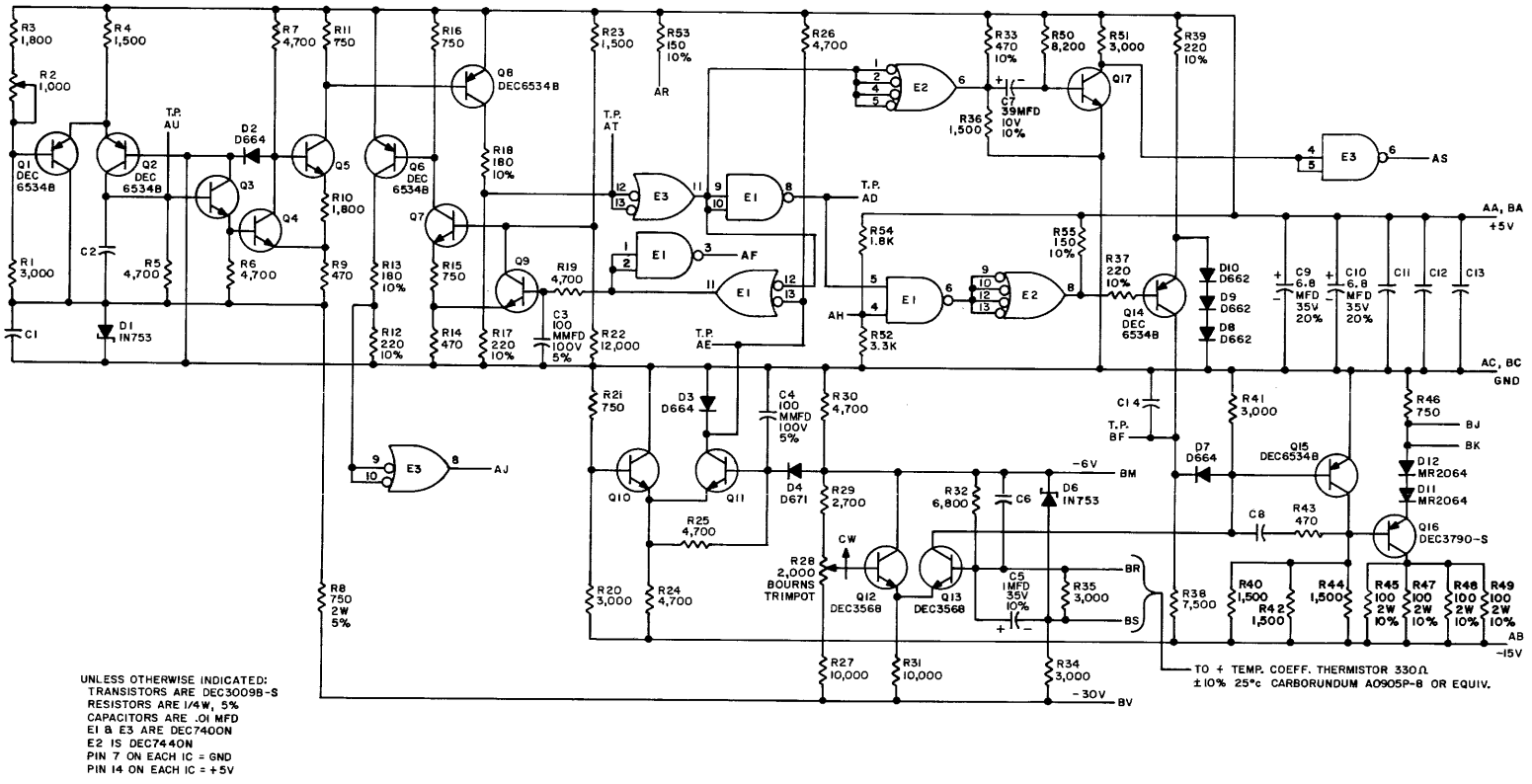
B-CS-G228-0-1 Inhibit Driver



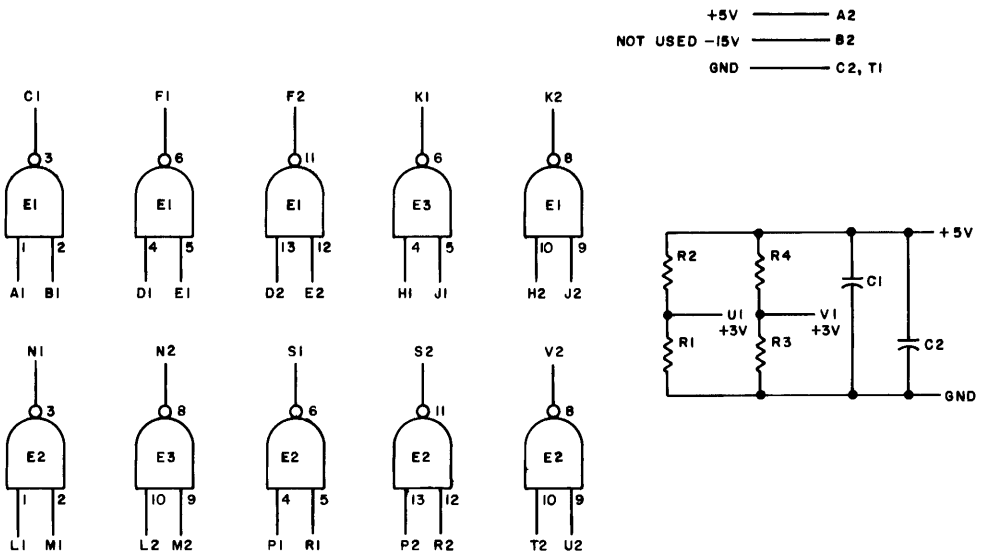
B-CS-G624-0-1 Resistor Board



B-CS-G805-0-1 Negative Regulator

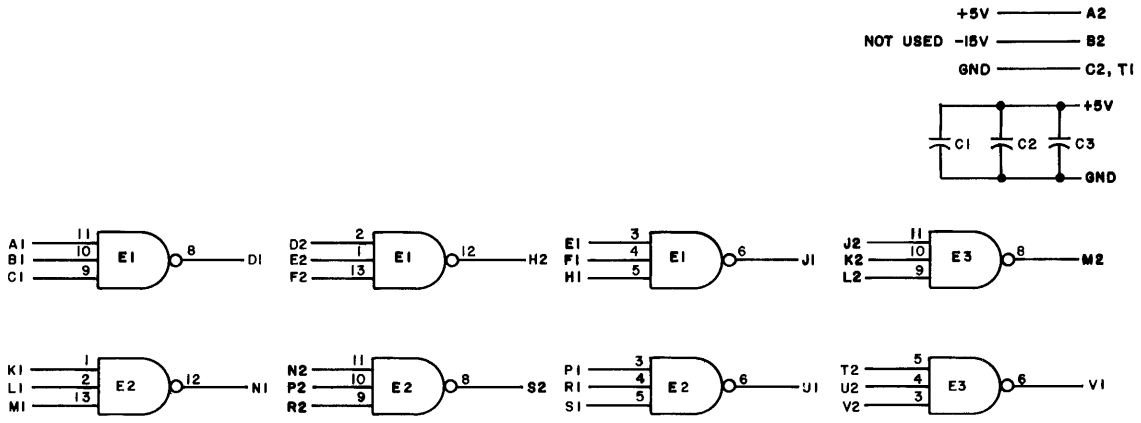


C-CS-G826-0-1 Regulator Control



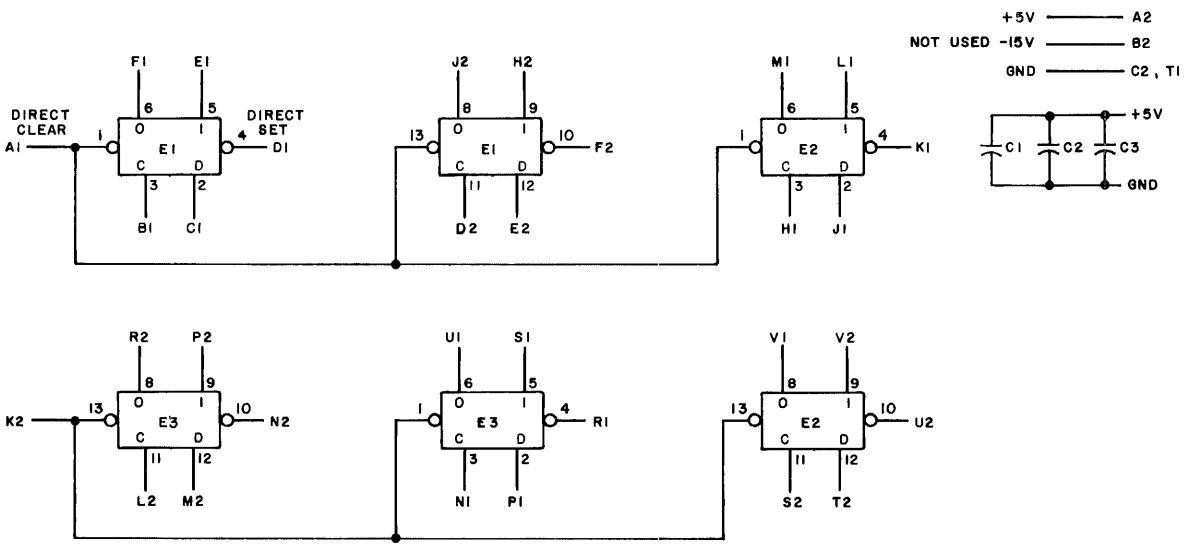
NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

B-CS-M113-0-1 10-2 Input NAND Gates



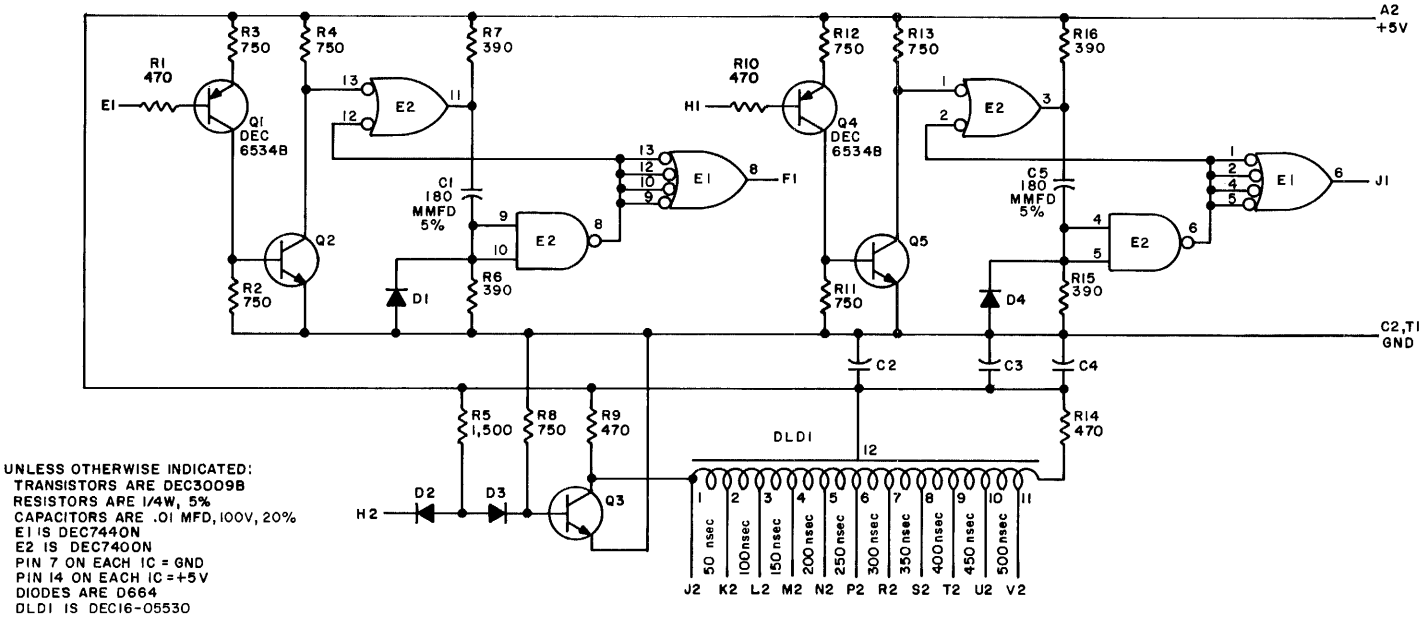
NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

B-CS-M115-0-1 8-3 Input NAND Gates



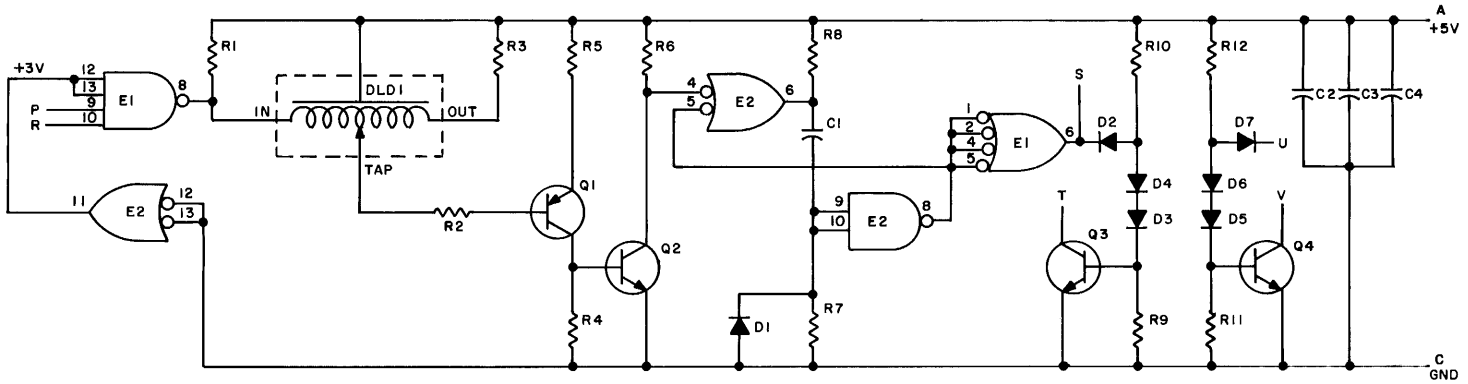
NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

B-CS-M310-0-1 Delay Line



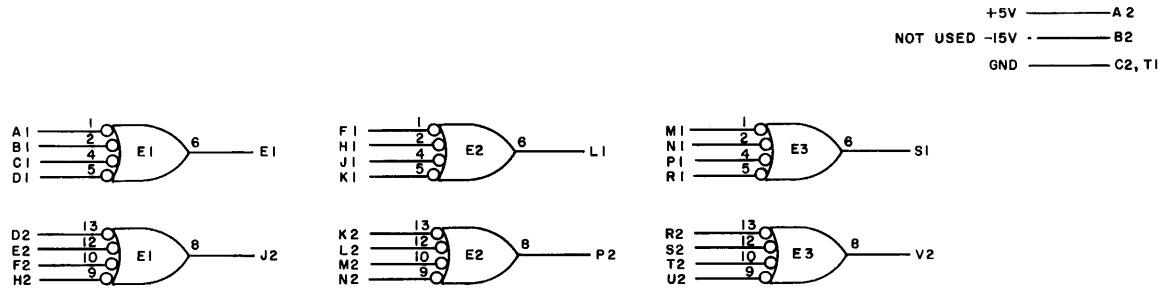
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC3009B
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE .01 MFD, 100V, 20%
E1 IS DEC7440N
E2 IS DEC7400N
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
DIODES ARE D664
DLDI IS DEC16-05530

B-CS-M360-0-1 Variable Delay



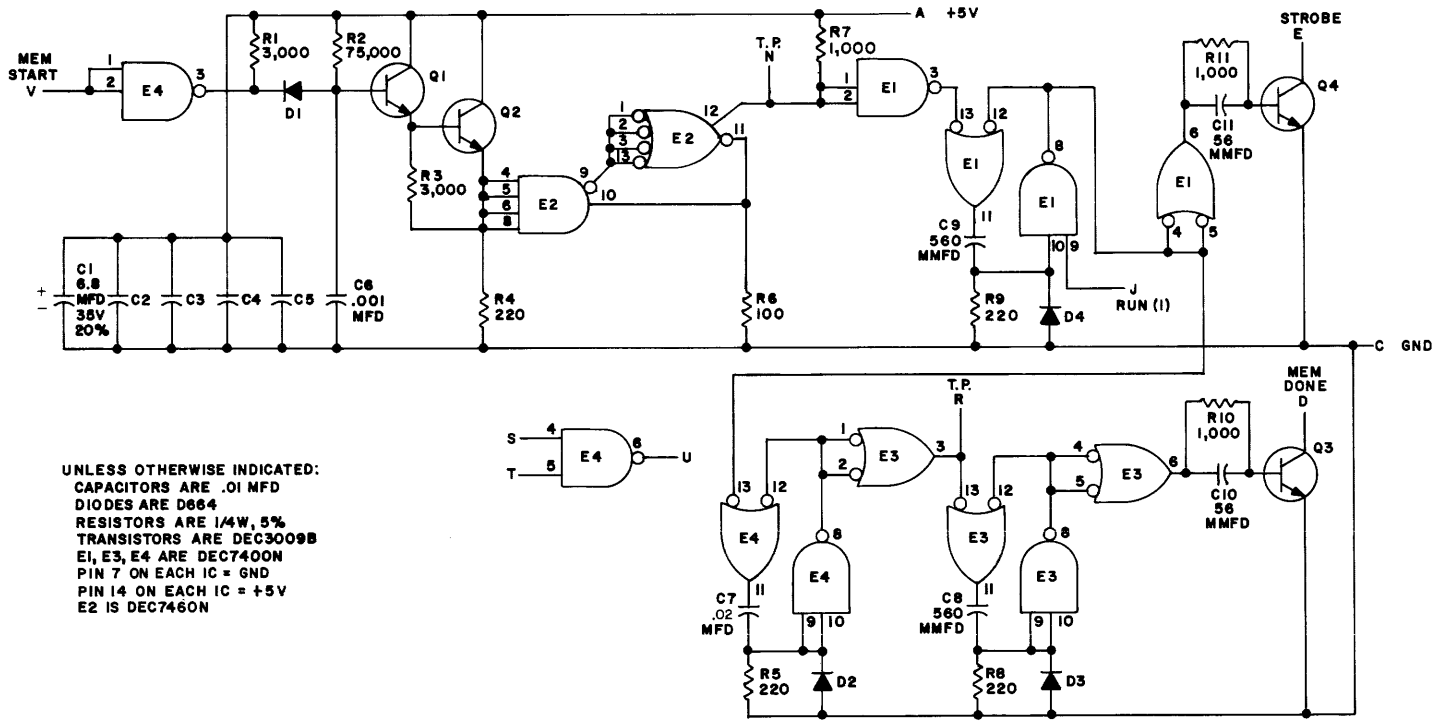
NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

B-CS-M360-0-1 Variable Delay M360



NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
USE THE ETCH BOARD OF THE M117

B-CS-M617-0-1 6-4 Input NOR Buffers



B-CS-M720-0-1 Memory Detection

MP8/I
MEMORY PARITY OPTION
FUNCTIONAL DESCRIPTION

MP8/I
MEMORY PARITY

INTRODUCTION

The MP8/I option provides a data-transmission check of each word written into or retrieved from memory. A parity bit is generated, and is written into memory with each MB data word. This option uses "odd parity" which generates a 1 in the parity bit when the contents of the MB contain an even number of 1s. The resulting number of 1s in both the MB and parity bit is always an odd number. The contents of the MB and parity bit are sensed when the memory read function occurs, and if the total (MB and parity) number of 1s is even, a parity error is generated.

The MP8/I option, contained within the PDP-8/I processor main frame, replaces the 12-bit core memory system with a 13-bit system that includes driving, inhibiting, sensing, parity-generating, and parity-checking circuitry, as well as a core-memory array constructed of 13 planes. The thirteenth plane stores the status of the parity bit in each memory address.

LOGIC DESCRIPTION

The following paragraphs describe the parity generation and checking networks, and the parity-error condition.

Parity Generator

The parity generator network consists of four sections (Drawing BS-MP8I-0-1, sheet 1) each of which samples inputs and provides specific outputs when the number of asserted inputs is odd. Three of these sections sample sets of four MB inputs (using both MB polarities) to determine within the sets of 4 an odd number of asserted bits. The fourth section samples the outputs of the first three sections to determine if an even number of these are asserted. If an even number are, the number of MB bits asserted is even and a parity bit is generated.

MB PARITY ODD, which is the fourth section output, is active and the P Inhibit Driver (Drawing BS-8I-0-14) is disabled. This allows a 1 to be written with the MB word into the address specified by MA.

Parity Check Network

After the data word and parity bit (PB) are read from memory to the SENSE register, the register outputs (designated MEM00 through MEM11) are applied through inverters to the parity-checking network (Drawing BS-MP8I-0-1, sheet 2). This network senses the number of 1s read from a memory address in the same way as the parity generator senses 1s in the MB. The parity bit is sampled in the fourth section, with inversion of MEM signals occurring prior to the first three sections.

The total memory word consisting of parity (MEMP) and data (MEMO-P) (Drawing BS-8I-0-14) should contain an odd number of 1s. If it does, MEM PARITY ODD (the fourth section output) is active and program operation continues normally. When the parity and data contains an even number of 1s, $\overline{\text{MEM PARITY EVEN}}$ output is active.

Parity Error

When an odd number of data bits are "picked up" or "dropped", MEM PARITY EVEN is generated, and combined with TP3 of the Fetch cycle of all instructions. This sets the PARITY ERROR flag (Drawing BS-MP8I-0-1, sheet 1), indicating that the data word in the MB has been altered, and is incorrect. The PARITY ERROR flag is connected to the PDP-8/I interrupt line

as MP INT, and generates INT RQST (Drawing BS-8I-0-10).

MP8/I PROGRAM INSTRUCTIONS

Two instructions are used with the memory parity option. Their generation and application are described below.

Skip On No Parity Error (SMP)

This instruction (octal code 6101) senses the PARITY ERROR (PE) flag status. If the PE flip-flop contains a 0, MP SKIP (Drawing BS-MP8I-0-1, sheet 1) is produced generating I/O SKIP (Drawing BS-8I-0-10). I/O SKIP forces the PC to increment by 1, thus the next sequential instruction is skipped. If the PE flip-flop contains a 1, the next instruction occurs and an appropriate subroutine is initiated.

When the SMP instruction is executed, the octal code 6101 is decoded in the following manner. Bits 0 through 2 of the instruction (octal code 6) decoded within the processor specify an IOT instruction. Bits 3 through 8 are decoded by the MP8/I logic to form the address code (octal code 10) of this option. Bits 9 through 11 allow generation of IOP pulses. Bit 11, in conjunction with an IOT instruction, generates IOP1 (octal code 1). $\overline{\text{MP SKIP}}$ is produced by combining the decoded IOT address level (10), and IOP1 with MP INT.

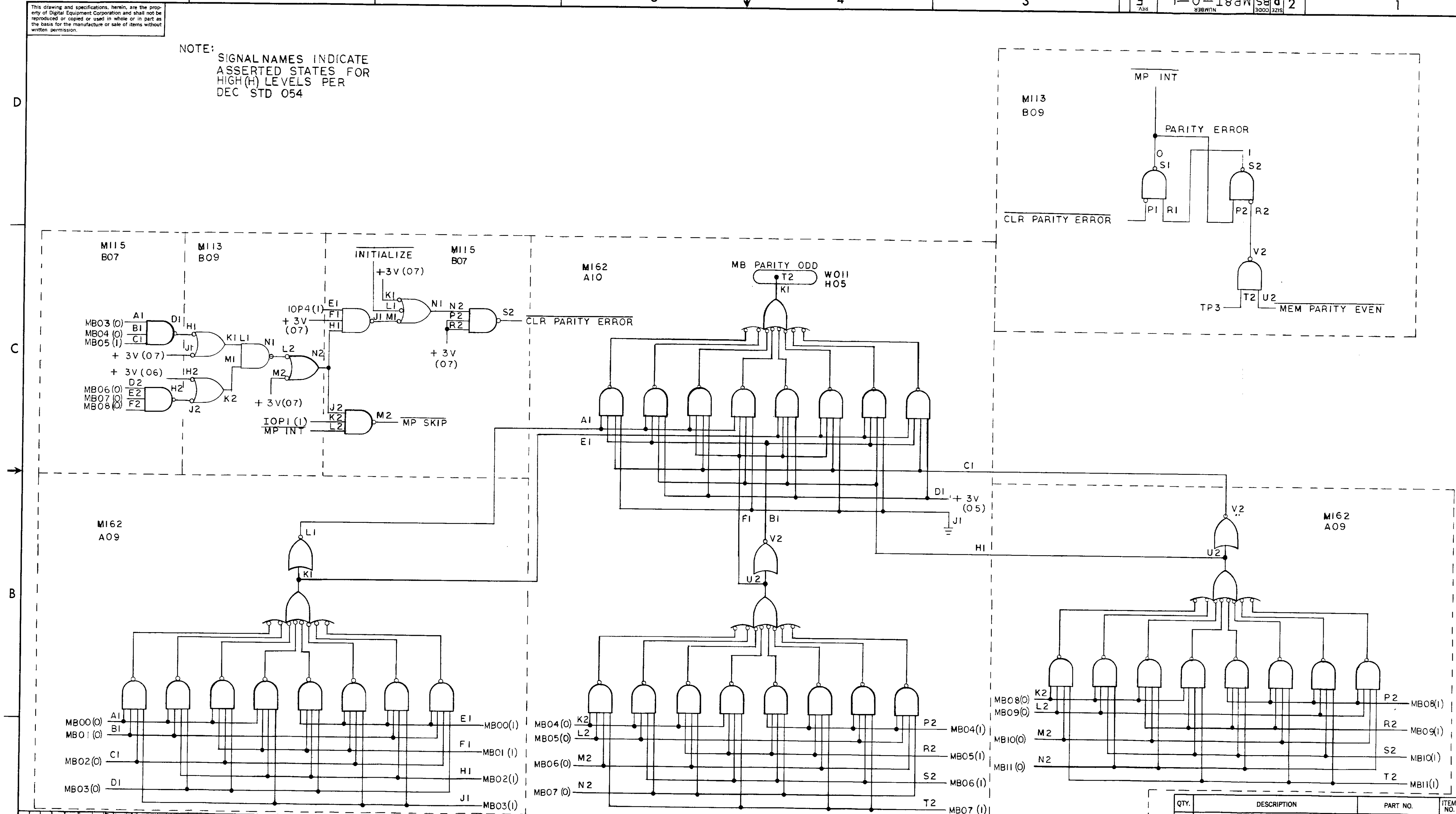
Clear Memory Parity Error (CMP)

This instruction (octal code 6104) clears the PE flip-flop after a parity-error condition has been acknowledged by the PDP-8/I. The 6104 instruction decodes to produce an IOP4 pulse and the octal address level 10. These two signals combine in the MP8/I option logic to produce CLR PARITY ERROR (Drawing BS-MP8I-0-1, sheet 1), which clears the PE flag.

ENGINEERING DRAWINGS

The following drawings pertaining to the MP8/I are contained in this section.

Drawing Number	Title	Revision
D-BS-MP8I-0-1	Memory Parity Option	F
B-CS-G020-0-1	Sense Amplifier	H
B-CS-G228-0-1	Inhibit Driver	E
B-CS-M113-0-1	10-2 Input NAND Gates	C
B-CS-M115-0-1	8-3 Input NAND Gates	C
B-CS-M162-0-1	Parity Circuit	A



REV.	CHANGE NO.	REVISIONS	CHK
A	ECO#1 9-6-67		
B	ECO#2		
C	ECO #4		
D			
E			
F	8I-00002	OLOUGHLIN	

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

DRN R.E. Bernier DATE 3 MAR 67
CHK'D DATE 8-16-67
ENG. E. de Castro DATE 10-11-67
PROJ. ENG. E. de Castro DATE 10-11-67
PROD DATE 9-21-67
FIRST USED ON E-UA-8I-0-0

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

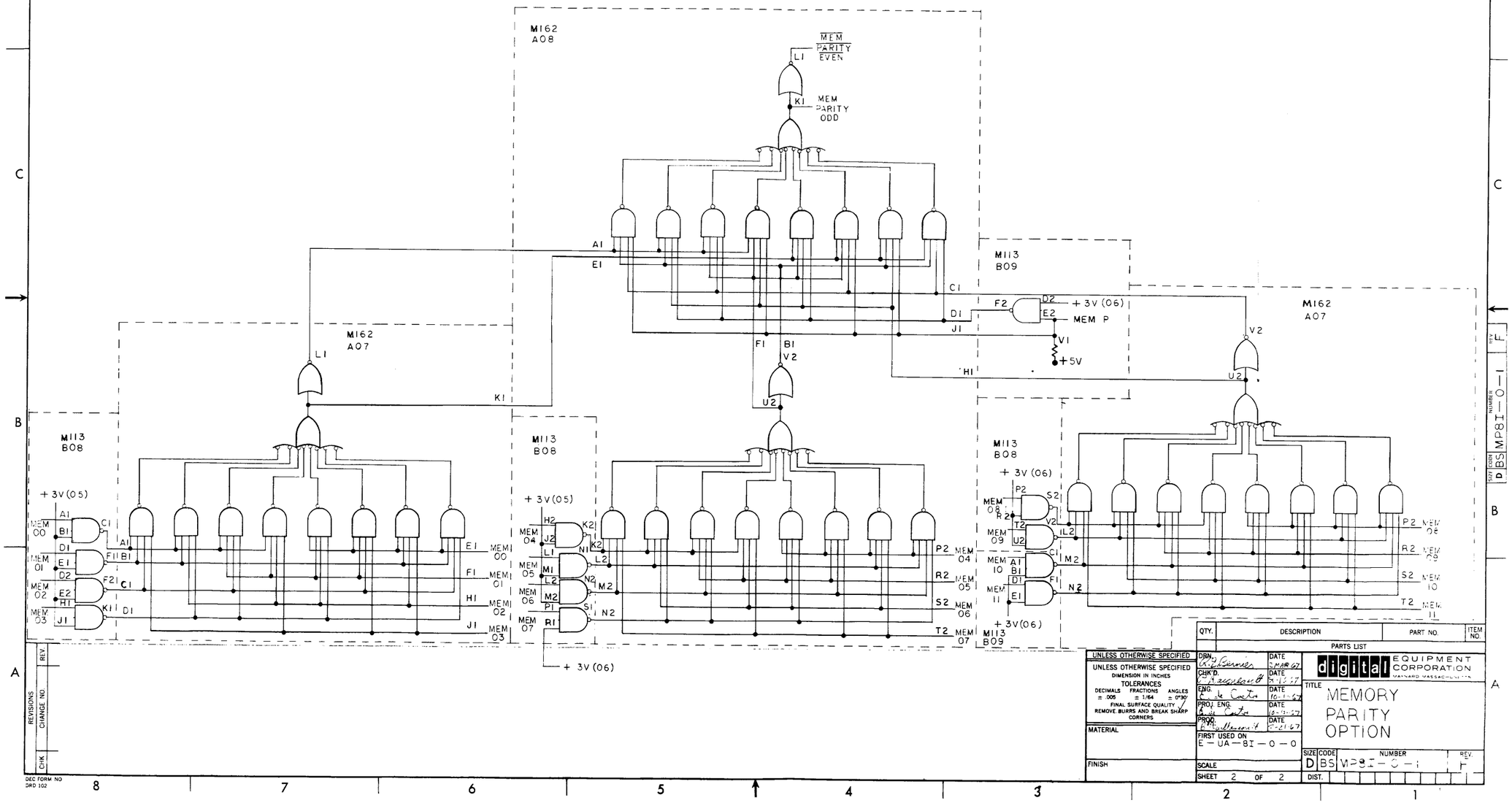
TITLE MEMORY PARITY OPTION

SIZE D CODE BS NUMBER MP8I-0-1 REV F

SCALE
SHEET 1 OF 2

DEC FORM NO DRD 102

NOTE:
SIGNAL NAMES INDICATE ASSERTED STATE
FOR HIGH LEVELS PER DEC STD 052



QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN.		DATE 5-MAR-67
CHK'D.		DATE 9-15-67
ENG.		DATE 10-1-67
PROJ. ENG.		DATE 10-21-67
PROD.		DATE 10-21-67

FIRST USED ON
E-UA-8I-0-0

SCALE

SHEET 2 OF 2

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

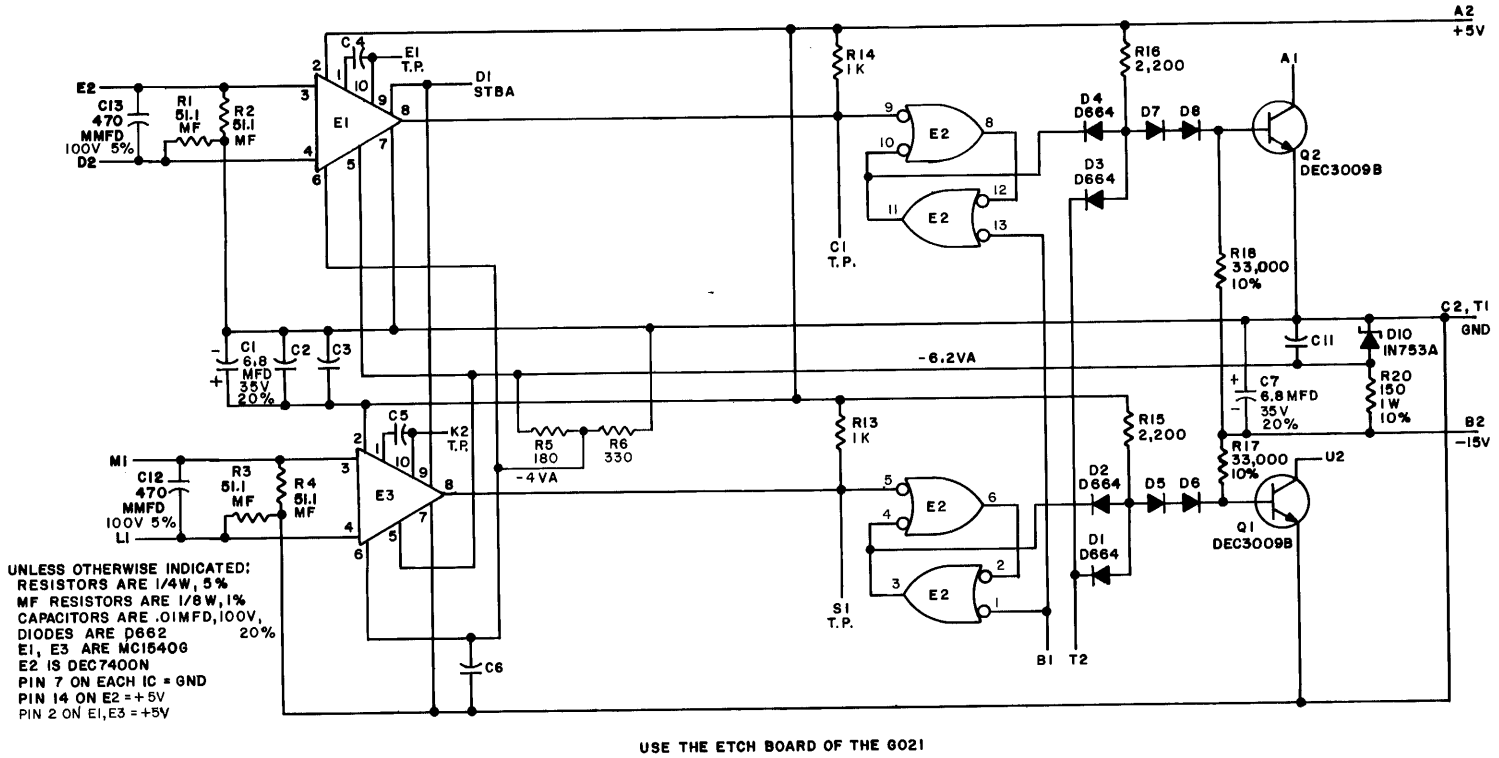
TITLE
MEMORY PARITY OPTION

SIZE D | CODE BS | NUMBER MP8I-0-1 | REV F

DIST.

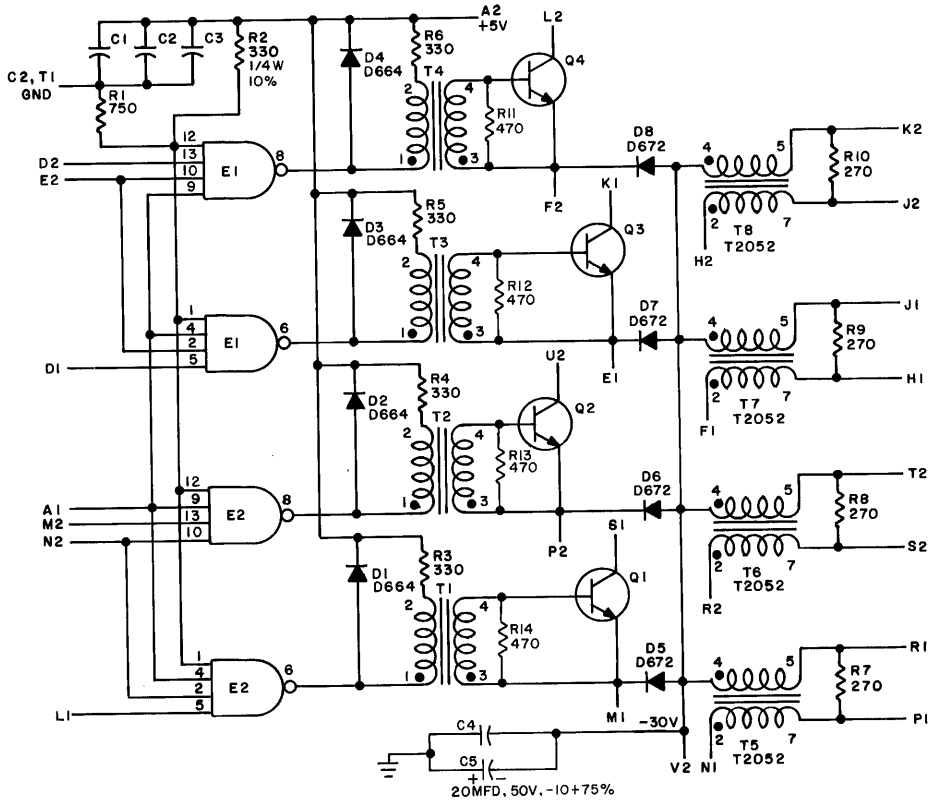
REVISIONS | REV. | CHANGE NO. | CHK

DEC FORM NO
DRD 102



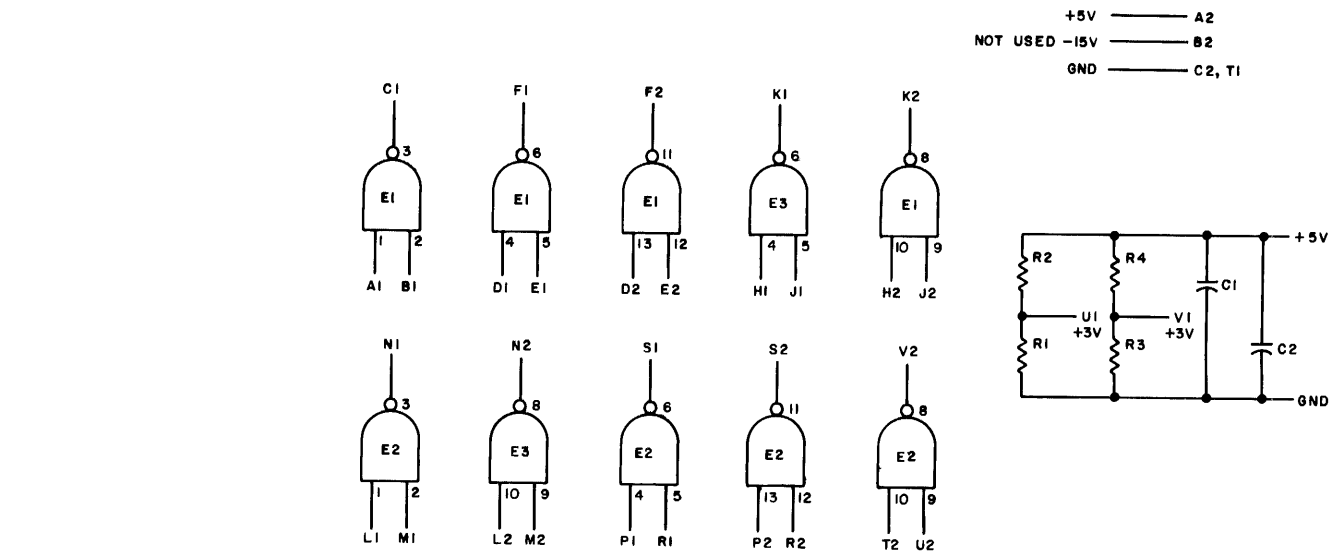
USE THE ETCH BOARD OF THE G021

B-CS-G020-0-1 Sense Amplifier



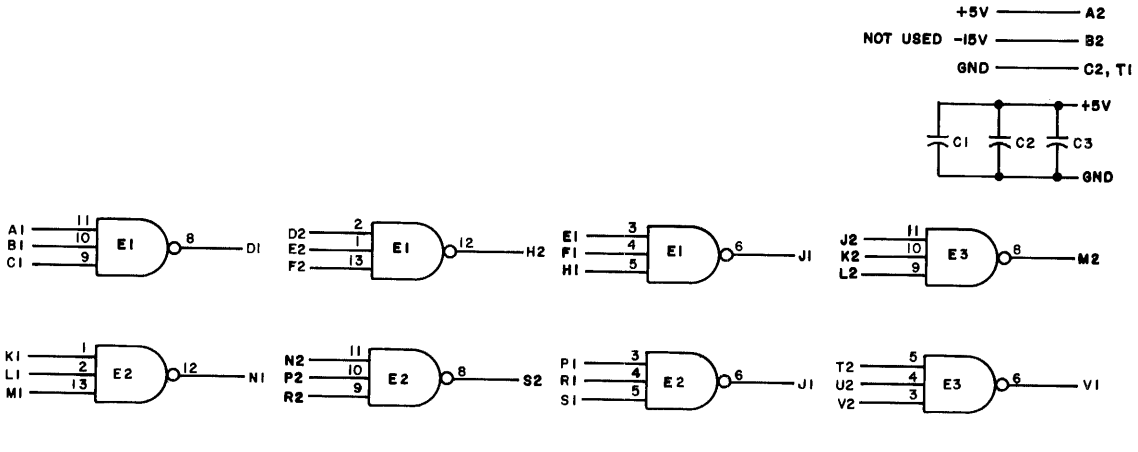
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC1008
RESISTORS ARE 1/4W, 5%
TRANSFORMERS ARE T2037
IC'S ARE DEC7440N
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
CAPACITORS ARE .01MFD, 100V, 20%

B-CS-G228-0-1 Inhibit Driver



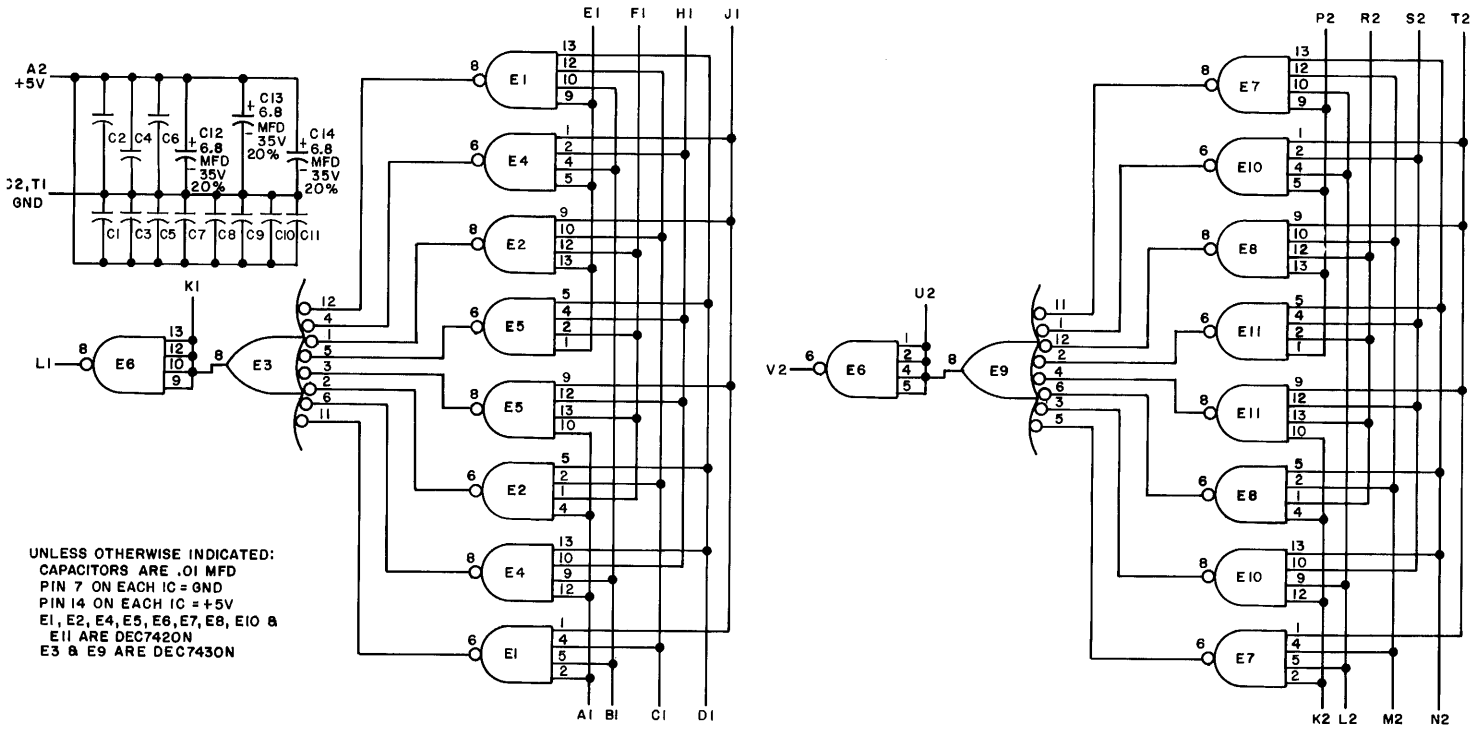
NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

B-CS-M113-0-1 10-2 Input NAND Gates



NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

B-CS-M115-0-1 8-3 Input NAND Gates



B-CS-M162-0-1 Parity Circuit

VC8/I
OSCILLOSCOPE DISPLAY OPTION
FUNCTIONAL DESCRIPTION

VC8/I
OSCILLOSCOPE DISPLAY

INTRODUCTION

The VC8/I Oscilloscope Display consists of a Tektronix Model RM503 Oscilloscope and its associated control logic. PDP-8/I control logic accepts 12-bit control instructions and 10-bit beam-positioning data words. The control instructions are interpreted to permit communication with the processor and intensity control of displayed points. The data words are converted to discrete analog voltages to provide 1024 display points on each of the X- and Y-axis of the cathode ray tube.

The VC8/I logic is contained on the M701 double-width integrated-circuit module and two A607 D/A Converter Modules located in the central processor main frame. Figure 1 shows the functional relationship between the PDP-8/I, the VC8/I control logic, and the display oscilloscope.

A photomultiplier light pen is optionally available for use with the VC8/I. This Type 370 light pen permits control over, or communication with, a running computer program.

The paragraphs which follow describe the operation of the control logic as it relates to both the PDP-8/I and the display oscilloscope. Operational and maintenance data on the Tektronix RM503 Oscilloscope is provided in the oscilloscope maintenance manual, provided by the manufacturer.

The maintenance procedures pertaining to the PDP-8/I also apply to the VC8/I control logic. Recommended maintenance procedures for the RM503 Oscilloscope are described in the respective Tektronix manual.

The VC8/I control logic accepts 10-bit words, describing horizontal and vertical plots, into X-axis and Y-axis buffers. The buffer outputs, converted from digital to analog levels, provide dc-level deflection inputs to the RM503. Logic circuits implement these operations by interpreting a 12-bit instruction located in the PDP-8/I memory buffer register.

The decoded instructions generate VC8/I control signals in the following manner. Memory buffer bits 0-2 contain the processor operation code 6$_8$, indicating an input/output instruction. Bits 3-8 contain the 6-bit address code identifying the instruction as one which pertains to the VC8/I. Three different address codes have been assigned to perform the necessary control functions. These

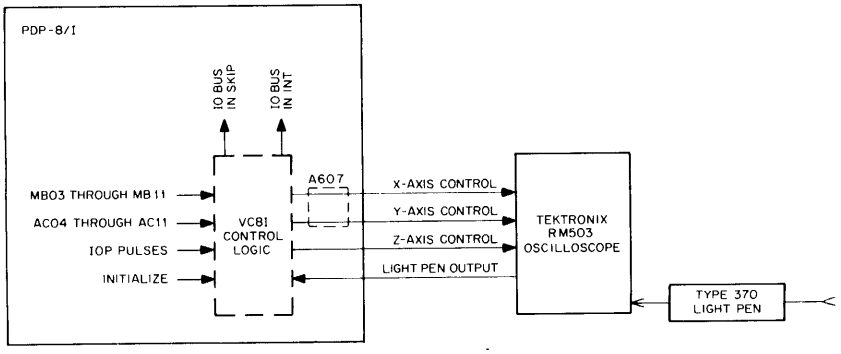


Figure 1 VC8/I Oscilloscope Display Block Diagram

addresses, and their functions are as follows: 05_8 (X-axis plotting and intensity control); 06_8 (Y-axis plotting and intensity control); and 07_8 (light-pen control).

Bits 9, 10, and 11 of the instruction generate IOP pulses in the PDP-8/I. The IOP pulses AND with levels produced by the decoding of the address bits to generate specific VC8/I control signals.

Table 1 lists the VC8/I control instructions and their respective operations

Table 1
Control Instructions

Mnemonic	Octal Code	Operation
DCX (DCY)	6051 (6061)	Generates an IOP1 pulse to clear the X(Y) buffer.
DXL (DYL)	6053 (6063)	Generates an IOP1 pulse to clear the X(Y) buffer, and an IOP2 pulse to load data from AC02-11.
DIX (DIY)	6054 (6064)	Generates an IOP4 pulse to intensify the oscilloscope display electron-beam to the degree indicated by the BR. This command combined with DXL (DYL) becomes the DXS(DYS) command.
DXS (DYS)	6057 (6067)	Generates IOP pulses 1,2, and 4 to perform all functions of the three instructions listed above.

Table 1 (Cont)
Control Instructions

Mnemonic	Octal Code	Operation
DSB	607X	Generates an IOP4 pulse to load the content of bits 10 and 11 of the instruction into the brightness register. Bits 10 and 11 are decoded by the BR as follows: 6075 = minimum brightness 6076 = minimum brightness 6077 = maximum brightness

LOGIC DESCRIPTION

The following paragraphs describe the operation of the VC8/I control logic. Logic circuitry for the oscilloscope display option appears on DEC Engineering Drawing D-BS-VC8I-0-1. Since the X-and Y-channels operate identically only the horizontal (X) channel logic and operation is discussed.

When the computer is turned on, or whenever the Start key is pressed, the PDP-8/I INITIALIZE level clears the light-pen flag flip-flop, and sets the brightness register flip-flops BR0 and BR1 to the 1 state.

Clearing and Loading the Buffer

The DCX (6051) instruction in the PDP-8/I memory buffer register is performed to clear the X-buffer register on the A607 module. When this

content of PDP-8/I memory buffer bits 10 and 11 into BR0 and BR1. There are four possible BR combinations; 00, 01, 10, and 11. Their assignments are listed below:

BR0	BR1	Assignment
0	0	----------
0	1	Partially enables low intensity AND gate
1	0	Partially enables medium intensity AND gate
1	1	Partially enables high intensity AND gate

NOTE

The 00 combination is not used because it disqualifies each intensity AND gate.

Three intensity amplifiers INT1 (low), INT2 (medium), and INT3 (high) control the RM503 Z-axis oscilloscope intensity. These amplifiers are AND-gate controlled by the combination of the intensity pulse and the output of the BR.

The intensity pulse can be generated by either the DIX (6054) or DIY (6064) instruction. Both instructions are employed because each can be modified to form either the DXS and DYS instructions, respectively. The DIX (DIY) address code IOT05 (IOT06) and IOP4 combine to generate the intensify pulse. After a 1 μs delay to ensure that the BR has settled, the intensity pulse turns on the intensity amplifier specified by the BR.

Light Pen Operation

The Type 370 Photomultiplier Light Pen communicates with, or controls a computer program when used with the VC8/I. The light pen detects a point of light on the cathode ray tube, and generates a negative voltage level, which is applied to the VC8/I control logic. This voltage level is not a standard DEC level, and is therefore an emitter follower buffered to provide the signal and impedance characteristics required for DEC logic operation.

The buffered light pen output, combines with LIGHT PEN STROBE to set the light-pen flag flip-flop. LIGHT PEN STROBE is generated by the active instensity amplifier.

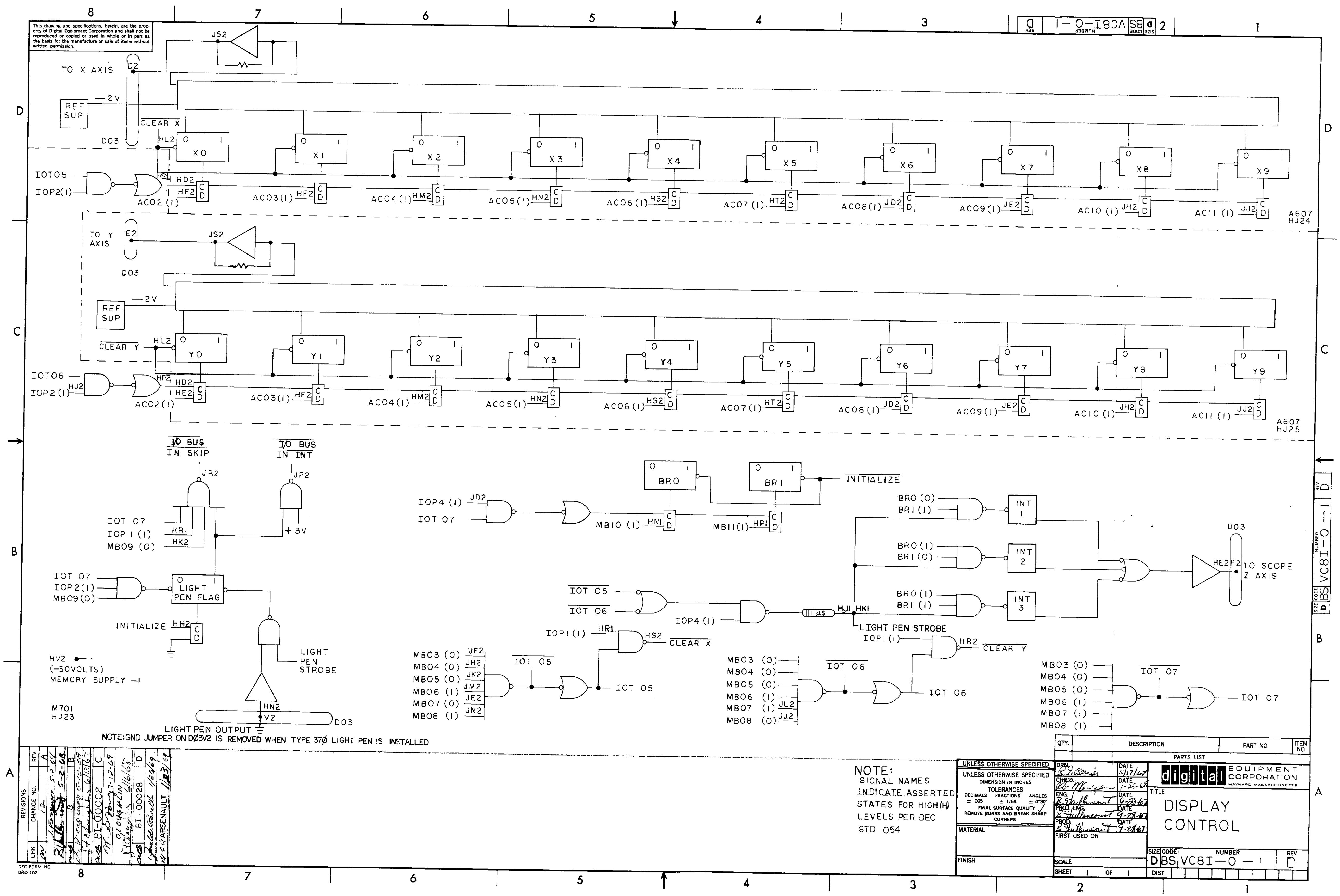
When the flag is set, its output partially enables the IO BUS IN SKIP gate and activates the IO BUS IN INT line, informing the PDP-8/I that some device is requesting service. The PDP-8/I then enters a programmed subroutine to determine which device caused the interrupt. This is performed by a series of "flag checking" skip instructions. A skip instruction is executed for each device attached to the IO BUS IN INT request line. When the 6071 instruction (skip if the light pen flag is a 1) is executed, the IO BUS IN SKIP line activates, incrementing the program counter by 1 and skipping the next sequential instruction. After the instruction is skipped, the PDP-8/I enters a servicing routine for this device.

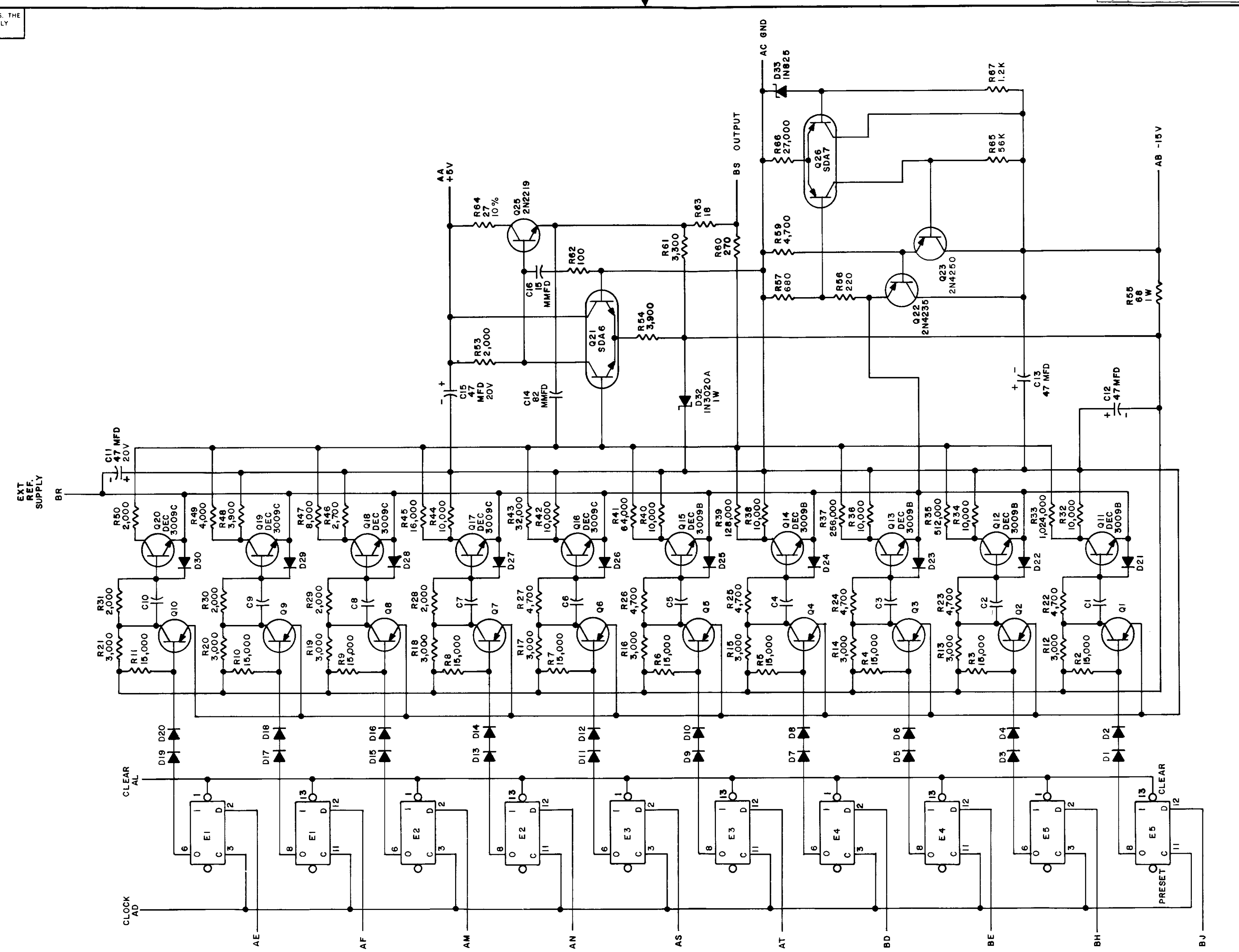
The light pen flag is cleared by either the INITIALIZE level or by the combination of an IOT07, IOP2 and memory buffer bit 9 in the 0 state.

ENGINEERING DRAWINGS

The following drawings pertaining to the VC8/I option are contained in this section.

Drawing Number	Title	Rev.
D-BS-VC8I-0-1	Display Control	D
D-CS-A607-0-1	10-Bit D-A Converter	C
B-CS-A701-0-1	Power Supply	-
C-CS-M701-0-1	Display Control	D


This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.
TO X AXIS
REF SUP
—2V
CLEAR X
D03
JS2
X0 X1 X2 X3 X4 X5 X6 X7 X8 X9
IOT05
IOP2(1)
AC02 (1)
AC03(1) AC04(1) AC05(1) AC06(1) AC07 (1) AC08(1) AC09(1) AC10 (1) AC11 (1)
A607 HJ24
TO Y AXIS
CLEAR Y
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 Y9
IOT06
A607 HJ25
I/O BUS IN SKIP
I/O BUS IN INT
IOT 07
IOP 1 (1)
MB09 (0)
+3V
IOP2(1)
LIGHT PEN FLAG
INITIALIZE
LIGHT PEN STROBE
HV2 (-30VOLTS) MEMORY SUPPLY -1
M701 HJ23
LIGHT PEN OUTPUT
D03
NOTE:GND JUMPER ON D03V2 IS REMOVED WHEN TYPE 370 LIGHT PEN IS INSTALLED
IOP4 (1)
MB10 (1)
MB11(1)
BR0
BR1
INITIALIZE
BR0 (0) BR1 (1)
BR0 (1) BR1 (0)
BR0 (1) BR1 (1)
INT 1
INT 2
INT 3
TO SCOPE Z AXIS
IOT 05
IOT 06
1 μs
LIGHT PEN STROBE
IOP1 (1)
CLEAR X
CLEAR Y
MB03 (0) MB04 (0) MB05 (0) MB06 (1) MB07 (0) MB08 (1)
MB03 (0) MB04 (0) MB05 (0) MB06 (1) MB07 (1) MB08 (0)
MB03 (0) MB04 (0) MB05 (0) MB06 (1) MB07 (1) MB08 (1)
IOT 05
IOT 06
IOT 07
NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH(H) LEVELS PER DEC STD 054
REVISIONS
DISPLAY CONTROL
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
D BS VC8I—0—1 D
SHEET 1 OF 1



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC-6B
DIODES ARE D664
CAPACITORS ARE 47 MMFD
RESISTORS ARE 1/4W, 5%
IC'S ARE DEC7474N
PIN 7 ON EACH IC = AC GND
PIN 14 ON EACH IC = AA +5V
R33 IS 1/2W, 1%, 25 PPM %
R35 IS 1/4W, 1%, 25 PPM %
R37, R39, R41 & R43 ARE 1/8W, .1%, 25 PPM%
R45, R47, R49 & R50 ARE .3W, .01%, 5 PPM%
Q16 THRU Q20 ARE SELECTED SILVER DOT

PARTS LIST IS A-PL-A607-0-0

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC-6B	NONE	SDA6	2N2060
DEC3009B	2N3009	D664	1N3606
DEC3009C	2N3009	1N3020	SAME
2N4234	SAME	1N825	SAME
DEC6534B	MPS6534	SDA7	SAME

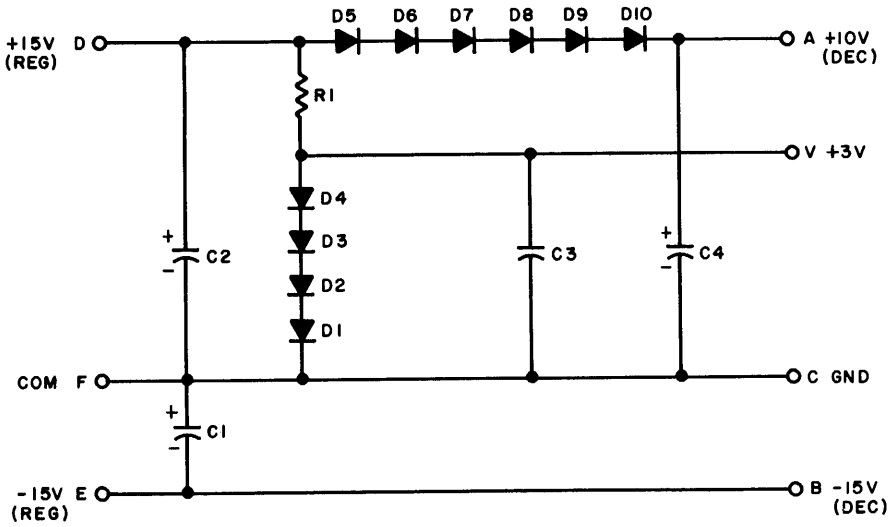
DIGITAL EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS

TITLE: 10 BIT D - A CONVERTER A607

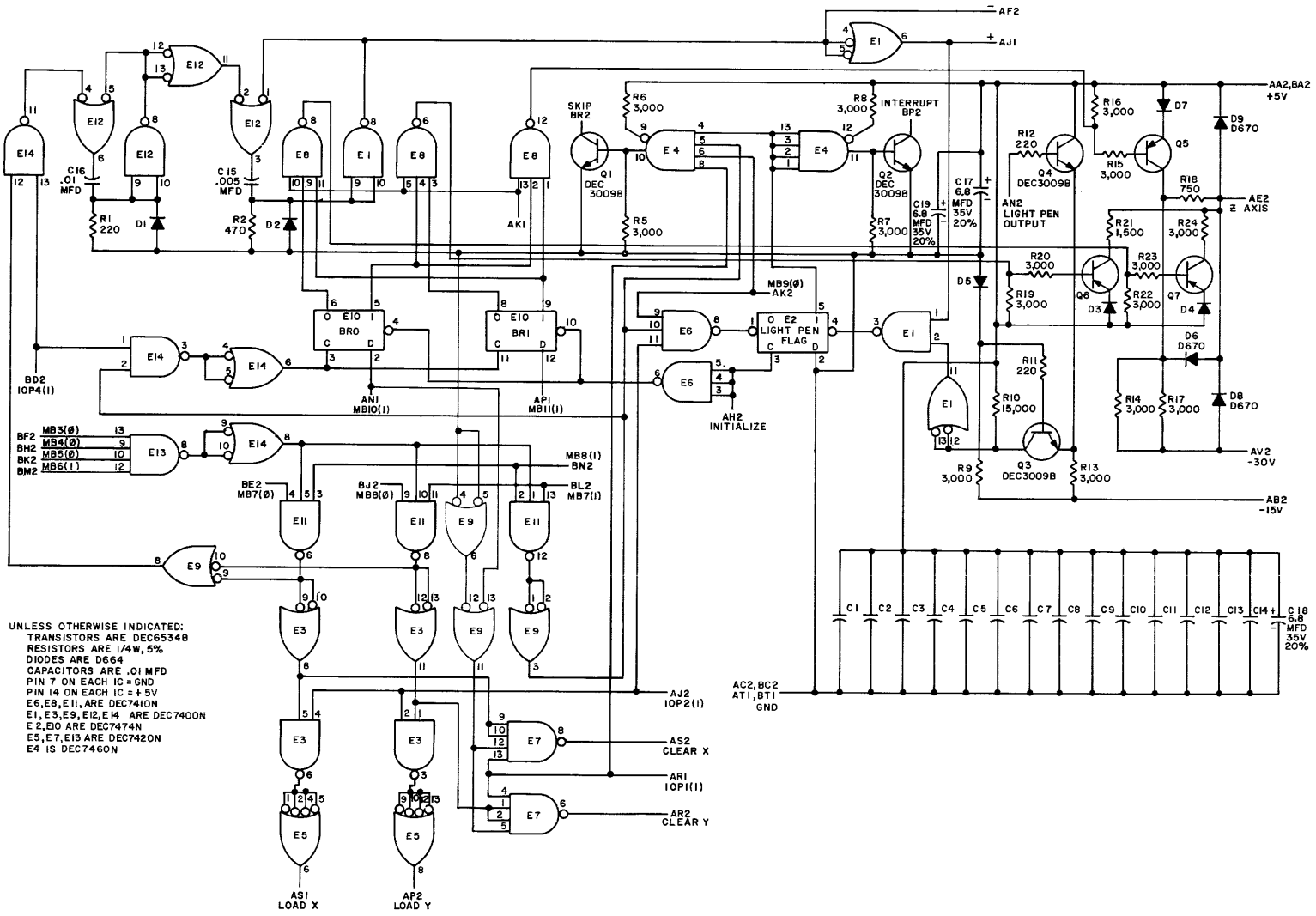
SIZE D | CODE CS | NUMBER A607-0-1 | REV. C

PRINTED CIRCUIT REV A B

DEC FORM NO. DRD 101



B-CS-A701-0-1 Power Supply



C-CS-M701-0-1 Display Control

instruction is executed, the address code 05_8 (bits 3 through 8) decodes to produce IOT05, and IOP1 is generated from MB11 in the processor. These signals NAND together in the control logic generating the CLEAR X pulse.

The DCX instruction, normally used only at the start of the program, is usually combined with the load instruction (DXL) to increase the speed of operation. This combined instruction (6053) produces both IOP1 and IOP2 pulses in the same computer cycle. The $\overline{\text{CLEAR X}}$ pulse (IOT05 IOP1) clears the X-buffer register. The load pulse (IOT05 IOP2) is generated 1 μs later. The load pulse appears on the X-buffer flip-flop C inputs and transfers a data word from PDP-8/I accumulator bits AC02 through AC11 into the X-buffer register.

Digital To Analog Conversion

The 10-bit data word contained in the X-buffer register generates an analog voltage between 0V and -2V by the A607 D/A Converter and Buffer Register Module. The analog voltage can be varied in 1024 (2^{10}) discrete intervals between its upper and lower limits in direct proportion to the numerical value of the coordinate data.

A 0V input signal from all X-buffer flip-flops to the D/A converter produces a 0V analog output; conversely, a +3V input from all these flip-flops generates a -2V output. The X and Y analog voltages are produced identically. The location of the oscilloscope beam on the cathode ray tube is determined by the vector sum of the two voltages applied to the RM503 inputs. Table 6-4 shows the relationship between the buffer register data and the analog voltage output.

Intensity Circuits

The brightness of the point displayed is determined by the 2-bit brightness register (BR). A PDP-8/I DSB (607X) instruction generates a load pulse (IOP4 IOT07). This pulse transfers the

Table 2
Buffer Data - D/A Converter Correlation

Digital Address and Flip-Flop States	Buffer Output and D/A Converter Input	D/A Converter Output
1 1 1 1 1 1 1 1 1 1	xxxxxxxxxx	most positive (0V)
1 1 1 1 1 1 1 1 1 0	xxxxxxxxxy	.
.	.	.
.	.	.
1 0 0 0 0 0 0 0 0 1	xyyyyyyyyx	.
1 0 0 0 0 0 0 0 0 0	xyyyyyyyyy	.
0 1 1 1 1 1 1 1 1 1	yxxxxxxxxx	.
0 1 1 1 1 1 1 1 1 0	yxxxxxxxxy	.
.	.	.
.	.	.
0 0 0 0 0 0 0 0 0 1	yyyyyyyyyx	.
0 0 0 0 0 0 0 0 0 0	yyyyyyyyyy	most negative (-2V)
0 = Zero State	x = 0V	
1 = One State	y = +3V	

VP8/I
INCREMENTAL PLOTTER OPTION
FUNCTIONAL DESCRIPTION

VP8/I INCREMENTAL PLOTTER

INTRODUCTION

The VP8/I Incremental Plotter consists of a California Computer Products Inc. digital incremental plotter and its associated control logic. The control logic accepts 12-bit instructions from the PDP-8/I and converts them to specific operational commands which are retransmitted to the plotter, producing the desired pen and drum movements. Discrete points may be plotted, and vertical, horizontal, or diagonal lines produced in any combination by the application of the proper programmed commands.

The control logic of the VP8/I is contained on one M704 double-width integrated-circuit module located in the central processor main frame. The control logic is compatible with CalComp Digital Incremental Plotter Models 563, 564, 565, or 566. Figure 1 shows the functional relationship between the PDP-8/I, the VP8/I control logic, and the incremental plotter.

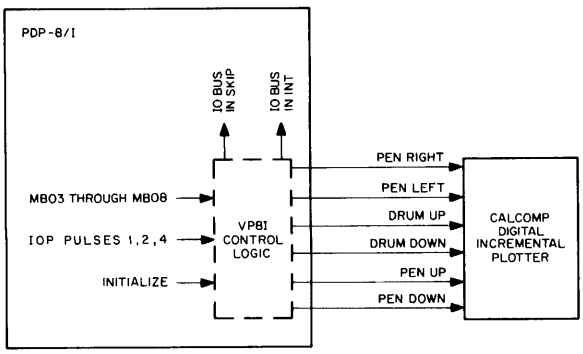


Figure 1 VP8/I Block Diagram

The paragraphs which follow describe the operation of the control logic portion of the plotter as it relates to both the PDP-8/I and the mechanism. Maintenance procedures, and a description of the plotter mechanism and its operation are provided in the CalComp Digital Incremental Plotter Maintenance Manual supplied with the system.

The maintenance procedures pertaining to the PDP-8/I also apply to the VP8/I control logic. The recommended maintenance procedures for the CalComp Plotters are described in the respective California Computer Products Inc. manuals.

LOGIC DESCRIPTION

The VP8/I control logic interprets a PDP-8/I instruction in the memory buffer register to generate control pulses that set one or more motion-control flip-flops. These flip-flops initiate plotter motion by moving the pen up, down, left or right, and/or moving the drum up or down.

The PDP-8/I instructions decode to initiate plotter functions in the following manner. Memory buffer bits 0-2 contain the operation code 6_8, indicating an input/output instruction. PDP-8/I memory buffer bits 3 through 8 contain a 6-bit address code that identifies the instruction as one pertaining to the VP8/I. Three address codes have been assigned to the plotter control. These codes and their functions are as follows: 50_8 (plotter flag and pen up); 51_8 (pen right and drum motions); and 52_8 (pen left and down, drum up).

Bits 9, 10, and 11 of the instruction generate IOP pulses in the PDP-8/I. The IOP pulses combine with levels in the VP8/I control logic produced by decoding the address bits to generate specific control signals that initiate plotter motions.

Logic Operation

The following paragraphs describe the operation of the VP8/I control logic. Logic circuitry for

this option appears on DEC Engineering Drawing D-BS-VP8I-0-1.

Whenever the computer is turned on, or the Start key is pressed, the PDP-8/I INITIALIZE level is generated. This signal clears the PLTR FLAG (plotter flag) and generates FAST OP DONE (fast operate done) to clear the PEN RIGHT, PEN LEFT, DRUM UP, and DRUM DOWN motion control flip-flops.

The plotter IOT (PLTR IOT) and the 50 INST level are the decoded address levels used in the VP8/I control logic. PLTR IOT is generated whenever the PDP-8/I I/O instruction contains 50_8, 51_8, or 52_8 (from memory buffer register bits 3 through 8). When active, this level is at +3V. It is the main IOT level and is used to generate every plotter motion.

The 50 INST level is generated and active (+3V) only when PDP-8/I memory buffer bits 7 and 8 are cleared. The inverse of this level, 50 INST, is also used. 50INST is generated whenever MB07 or MB08 is set; i.e., a 51_8 or 52_8 address code. These IOT levels (PLTR IOT, 50 INST, and 50INST) combine with the IOP pulses to generate specific control pulses.

The plotter operations are classified as being either fast (pen right, pen left, drum up, drum down) or slow (pen up, pen down) motions.

When a fast-motion instruction is executed, the following events occur in sequence. The motion control flip-flop sets initiating the plotter motion, and the first 2.5-ms delay is triggered. After the delay, FAST OP DONE is generated to clear all fast motion-control flip-flops, and the second 2.5-ms delay is triggered. After this second delay time (5.0 ms total), the plotter flag sets.

When a slow-motion instruction is performed, the events occur in a manner similiar to the fast-motion operation. The slow-motion flip-flop (either PEN UP, or PEN DOWN) sets, and the first 35-ms delay is triggered. After this delay period, SLOW OP DONE is generated and the second 35-ms delay is triggered. SLOW OP DONE clears both the PEN UP and PEN DOWN motion-control flip-flops. After the second delay time (70 ms total) the plotter flag sets. This long delay time allows the drum to settle in position. This prevents erroneous or vague plots.

The plotter flag is set by the execution of any plotter-motion instruction. When this occurs, the IO BUS IN INT line activates (0V), and the IO BUS IN SKIP gate is partially enabled. IO BUS IN INT indicates to the PDP-8/I that a device is requesting service if the program interrupt facility is enabled. Under program control, the PDP-8/I then enters a search subroutine to determine which device caused the interrupt.

This search is performed by a series of "flag checking" skip instructions. A skip instruction is executed for each device attached to the interrupt line. The plotter flag status is checked by the 6501 instruction. When the plotter flag is set and this instruction is performed, the IO BUS IN SKIP gate is enabled, activating the skip line (0V). This line causes the PDP-8/I program counter to increment by one, skipping the next sequential instruction in the program. When 6501 results in a skipped instruction, the program enters a VP8/I service routine. Usually, instruction 6502 is the first command performed in this routine. This instruction clears the plotter flag. The next VP8/I motion instruction is then performed.

VP8/I INSTRUCTION DESCRIPTIONS

Table 1 describes each plotter instruction.

Table 1
VP8/I Instructions

Mnemonic	Octal Code	Operation
PLSF	6501	Skip On Plotter Flag. This instruction decodes to generate PLTR IOT, 50INST, and IOP1 to check the flag status. If the flag is set, IO BUS IN SKIP is generated.
PLCF	6502	Clear The Plotter Flag. This instruction decodes to generate PLTR IOT, 50INST, and IOP2 to clear the flag.
PLPU	6504	Pen Up. This instruction decodes to generate PLTR IOT, 50INST, and IOP4 to raise the plotter pen from the surface of the paper. PLPU is a slow operation.
PLPD	6524	Pen Down. After the drum and/or pen are moved, a PLPD instruction decodes to generate PLTR IOT, IOP4 and MB07(1). This lowers the pen to the surface of the paper. PLPD is a slow operation.
PLPR	6511	Pen Right. This instruction decodes to generate PLTR IOT, IOP1 and MB08(1) to move the plotter pen one increment to the right. It is a fast operation. This instruction can be combined with the drum up (6512) or drum down (6514) instruction to produce a diagonal plot.
PLPL	6521	Pen Left. This instruction decodes to generate PLTR IOT, IOP1 and MB07(1). It is a fast operation. PLPL moves the plotter pen one increment to the left. This instruction can be combined with the drum up (6522) instruction to produce a diagonal plot.
PLDU (PLUD)	6512 (6522)	Drum Up. These instructions decode to generate PLTR IOT, 50INST, and IOP2. Both instructions move the drum up one increment. Each is a fast operation. Both instructions are needed so the drum up motion can combine with pen right (pen left) motion instructions.
PLDD	6514	Drum Down. This instruction decodes to generate PLTR IOT, IOP4, and MB08(1). PLDD is a fast operation that moves the drum down one increment. It can combine with the PLPR instruction.

ENGINEERING DRAWINGS

The following drawings pertaining to the VP8/I are included in this section.

Drawing Number	Title	Revision
D-BS-VP8I-0-1	Plotter Control	C
D-CS-M704-0-1	Plotter Control	E

PR PL DU DD PU PD

15 4 3 1 2 9 10 — CANNON SK-19-21C-/2

C2 P2 R2 S2 T2 U2 V2 — W023 D02

HJ2 HL2 HN2 HR2 HT2 HV2

FAST OP DONE — PEN RIGHT — PEN LEFT — DRUM UP — DRUM DOWN — SLOW OP DONE — PEN UP — PEN DOWN

MB08 (1) HK2 C D — MB07 (1) HS2 C D — C D — MB08 (1) C D — C D — MB07 (1) C D

50 INST — HU2 — 50 INST

MB07 (0) — MB08 (0)

IOP1 (1) JH2 — PLTR IOT

PLTR IOT — HM2 JP2 — IOP 2 (1)

IOP4 (1) — PLTR IOT

IO BUS IN SKIP — JE2

IO BUS IN INT — JF2 — + 3V

PLTR IOT
IOP1 (1)
50 INST

PLTR IOT
IOP2 (1)
50 INST

PLTR FLAG

INITIALIZE — JN2 — INITIALIZE

HF2 HE2
MB03 (1) HH2 MB05 (1)
MB04 (0) HD2 MB06 (0)

MB07 (1)
MB08 (1)

PLTR IOT
IOP 4 (1) JVI
MB08 (0)

SS I 35 MS O — JK2 — SS I 35 MS O

INITIALIZE — JD2 — SLOW OP DONE

PLTR FLAG (0) JS2

IOP 4 (1) JT2
MB07 (0) JUI

IOP 1 (0) JL2
IOP 2 (0) JM2

PLTR IOT
50 INST

SS I 2.5 MS O — JJ2 — SS I 2.5 MS O

INITIALIZE — HP2 — FAST OP DONE

NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054

M704
HJ29

REVISIONS	REV	CHK
CHANGE NO. 12	A	
18	B	
81-00002	C	

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

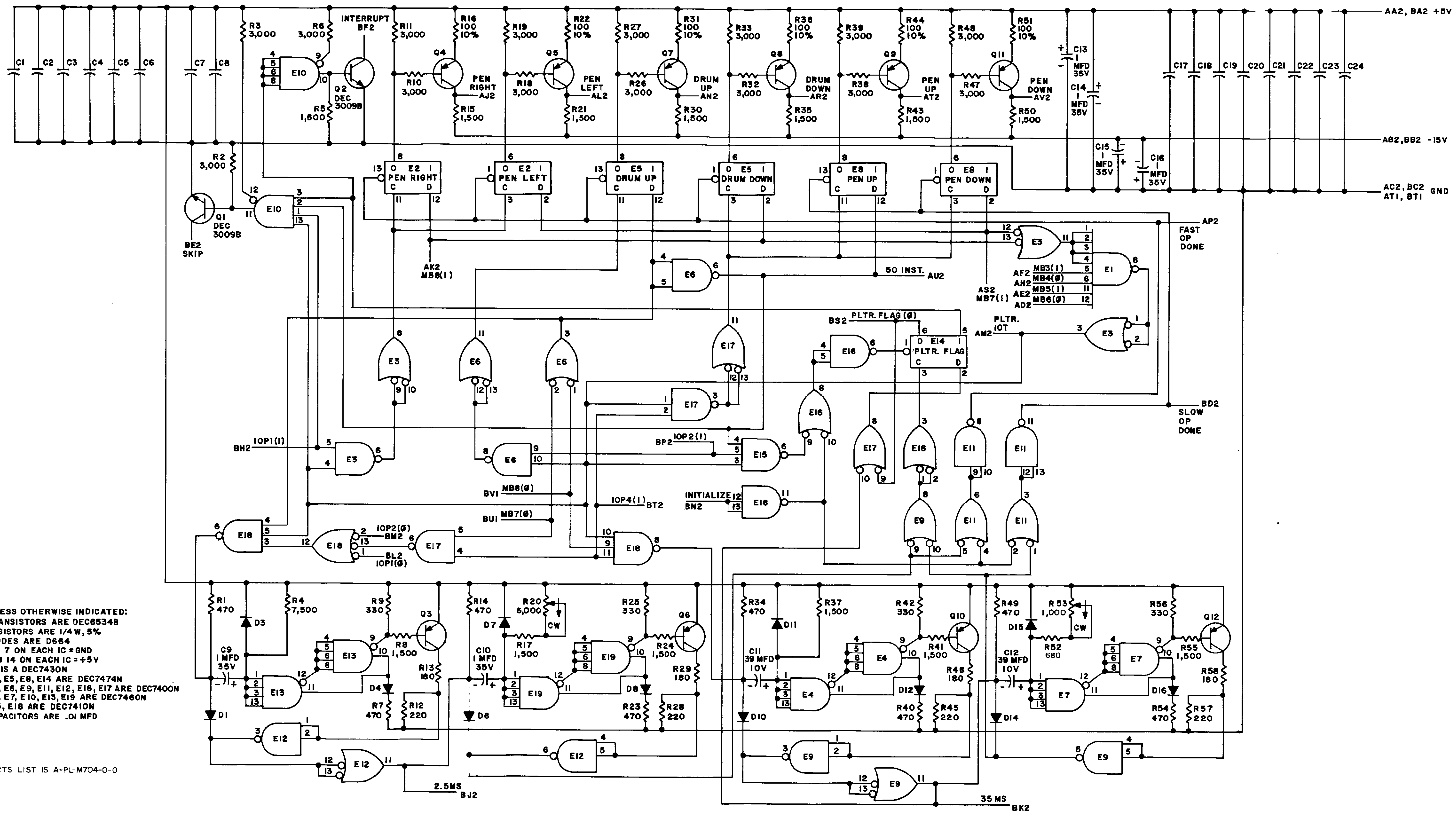
DRN. — DATE 5/12/67
CHK'D. — DATE 11-27-67
ENG. — DATE 11-25-67
PROJ ENG. — DATE 11-24-67
PROD. — DATE 11-25-67
FIRST USED ON
SCALE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE
PLOTTER CONTROL

SIZE D | CODE BS | NUMBER VP8I-0-1 | REV C
DIST.

DEC FORM NO DRD 102



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC6534B
RESISTORS ARE 1/4 W, 5%
DIODES ARE D664
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1 IS A DEC7430N
E2, E5, E8, E14 ARE DEC7474N
E3, E6, E9, E11, E12, E16, E17 ARE DEC7400N
E4, E7, E10, E13, E19 ARE DEC7460N
E15, E18 ARE DEC7410N
CAPACITORS ARE .01 MFD

PARTS LIST IS A-PL-M704-0-0

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC3009B	2N3009		
DEC6534B	MPS6534		
D664	IN3606		

DRN. M. Waller DATE 9-28-67
CHK'D R. Schneeman DATE 9/28/67
ENG. DATE 9/28/67
PROD. 2 DATE

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE PLOTTER CONTROL M704

SIZE D | CODE CS | NUMBER M704-0-1 | REV E

PRINTED CIRCUIT REV. B

DEC FORM NO. DRD 101

KW8/I
REAL-TIME CLOCK OPTION
FUNCTIONAL DESCRIPTION

KW8/I REAL-TIME CLOCK

INTRODUCTION

This option provides a method of accurately measuring time intervals. There are six KW8/I configurations. The basic KW8/I consists of a frequency source, and a clock control. The basic real-time clock configurations are: KW8/IA (M501 Line Frequency source); KW8/IB (M401 Variable Clock); and KW8/IC (M405 Crystal Clock).

An M709 Clock Control Module (M709) can be added to each of the basic clocks to provide six KW8/I configurations. The M709 Clock Counter contains preset and readout registers with associated controls. Addition of this module allows hardware -interval counting, reducing program instruction time; therefore, more efficient use is made of computer time. The real-time clock options are then designated as KW8/ID, KW8/IE, and KW8/IF, respectively. The logic for the KW8/I option is contained within the PDP-8/I processor main frame. The KW8/I maintenance procedures are the same as those of the PDP-8/I.

LOGIC DESCRIPTION

The following paragraphs describe the frequency-source configurations, the clock control logic, and the clock counter.

Frequency Sources

The frequency sources provide pulses at a specific frequency, to the clock control. Refer to Engineering Drawing BS-KW8I-0-1.

The M401 Variable Clock Source (KW8/IB) produces pulses only when enabled by CLOCK ENABLE. This enable level is generated by the M708 Clock Control when specific IOT instructions are performed (refer to KW8/I Instruction Descriptions). The initial pulse output from this clock is "masked" by the clock control, therefore, the first pulse allowed is approximately that of the clock period.

The Line Frequency Clock (KW8/IA) produces its output by stepping-down the line voltage through a clock transformer to 6.3 Vac. The frequency is either 50 Hz or 60 Hz depending on the line source, and is an important consideration in time-interval measurements. The stepped-down voltage is applied to a Schmitt trigger which generates a square wave used as the clock source.

The M405 Crystal Clock (KW8/IC), and the Line Frequency Clock (KW8/IA) outputs are asynchronous to program execution. This allows the variation of the first clock pulse occurrence to be as long as one full period. The variable clock has less inaccuracy in its first period because of the masking, therefore, the overall accuracy of the variable clock may exceed that of the crystal, or line frequency clocks.

The basic accuracy and stability of the KW8/I is that of the frequency source. The overall accuracy of the real-time clock, however, involves the clock frequency and its relationship to the instruction time of the service loop. The number of clock pulses counted in a time interval is also a consideration because of the inaccuracy of the first clock period. The clock period should be greater than the time required to service the loop including the skip and IOT instructions, to prevent occurrence of more than one pulse count during the service routine. A maximum frequency of 100 kHz is required for KW8/IA, B, and C configurations because of finite instruction time.

Clock Control

The M708 Clock Control decodes various IOT instructions to allow a skip and/or interrupt after a clock pulse has set the flag. Certain IOT commands may also enable or disable the M401 Variable Clock by generating CLOCK ENABLE. The interrupt flag (IF) may also be disabled preventing real-time clock operation.

When a clock pulse sets the flag, I/O BUS IN INT is generated, indicating to the PDP-8/I that an I/O device is requesting service. A subroutine is then entered, and the status of the flag is checked. If the flag contains a one, the service loop is performed. A PDP-8/I memory location is incremented to store the number of counts.

Clock Counter

The KW8/IA, B, and C configurations may be modified to become the KW8/ID, E, and F options by the addition of the M709 Clock Counter Module. This logic contains a counter register, an output buffer register, input/output gating, and control logic for loading reading, counting and synchronizing.

A number in the accumulator containing the desired number of counts is complemented, and incremented by the clock counter logic. The number is loaded into the count register by the CECL instruction which generates LOAD COUNTER in the M708 Clock Control. The rising edge of each clock pulse transfers the contents of the count register to the output buffer. The contents of this buffer can be read into the accumulator by the CRCA instruction without disturbing the contents of the count register. The count read is the last counter value if this instruction occurs during the clock pulse.

The trailing edge of the clock pulse increments the count register. When the desired number of counts minus one have occurred, OVERFLOW is generated. This level enables the flag within the M708 Clock Control, and permits the next clock pulse to set the flag, producing I/O BUS IN INT.

Since the addition of the M709 Clock Counter allows logic hardware to perform the counting function, when counts greater than 10 are performed, the maximum counting frequency can be extended to a limit imposed by the propogation delay of the counter. This limit is 1 MHz.

KW8/I INSTRUCTION DESCRIPTIONS

Table 1 lists the KW8/I instructions and contains descriptions of their operations.

Table 1
KW8/I Instruction Description

Mnemonic	Octal Code	KW8/I's Affected	Description
CCFF	6132	KW8/IA KW8/IB KW8/IC	The flag, flag buffer, clock enable, and interrupt enable flip-flops are cleared. This disables the real time clock.
CCEC	6136	KW8/IA KW8/IB KW8/IC	All clock control flip-flops are first cleared, then the clock enable flip-flop is set. For the variable frequency clock, the frequency source is enabled synchronously with program operation. With all clocks the data input to the flag is enabled after IOP2 time. This represents an 800-ns mask, after the clock is enabled.

Table 1 (Cont)
KW8/I Instruction Description

Mnemonic	Octal Code	KW8/I's Affected	Description
CECI	6137	KW8/IA KW8/IB KW8/IC	All clock control flip-flops are cleared, then the clock enable, and interrupt enable flip-flops are set. The clock enable flip-flop is described with the CCEC instruction. The interrupt enable flip-flop allows an IO BUS IN INT signal when the flag is set.
CSCF	6133	KW8/IA KW8/IB KW8/IC KW8/ID KW8/IE KW8/IF	When the flag flip-flop has been set by a clock pulse, the flag buffer flip-flop is set to a one. Upon execution of this instruction an IO BUS IN SKIP is generated if the flag is set. The content of the PC is incremented by one so the next sequential instruction is skipped. The flag flip-flop is then cleared. If the flag flip-flop has not been set, no skip is generated nor is the flag flip-flop cleared.
CCFF	6132	KW8/ID KW8/IE KW8/IF	The operations described above for this instruction are performed. In addition, the OVERFLOW gating is disabled.
CECL	6136	KW8/ID KW8/IE KW8/IF	The operations are the same as that of the CCEC instruction, except that the data input to the flag is not enabled until both CLOCK ENABLE and OVERFLOW are set. All M709 counter bits are set at IOP2, and then cleared according to the accumulator prior to IOP4. At IOP4 the contents of the counter (the one's complement of the accumulator) are transferred to the output buffer. At the end of IOP4, the counter is incremented by one to provide the two's complement of the accumulator.
CEIL	6137	KW8/ID KW8/IE KW8/IF	Operations are the same as those described in the CECI instruction, except that the M709 is loaded according to the CECL instruction.
CRCA	6134, or 6135	KW8/ID KW8/IE KW8/IF	The output buffer is gated to the I/O BUS during IOP4, and a CLK AC CLR signal generated. This register contains the last count in the count register. The transfer from the count register is synchronized with this instruction so that a transfer that would occur during this instruction is not made.

PROGRAMMING EXAMPLES

The following examples further clarify the KW8/I instruction set.

Counting in program for KW8/IA, KW8/IB, and KW8/IC clocks.

```
6136   CLR control flip-flops, enable clock.
6133   Skip and clear flag.
5---   JMP -1
2---   ISZ B
5---   JMP -3
```

Location B - Two's complement of desired count.

Counting with Preset and Read-out Clock (KW8/ID, KW8/IE, and KW8/IF)

```
7200   CLA
1---   TAD B
6137   CLR control flip-flops, enable clock,
       and interrupt.
```

Location B - Desired count of clock pulses.

The preset count register with the interrupt facility enabled allows a more efficient use of machine time. While counting out an interval of time, the machine can process other programs instead of looping.

Single count with KW8/I

```
6136   CLR control flip-flops, Enable Clock.
6133   Skip if flag is set.
5---   JMP -1
```

By using the Variable Clock (KW8/IB), one clock cycle can be counted accurately. This improvement of first cycle accuracy can be used for multiple counts either in a Fixed Interval Clock (KW8/IB), or with Preset and Read-out Counter (KW8/IE).

Measurement of an Interval.

```
7200   CLA
1---   TAD B
6136   CLR control flip-flops, enable
       clock and load counter
6---   Begin interval
  :
  :
6---   End of interval
6134
  or
6135   Read clock
```

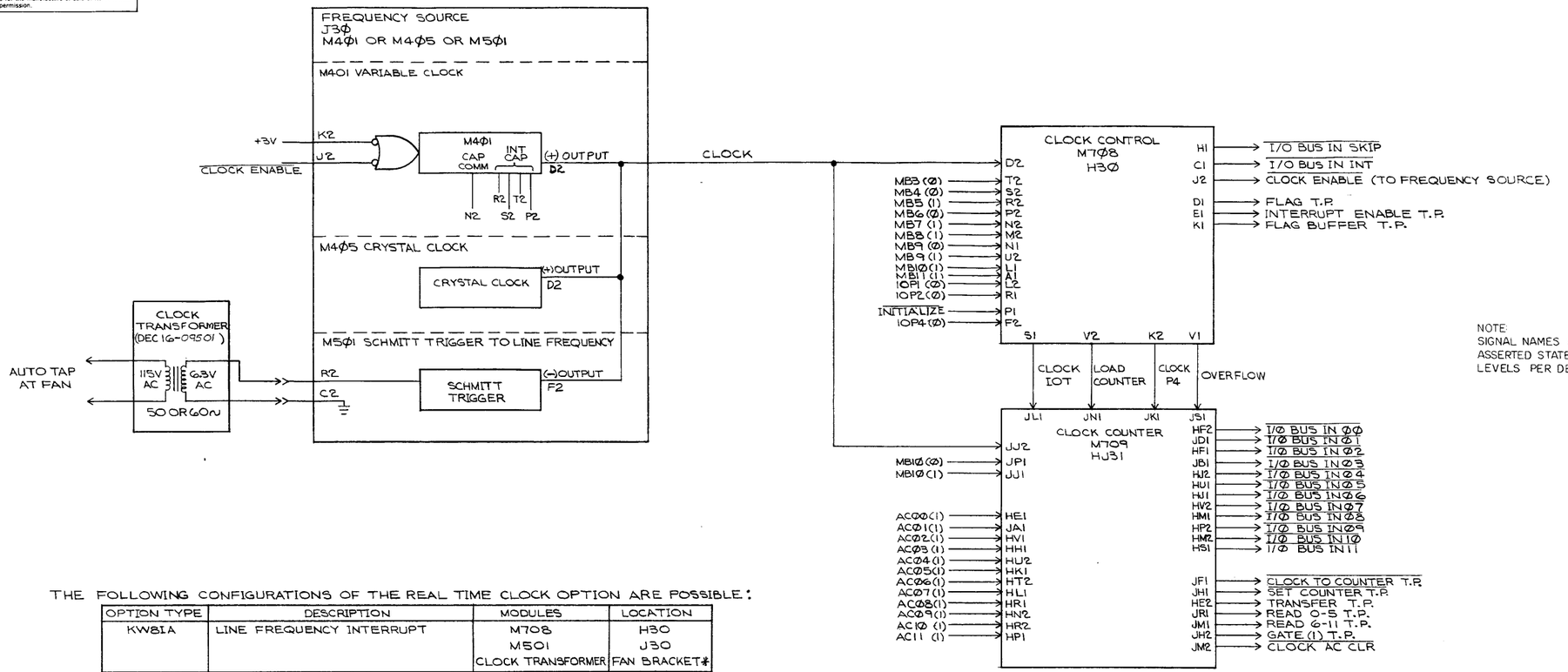
Location B - (0000_8), two's complement of zero.

The initialization of the preset and read-out clock with zero at the beginning of the interval allows a direct read-out of the number of clock pulses occurring during the interval. If the interval is greater than (7777_8) pulses, a service of OVERFLOW would have to be effected.

ENGINEERING DRAWINGS

The following drawings pertaining to the KW8/I are included in this section.

Drawing Number	Title	Rev.
D-BS-KW8I-0-1	Real Time Clock Option	C
D-BS-KW8I-0-2	Clock Control M708	A
D-BS-KW8I-0-3	Clock Counter M709	A
B-CS-M401-0-1	Clock	J
B-CS-M405-0-1	Not Available	-
B-CS-M501-0-1	Schmitt Trigger	A



NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054

THE FOLLOWING CONFIGURATIONS OF THE REAL TIME CLOCK OPTION ARE POSSIBLE:

OPTION TYPE	DESCRIPTION	MODULES	LOCATION
KW8IA	LINE FREQUENCY INTERRUPT	M708 M501 CLOCK TRANSFORMER	H3Ø J3Ø FAN BRACKET*
KW8IB	VARIABLE CLOCK INTERRUPT	M708 M401	H3Ø J3Ø
KW8IC	CRYSTAL CLOCK INTERRUPT	M708 M405	H3Ø J3Ø
KW8ID	KW8IA WITH PRESET AND READOUT	M708 M709 M501 CLOCK TRANSFORMER	H3Ø HJ31 J3Ø FAN BRACKET*
KW8IE	KW8IB WITH PRESET AND READOUT	M708 M709 M401	H3Ø HJ31 J3Ø
KW8IF	KW8IC WITH PRESET AND READOUT	M708 M709 M405	H3Ø HJ31 J3Ø

* MTG & WIRING INFORMATION ON PRINT # D-UA-KW8I-Ø-Ø

REVISIONS		
CHK	CHANGE NO.	REV
[illegible]	RT-00002	A
W.S. Hunt 7-12-68		
[illegible]	BI-00009	B
[illegible]		
OLOUGHLIN	BI CC046	C
ARSENAULT		

DEC FORM NO DRD 102 A

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

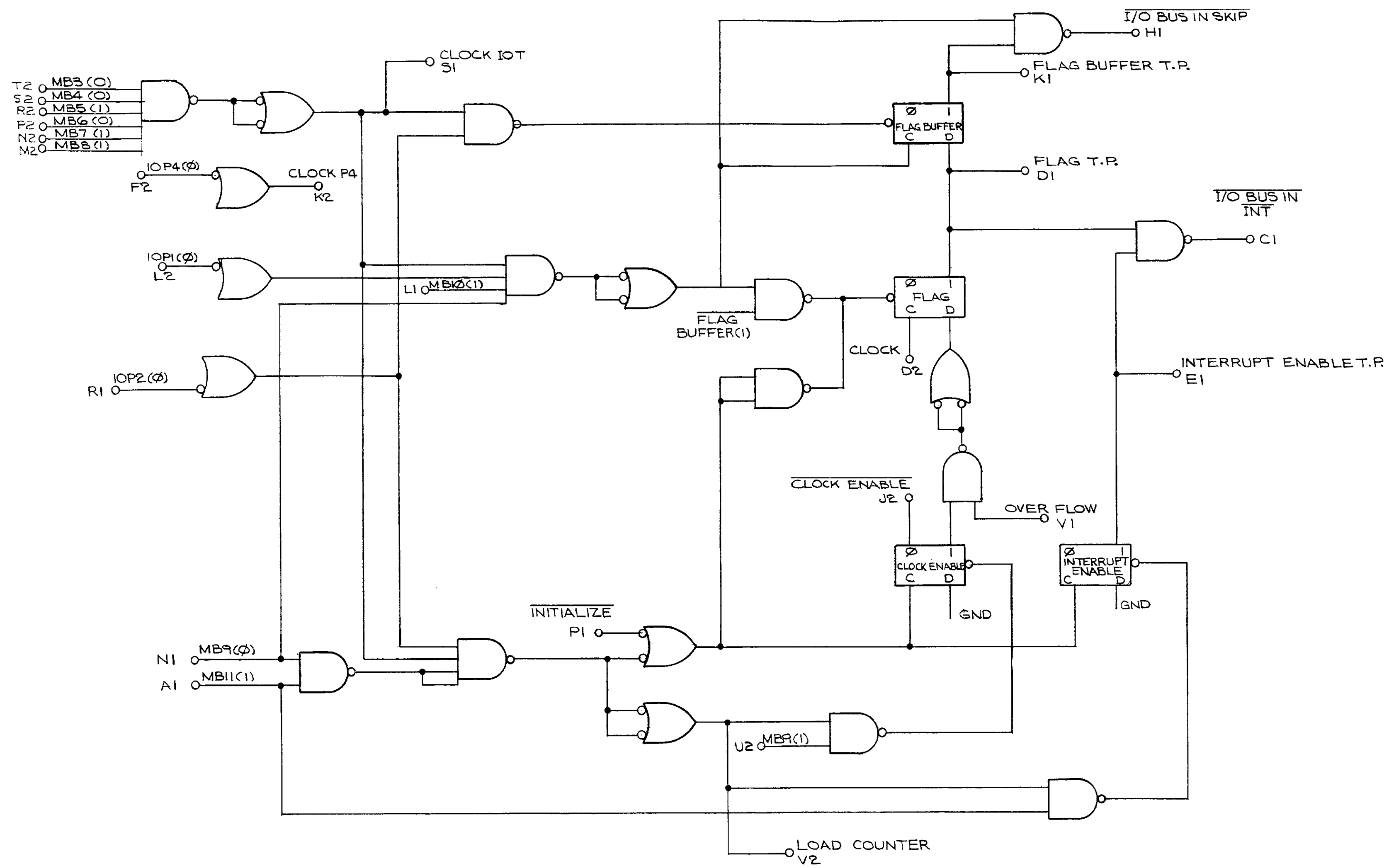
DRN	J. Madden	DATE 4/9/68
CHK'D	[illegible]	DATE 4/24/68
ENG.	[illegible]	DATE 5/2/68
PROJ. ENG.	[illegible]	DATE 5/2/68
PROD.	[illegible]	DATE 5/7/68

FIRST USED ON D-UA-KW8I-Ø-Ø
SCALE
SHEET OF

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE
REAL TIME CLOCK OPTION KW8I

SIZE D | CODE BS | NUMBER KW8I-Ø-1 | REV C
DIST.



NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —
FINISH —

DRN. DATE 4/4/68
CHK'D. DATE 4/29/68
ENG. DATE 5/2/67
PROJ. ENG. DATE 5/2/67
PROD. DATE 5/2/65
FIRST USED ON D-UA-KW8I-Ø-Ø
SCALE —
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

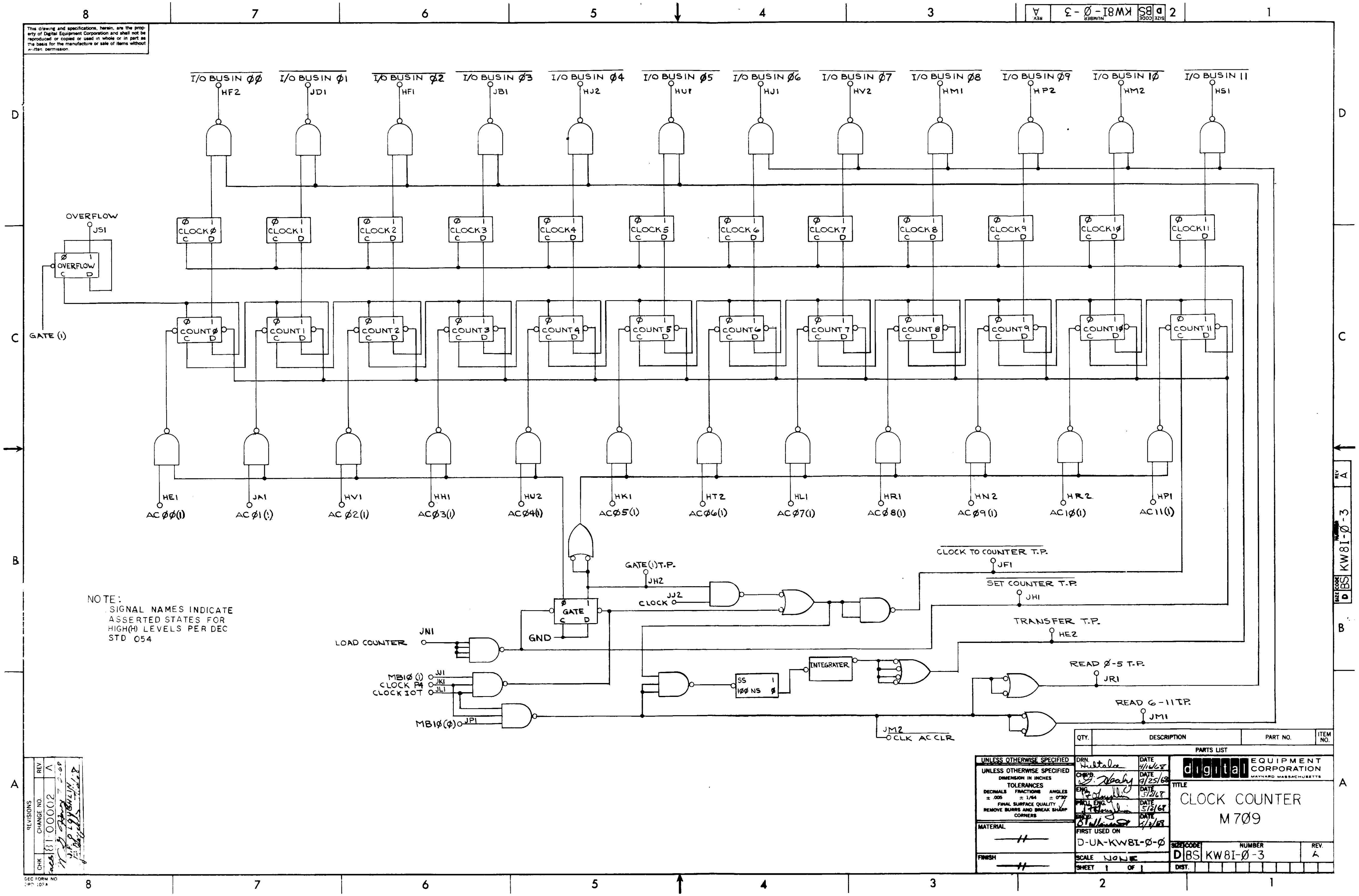
TITLE
CLOCK CONTROL M708

SIZE D CODE BS NUMBER KW8I-Ø-2 REV. A

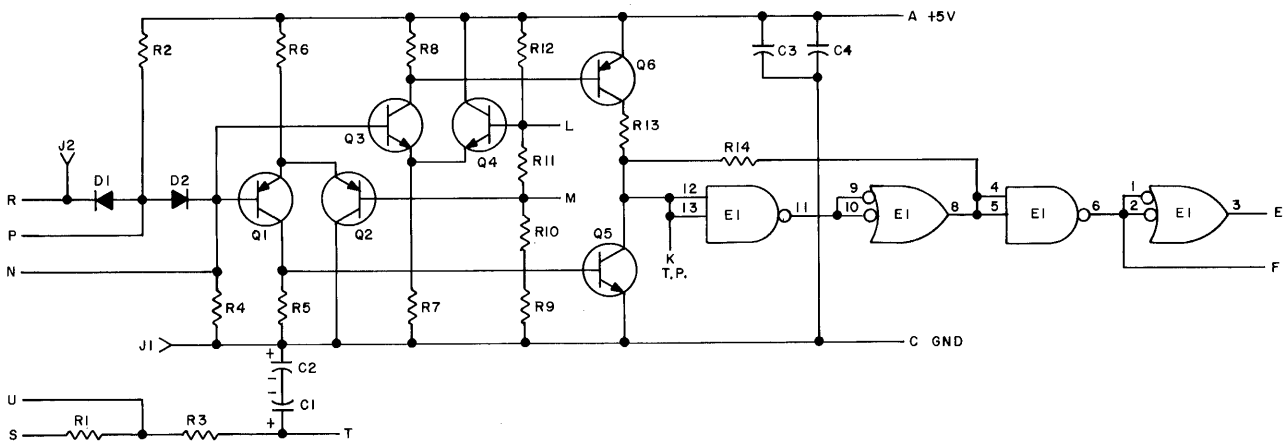
REVISIONS: REV. A, CHANGE NO. CI-00002, O'LOUGHLIN

DEC FORM NO DRD 102A

1-RTC9

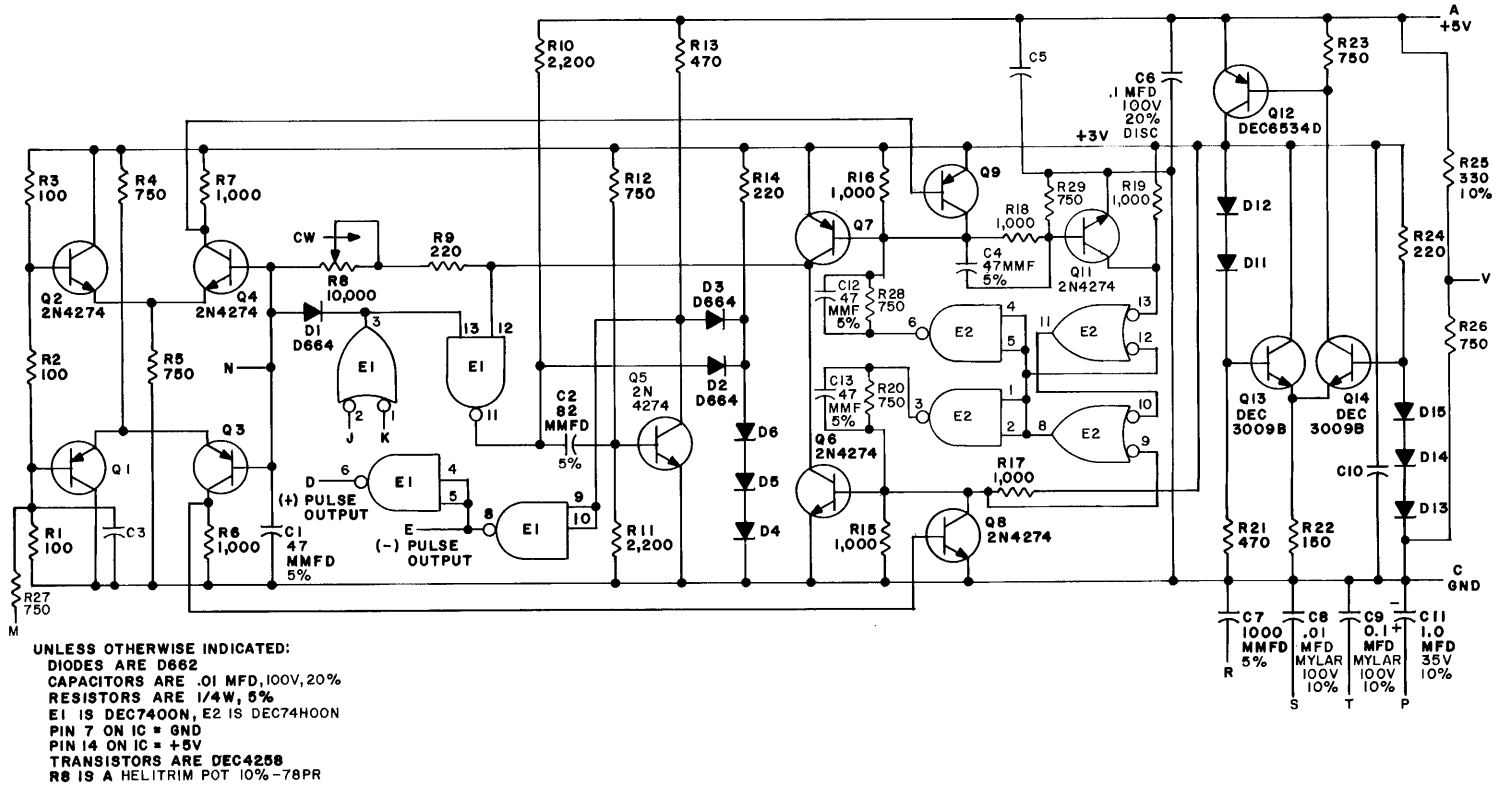

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.
I/O BUS IN ØØ HF2
I/O BUS IN Ø1 JD1
I/O BUS IN Ø2 HF1
I/O BUS IN Ø3 JB1
I/O BUS IN Ø4 HJ2
I/O BUS IN Ø5 HU1
I/O BUS IN Ø6 HJ1
I/O BUS IN Ø7 HV2
I/O BUS IN Ø8 HM1
I/O BUS IN Ø9 HP2
I/O BUS IN 1Ø HM2
I/O BUS IN 11 HS1
OVERFLOW JS1
OVERFLOW
CLOCK Ø
CLOCK 1
CLOCK 2
CLOCK 3
CLOCK 4
CLOCK 5
CLOCK 6
CLOCK 7
CLOCK 8
CLOCK 9
CLOCK 1Ø
CLOCK 11
GATE (1)
COUNT Ø
COUNT 1
COUNT 2
COUNT 3
COUNT 4
COUNT 5
COUNT 6
COUNT 7
COUNT 8
COUNT 9
COUNT 1Ø
COUNT 11
HE1 ACØØ(1)
JA1 ACØ1(1)
HV1 ACØ2(1)
HH1 ACØ3(1)
HU2 ACØ4(1)
HK1 ACØ5(1)
HT2 ACØ6(1)
HL1 ACØ7(1)
HR1 ACØ8(1)
HN2 ACØ9(1)
HR2 AC1Ø(1)
HP1 AC11(1)
NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH(H) LEVELS PER DEC STD 054
GATE(1)T.P. JH2
JJ2 CLOCK
GATE
GND
CLOCK TO COUNTER T.P. JF1
SET COUNTER T.P. JH1
TRANSFER T.P. HE2
LOAD COUNTER JN1
MB1Ø (1) JJ1
CLOCK P4 JK1
CLOCK IOT JL1
MB1Ø(Ø) JP1
SS 1 1ØØ NS Ø
INTEGRATER
READ Ø-5 T.P. JR1
READ 6-11 T.P. JM1
JM2 CLK AC CLR
QTY. DESCRIPTION PART NO. ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN. DATE 4/16/68
CHKD. DATE 4/25/68
ENG. DATE 5/1/68
PROJ. ENG. DATE 5/3/68
PROD. DATE 4/8/68
FIRST USED ON D-UA-KW8I-Ø-Ø
SCALE NONE
SHEET 1 OF 1
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
TITLE CLOCK COUNTER M7Ø9
SIZE D CODE BS NUMBER KW8I-Ø-3 REV. A
REVISIONS REV CHANGE NO. A 81-00012
DEC FORM NO.

I-RTC11



NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

B-CS-M501-0-1 Schmitt Trigger



UNLESS OTHERWISE INDICATED:
DIODES ARE D662
CAPACITORS ARE .01 MFD, 100V, 20%
RESISTORS ARE 1/4W, 5%
E1 IS DEC7400N, E2 IS DEC74H00N
PIN 7 ON IC = GND
PIN 14 ON IC = +5V
TRANSISTORS ARE DEC4258
R8 IS A HELITRIM POT 10%-78PR

B-CS-M401-0-1 Clock

I-RTC13

PART II

ENGINEERING DRAWINGS

ENGINEERING DRAWINGS

This Section contains reduced copies of DEC block schematics, circuit schematics, and other engineering drawings necessary for understanding and maintaining this equipment. Only those drawings which are essential and are not available in the referenced pertinent documents are included. Should any discrepancy exist between the drawings in this chapter and those supplied with the equipment, assume that the latter drawings are correct.

DRAWING NUMBERS

DEC engineering drawing numbers contain five groups of information, separated by hyphens. A drawing number such as BS-D-9999-1-5 consists of the following information reading from left to right: a 2- or 3-letter code specifying the type of drawing (BS); a 1-letter code specifying the size of the original drawing (D); the type number of the equipment (9999); the manufacturing series of the equipment (1); and the drawing number within a particular series (5). The drawing type codes are:

BS	block schematic or logic diagram	PW	power wiring
CD	cable diagram	RS	replacement schematic
CL	cable list	UML	utilization module list
CS	circuit schematic	WD	wiring diagram
FD	flow diagram	WL	wiring list

CIRCUIT SYMBOLS

Block schematic engineering drawings of DEC equipment indicate signal flow, logical functions, circuit type and physical location, wiring, and other pertinent information. Individual circuits are shown in block or semiblock form, using symbols that define circuit operation. These symbols are similar to those appearing in both the FLIP CHIP Modules Catalog and the System Modules Catalog but are often simplified.

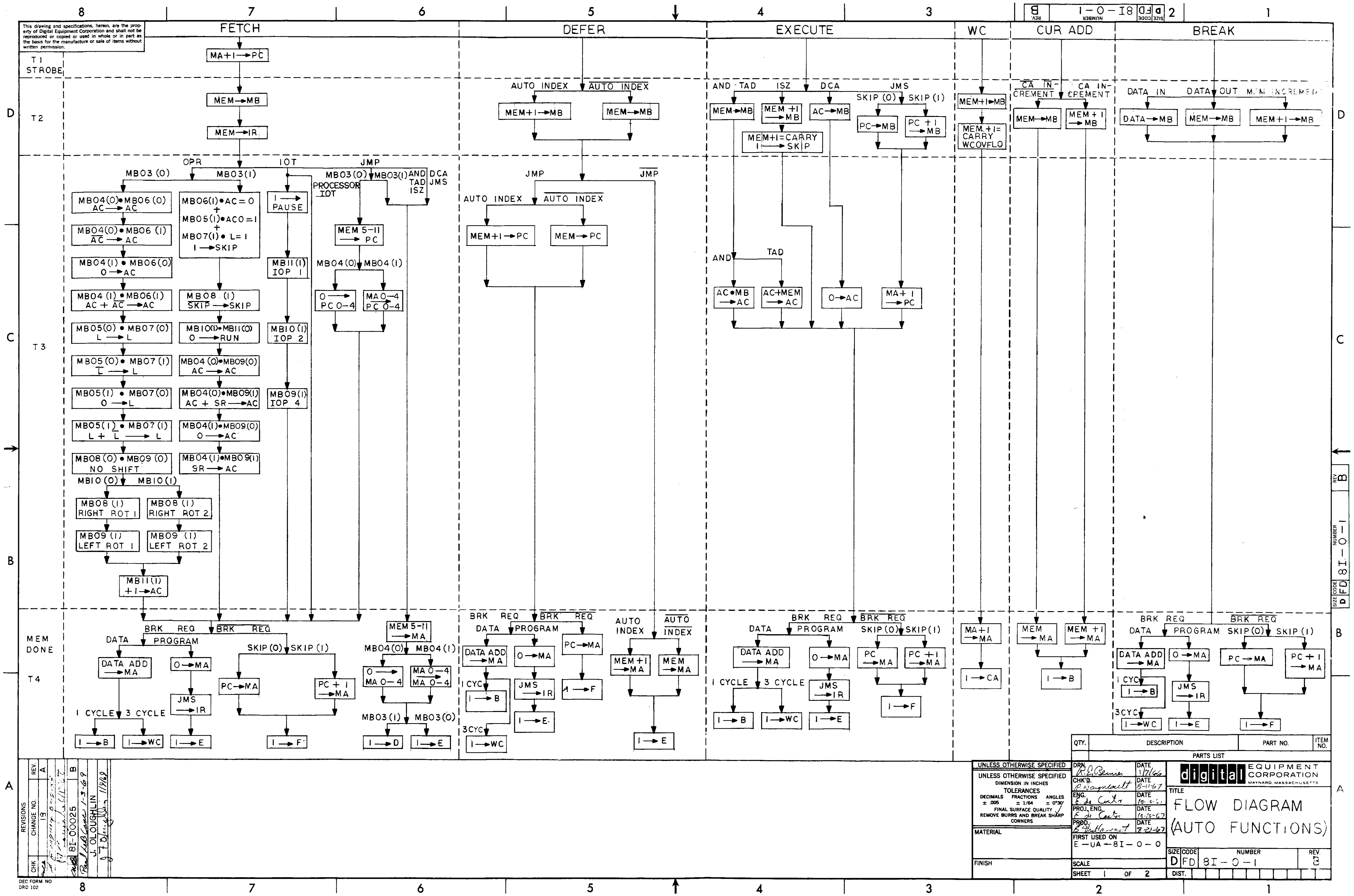
LOCATION DESIGNATIONS

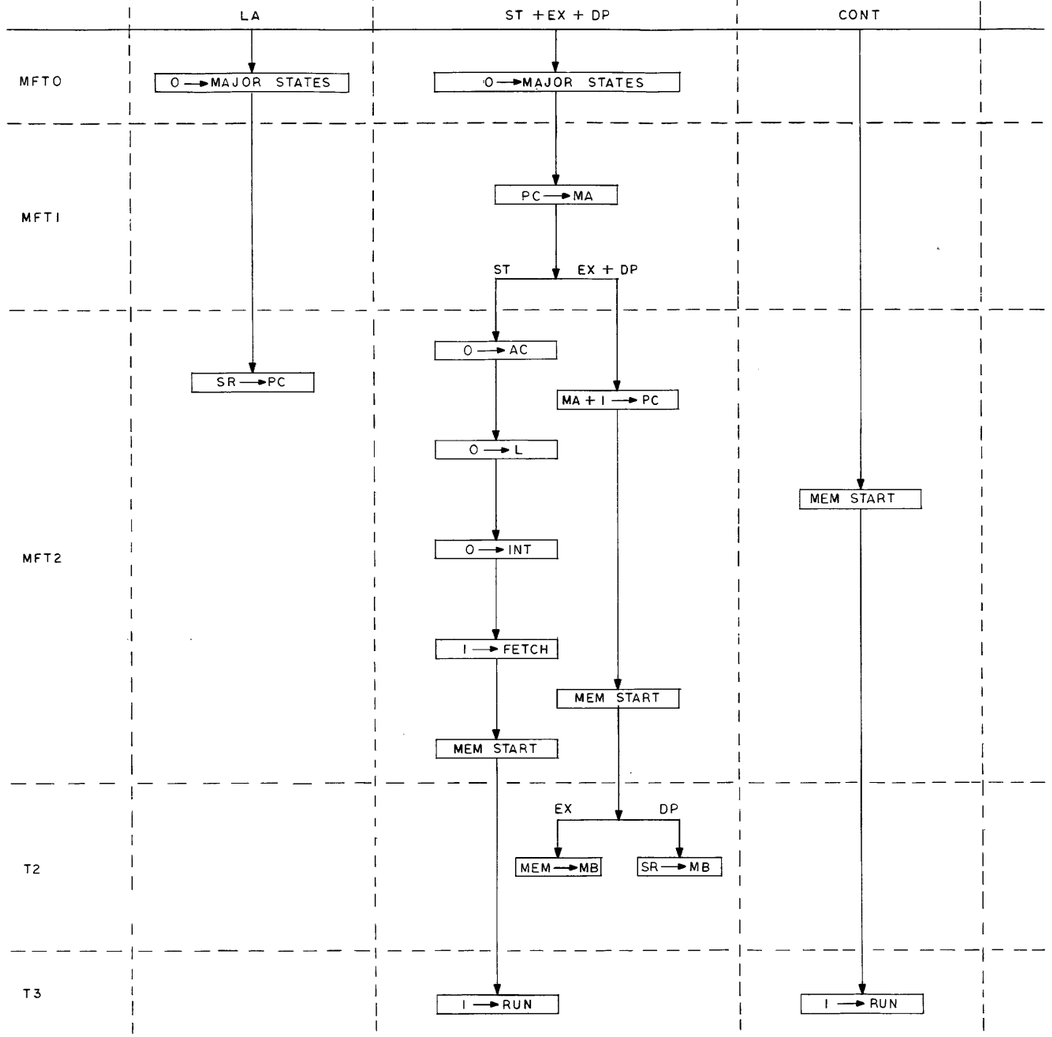
The following scheme is used to specify signal locations. The first capital letter designates one of the horizontal rows of modules within the mounting frame. The module receptacles within these rows are numbered from left to right as viewed from the wiring side. The module receptacle number follows the first capital letter. The second capital letter denotes the pin location. Finally, the last number specifies the group. Since M-series modules are double-sided, they consist of two groups of 18 connectors, each containing all of the letters except G, I, O and Q; this number specifies the group. For example, the signal BMB08(0) terminates at location J04M2. This location is found in row J, the fourth cable connector slot, pin M on side 2.

ENGINEERING DRAWINGS

Drawing Number	Title	Rev.
D-FD-8I-0-1	Flow Diagram	B
D-BS-8I-0-2	Timing Manual Functions and Run	Z
D-BS-8I-0-3	Instruction Reg and Major States	J
D-BS-8I-0-4	Reg Output Gate Control	J
D-BS-8I-0-5	Shift and Carry Gate Control	H
D-BS-8I-0-6	Reg Input Control and Skip	H
D-BS-8I-0-7	Interrupt and Break Control	L
D-BS-8I-0-8	Major Registers	E

Drawing Number	Title	Rev.
D-BS-8I-0-9	Major Registers Gating	E
D-BS-8I-0-10	I/O Level Converter	E
D-BS-8I-0-11	Teletype Receivers	D
D-BS-8I-0-12	Teletype Transmitter	C
D-BS-8I-0-13	Memory Control	F
D-BS-8I-0-14	Sense Ampls and Inhibit Drivers	D -
D-BS-8I-0-15	X Axis Selection	C
D-BS-8I-0-16	Y Axis Selection	C
Circuit Schematics		
D-CS-A607-0-1	10 Bit D-A Converter	C
B-CS-G020-0-1	Sense Amplifier	H
B-CS-G021-0-1	Sense Amplifier	H
B-CS-G221-0-1	Memory Selector	D
B-CS-G228-0-1	Inhibit Driver	E
B-CS-G624-0-1	Resistor Board	D
B-CS-G805-0-1	Negative Regulator	F
C-CS-G826-0-1	Regulator Control	L
B-CS-M040-0-1	Solenoid Driver	E
B-CS-M113-0-1	10-2 Input NAND Gates	C
B-CS-M115-0-1	8-3 Input NAND Gates	C
B-CS-M117-0-1	6-4 Input NAND Gates	E
B-CS-M160-0-1	Gate Module	B
B-CS-M162-0-1	Parity Circuit	A
B-CS-M216-0-1	Six Flip-Flops	B
D-CS-M220-0-1	Major Registers	C
B-CS-M310-0-1	Delay Line	D
B-CS-M360-0-1	Variable Delay	B
B-CS-M401-0-1	Clock	J
B-CS-M452-0-1	Variable Clock	A
B-CS-M501-0-1	Schmitt Trigger	A
B-CS-M506-0-1	Negative Input Converter	D
B-CS-M617-0-1	6-4 Input NOR Buffers	B
B-CS-M650-0-1	Negative Output Converter	C
C-CS-M700-0-1	Manual Timing Generator	B
C-CS-M701-0-1	Display Control	D
B-CS-M703-0-1	Power Fail	F
D-CS-M704-0-1	Plotter Control	E
C-CS-M705-0-1	Reader Control	B
C-CS-M706-0-1	Teletype Receiver	L
C-CS-M707-0-1	Teletype Transmitter	D
C-CS-M710-0-1	Punch Control	C
C-CS-M715-0-1	Reader Clock	F
B-CS-M720-0-1	Memory Detection	A


This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.
FETCH
DEFER
EXECUTE
WC
CUR ADD
BREAK
T1 STROBE
T2
T3
MEM DONE
T4
MA+1→PC
MEM→MB
MEM→IR
OPR
IOT
JMP
MB03(0)
MB03(1)
MB04(0)•MB06(0) AC→AC
MB04(0)•MB06(1) AC→AC
MB04(1)•MB06(0) 0→AC
MB04(1)•MB06(1) AC+AC→AC
MB05(0)•MB07(0) L→L
MB05(0)•MB07(1) L→L
MB05(1)•MB07(0) 0→L
MB05(1)•MB07(1) L+L→L
MB08(0)•MB09(0) NO SHIFT
MB10(0)
MB10(1)
MB08(1) RIGHT ROT 1
MB08(1) RIGHT ROT 2
MB09(1) LEFT ROT 1
MB09(1) LEFT ROT 2
MB11(1) +1→AC
MB06(1)•AC=0 + MB05(1)•AC0=1 + MB07(1)•L=1 1→SKIP
MB08(1) SKIP→SKIP
MB10(1)•MB11(0) 0→RUN
MB04(0)•MB09(0) AC→AC
MB04(0)•MB09(1) AC+SR→AC
MB04(1)•MB09(0) 0→AC
MB04(1)•MB09(1) SR→AC
1→PAUSE
MB11(1) IOP 1
MB10(1) IOP 2
MB09(1) IOP 4
PROCESSOR IOT
MB03(0)
MB03(1)
AND TAD ISZ
DCA JMS
MEM 5-11 → PC
MB04(0)
MB04(1)
0→PC 0-4
MA 0-4 → PC 0-4
BRK REQ
BRK REQ
DATA
PROGRAM
DATA ADD→MA
0→MA
JMS→IR
1 CYCLE
3 CYCLE
1→B
1→WC
1→E
SKIP (0)
SKIP (1)
PC→MA
PC+1→MA
1→F
MEM 5-11→MA
0→MA 0-4
MA 0-4→MA 0-4
MB03(1)
MB03(0)
1→D
AUTO INDEX
AUTO INDEX
MEM+1→MB
MEM→MB
JMP
JMP
MEM+1→PC
MEM→PC
1 CYC
3 CYC
MEM+1→MA
MEM→MA
AND
TAD
ISZ
DCA
JMS
SKIP (0)
SKIP (1)
MEM+1
MEM+1=CARRY 1→SKIP
AC→MB
PC→MB
PC+1→MB
AC•MB→AC
AC+MEM→AC
0→AC
MA+1→PC
MEM+1→MB
MEM+1=CARRY WCOVFLO
MA+1→MA
1→CA
CA INCREMENT
CA INCREMENT
MEM→MB
MEM+1→MB
MEM→MA
MEM+1→MA
DATA IN
DATA OUT
MEM INCREMENT
DATA→MB
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN. DATE 1/7/66
CHK'D.
ENG.
PROJ. ENG.
PROD.
FIRST USED ON E-UA-8I-0-0
SCALE
SHEET 1 OF 2
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE FLOW DIAGRAM (AUTO FUNCTIONS)
SIZE D CODE FD NUMBER 8I-0-1 REV. B
DIST.
REVISIONS
REV. A CHANGE NO. 19
REV. B 8I-00025 J. OLOUGHLIN
DEC FORM NO DRD 102



QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. R. J. Berner	DATE 2/7/67	
CHK'D. P. Marineault	DATE 3-11-67	
ENG. R. de Castro	DATE 10-6-67	
PROJ. ENG. R. de Castro	DATE 10-10-67	
PROG. A. Guillemette	DATE 8-21-67	

FIRST USED ON
E-UA-8I-0-0

SCALE

SHEET 2 OF 2

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

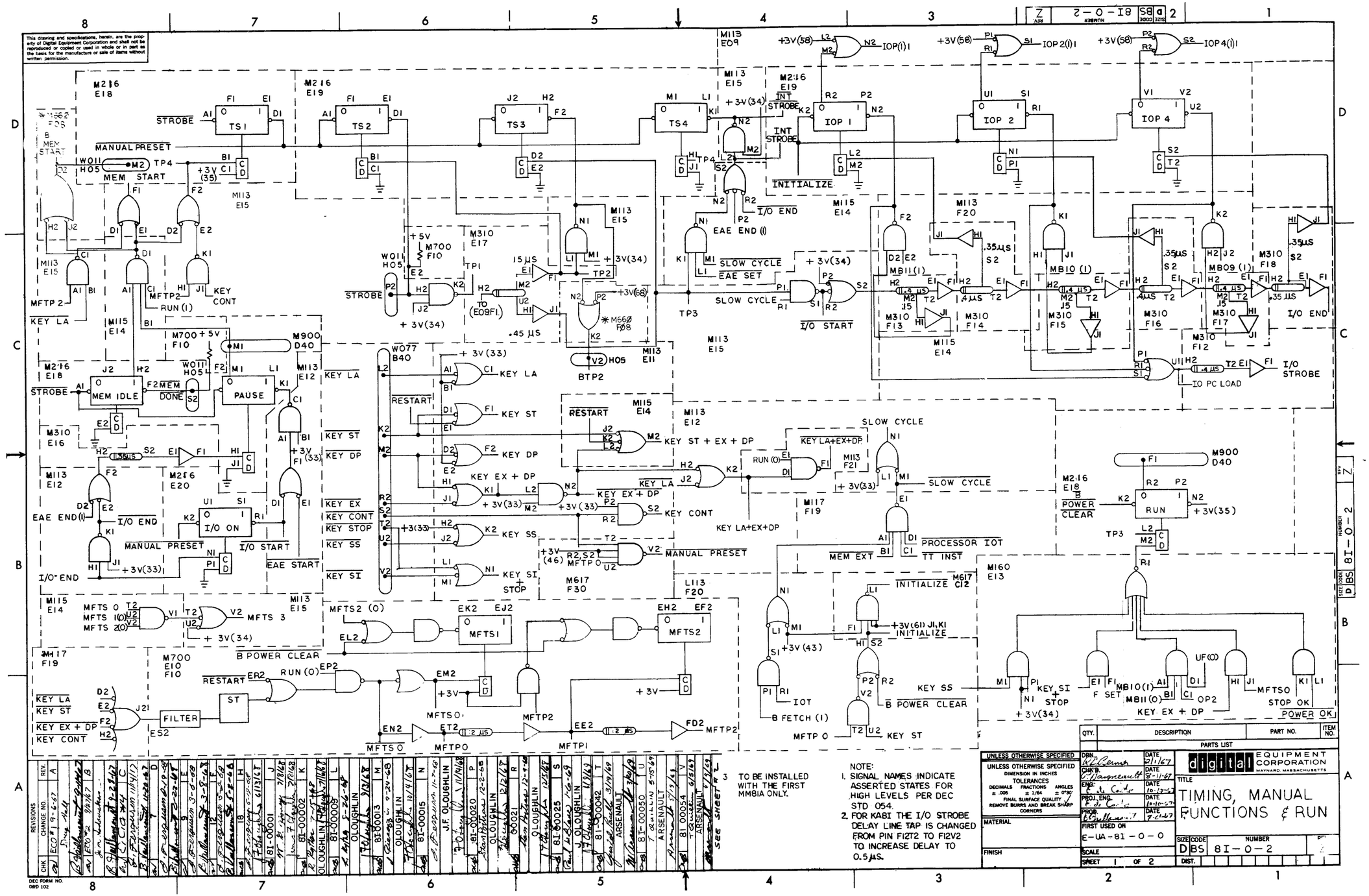
TITLE
FLOW DIAGRAM
(MAN FUNCTIONS)

SIZE	CODE	NUMBER	REV.
D	FD	8I-0-1	B

DIST.

REVISIONS | REV. | CHANGE NO. | CHK

DEC FORM NO ORD 102



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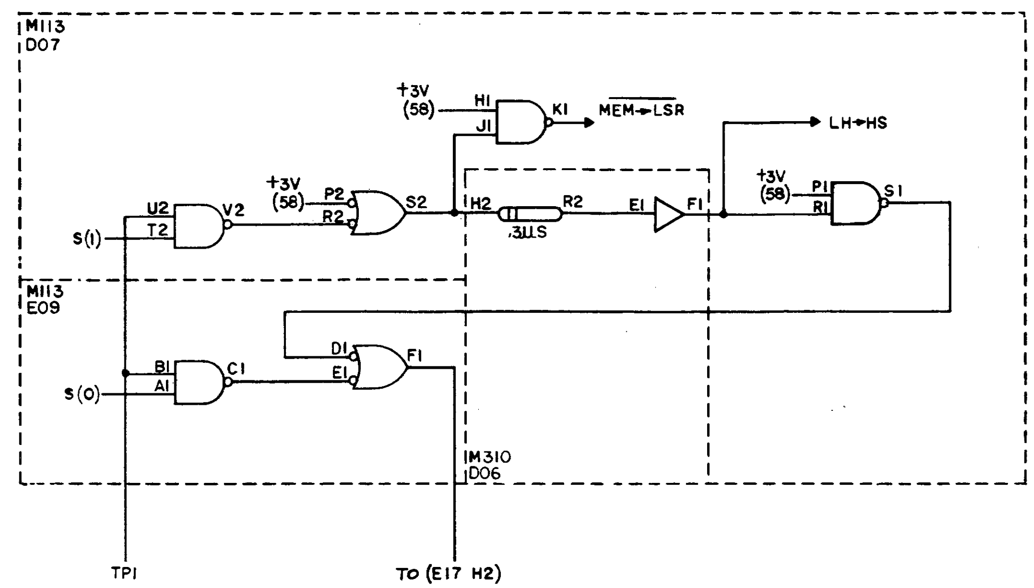


CHK	CHANGE NO.	REV.
	8I 00081 T Quill 11-3-69	W
	ARSENAULT	
R.P.	8I-00085 12-5-69	Y
	M. ARSENAULT 12/9/69	
	8I-00086 12-11-69	Z
	M. ARSENAULT 12/11/69	

REVISIONS

DEC FORM NO. DRD 102A

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

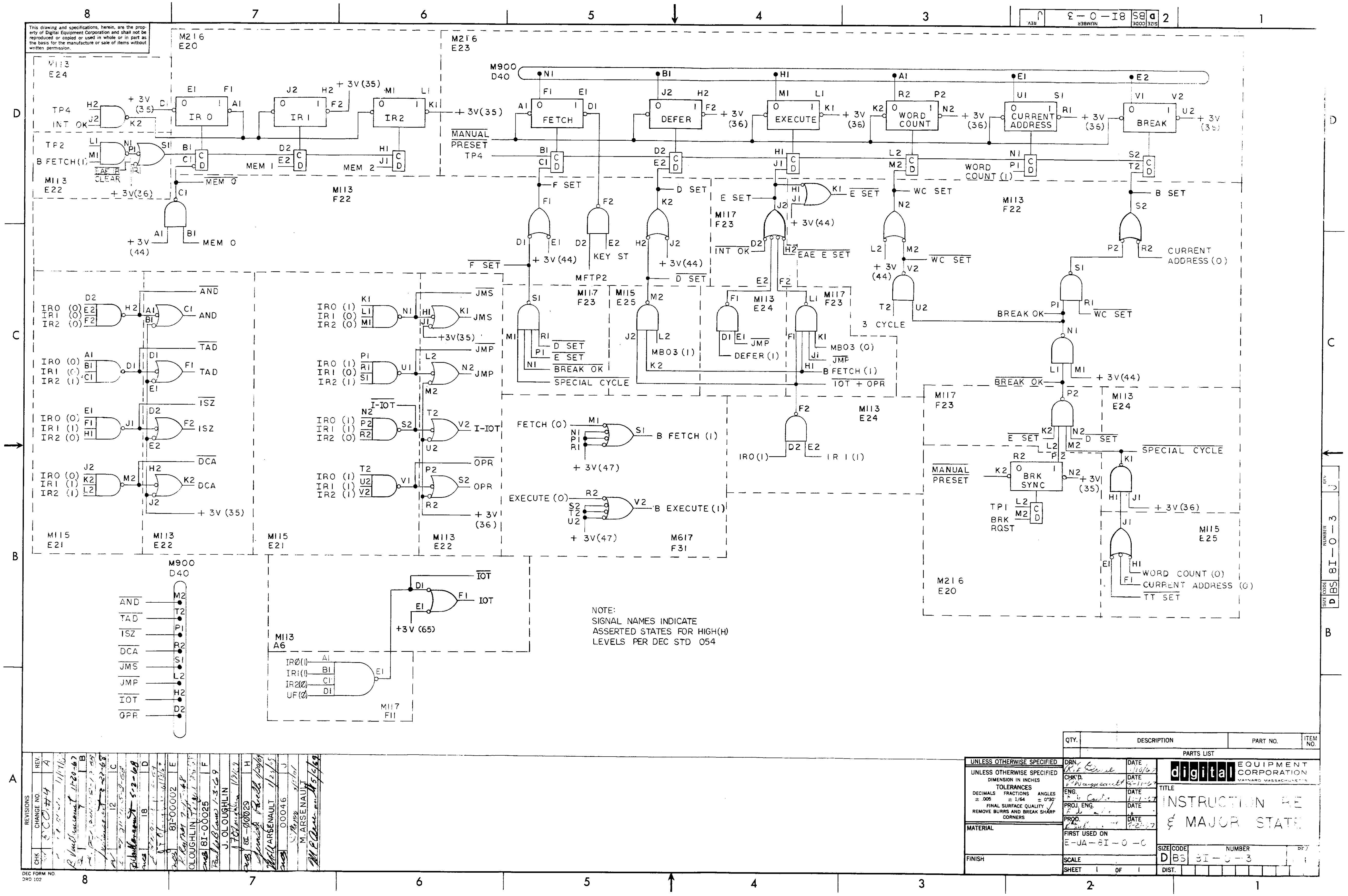
DRN. DATE 9-24-68
CHK'D. DATE
ENG. DATE
PROJ. ENG. DATE
PROD. DATE
FIRST USED ON E-UA-8I-0-0
SCALE
SHEET 2 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
TIMING MANUAL
FUNCTIONS & RUN

SIZE D CODE BS NUMBER 8I-0-2 REV. Z

DIST.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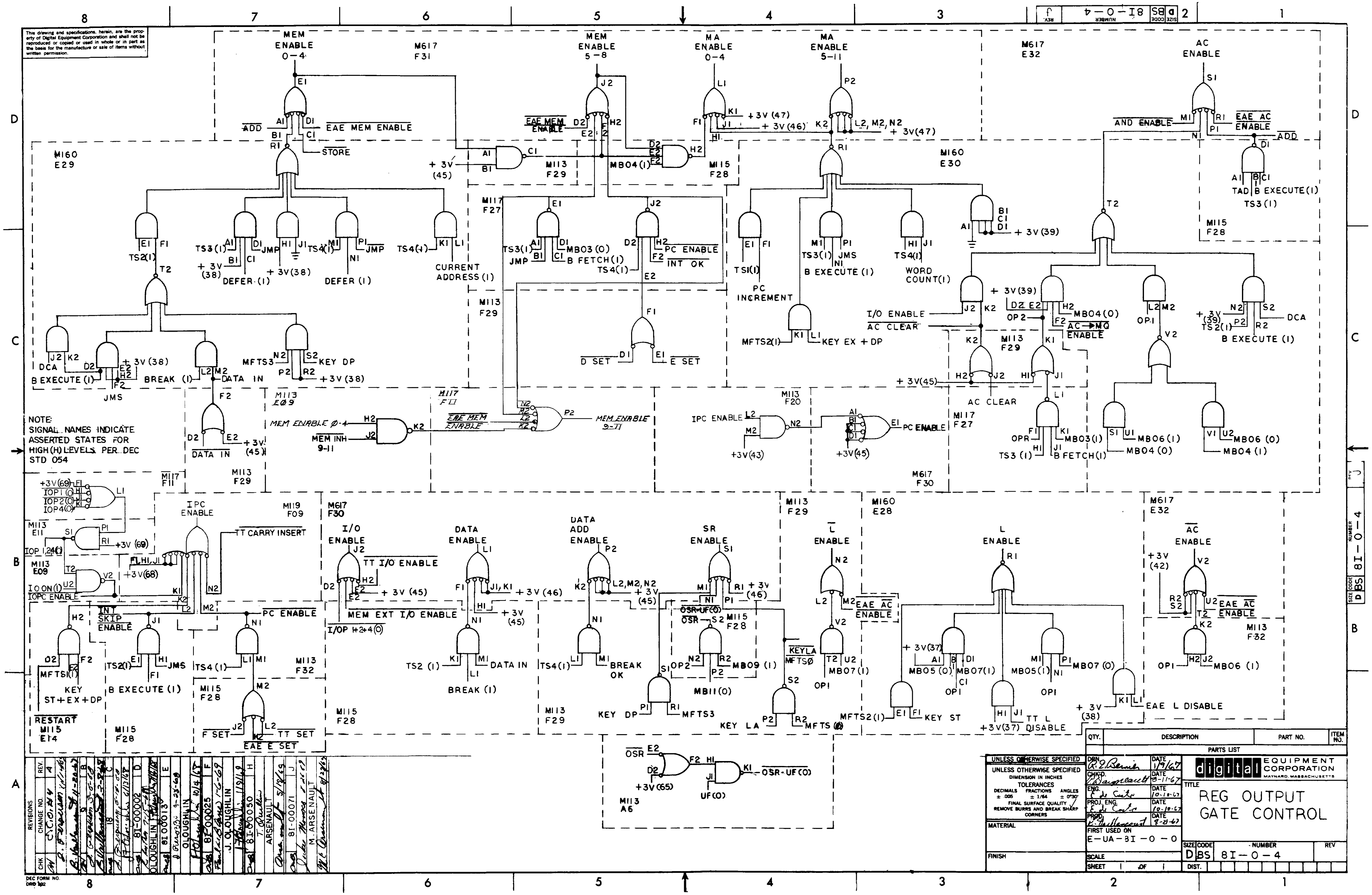
D BS 8I-0-3 J
M216 E20
M216 E23
M113 E24
M900 D40
TP4
INT OK
TP2
B FETCH (1)
M113 E22
IR 0
IR 1
IR 2
MEM 1
MEM 2
MEM 0
M113 F22
FETCH
DEFER
EXECUTE
WORD COUNT
CURRENT ADDRESS
BREAK
MANUAL PRESET
F SET
D SET
E SET
WC SET
B SET
M117 F23
INT OK
EAE E SET
KEY ST
MFTP2
M115 E25
M113 E24
3 CYCLE
BREAK OK
CURRENT ADDRESS (0)
D SET
E SET
BREAK OK
SPECIAL CYCLE
MB03 (1)
DEFER (1)
JMP
MB03 (0)
B FETCH (1)
IOT + OPR
AND
TAD
ISZ
DCA
JMS
JMP
I-IOT
OPR
IOT
M115 E21
M113 E22
FETCH (0)
B FETCH (1)
EXECUTE (0)
B EXECUTE (1)
M617 F31
IR 0 (1)
IR 1 (1)
M113 A6
M117 F11
BRK SYNC
BRK RQST
SPECIAL CYCLE
WORD COUNT (0)
CURRENT ADDRESS (0)
TT SET
M216 E20
M115 E25
NOTE:
SIGNAL NAMES INDICATE
ASSERTED STATES FOR HIGH(H)
LEVELS PER DEC STD 054
QTY. DESCRIPTION PART NO. ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE
INSTRUCTION RE & MAJOR STATE
FIRST USED ON E-JA-8I-0-0
SIZE D CODE BS NUMBER 8I-0-3
SHEET 1 OF 1
DEC FORM NO. DRD 102
REVISIONS
8I-00002
OLOUGHLIN
8I-00025
J. OLOUGHLIN
ARSENAULT
00046
M. ARSENAULT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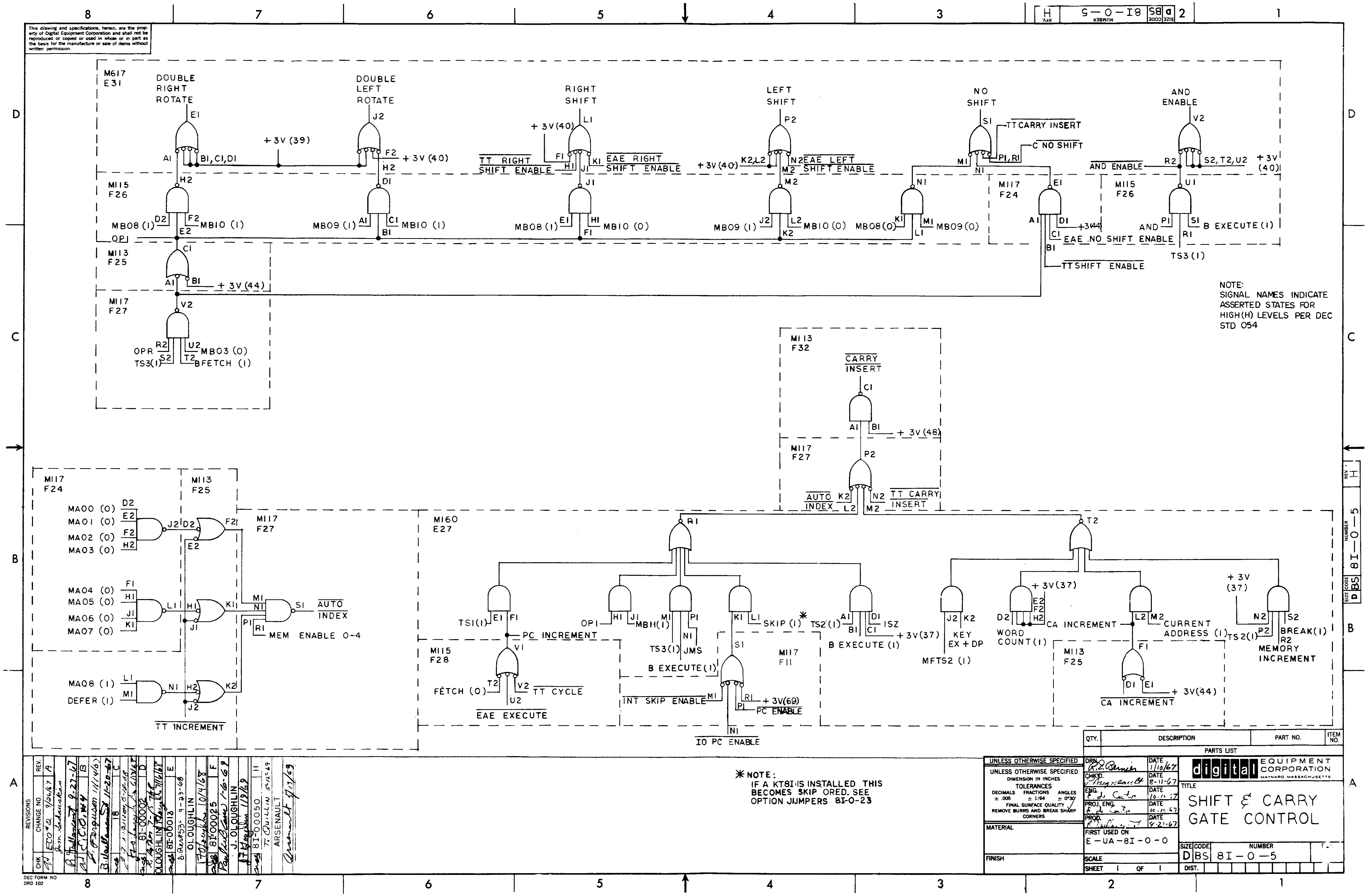
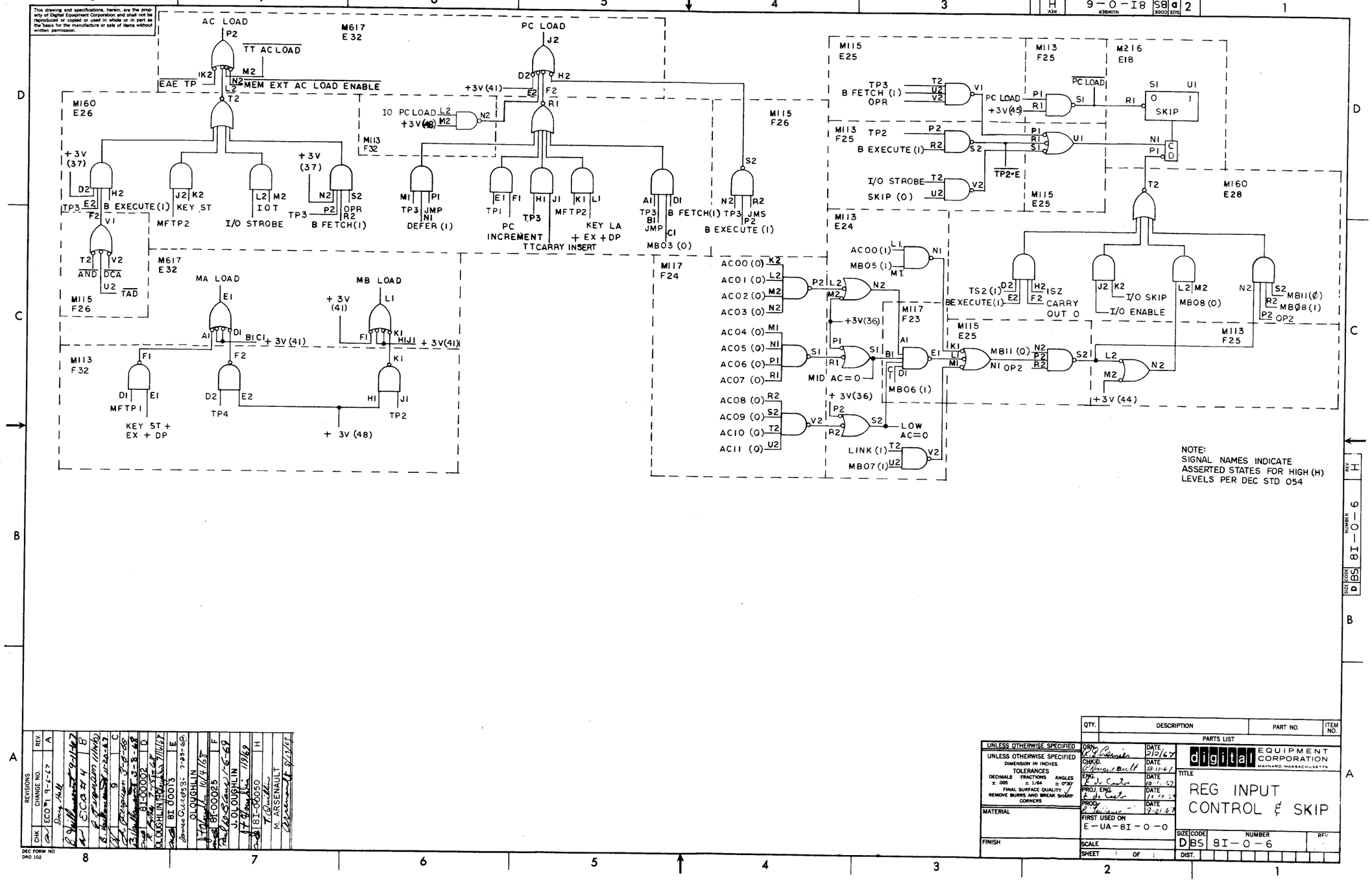
MEM ENABLE 0-4
MEM ENABLE 5-8
MA ENABLE 0-4
MA ENABLE 5-11
AC ENABLE
NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054
IPC ENABLE
I/O ENABLE
DATA ENABLE
DATA ADD ENABLE
SR ENABLE
L ENABLE
AC ENABLE
PC ENABLE
TT CARRY INSERT
MEM EXT I/O ENABLE
EAE L DISABLE
TT L DISABLE
OSR-UF(0)
REG OUTPUT GATE CONTROL
EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
FIRST USED ON E-UA-8I-0-0
D BS 8I-0-4
SHEET 1 OF 1
PARTS LIST
QTY. DESCRIPTION PART NO. ITEM NO.



This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.
M617 E31
DOUBLE RIGHT ROTATE
DOUBLE LEFT ROTATE
RIGHT SHIFT
LEFT SHIFT
NO SHIFT
AND ENABLE
TT CARRY INSERT
C NO SHIFT
TT RIGHT SHIFT ENABLE
EAE RIGHT SHIFT ENABLE
EAE LEFT SHIFT ENABLE
AND ENABLE
M115 F26
M113 F25
M117 F27
M117 F24
EAE NO SHIFT ENABLE
TT SHIFT ENABLE
B EXECUTE (1)
TS3 (1)
MB03 (0)
BFETCH (1)
NOTE: SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH(H) LEVELS PER DEC STD 054
M113 F32
CARRY INSERT
AUTO INDEX
TT CARRY INSERT
M160 E27
PC INCREMENT
M115 F28
FETCH (0)
TT CYCLE
EAE EXECUTE
B EXECUTE (1)
INT SKIP ENABLE
PC ENABLE
IO PC ENABLE
SKIP (1)
M117 F11
ISZ
KEY EX + DP
MFTS2 (1)
WORD COUNT (1)
CA INCREMENT
CURRENT ADDRESS (1)
BREAK (1)
MEMORY INCREMENT
TT INCREMENT
MEM ENABLE 0-4
MA08 (1)
DEFER (1)
* NOTE: IF A KT8I IS INSTALLED THIS BECOMES SKIP ORED. SEE OPTION JUMPERS 8I-0-23
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE
SHIFT & CARRY GATE CONTROL
FIRST USED ON E-UA-8I-0-0
D BS 8I-0-5
SHEET 1 OF 1



NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054

REVISIONS			
CHK	CHANGE NO.	REV.	
	ECO# 11-2-67	A	
	ECO # 4	B	
	ECO # 5	C	
	ECO # 6	D	
	81-00002	E	
	81-00013	F	
	81-00025	H	
	81-00050		

DEC FORM NO DRD 102

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

DRN.		DATE 2/2/67
CHK'D.		DATE 8-11-67
ENG.		DATE 10-1-67
PROJ. ENG.		DATE 12-10-67
PROD.		DATE 9-21-67

FIRST USED ON E-UA-8I-0-0

SCALE

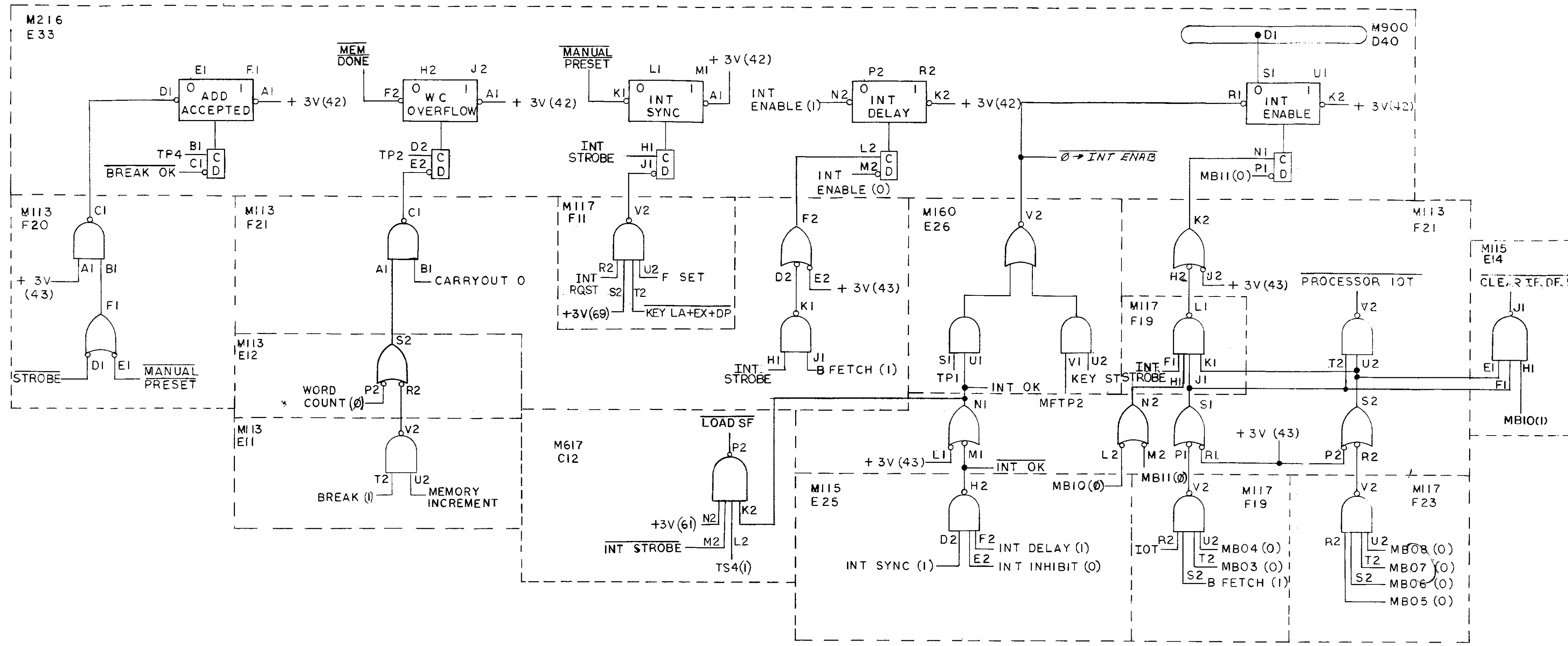
SHEET OF

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
REG INPUT CONTROL & SKIP

SIZE D | CODE BS | NUMBER 8I-0-6 | REV H

DIST.



NOTE:
SIGNAL NAMES INDICATE
ASSERTED STATES FOR HIGH (H)
LEVELS PER DEC STD 054

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. R. Q. Bernier	DATE 2/3/67	
CHK'D. P. Baugneault	DATE	
ENG. E. de Castro	DATE	
PROJ. ENG.	DATE	
PROD.	DATE	
FIRST USED ON E-UA-8I-0-0		
SCALE		
SHEET 1 OF 1		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
INTERRUPT & BREAK CONTROL

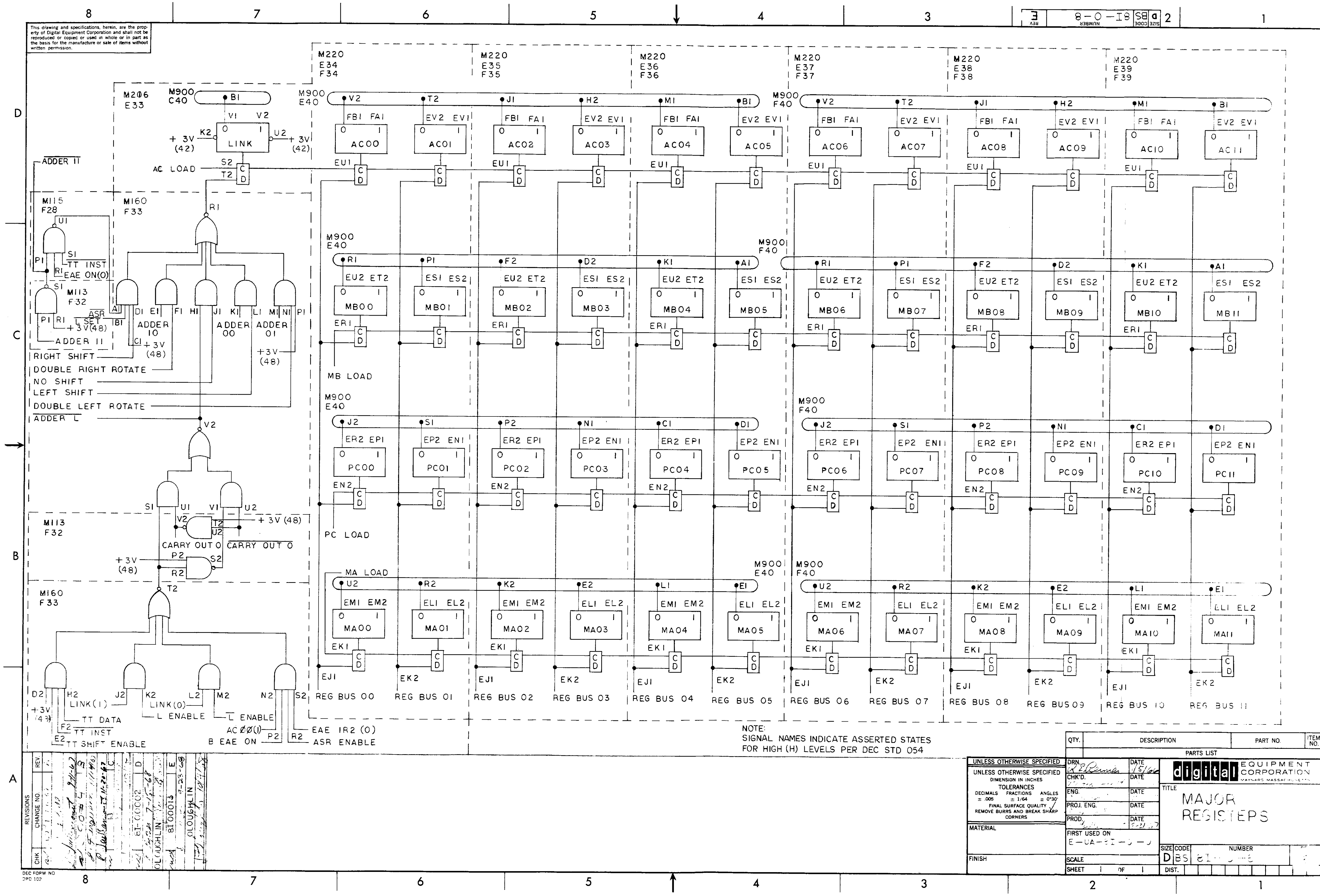
SIZE	CODE	NUMBER	REV
D	BS	8I-0-7	L

DIST.

REVISIONS

CHK	CHANGE NO.	REV.
	ECO #2	A
	EC 0.774	B
	9	C
	10	D
	13	E
	18	F
	8I-00002	H
	8I-00020	J
	OLOUGHLIN	
	8I-00069	K
	M. ARSENAULT	
	8I-00081	L
	ARSENAULT	

DEC FORM NO DRD 102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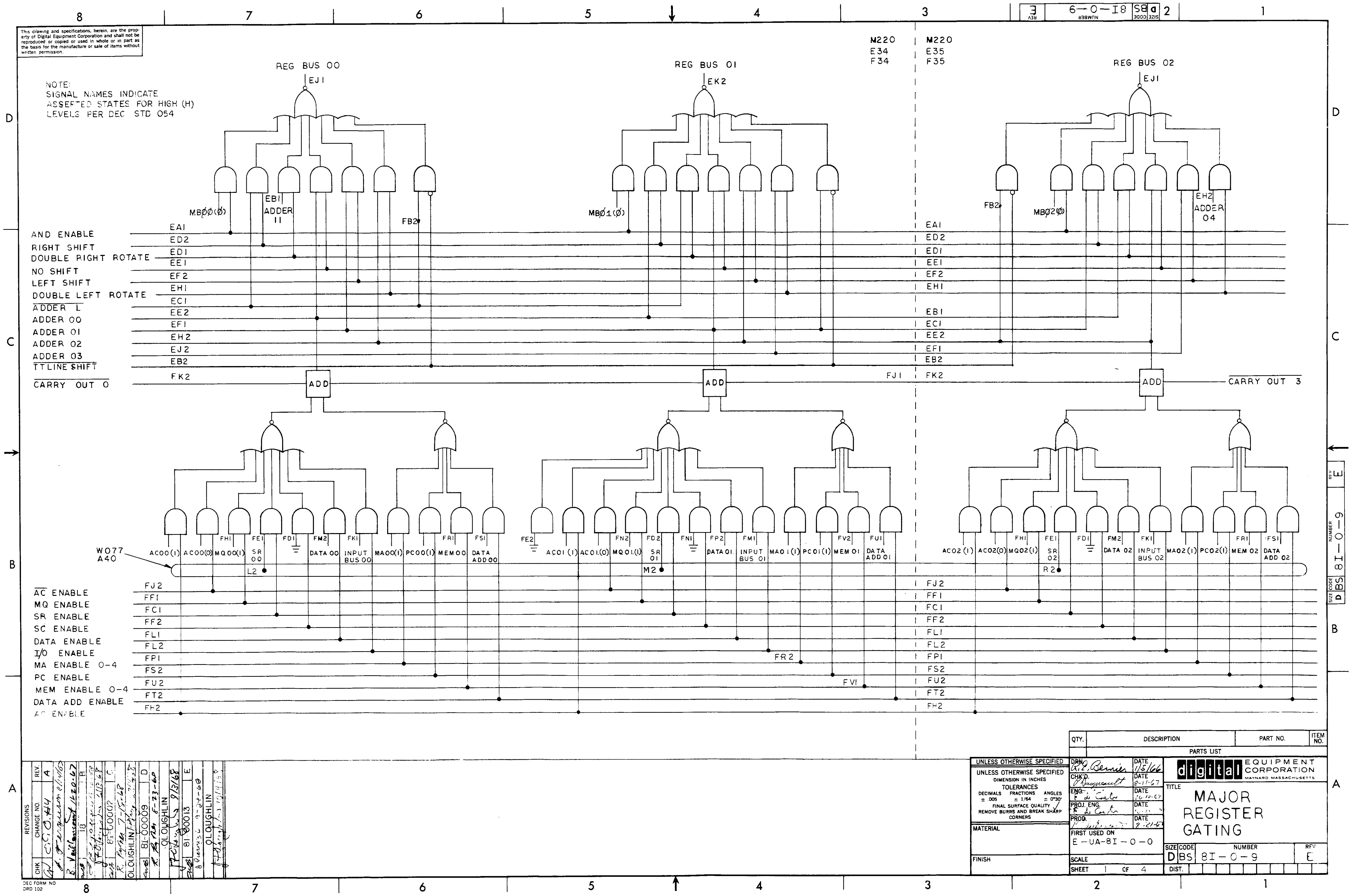
M220 E34 F34
M220 E35 F35
M220 E36 F36
M220 E37 F37
M220 E38 F38
M220 E39 F39
M206 E33
M900 C40
LINK
AC LOAD
ADDER II
M115 F28
M160 F33
M113 F32
TT INST
EAE ON(0)
ASR
L SET
ADDER 10
ADDER 00
ADDER 01
RIGHT SHIFT
DOUBLE RIGHT ROTATE
NO SHIFT
LEFT SHIFT
DOUBLE LEFT ROTATE
ADDER L
AC00 AC01 AC02 AC03 AC04 AC05 AC06 AC07 AC08 AC09 AC10 AC11
MB00 MB01 MB02 MB03 MB04 MB05 MB06 MB07 MB08 MB09 MB10 MB11
MB LOAD
PC00 PC01 PC02 PC03 PC04 PC05 PC06 PC07 PC08 PC09 PC10 PC11
PC LOAD
CARRY OUT 0
MA LOAD
MA00 MA01 MA02 MA03 MA04 MA05 MA06 MA07 MA08 MA09 MA10 MA11
REG BUS 00
REG BUS 01
REG BUS 02
REG BUS 03
REG BUS 04
REG BUS 05
REG BUS 06
REG BUS 07
REG BUS 08
REG BUS 09
REG BUS 10
REG BUS 11
LINK(1)
LINK(0)
TT DATA
L ENABLE
TT SHIFT ENABLE
B EAE ON
AC ØØ(1)
EAE IR2 (0)
ASR ENABLE
NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES
FOR HIGH (H) LEVELS PER DEC STD 054
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
PARTS LIST
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
MAJOR REGISTERS
SIZE D
CODE BS
NUMBER 8I-0-8
SHEET 1 OF 1
REV E


NOTE:
SIGNAL NAMES INDICATE
ASSERTED STATES FOR HIGH (H)
LEVELS PER DEC STD 054
REG BUS 00
REG BUS 01
REG BUS 02
M220 E34 F34
M220 E35 F35
AND ENABLE
RIGHT SHIFT
DOUBLE RIGHT ROTATE
NO SHIFT
LEFT SHIFT
DOUBLE LEFT ROTATE
ADDER L
ADDER 00
ADDER 01
ADDER 02
ADDER 03
TT LINE SHIFT
CARRY OUT 0
CARRY OUT 3
ADD
AC ENABLE
MQ ENABLE
SR ENABLE
SC ENABLE
DATA ENABLE
I/O ENABLE
MA ENABLE 0-4
PC ENABLE
MEM ENABLE 0-4
DATA ADD ENABLE
AC ENABLE
MAJOR REGISTER GATING
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
D BS 8I-0-9 E
FIRST USED ON E-UA-8I-0-0
SHEET 1 OF 4

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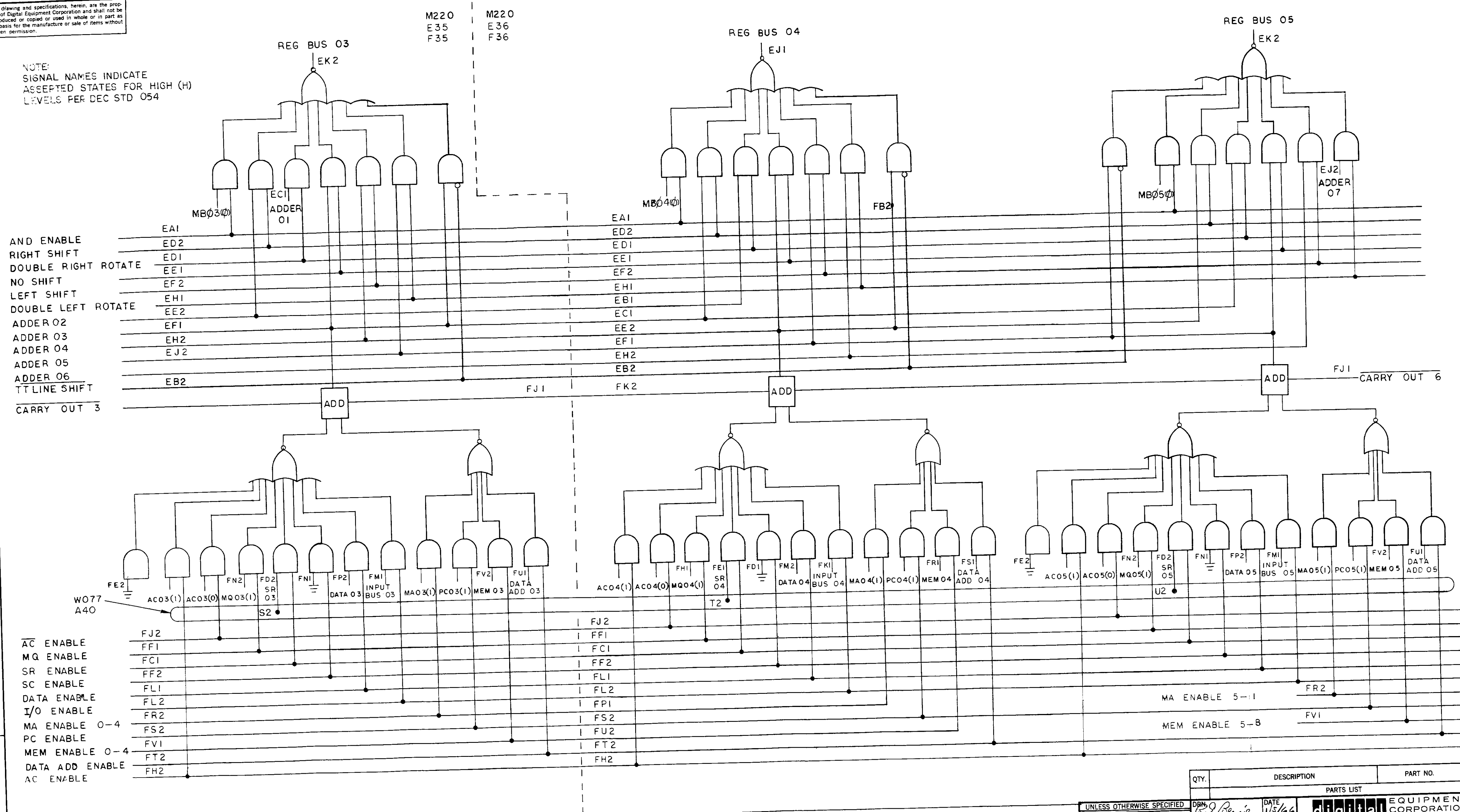


QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. R.J. Bennile DATE 1/5/66
CHK'D. DATE 8-11-67
ENG. F. de Castro DATE 10-1-67
PROJ. ENG. F. de Castro DATE 10-1-67
PROD. DATE 1-21-67

FIRST USED ON E-UA-8I-0-0

SCALE
SHEET 2 OF 4

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

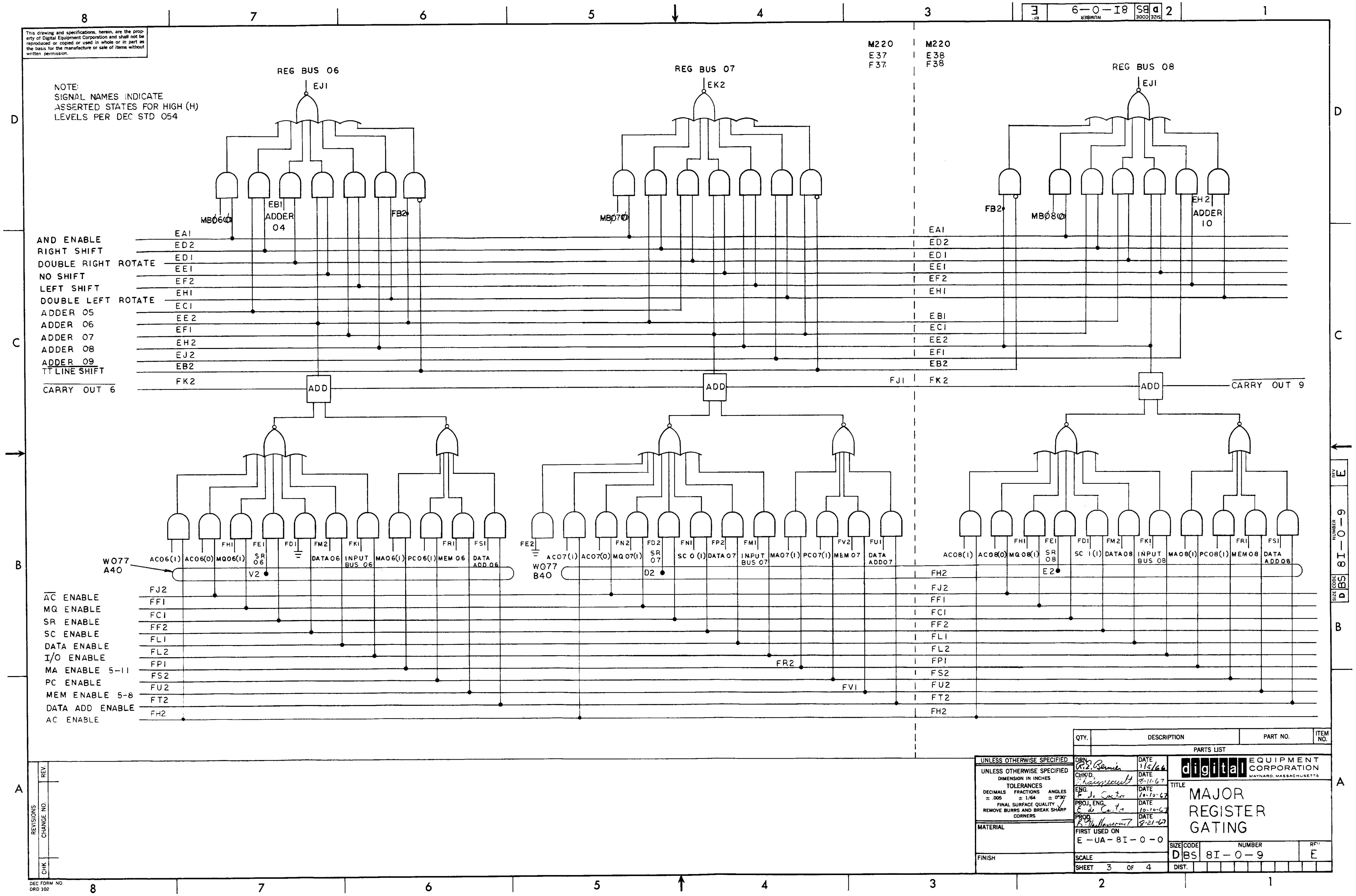
TITLE
MAJOR REGISTER GATING

SIZE D CODE BS NUMBER 8I-0-9 REV E

DIST.

REVISIONS | REV. | CHANGE NO. | CHK

DEC FORM NO DRD 102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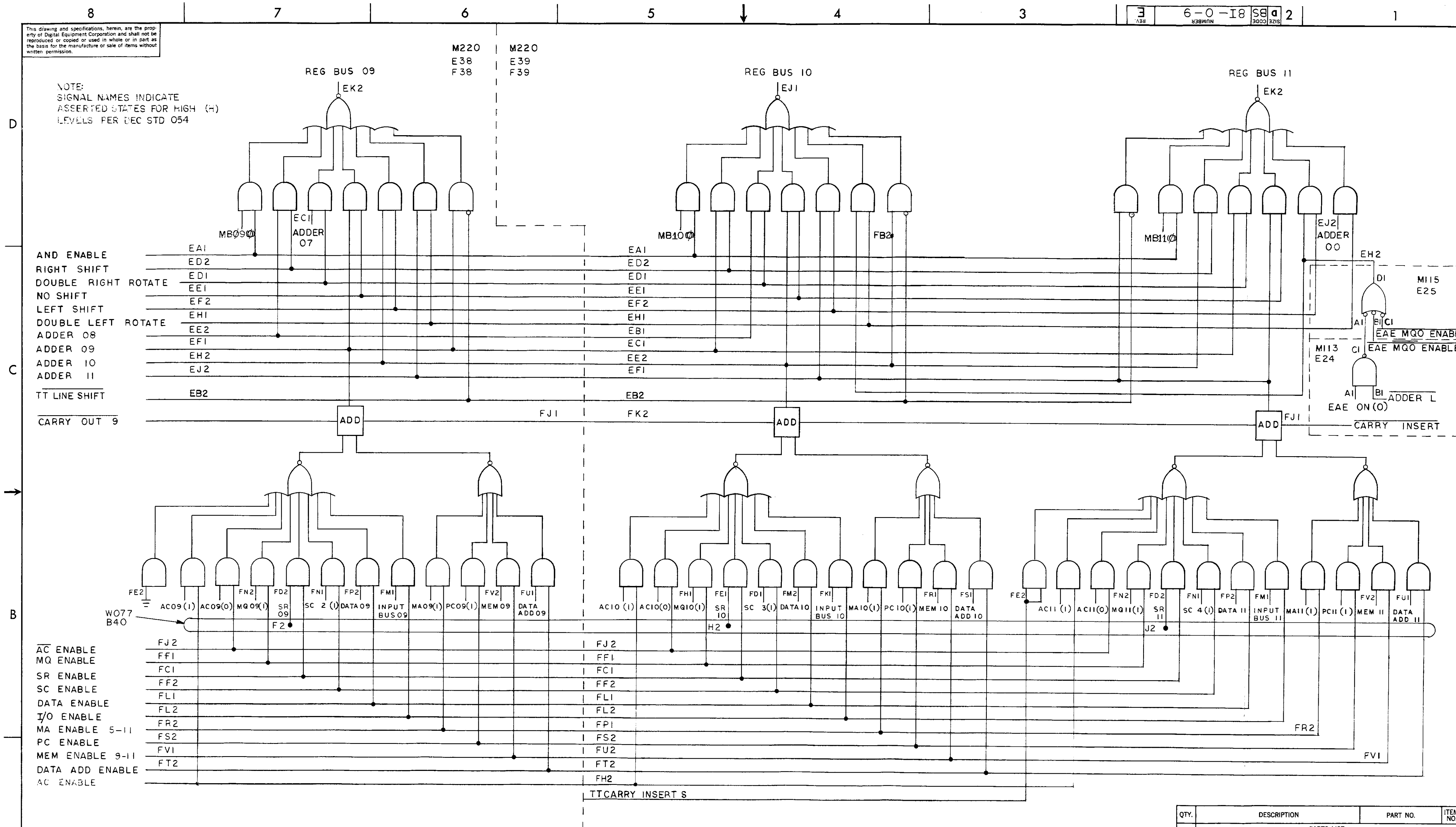
NOTE:
SIGNAL NAMES INDICATE
ASSERTED STATES FOR HIGH (H)
LEVELS PER DEC STD 054
REG BUS 06
REG BUS 07
REG BUS 08
M220 E37 F37
M220 E38 F38
AND ENABLE
RIGHT SHIFT
DOUBLE RIGHT ROTATE
NO SHIFT
LEFT SHIFT
DOUBLE LEFT ROTATE
ADDER 05
ADDER 06
ADDER 07
ADDER 08
ADDER 09
TT LINE SHIFT
CARRY OUT 6
CARRY OUT 9
ADD
AC ENABLE
MQ ENABLE
SR ENABLE
SC ENABLE
DATA ENABLE
I/O ENABLE
MA ENABLE 5-11
PC ENABLE
MEM ENABLE 5-8
DATA ADD ENABLE
AC ENABLE
W077 A40
W077 B40
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
QTY. DESCRIPTION PART NO. ITEM NO.
PARTS LIST
FIRST USED ON E-UA-8I-0-0
SHEET 3 OF 4
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE MAJOR REGISTER GATING
SIZE D CODE BS NUMBER 8I-0-9 REV E
DEC FORM NO DRD 102



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NOTE:
SIGNAL NAMES INDICATE
ASSERTED STATES FOR HIGH (H)
LEVELS PER DEC STD 054
REG BUS 09
REG BUS 10
REG BUS 11
M220 E38 F38
M220 E39 F39
AND ENABLE
RIGHT SHIFT
DOUBLE RIGHT ROTATE
NO SHIFT
LEFT SHIFT
DOUBLE LEFT ROTATE
ADDER 08
ADDER 09
ADDER 10
ADDER 11
TT LINE SHIFT
CARRY OUT 9
ADD
M115 E25
M113 E24
EAE MQO ENABLE
ADDER L
EAE ON (0)
CARRY INSERT
AC ENABLE
MQ ENABLE
SR ENABLE
SC ENABLE
DATA ENABLE
I/O ENABLE
MA ENABLE 5-11
PC ENABLE
MEM ENABLE 9-11
DATA ADD ENABLE
AC ENABLE
TTCARRY INSERT S
W077 B40

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. R.J. Bernier DATE 1/5/67
CHK'D. DATE 8-11-67
ENG. DATE 10-10-67
PROJ. ENG. DATE 10-12-67
PROD. DATE 9-21-67
FIRST USED ON E-UA-8I-0-0
SCALE
SHEET 4 OF 4

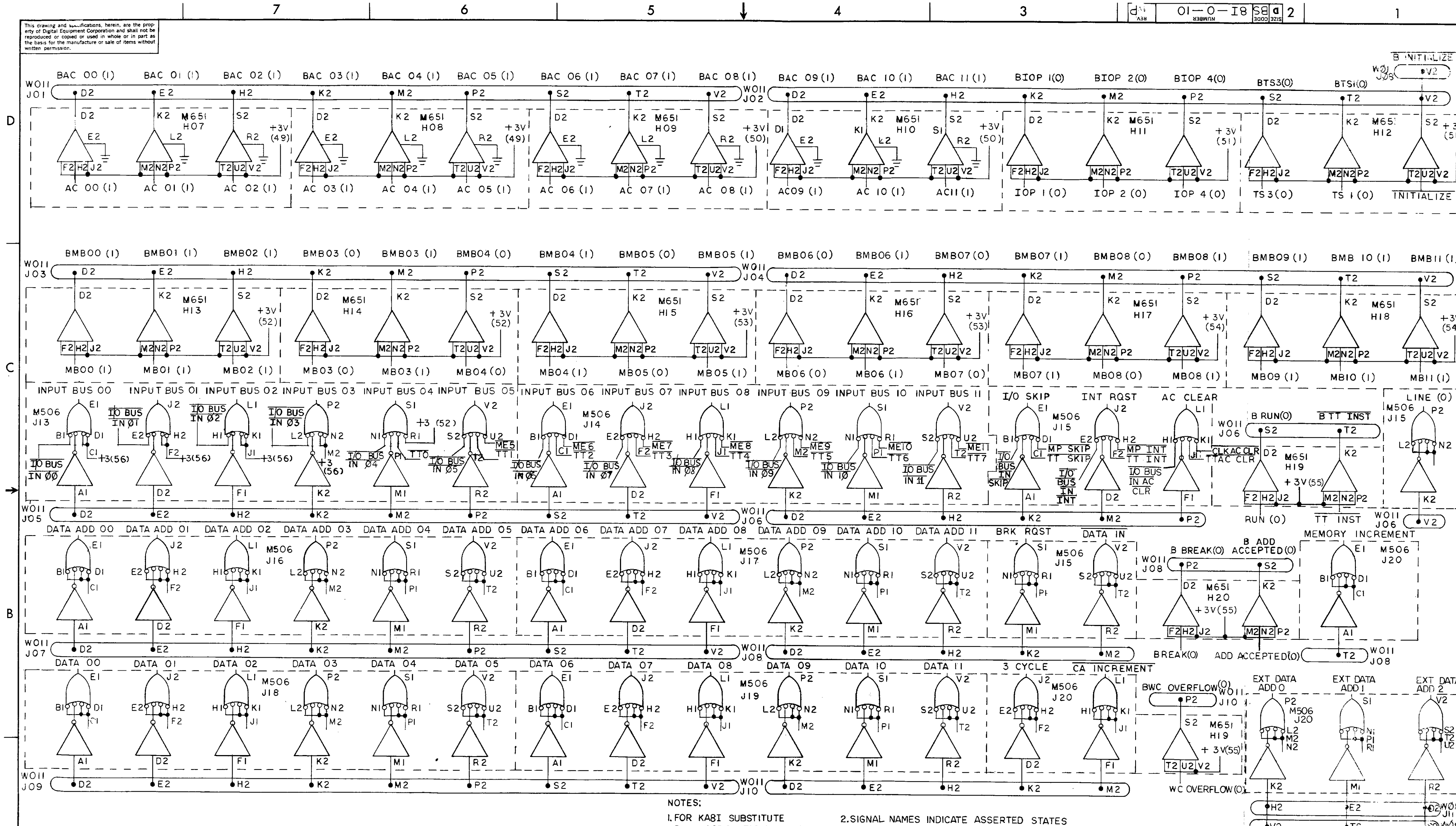
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
MAJOR REGISTER GATING

SIZE D CODE BS NUMBER 8I-0-9 REV E

DIST.

DEC FORM NO DRD 102



NOTES:

1. FOR KA8I SUBSTITUTE D-BS-KA8I-0-1 FOR THIS PRINT

2. SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054

REV.	CHANGE NO.
A	ECO#2 9/12/67
B	ECO #4
C	8
D	10
E	12
F	8I-00002
H	8I-00009
J	8I 00013
K	8I-00025
L	8I-00034
M	00059
N	8I-00067
P	8I-00084

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30' FINAL SURFACE QUALITY √ REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

FIRST USED ON E-UA-8I-0-0

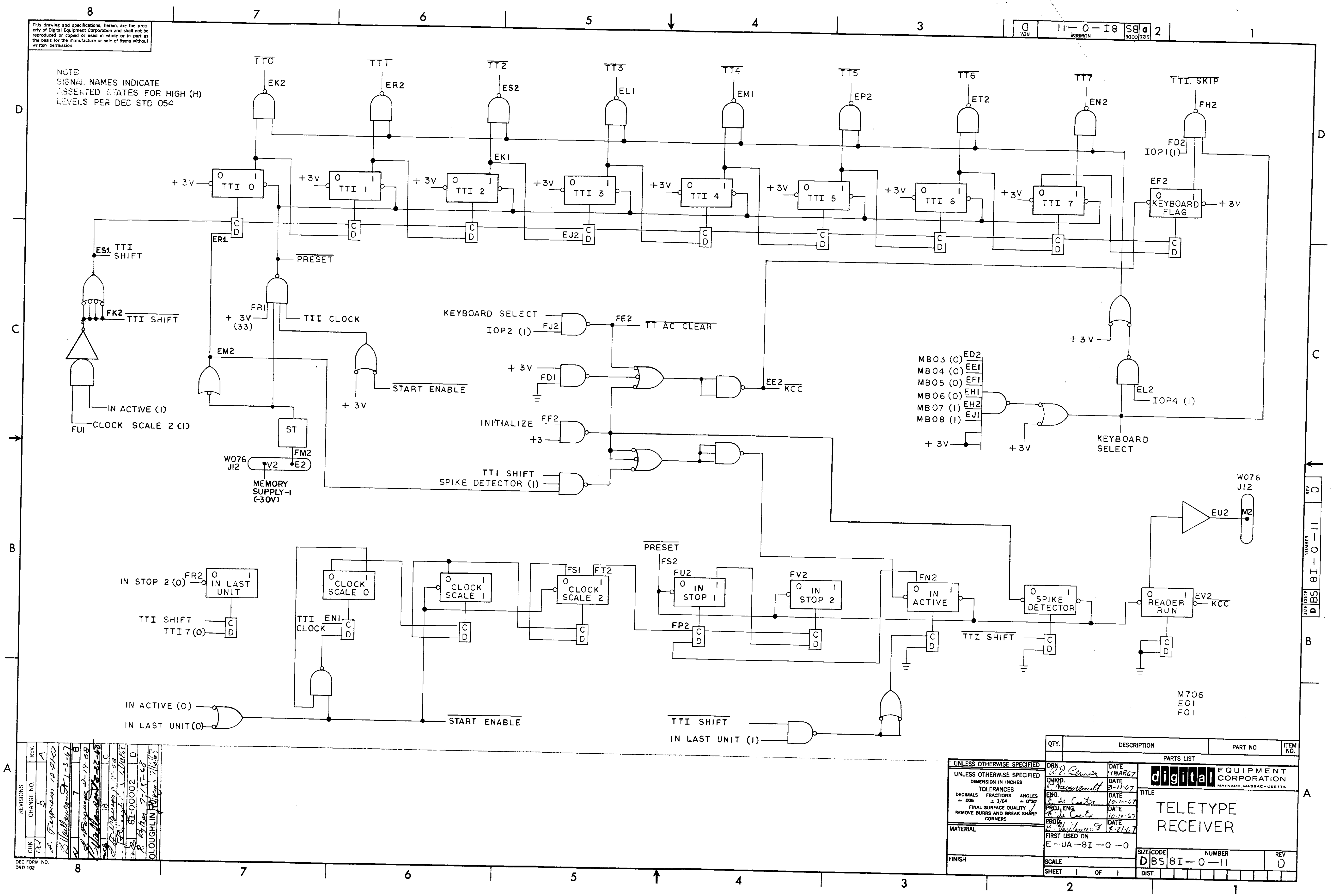
DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE I/O LEVEL CONVERTERS

SIZE D CODE BS NUMBER 8I-0-10 REV P

SHEET 1 OF 1

DEC FORM NO DRD 102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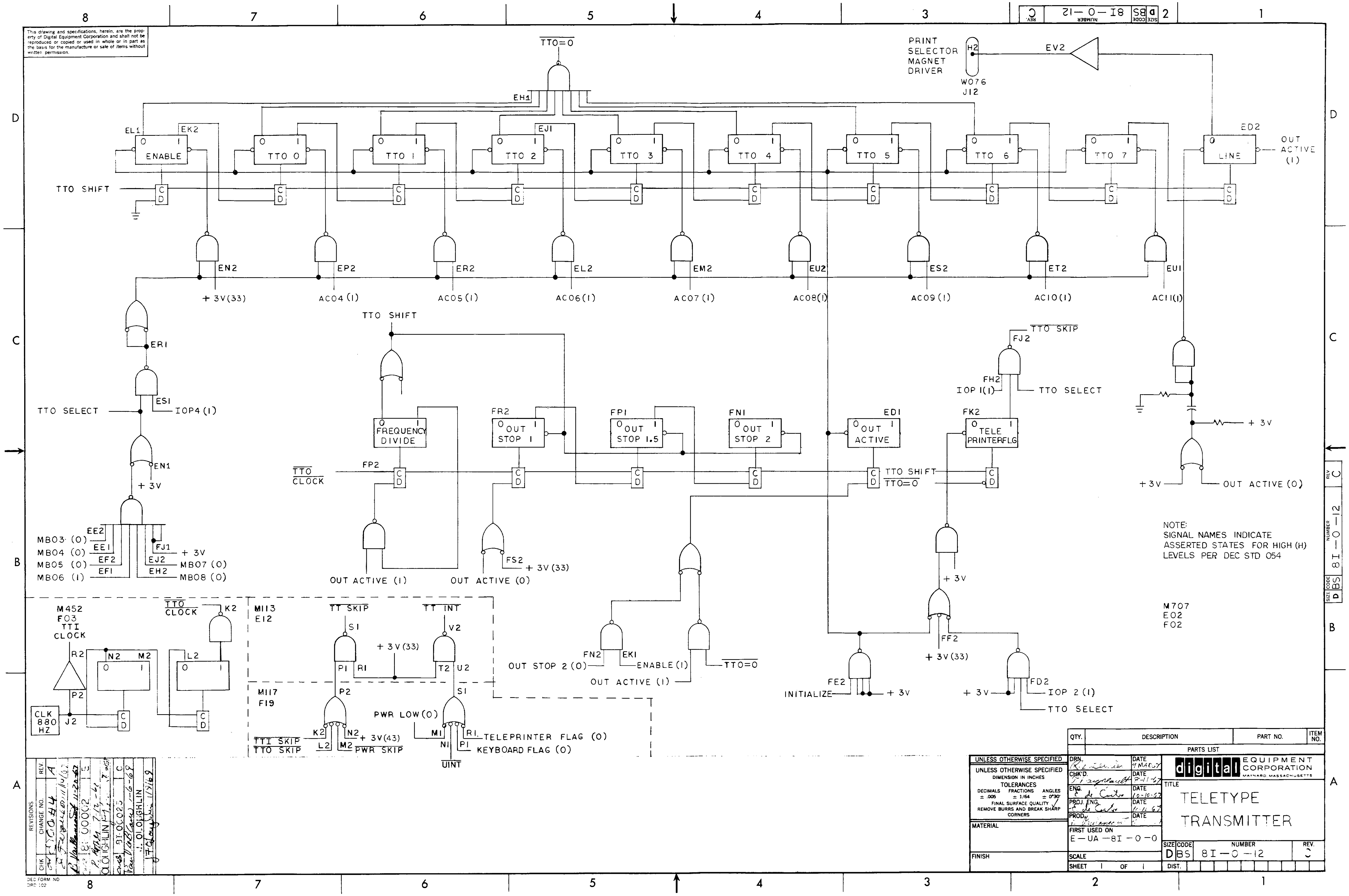
NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054
TT0
TT1
TT2
TT3
TT4
TT5
TT6
TT7
TTI. SKIP
EK2
ER2
ES2
EL1
EM1
EP2
ET2
EN2
FH2
FD2
IOP1(1)
EF2
EK1
+3V
TTI 0
TTI 1
TTI 2
TTI 3
TTI 4
TTI 5
TTI 6
TTI 7
KEYBOARD FLAG
C D
ER1
EJ2
ES1 TTI SHIFT
PRESET
FRI
FK2
TTI SHIFT
+3V (33)
TTI CLOCK
KEYBOARD SELECT
IOP2 (1)
FJ2
FE2
TT AC CLEAR
EM2
START ENABLE
FD1
EE2
KCC
IN ACTIVE (1)
CLOCK SCALE 2 (1)
FU1
ST
FM2
W076 J12
V2
E2
MEMORY SUPPLY-1 (-30V)
INITIALIZE
FF2
+3
TTI SHIFT
SPIKE DETECTOR (1)
MB03 (0) ED2
MB04 (0) EE1
MB05 (0) EF1
MB06 (0) EH1
MB07 (1) EH2
MB08 (1) EJ1
EL2
IOP4 (1)
KEYBOARD SELECT
W076 J12
EU2
M2
PRESET
FS2
IN STOP 2 (0)
FR2
IN LAST UNIT
CLOCK SCALE 0
CLOCK SCALE 1
CLOCK SCALE 2
FS1
FT2
FU2
IN STOP 1
FV2
IN STOP 2
FN2
IN ACTIVE
SPIKE DETECTOR
READER RUN
EV2
KCC
TTI SHIFT
TTI 7(0)
TTI CLOCK
EN1
FP2
TTI SHIFT
M706
E01
F01
IN ACTIVE (0)
IN LAST UNIT(0)
START ENABLE
TTI SHIFT
IN LAST UNIT (1)
REVISIONS
CHK
CHANGE NO.
REV.
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005
FRACTIONS ± 1/64
ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH
DRN.
CHK'D.
ENG.
PROJ. ENG.
PROD.
DATE
FIRST USED ON
E-UA-8I-0-0
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
TELETYPE RECEIVER
SIZE D
CODE BS
NUMBER 8I-0-11
REV D
SCALE
SHEET 1 OF 1
DIST.
DEC FORM NO. DRD 102



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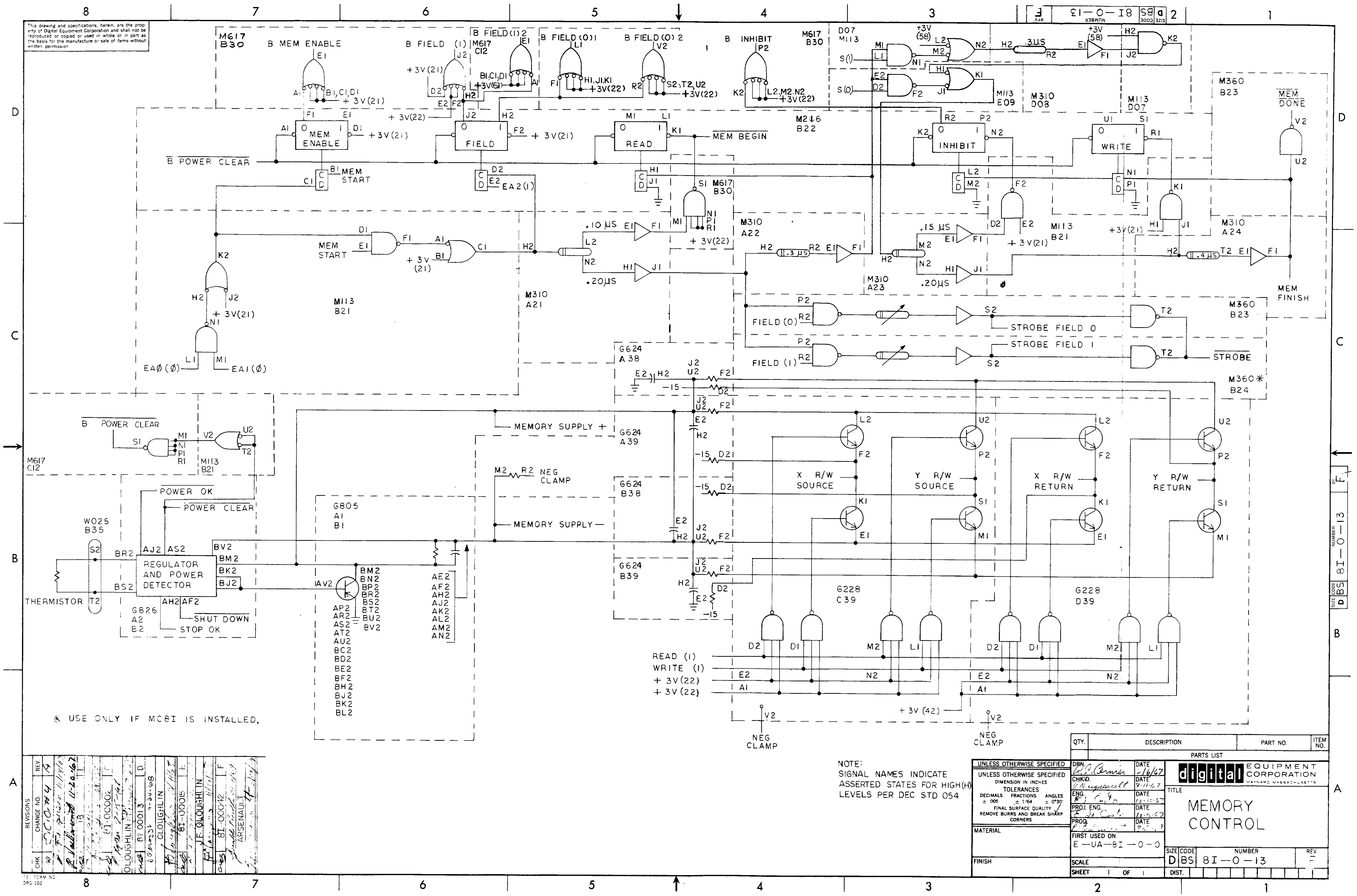
DIGITAL EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS

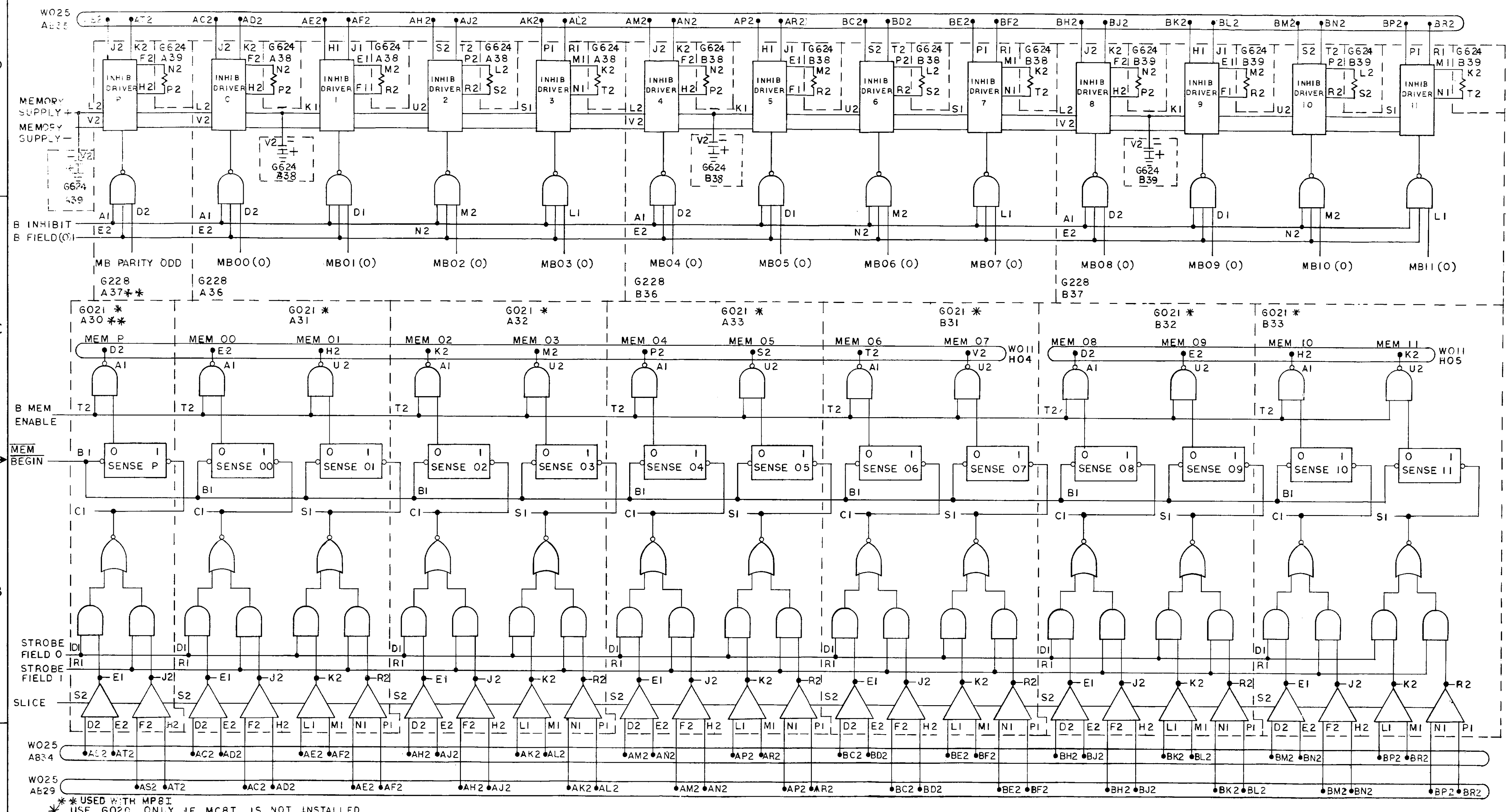
TITLE: TELETYPE TRANSMITTER

SIZE D | CODE BS | NUMBER 8I-0-12 | REV. C

FIRST USED ON E-UA-8I-0-0

SHEET 1 OF 1


B MEM ENABLE
B FIELD (1)
B FIELD (1) 2
B FIELD (0) 1
B FIELD (0) 2
B INHIBIT
MEM ENABLE
FIELD
READ
INHIBIT
WRITE
MEM BEGIN
B POWER CLEAR
MEM START
MEM DONE
MEM FINISH
FIELD (0)
FIELD (1)
STROBE FIELD 0
STROBE FIELD 1
STROBE
POWER OK
POWER CLEAR
REGULATOR AND POWER DETECTOR
THERMISTOR
SHUT DOWN
STOP OK
MEMORY SUPPLY +
MEMORY SUPPLY −
NEG CLAMP
X R/W SOURCE
Y R/W SOURCE
X R/W RETURN
Y R/W RETURN
READ (1)
WRITE (1)
* USE ONLY IF MC8I IS INSTALLED.
NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH(H) LEVELS PER DEC STD 054
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
MEMORY CONTROL
D BS 8I-0-13



✱✱ USED WITH MP8I

✱ USE G020 ONLY IF MC8I IS NOT INSTALLED

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NOTE:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH(H) LEVELS PER DEC STD 054

REV.	CHANGE NO.	REVISIONS
A	EC 0414	
B	8I-00002	
C	8I-00002	
D	OLOUGHLIN 8I-0005	

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

		DATE
DRN.	R. E. Berner	1/3/67
CHK'D.		8-11-67
ENG.		10-10-67
PROJ. ENG.		10-10-67
PROD.		9-21-67

FIRST USED ON E-UA-8I-0-0

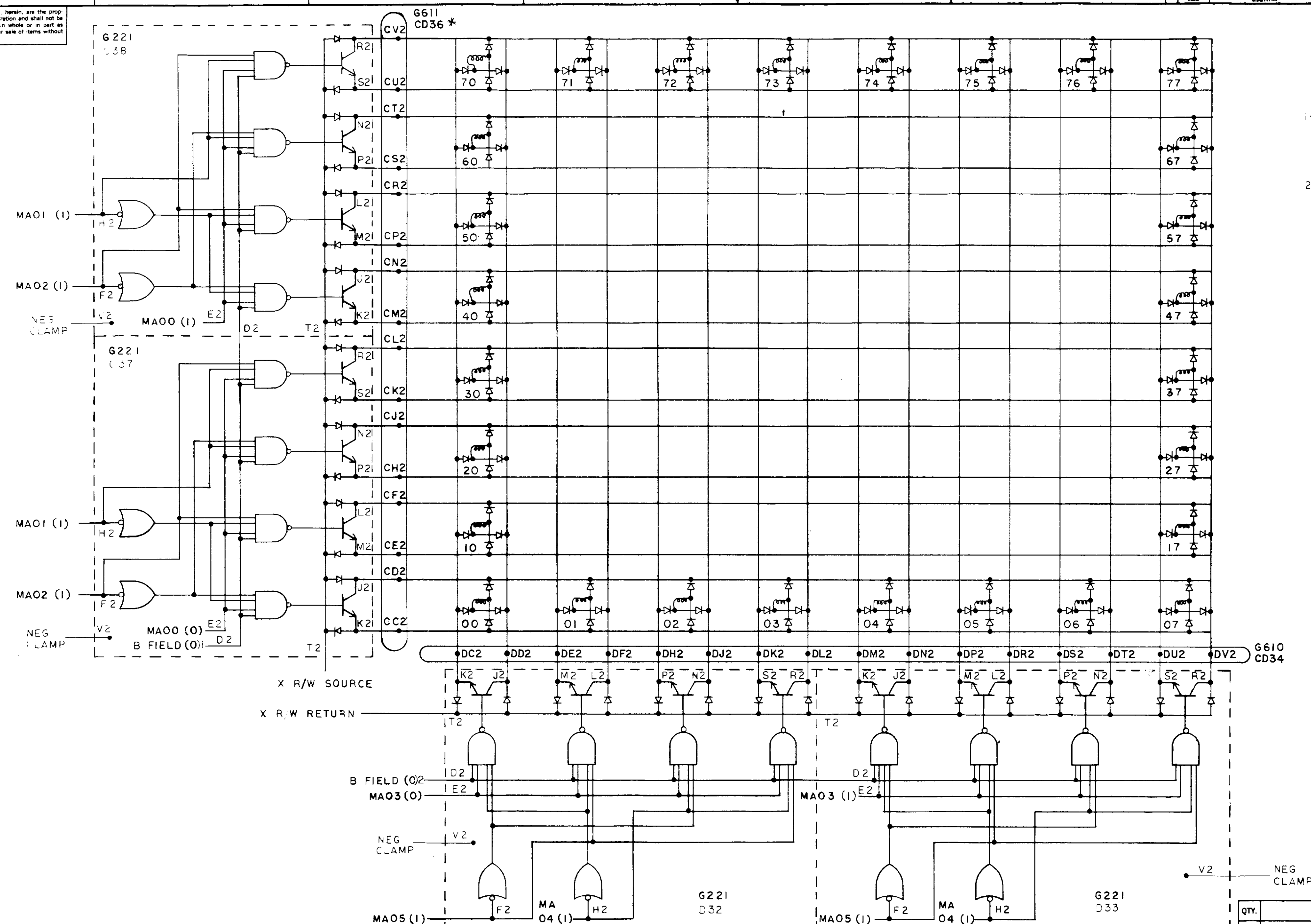
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
SENSE AMPS & INHIBIT DRIVERS

SIZE	CODE	NUMBER	REV.
D	BS	8I-0-14	D

SCALE
SHEET 1 OF 1
DIST.

DEC FORM NO. DRD 102



NOTES:

1 ✱ G6 IN CD36 IS REPLACED WITH A G612 IF MPR IS INSTALLED

2 SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH LEVELS PER DEC STD 054

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

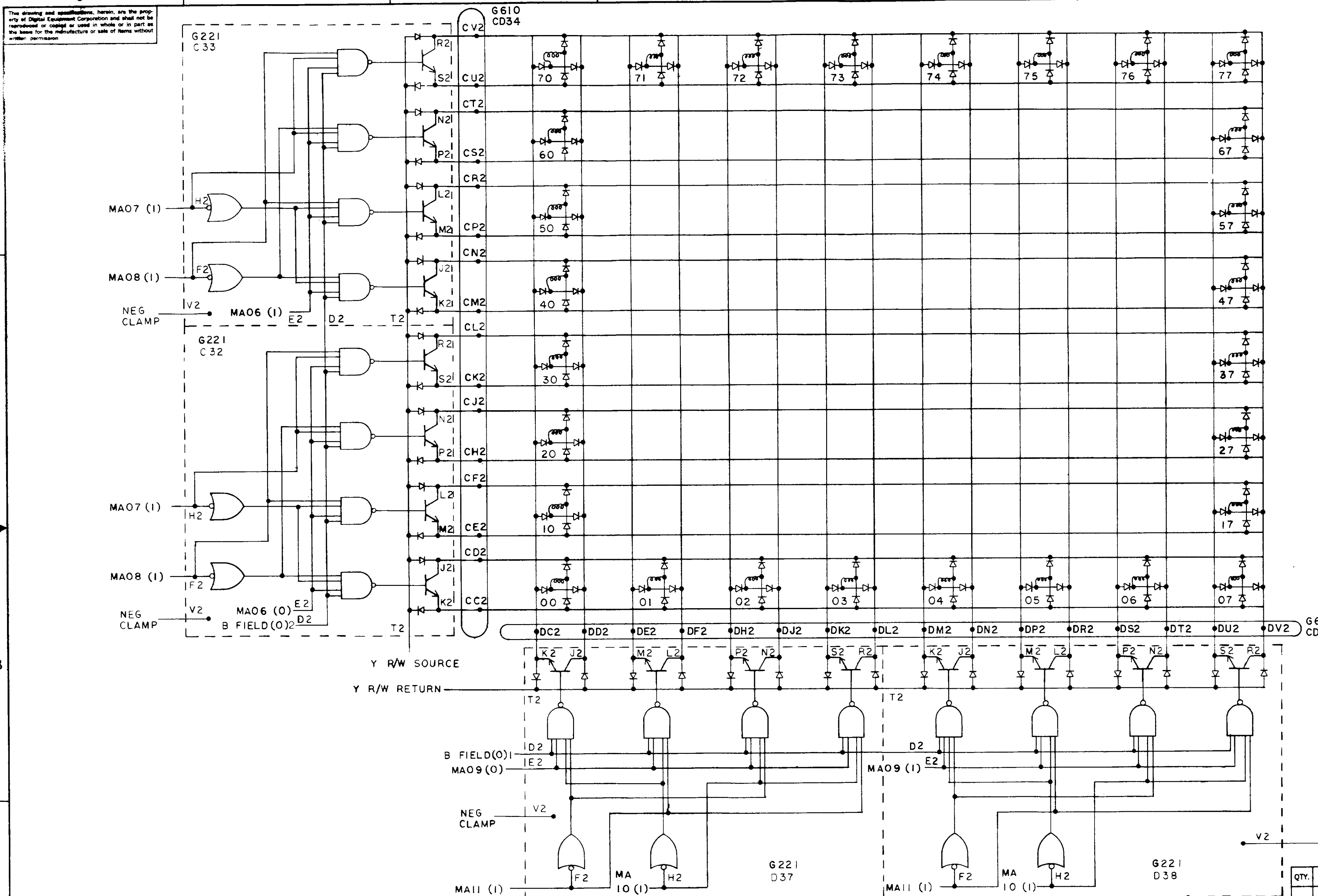
FINISH

DRN. R. J. Bernier DATE 7/7/67
CHK'D. DATE 8-11-67
ENG. DATE
PROJ. ENG. DATE
PROD. DATE
FIRST USED ON E-JA-8I-0-0
SCALE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
X AXIS SELECTION

SIZE D CODE BS NUMBER 8I-0-15 REV. C



NOTES:

1. * G611 IN CD36 IS REPLACED WITH A G612 IF MP8I IS INSTALLED
2. SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD 054

UNLESS OTHERWISE SPECIFIED		
DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	DRN R. J. Bernier	DATE 2/7/67
MATERIAL	CHKD.	DATE
FINISH	ENG. E. de Castro	DATE 10-10-67
	PROJ. ENG. E. de Castro	DATE 10-10-67
	PROD.	DATE

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

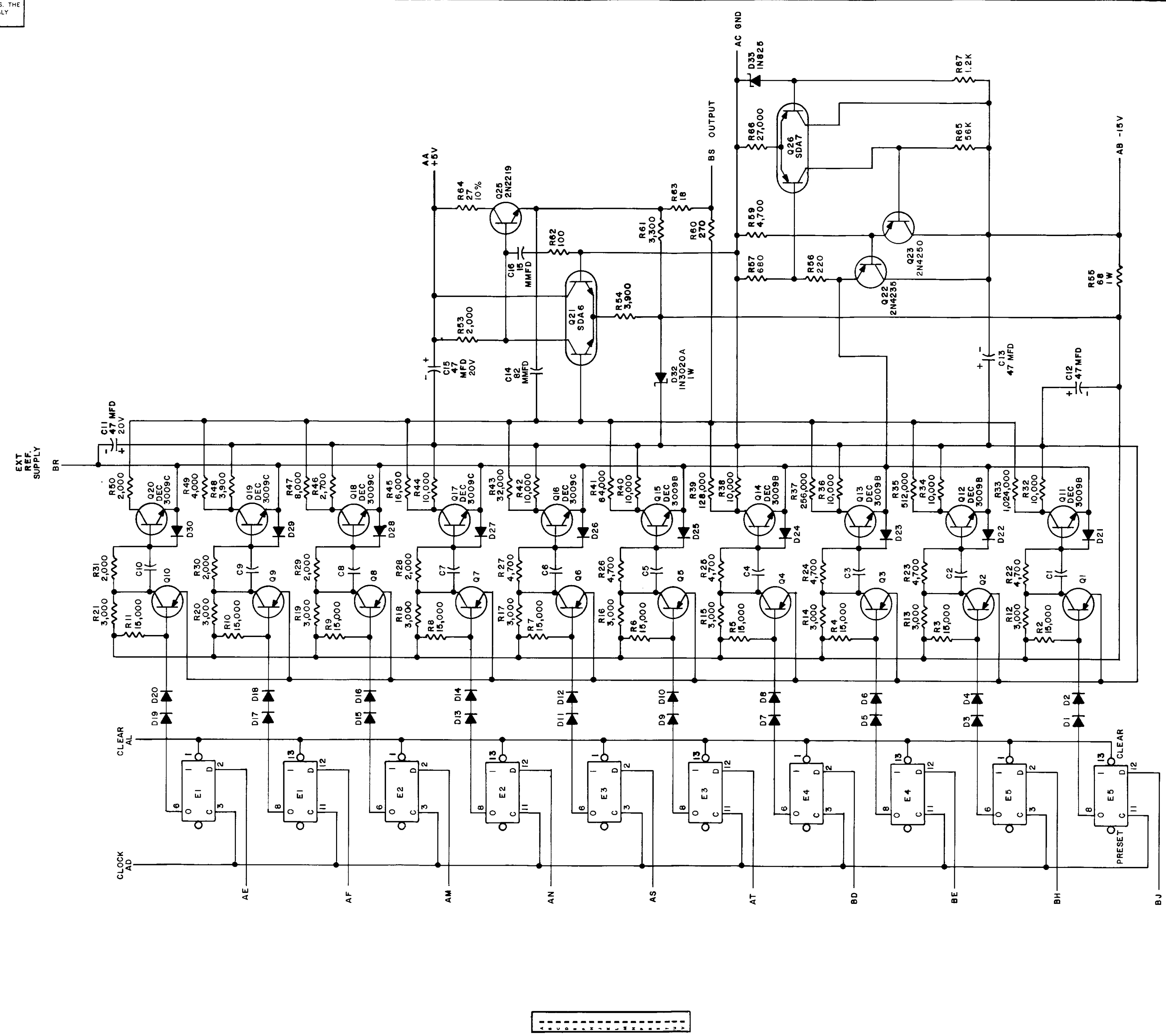
TITLE Y AXIS SELECTION

FIRST USED ON E-UA-8I-0-0

SIZE D CODE BS NUMBER 8I-0-16 REV C

SCALE

SHEET 1 OF 1



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC-6B
DIODES ARE D664
CAPACITORS ARE 47 MMFD
RESISTORS ARE 1/4W, 5%
IC'S ARE DEC7474N
PIN 7 ON EACH IC = AC GND
PIN 14 ON EACH IC = AA +5V
R33 IS 1/2W, 1%, 25 PPM °/c
R35 IS 1/4W, 1%, 25 PPM °/c
R37, R39, R41 & R43 ARE 1/8W, .1%, 25 PPM °/c
R45, R47, R49 & R50 ARE .3W, .01%, 5 PPM °/c
Q16 THRU Q20 ARE SELECTED SILVER DOT

PARTS LIST IS A-PL-A607-0-0

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC-6B	NONE	SDA6	2N2060
DEC3009B	2N3009	D664	1N3606
DEC3009C	2N3009	1N3020	SAME
2N4234	SAME	1N825	SAME
DEC6534B	MPS6534	SDA7	SAME

DRN M. Haller DATE 7-13-67
CHK'D R. Silverman DATE 7/27/67
ENG. S. Kidder DATE 8/13/67
PROD. DATE

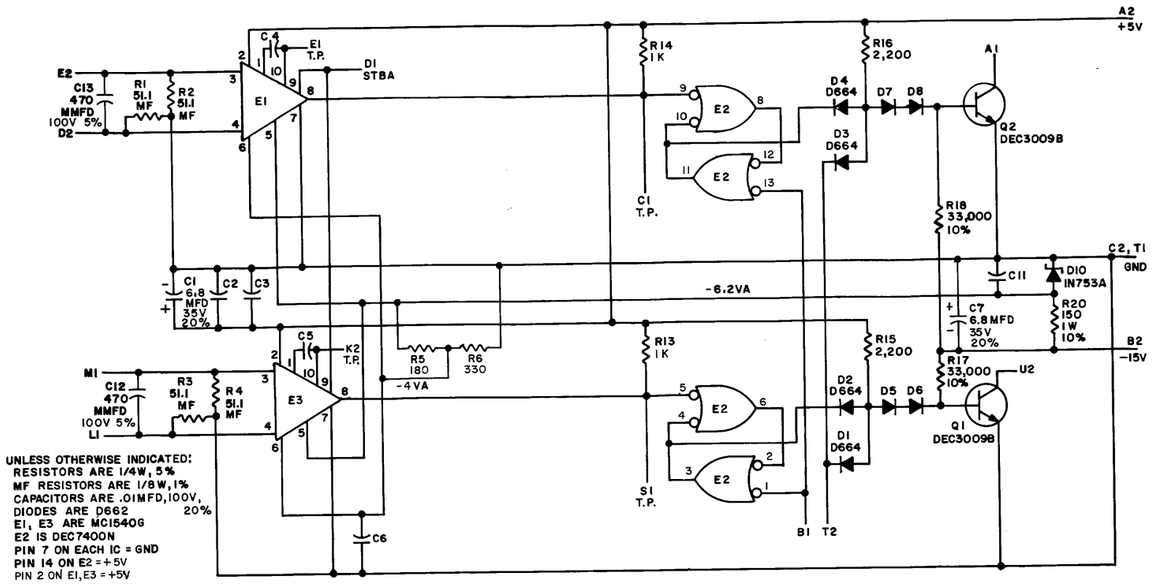
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE 10 BIT D-A CONVERTER A607

SIZE D | CODE CS | NUMBER A607-0-1 | REV. C

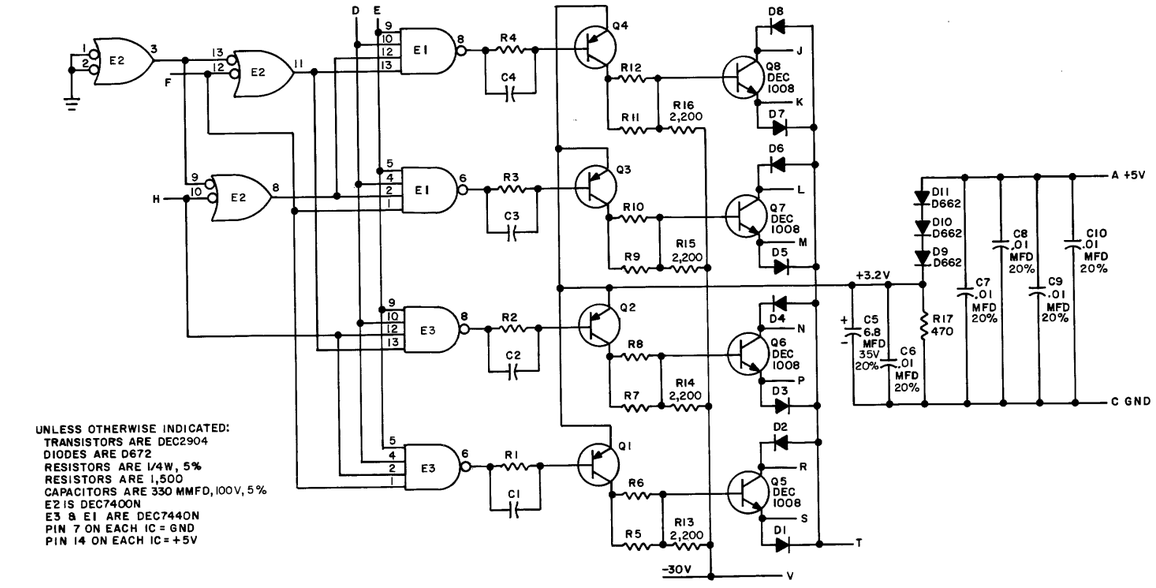
PRINTED CIRCUIT REV. A B

DEC FORM NO. DRD 101

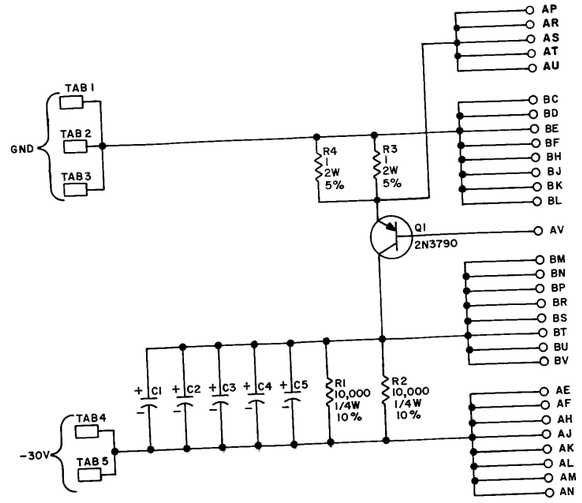


USE THE ETCH BOARD OF THE G021

B-CS-G020-0-1 Sense Amp.

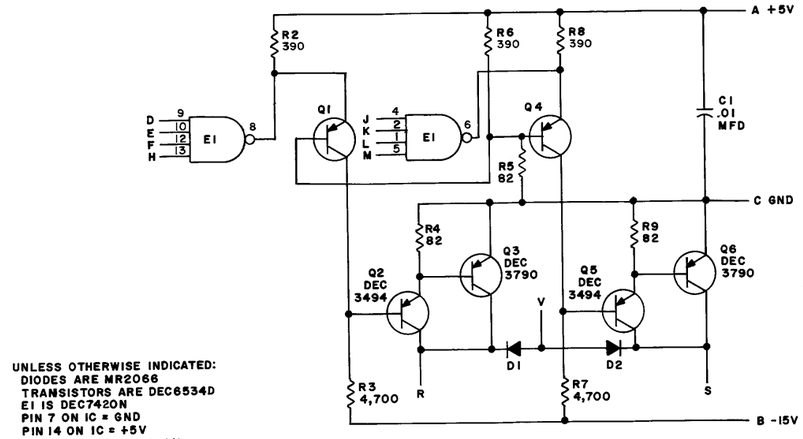


B-CS-G221-0-1 Memory Selector



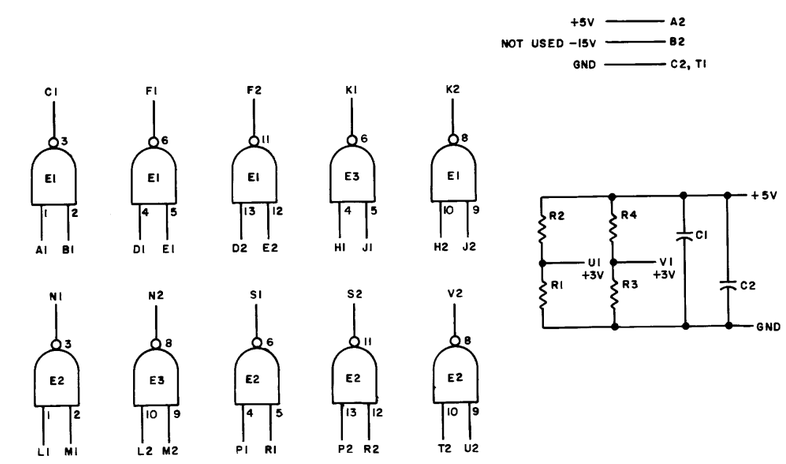
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 20MFD 50V
TABS ARE 250 SERIES FASTON TABS TYPE **60465-2** (AMP INC)
Q1 IS MOUNTED ON HEAT SINK, WAKEFIELD TYPE NC-623-A USING AN ANODIZED ALUMINUM INSULATING WASHER & WAKEFIELD TYPE 120 THERMAL JOINT COMPOUND

B-CS-G805-0-1 Negative Regulator



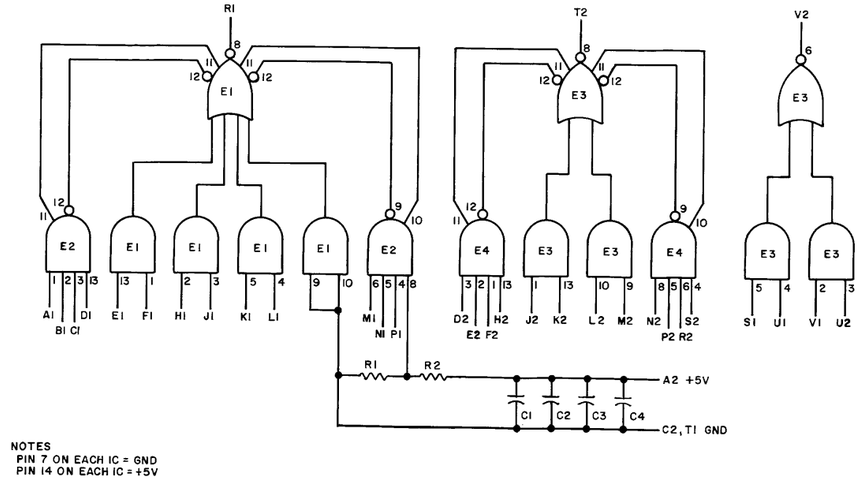
UNLESS OTHERWISE INDICATED:
DIODES ARE MR2066
TRANSISTORS ARE DEC6534D
E1 IS DEC7420N
PIN 7 ON IC = GND
PIN 14 ON IC = +5V
RESISTORS ARE 1/4W, 10%

B-CS-M040-0-1 Solenoid Driver



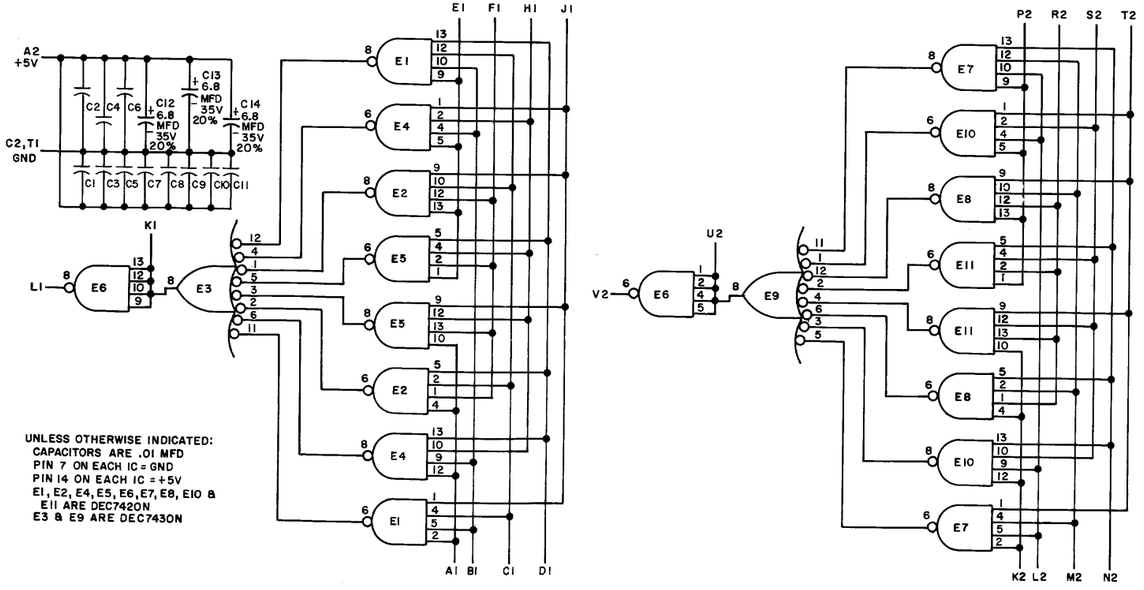
NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

B-CS-M113-0-1 10-2 Input NAND Gates



NOTES
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

B-CS-M160-0-1 Gate Module



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01 MFD
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1, E2, E4, E5, E6, E7, E8, E10 & E11 ARE DEC7420N
E3 & E9 ARE DEC7430N

B-CS-M162-0-1 Parity Circuit

SIZE D | CODE CS | NUMBER M220-0-1 | REV C

AC2 E10 · AC3 E10 · MB2 E8 · MB3 E8 · PC2 E9 · PC3 E9 · MA2 E4 · MA3 E4

+5V — AA2, BA2

GND — AC2, AT1, BC2, BT1

R6 330 5% · R7 750 5% · C9 · C1 · C2 · C3 · C4 · C5 · C6 · C7 · C8

R4 3,000 5% · R5 3,000 5% · R3 3,000 5% · Q1 DEC3009B

TT LINE SHIFT — AB2

AND	AA1
SHIFT RIGHT	AD2
SHIFT RIGHT TWICE	AD1
NO SHIFT	AE1
SHIFT LEFT	AF2
SHIFT LEFT TWICE	AH1
ADDER 1	AC1
ADDER 2	AE2
ADDER 3	AF1
ADDER 4	AH2

MB2(0) — ADDER 0 AB1 — BB2 — MB3(0) — ADDER 5 AJ2

ADDER 2 E13 — BK2 C2 — ADDER 3 E13 — CO. BJ1

AC ENABLE	BH2
AC ENABLE	BJ2
MQ ENABLE	BF1
SR ENABLE	BC1
SC ENABLE	BF2
DATA ENABLE	BL1
IO ENABLE	BL2
MA ENABLE	BP1
PC ENABLE	BS2
MEM ENABLE	BU2
DATA ADDRESS ENABLE	BT2

AC2 (1) · AC2 (0) · MQ2 (1) BH1 · SR2 BE1 · SC2 BD1 · DATA 2 BM2 · IO2 BK1 · MA2 (1) · PC2 (1) · MEM 2 BR1 · DATA ADD. 2 BS1

BE2 · AC3 (1) · AC3 (0) · MQ3 (1) BN2 · SR3 BD2 · SC3 BN1 · DATA 3 BP2 · IO3 BM1 · MA3 (1) · PC3 (1) · MEM 3 BV2 · DATA ADDRESS 3 BU1 · BR2 · BV1

UNLESS OTHERWISE INDICATED:
E4, E8, E9, E10 ARE DEC7474N

E3, E5, E6 ARE DEC7460N
E1, E2, E12, E15, E14, E16, E17, E18 ARE DEC7453N
E13 IS DEC7482N
PIN 7 ON EACH IC EXCEPT E13 = GND
PIN 11 ON E13 = GND
PIN 14 ON EACH IC EXCEPT E13 = +5V
PIN 4 ON E13 = +5V
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE 6.8 MFD, 35V, 20%
E7 & E11 ARE DEC7440N

PARTS LIST A-PL-M220-0-0

REVISIONS	CHG NO.	REV
MR	00001	A
MR	00002	B
MR	00003	C

DRN M. Waller DATE 3-15-67
CHKD DATE 3/15/67
ENGR DATE 3/16/67
PROD DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC30098	2N3009		

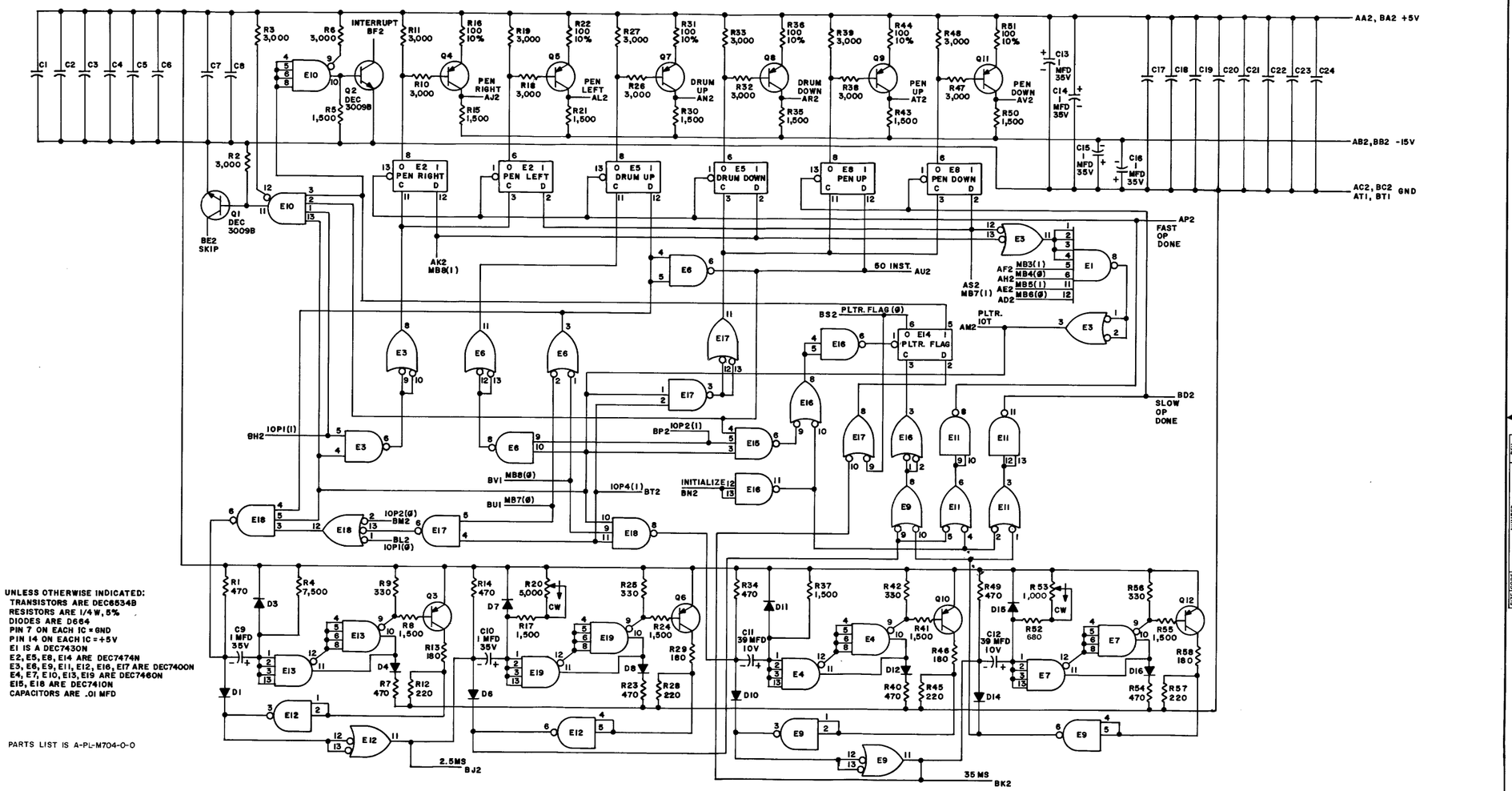
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: MAJOR REGISTERS M220

SIZE D | CODE CS | NUMBER M220-0-1 | REV C | PRINTED CIRCUIT REV.

DEC FORM NO. DRD 101

REV. C | NUMBER M220-0-1 | SIZE D | CODE CS



REV E | SIZE D | CS CODE | NUMBER M704-0-1

REVISIONS		
CHG NO.	CHG	REV
7042	C	
10001	D	
10002	E	

DRN. Jm Haller DATE 9-28-67
CHK'D E. Peterson DATE 9/28/67
PROD. DATE

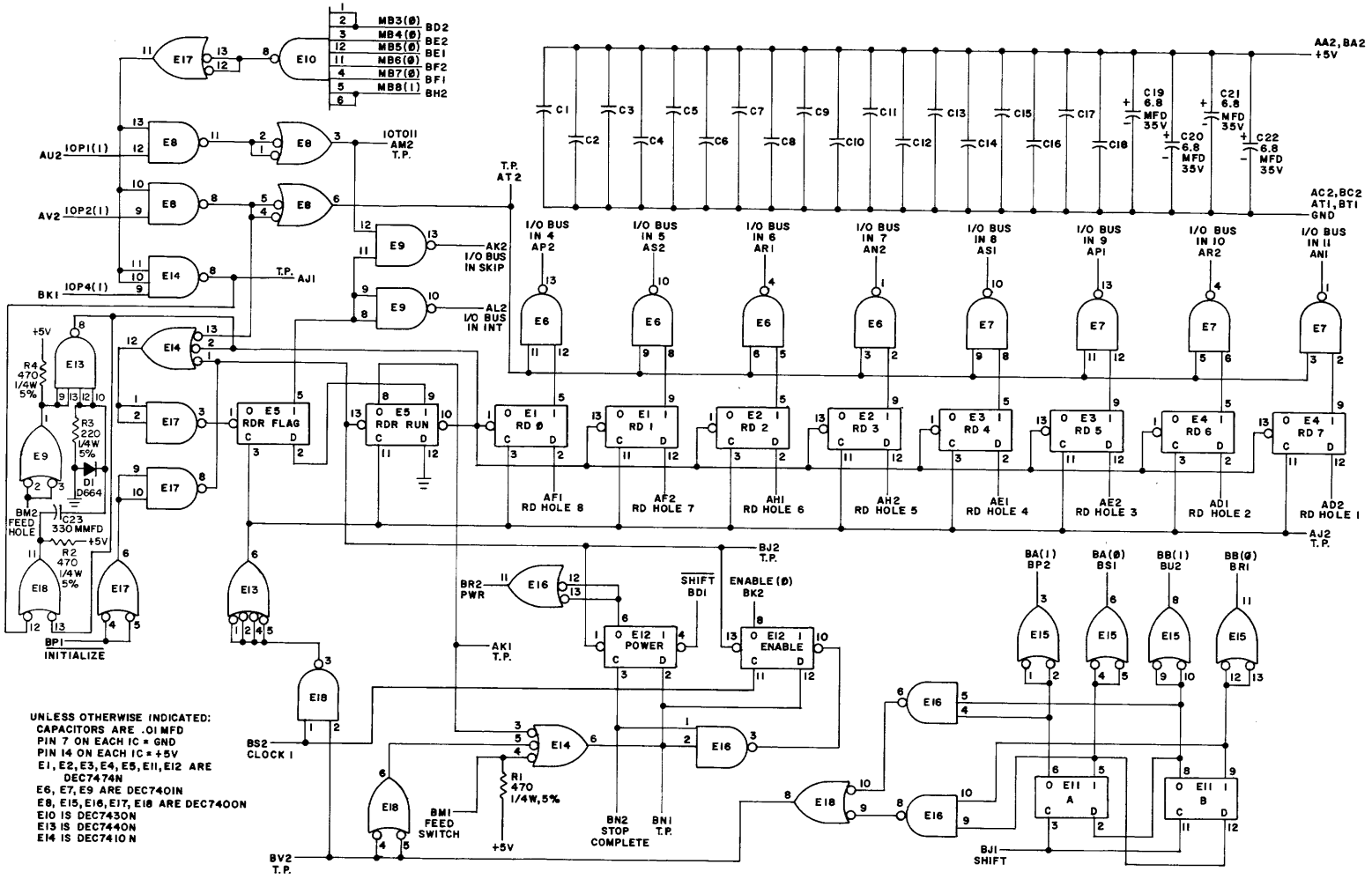
TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3009B	2N3009		
DEC6534B	MPS6534		
D664	IN3606		

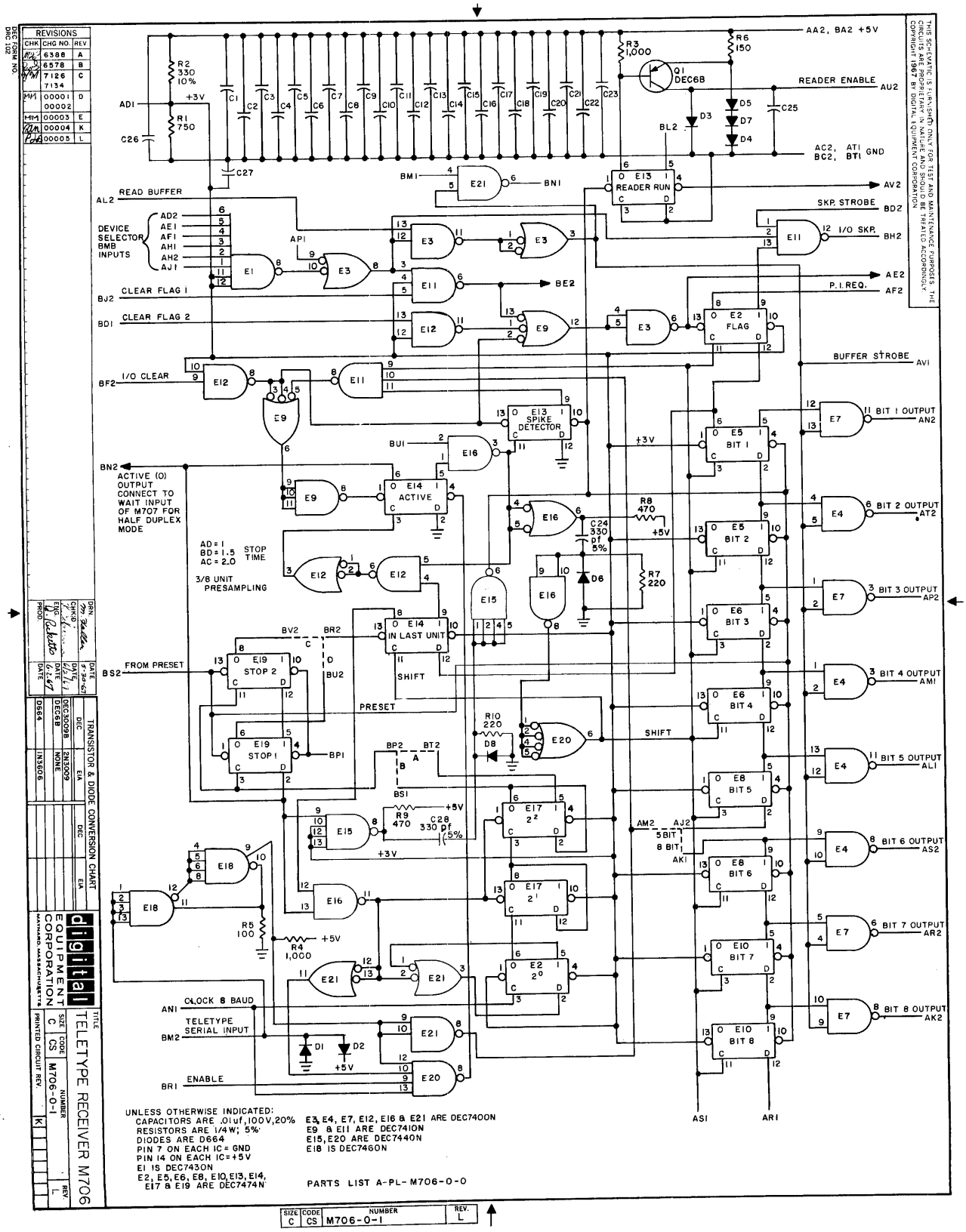
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: PLOTTER CONTROL M704
SIZE D | CODE | CS | NUMBER M704-0-1 | REV E
PRINTED CIRCUIT REV. B

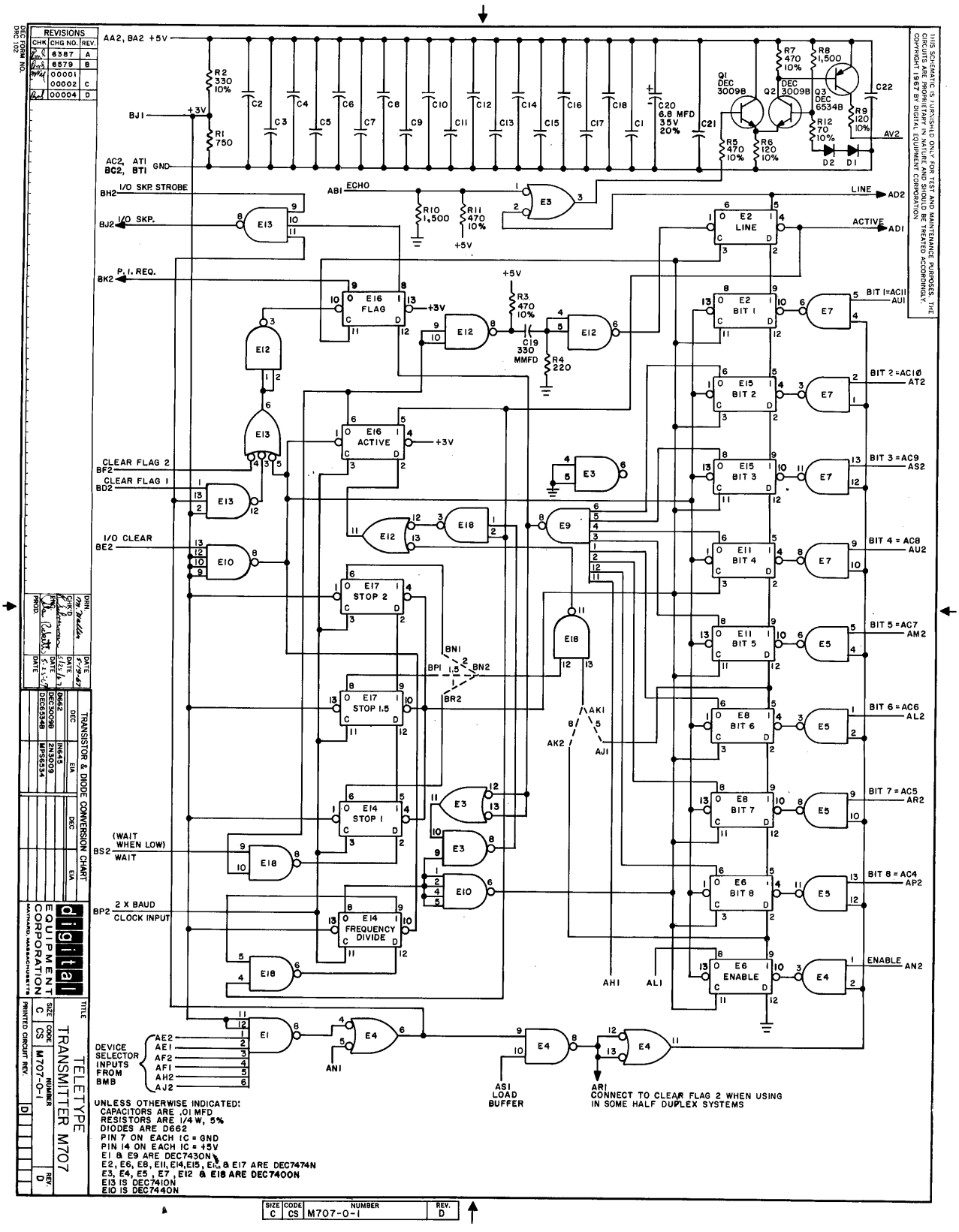
DEC FORM NO. DRG 101

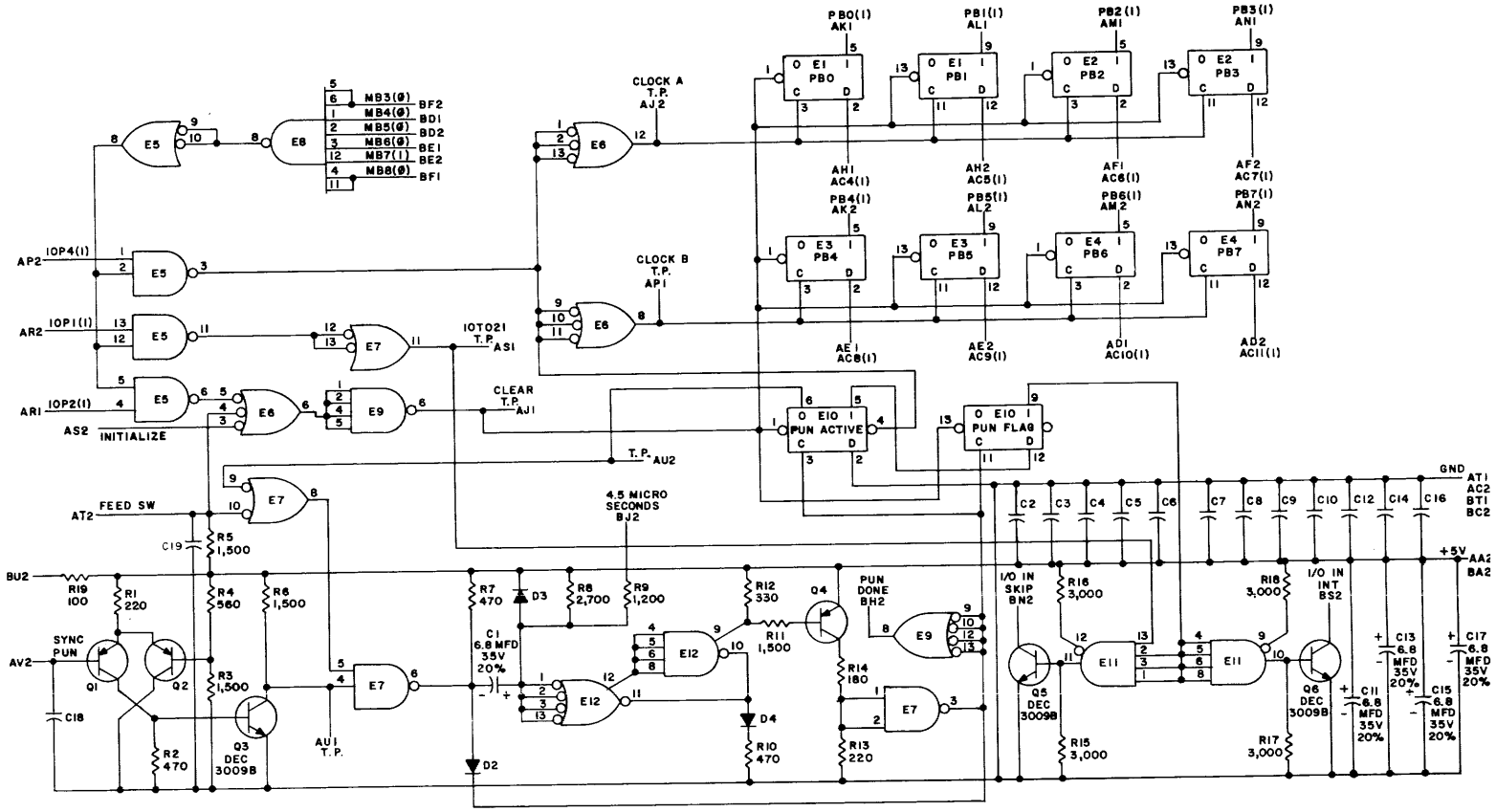


C-CS-M705-0-1 Reader Control



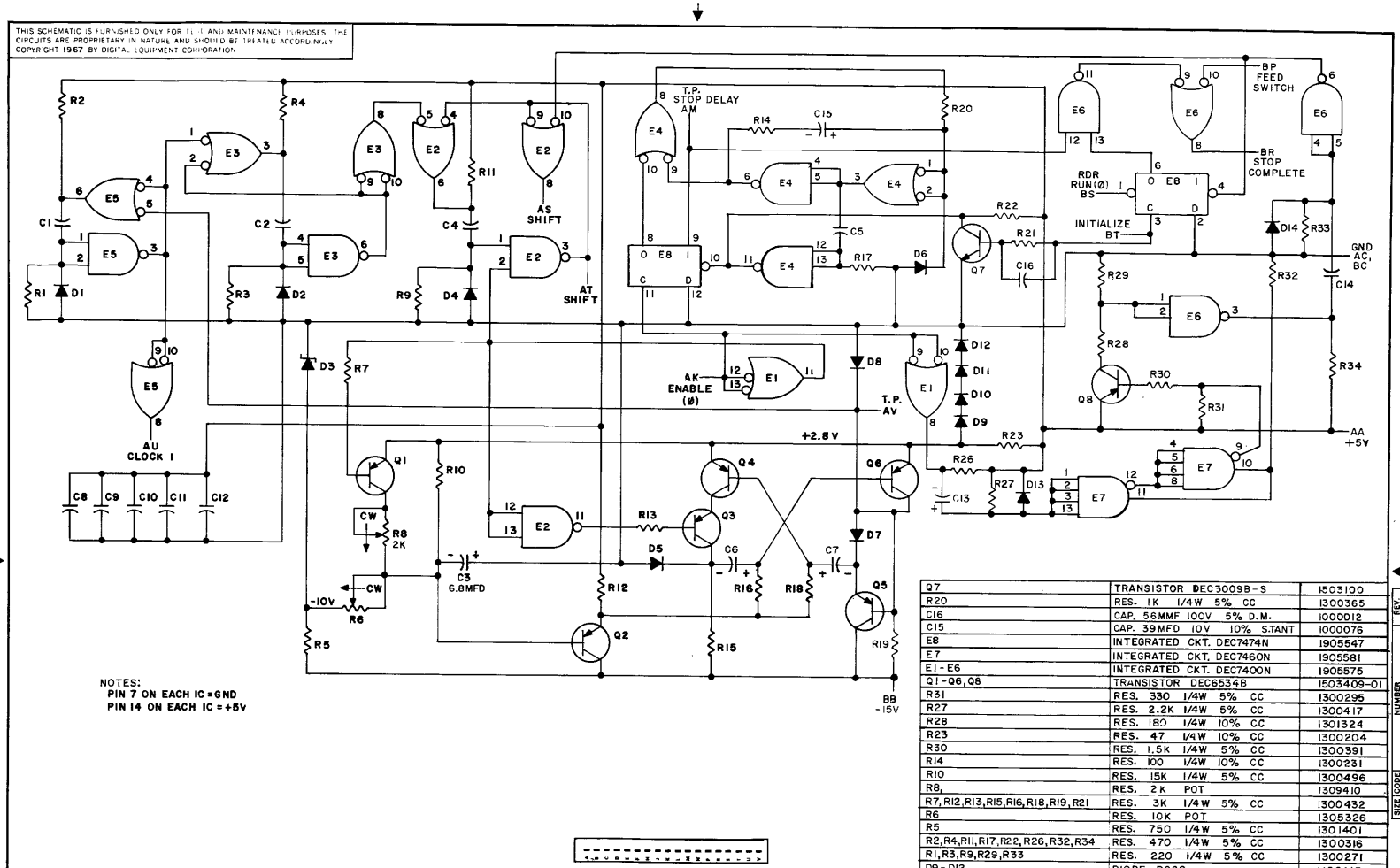
SIZE C | CODE CS | NUMBER M706-0-1 | REV. L


REVISIONS
CHK | CHG NO. | REV.
6387 | A
6579 | B
00001 | C
00002 | D
00004 | D
AA2, BA2 +5V
BJ1
+3V
AC2, ATI
BC2, BTI
GND
R1 750
R2 330 10%
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18
C20 6.8 MFD 35V 20%
C21
C22
Q1 DEC 3009B
Q2 DEC 3009B
Q3 DEC 6534B
R5 470 10%
R6 120 10%
R7 470 10%
R8 1,500
R9 120 10%
R12 70 10%
D1
D2
AV2
BH2 I/O SKP STROBE
BJ2 I/O SKP.
BK2 P.I. REQ.
ABI ECHO
R10 1,500
R11 470 10%
+5V
LINE
AD2
ACTIVE
ADI
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18
E16 FLAG
E16 ACTIVE
E2 LINE
E2 BIT 1
E15 BIT 2
E15 BIT 3
E11 BIT 4
E11 BIT 5
E8 BIT 6
E8 BIT 7
E6 BIT 8
E6 ENABLE
R3 470 10%
C19 330 MMFD
R4 220
BIT 1=ACII AUI
BIT 2=AC1Ø AT2
BIT 3=AC9 AS2
BIT 4=AC8 AU2
BIT 5=AC7 AM2
BIT 6=AC6 AL2
BIT 7=AC5 AR2
BIT 8=AC4 AP2
ENABLE AN2
CLEAR FLAG 2
BF2
CLEAR FLAG 1
BD2
I/O CLEAR
BE2
E17 STOP 2
E17 STOP 1.5
E14 STOP 1
E14 FREQUENCY DIVIDE
BN1
BP1
BN2
BR2
AK1
AK2
AJ1
AH1
AL1
(WAIT WHEN LOW) WAIT
BS2
2 X BAUD CLOCK INPUT
BP2
DEVICE SELECTOR INPUTS FROM BMB
AE2
AE1
AF2
AF1
AH2
AJ2
AN1
ASI LOAD BUFFER
ARI CONNECT TO CLEAR FLAG 2 WHEN USING IN SOME HALF DUPLEX SYSTEMS
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01 MFD
RESISTORS ARE 1/4 W, 5%
DIODES ARE D662
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1 & E9 ARE DEC7430N
E2, E6, E8, E11, E14, E15, E16 & E17 ARE DEC7474N
E3, E4, E5, E7, E12 & E18 ARE DEC7400N
E13 IS DEC7410N
E10 IS DEC7440N
TRANSISTOR & DIODE CONVERSION CHART
DEC | EIA
D662 | IN645
DEC3009B | 2N3009
DEC6534B | MPS6534
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE TELETYPE TRANSMITTER M707
SIZE C | CODE CS | NUMBER M707-0-1 | REV. D
PRINTED CIRCUIT REV. D
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.
COPYRIGHT 1967 BY DIGITAL EQUIPMENT CORPORATION



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
TRANSISTORS ARE DEC6534B
CAPACITORS ARE .01 MFD
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1, E2, E3, E4, E10 ARE DEC7474N
E5, E7 ARE DEC7400N
E6 IS DEC7410N
E8 IS DEC7430N
E9 IS DEC7440N
E11, E12 ARE DEC7460N
DIODES ARE D664

C-CS-M710-0-1 Punch Control



Q7	TRANSISTOR DEC3009B-S	1503100
R20	RES. 1K 1/4W 5% CC	1300365
C16	CAP. 56MMF 100V 5% D.M.	1000012
C15	CAP. 39MFD 10V 10% S.TANT	1000076
E8	INTEGRATED CKT. DEC7474N	1905547
E7	INTEGRATED CKT. DEC7460N	1905581
E1-E6	INTEGRATED CKT. DEC7400N	1905575
Q1-Q6,Q8	TRANSISTOR DEC6534B	1503409-01
R31	RES. 330 1/4W 5% CC	1300295
R27	RES. 2.2K 1/4W 5% CC	1300417
R28	RES. 180 1/4W 10% CC	1301324
R23	RES. 47 1/4W 10% CC	1300204
R30	RES. 1.5K 1/4W 5% CC	1300391
R14	RES. 100 1/4W 10% CC	1300231
R10	RES. 15K 1/4W 5% CC	1300496
R8,	RES. 2K POT	1309410
R7,R12,R13,R15,R16,R18,R19,R21	RES. 3K 1/4W 5% CC	1300432
R6	RES. 10K POT	1305326
R5	RES. 750 1/4W 5% CC	1301401
R2,R4,R11,R17,R22,R26,R32,R34	RES. 470 1/4W 5% CC	1300316
R1,R3,R9,R29,R33	RES. 220 1/4W 5% CC	1300271
D9-D12	DIODE D662	1100113
D1,D2,D4-D8,D13,D14	DIODE D664	1100114
D3	DIODE 1N758	1103116
C13	CAP. 2.2MFD 35V 10% S.TANT	1002431
C6,C7	CAP. 1 MFD 35V 10% S.TANT	1001776
C5	CAP. 330MMF 100V 5% D.M	1000023
C3	CAP. 6.8MFD 35V 10% S.TANT	1005306
C2,C8-C12	CAP. .01 MFD 100V 20% DISC	1001610
C1,C4,C14	CAP. 560MMF 100V 5% D.M	1000025
	PARTS LIST	A-PL-M715-0-0
REFERENCE DESIGNATION	DESCRIPTION	PART NO.

PARTS LIST

REVISIONS			
CHK	CHG NO.	REV	
	70118	B	
	71147	C	
	00001	D	
	00002	E	
	00003	F	

DRN. M. Fuller DATE 10-16-67
CHKD DATE 11/1/67
ENGR DATE 11/2/67
PROD. DATE

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC6534B	MPS6534		
D662	IN645		
D664	IN5606		
IN758	SAME		

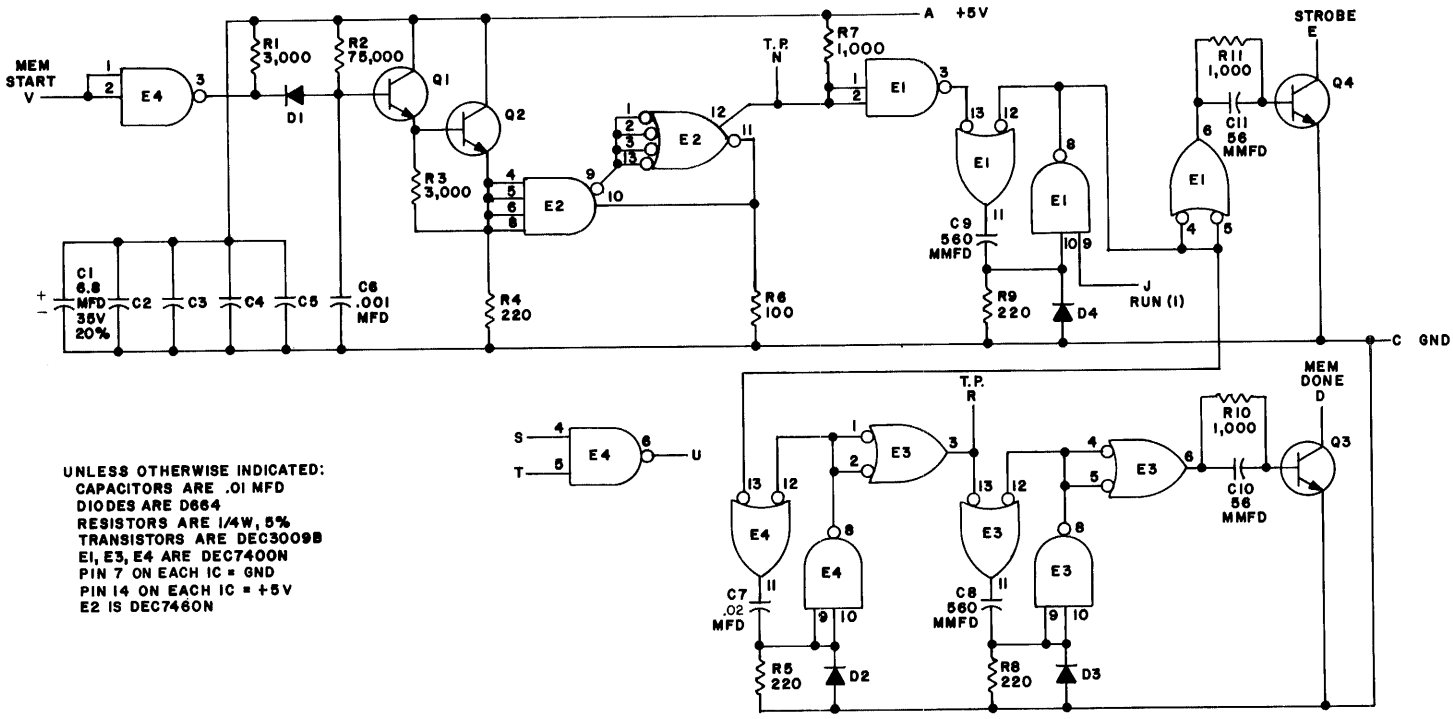
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: READER CLOCK M715

SIZE	CODE	NUMBER	REV.
C	CS	M715-0-1	F

PRINTED CIRCUIT REV. C

DEC FORM NO. DRC 102



B-CS-M720-0-1 Memory Detection

PART III

APPENDICES

APPENDIX A
LOGIC SYMBOLOGY

The symbology employed with the PDP-8/I and M-series modules is similar in nature to MIL-STD-806B. This appendix describes the modified DEC symbology with definitions of logic functions, graphic representations of the functions, and examples of their application. A Table of Combinations is also shown.

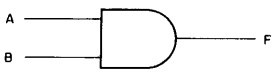
A.1 LOGIC SYMBOLS

In the following list of logic symbols, truth tables accompany the graphic representations. The truth tables use the letters H to mean HIGH (+3V), and L to mean LOW (0V).

A.1.1 State Indicator

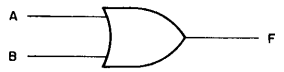
The presence of the small circle symbol at the input(s) of a function indicates that the relativelylow (L) input signal activates the functions; the absence of this small circle indicates that a relatively high (H) input signal activates the function. Similarly, a small circle at the output of a function indicates that the output terminal of the activated function is relatively low, whereas, with the absence of the circle at the output of the symbol, the output is relatively high. Examples of this symbology are shown below with the AND and OR functions, and also in Table A-1.

A.1.1.1 State Indicator Absent - AND - The symbol shown below represents the AND function. The output (F) is high only when the inputs (A and B) are high.



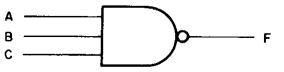
INPUT		OUTPUT
A	B	F
L	L	L
L	H	L
H	L	L
H	H	H

OR - The symbol shown below represents the OR function. The OR output (F) is high if any one or more inputs (A and B) is high.



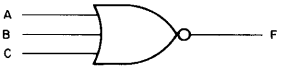
INPUT		OUTPUT
A	B	F
L	L	L
L	H	H
H	L	H
H	H	H

A.1.1.2 State Indicator Present - NAND - The symbol shown below represents one version of the NAND function. The output is low only when all of the inputs are high. NAND logic is the major gate configuration of the PDP-8/I.



INPUT			OUTPUT
A	B	C	F
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

NOR - The symbol shown below represents one version of the NOR function. The output is low if one or more of the inputs is high.



INPUT			OUTPUT
A	B	C	F
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

NOR - The symbol shown below represents another version of the NOR functions. The output is high if one or more of the inputs is low. Note that the truth table for this function is identical to one version of the NAND function.

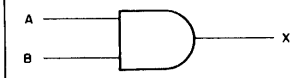
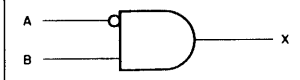
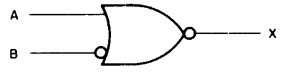
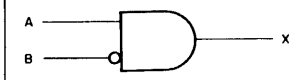
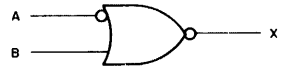
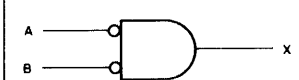
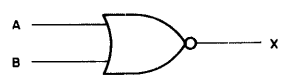
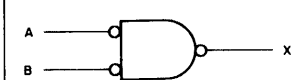
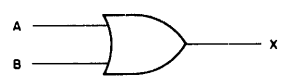
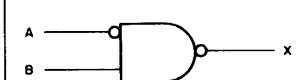
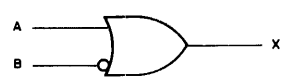
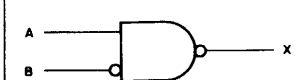
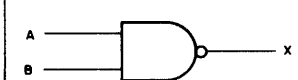
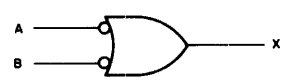
INPUT			OUTPUT
A	B	C	F
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

A.1.2 Table of Combinations

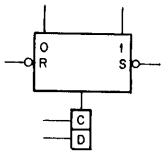
Figure A-1 illustrates the applications and functions of two variables and equivalents as well as the relationship to DEC-DTL logic.

A.1.3. Flip-Flop

The flip-flop is a device that stores a single bit of information. It has three possible inputs, set (S), clear (R), and the data input (C and D). There are two data outputs, 0 and 1. The graphical representation of the D type flip-flop is shown below. If the D input is high when a pulse appears at the C input, the flip-flop will set (1). Similarly, if the D input is low when input C is pulsed, the flip-flop clears (0). The converse of the above two statements is true when the graphic symbol D input has a small circle preceding it. The direct clear and direct set inputs are normal-

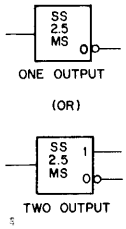
AND	OR	A B C
		H H H H L L L H L L L L
		H H L H L L L H H L L L
		H H L H L H L H L L L L
		H H L H L L L H L L L H
		H H H H L H L H H L L L
		H H H H L L L H H L L H
		H H H H L L L H H L L H
		H H L H L H L H H L L H

ly high. The clear and set functions occur with a high-to-low transition.



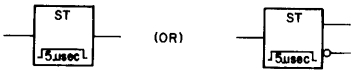
A.1.4 Single-Shot Functions

The symbol shown below represents the single-shot (SS) function. Output signal shape, amplitude, duration and polarity are determined by the circuit characteristics of this device. The unactuated state of the SS is either a 0 or a 1. When the input is actuated by a high-to-low level change, the 1 output goes high and remains high for the duration of the active time of the device. Similarly, when the input is actuated, the 0 output goes low for the time duration of the device.



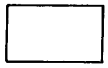
A.1.5 Schmitt Trigger

The symbol shown below represents the Schmitt trigger (ST) function. The device is actuated when the input signal crosses a certain threshold voltage. Output signal amplitude and polarity are determined by the circuit characteristics of this device. The unactuated state of the ST is either 0 or 1. When actuated, it changes to the opposite state and remains there until the input no longer remains above the actuating threshold voltage.



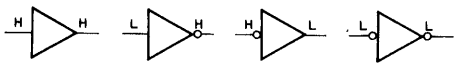
A.1.6 General Logic Symbols

Symbols for functions not specified elsewhere are normally represented as shown below. An example of this symbology is the PDP-8/I Inhibit Driver.



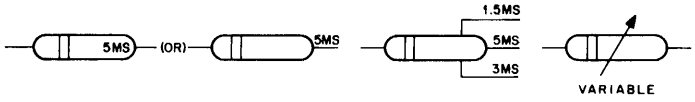
A.1.7 Amplifier

This symbol represents a linear or nonlinear current or voltage amplifier. Level changers, inverters, emitter followers and lamp drivers are examples of devices for which this symbol is applicable.



A.1.8 Time Delay Symbol

The symbol for a delay is shown below. The duration is specified within the symbol except when there are two or more outputs, in this case the outputs have the duration time adjacent to each output.



APPENDIX B
TABLES OF PDP-8/I INSTRUCTIONS

Memory Reference Instructions

Mnemonic Symbol	Operation Code	Direct Addr. States Entered	Direct Addr. Execution Time (μs)	Indirect Addr. States Entered	Indirect Addr. Execution Time (μs)	Operation
AND Y	0	F,E	3.0	F,D,E	4.5	Logical AND. The AND operation is performed between the content of memory location Y and the content of the AC. The result is left in the AC, the original content of the AC is lost, and the content of Y is restored. Corresponding bits of the AC and Y are operated upon independently. ACj ∧ Yj=>ACj
TAD Y	1	F,E	3.0	F,D,E	4.5	Two's complement add. The content of memory location Y is added to the content of the AC in two's complement arithmetic. The result of this addition is held in the AC, the original content of the AC is lost, and the content of Y is restored. If there is a carry from AC0, the link is complemented. AC + Y = > AC
ISZ Y	2	F,E	3.0	F,D,E	4.5	Increment and skip if zero. The content of memory location Y is incremented by one. If the Y then equals zero, the content of the PC is incremented and the next instruction is skipped. If the resultant content of Y does not equal zero, the program proceeds to the next instruction. The incremented content of Y is restored to memory. If resultant Y = 0, PC + 1 = > PC.

Memory Reference Instructions (Cont)

Mnemonic Symbol	Operation Code	Direct Addr. States Entered	Direct Addr. Execution Time (μs)	Indirect Addr. States Entered	Indirect Addr. Execution Time (μs)	Operation
DCA Y	3	F,E	3.0	F,D,E	4.5	Deposit and clear AC. The content of the AC is deposited in core memory at address Y and the AC is cleared. The previous content of memory location Y is lost. AC = > Y 0 = > AC
JMS Y	4	F,E	3.0	F,D,E	4.5	Jump to subroutine. The content of the PC is deposited in core memory location Y and the next instruction is taken from core memory location Y + 1. PC + 1 = > Y Y + 1 = > PC
JMP Y	5	F	1.5	F,D	3.0	Jump to Y. Address Y is set into the PC so that the next instruction is taken from core memory address Y. The original content of the PC is lost. Y = > PC

Group 1 Operate Microinstructions

Mnemonic Symbol	Octal Code	Sequence	Operation
NOP	7000	--	No operation. Causes a 1.5 μs program delay.
IAC	7001	3	Increment AC. The content of the AC is incremented by one in two's complement arithmetic.
RAL	7004	4	Rotate AC and L left. The content of the AC and the L are rotated left one place.
RTL	7006	4	Rotate two places to the left. Equivalent to two successive RAL operations.
RAR	7010	4	Rotate AC and L right. The content of the AC and L are rotated right one place.
RTR	7012	4	Rotate two places to the right. Equivalent to two successive RAR operations.
CML	7020	2	Complement L.
CMA	7040	2	Complement AC. The content of the AC is set to the one's complement of its current content.
CIA	7041	2,3	Complement and increment accumulator. Used to form two's complement.
CLL	7100	1	Clear L.
CLL RAL	7104	1,4	Shift positive number one left.
CLL RTL	7106	1,4	Clear link, rotate two left.
CLL RAR	7110	1,4	Shift positive number one right.
CLL RTR	7112	1,4	Clear link, rotate two right.
STL	7120	1,2	Set link, The L is set to contain a binary 1.
CLA	7200	1	Clear AC. To be used alone or in OPR 1 combinations.
CLA IAC	7201	1,3	Set AC = 1.
GLK	7204	1,4	Get link. Transfer L into AC11.
CLA CLL	7300	1	Clear AC and L.
STA	7240	2	Set AC = -1. Each bit of the AC is set to contain a 1.

Group 2 Operate Microinstructions

Mnemonic Symbol	Octal Code	Sequence	Operation
HLT	7402	3	Halt. Stops the program after completion of the cycle in process. If this instruction is combined with others in the OPR 2 group the other operations are completed before the end of the cycle.
OSR	7404	3	OR with switch register. The OR function is performed between the content of the SR and the content of the AC, with the result left in the AC.
SKP	7410	1	Skip, unconditional. The next instruction is skipped.
SNL	7420	1	Skip if L $\neq$ 0.
SZL	7430	1	Skip if L = 0.
SZA	7440	1	Skip if AC = 0.
SNA	7450	1	Skip if AC $\neq$ 0.
SZA SNL	7460	1	Skip if AC = 0, or L = 1, or both.
SNA SZL	7470	1	Skip if AC $\neq$ 0 and L = 0.
SMA	7500	1	Skip on minus AC. If the content of the AC is a negative number, the next instruction is skipped.
SPA	7510	1	Skip on positive AC. If the content of the AC is a positive number, the next instruction is skipped.
SMA SNL	7520	1	Skip if AC < 0, or L = 1, or both.
SPA SZL	7530	1	Skip if AC > 0 and if L = 0.
SMA SZA	7540	1	Skip if AC < 0.
SPA SNA	7550	1	Skip if AC > 0.
CLA	7600	2	Clear AC. To be used alone or in OPR 2 combinations.
LAS	7604	1,3	Load AC with SR.
SZA CLA	7640	1,2	Skip if AC = 0, then clear AC.
SNA CLA	7650	1,2	Skip if AC $\neq$ 0, then clear AC.
SMA CLA	7700	1,2	Skip if AC < 0, then clear AC.
SPA CLA	7710	1,2	Skip if AC > 0, then clear AC.

Extended Arithmetic Element Microinstructions

Mnemonic Symbol	Octal Code	Sequence	Operation
MUY	7405	3	Multiply. The number held in the MQ is multiplied by the number held in core memory location PC + 1 (or the next successive core memory location after the MUY Command). At the conclusion of this command the most significant 12 bits of the product are contained in the AC and the least significant 12 bits of the product are contained in the MQ. Y x MQ = > AC, MQ.
DVI	7407	3	Divide. The 24-bit dividend held in the AC (most significant 12 bits) and the MQ (least significant 12 bits) is divided by the number held in core memory location PC + 1 (or the next successive core memory location following the DVI command). At the conclusion of this command the quotient is held in the MQ, the remainder is in the AC, and the L contains a 0. If the L contains a 1, divide overflow occurred so the operation was concluded after the first cycle of the division. AC, MQ ÷ Y = > MQ.
NMI	7411	3	Normalize. This instruction is used as part of the conversion of a binary number to a fraction and an exponent for use in floating-point arithmetic. The combined content of the AC and the MQ is shifted left by this one command until the content of AC0 is not equal to the content of AC1, to form the fraction. Zeros are shifted into vacated MQ11 positions for each shift. At the conclusion of this operation, the step counter contains a number equal to the number of shifts performed. The content of L is lost. ACj = > ACj -1 AC0 = > L MQ 0 = > AC11 MQj = > MQj -1 0 = > MQ11 until AC0 ≠ AC1
SHL	7413	3	Shift arithmetic left. This instruction shifts the combined content of the AC and MQ to the left one position more than the number of positions indicated by the content of core memory at address PC + 1 (or the next successive core memory location following the SHL command). During the shifting, zeros are shifted into vacated MQ11 positions.

Extended Arithmetic Element Microinstructions (Cont)

Mnemonic Symbol	Octal Code	Sequence	Operation
SHL (Cont)			Shift Y + 1 positions as follows. ACj = > ACj - 1 AC0 = > L MQ0 = > AC11 MQj = > MQj - 1 0 = > MQ11
ASR	7415	3	Arithmetic shift right. The combined content of the AC and the MQ is shifted right one position more than the number contained in memory location PC + 1 (or the next successive core memory location following the ASR command). The sign bit, contained in AC0, enters vacated positions, the sign bit is preserved, information shifted out of MQ11 is lost, and the L is undisturbed during this operation. Shift Y + 1 positions as follows: AC0 = > AC0 ACj = > ACj + 1 AC11 = > MQ0 MQj = > MQj + 1
LSR	7417	3	Logical shift right. The combined content of the AC and MQ is shifted left one position more than the number contained in memory location PC + 1 (or the next successive core memory location following the LSR command). This command is similar to the ASR command except that zeros enter vacated positions instead of the sign bit entering these locations. Information shifted out of MQ11 is lost and the L is undisturbed during this operation. Shift Y + 1 positions as follows: 0 = > AC0 ACj = > ACj + 1 AC11 = > MQ0 MQj = > MQj + 1
MQL	7421	2	Load multiplier quotient. This command clears the MQ, loads the content of the AC into the MQ, then clears the AC. 0 = > MQ AC = > MQ 0 = > AC
SCA	7441	2	Step counter load into accumulator. The content of the step counter is transferred into the AC. The AC should be cleared prior to issuing this command or the CLA command can be

Extended Arithmetic Element Microinstructions (Cont)

Mnemonic Symbol	Octal Code	Sequence	Operation
SCA (Cont)			combined with the SCA to clear the AC, then effect the transfer. SC V AC = > AC
SCL	7403	3	Step counter load from memory. Loads complement of bits 7 through 11 of the word in memory following the instruction into the step counter. $\overline{MB_{7-11}}$ = > SC PC + 2 = > PC
MQA	7501	2	Multiplier quotient load into accumulator. The content of the MQ is transferred into the AC. This command is given to load the 12 least significant bits of the product into the AC following a multiplication, or to load the quotient into the AC following a division. The AC should be cleared prior to issuing this command or the CLA command can be combined with the MQA to clear the AC then effect the transfer. MQ V AC = > AC
CLA	7601	1	Clear accumulator. The AC is cleared during sequence 1, allowing this command to be combined with the other EAE commands that load the AC during sequence 2 (such as SCA and MQA). 0 = > AC
CAM	7621	1,2	Clear accumulator and multiplier quotient. CAM = CLA LMQ.

Basic IOT Microinstructions

Mnemonic	Octal	Operation
Program Interrupt		
ION	6001	Turn interrupt on and enable the computer to respond to an interrupt request. When this instruction is given, the computer executes the next instruction, then enables the interrupt. The additional instruction allows exit from the interrupt subroutine before allowing another interrupt to occur.
IOF	6002	Turn interrupt off; i.e., disable the interrupt.
High Speed Perforated-Tape Reader and Control		
RSF	6011	Skip if reader flag is a 1.
RRB	6012	Read the content of the reader buffer and clear the reader flag. (This instruction does not clear the AC.) RB V AC 4-11 = > AC 4-11
RFC	6014	Clear reader flag and reader buffer, fetch one character from tape and load it into the reader buffer, and set the reader flag when done.
High Speed Perforated-Tape Punch and Control		
PSF	6021	Skip if punch flag is a 1.
PCF	6022	Clear punch flag and punch buffer.
PPC	6024	Load the punch buffer from bits 4 through 11 of the AC and punch the character. (This instruction does not clear the punch flag or punch buffer.) AC 4-11 V PB = > PB
PLS	6026	Clear the punch flag, clear the punch buffer, load the punch buffer from the content of bits 4 through 11 of the accumulator, punch the character, and set the punch flag to 1 when done.
Teletype Keyboard/Reader		
KSF	6031	Skip if keyboard flag is a 1.
KCC	6032	Clear AC and clear keyboard flag.
KRS	6034	Read keyboard buffer static. (This is a static command in that neither the AC nor the keyboard flag is cleared.) TTI V AC 4-11 = > AC 4-11
KRB	6036	Clear AC, clear keyboard flag, and read the content of the keyboard buffer into the content of AC 4-11.
Teletype Teleprinter/Punch		
TSF	6041	Skip if teleprinter flag is a 1.
TCF	6042	Clear teleprinter flag.
TPC	6044	Load the TTO from the content of AC 4-11 and print and/or punch the character.

Basic IOT Microinstructions (Cont)

Mnemonic	Octal	Operation
Teletype Teleprinter/Punch (cont)		
TLS	6046	Load the TTO from the content of AC 4-11, clear the teleprinter flag, and print and/or punch the character.
Oscilloscope Display Type VC8/I and Precision CRT Display Type 30N		
DCX	6051	Clear X-coordinate buffer.
DXL	6053	Clear and load X-coordinate buffer. AC 2-11 = > YB
DIX	6054	Intensify the point defined by the content of the X- and Y-coordinate buffers.
DXS	6057	Executes the combined functions of DXL followed by DIX.
DCY	6061	Clear Y-coordinate buffer.
DYL	6063	Clear and load Y-coordinate buffer. AC 2-11 = > YB
DIY	6064	Intensify the point defined by the content of the X- and Y-coordinate buffers.
DYS	6067	Executes the combined functions of DYL followed by DIY.
Oscilloscope Display Type VC8/I		
DSB	6075	Set minimum brightness.
DSB	6076	Set medium brightness.
DSB	6077	Set maximum brightness.
DSB	6074	Zero brightness.
Precision CRT Display Type 30N		
DLB	6074	Load brightness register (BR) from bits 9 through 11 of the AC. AC 9-11 = > BR
Light Pen Type 370		
DSF	6071	Skip if display flag is a 1.
DCF	6072	Clear the display flag.
Memory Parity Type MP8/I		
SMP	6101	Skip if memory parity error flag = 0.
CMP	6104	Clear memory parity error flag.
Automatic Restart Type KP8/I		
SPL	6102	Skip if power is low.

Mnemonic	Octal	Operation
Memory Extension Control Type MC8/I		
CDF	62N1	Change to data field N. The data field register is loaded with the selected field number (0 to 7). All subsequent memory requests for operands are automatically switched to that data field until the data field number is changed by a new CDF command.
CIF	62N2	Prepare to change to instruction field N. The instruction buffer register is loaded with the selected field number (0 to 7). The next JMP or JMS instruction causes the new field to be entered.
RDF	6214	Read data field into AC 6-8. Bits 0-5 and 9-11 of the AC are not affected.
RIF	6224	Same as RDF except reads the instruction field.
RIB	6234	Read interrupt buffer. The instruction field and data field stored during an interrupt are read into AC 6-8 and 9-11 respectively.
RMF	6244	Restore memory field. Used to exit from a program interrupt.
Data Communications Systems Type 680		
TTINCR	6401	The content of the line select register is incremented by one.
TTI	6402	The line status word is read and sampled. If the line is active for the fourth time, the line bit is shifted into the character assembly word. If the line is active for a number of times less than four, the count is incremented. If the line is not active, the active/inactive status of the line is recorded.
TTO	6404	The character in the AC is shifted right one position, zeros are shifted into vacated positions, and the original content of AC11 is transferred out of the computer on the Teletype line.
TTCL	6411	The line select register is cleared.
TTSL	6412	The line select register is loaded by an OR transfer from the content of AC5-11, then the AC is cleared.
TTRL	6414	The content of the line select register is read into AC5-11 by an OR transfer.
TTSKP	6421	Skip if clock 1 flag is a 1.
TTXON	6424	Clock 1 is enabled to request a program interrupt and clock 1 flag is cleared.
TTXOF	6422	Clock 1 is disabled from causing a program interrupt and clock 1 flag is cleared.
Incremental Plotter and Control Type VP8/I		
PLSF	6501	Skip if plotter flag is a 1.
PLCF	6502	Clear plotter flag.
PLPU	6504	Plotter pen up. Raise pen off of paper.

Mnemonic	Octal	Operation
Incremental Plotter and Control Type VP8/1 (Cont)		
PLPR	6511	Plotter pen right.
PLDU	6512	Plotter drum (paper) upward.
PLDD	6514	Plotter drum (paper) downward.
PLPL	6521	Plotter pen left.
PLUD	6522	Plotter drum (paper) upward. (Same as 6512.)
PLPD	6524	Plotter pen down. Lower pen on to paper.
Serial Magnetic Drum System Type 251		
DRCR	6603	Load the drum core location counter with the core memory location information in the accumulator. Prepare to read one sector of information from the drum into the specified core location. Then clear the AC.
DRCW	6605	Load the drum core location counter with the core memory location information in the accumulator. Prepare to write one sector of information into the drum from the specified core location. Then clear the AC.
DRCF	6611	Clear completion flag and error flag.
DREF	6612	Clear the AC then load the condition of the parity error and data timing error flip-flops of the drum control into accumulator bits 0 and 1 respectively, to allow programmed evaluation of an error flag.
DRTS	6615	Load the drum address register with the track and sector address held in the accumulator. Clear the completion and error flags, and begin a transfer (reading or writing). Then clear the AC.
DRSE	6621	Skip next instruction if the error flag is a 0 (no error).
DRSC	6622	Skip next instruction if the completion flag is a 1 (sector transfer is complete).
DRCN	6624	Clear error flag and completion flag, then initiate transfer of next sector.
Serial Magnetic Drum System Type RM08		
DRCR	6603	Load the drum core location counter with the core memory location information in the accumulator. Prepare to read one sector of information from the drum into the specified core location. Then clear the AC.
DRCW	6605	Load the drum core location counter with the core memory location information in the accumulator. Prepare to write one sector of information into the drum from the specified core location. Then clear the AC.
DRCF	6611	Clear completion flag and error flag.

Mnemonic	Octal	Operation
Serial Magnetic Drum System Type RM08 (Cont)		
DRES	6612	Clear the AC then load the condition of the parity error and data timing error flip-flops of the drum control into accumulator bits 0 and 1 respectively to allow programmed evaluation of an error flag. The contents of the drum sector counter are transferred into bits AC 6-11.
DRTS	6615	Load the drum address register with the track and sector address held in the accumulator. Clear the completion and error flags, and begin a transfer (reading or writing). Then clear the AC.
DRSE	6621	Skip next instruction if the error flag is a 0 (no error).
DRSC	6622	Skip next instruction if the completion flag is a 1 (sector transfer is complete).
DRFS	6624	Loads the drum field register with the contents of the accumulator bits 10 and 11. Loads the sector number register with the contents of the accumulator bits 0-5, to specify the number of sectors to be transferred. Loads the three most significant bits of the drum core location register (DCL_{0-2}) with the contents of the AC bits 5, 7, 8 to specify the core memory block to be used during the drum transfer.
Random Access Disk File (Type DF32)		
DCMA	6601	Clears memory address register, parity error and completion flags. This instruction clears the disk memory request flag and interrupt flags.
DMAR	6603	The contents of the AC are loaded into the disk memory address register and the AC is cleared. Begin to read information from the disk into the specified core location. Clears parity error and completion flags. Clears interrupt flags.
DMAW	6605	The contents of the AC are loaded into the disk memory address register and the AC is cleared. Begin to write information into the disk from the specified core location. Clears parity error and completion flags.
DCEA	6611	Clears the disk extended address and memory address extension register.
DSAC	6612	Skips next instruction if address confirmed flag is a 1. (AC is cleared.)
DEAL	6615	The disk extended address extension registers are cleared and loaded with the track data held in the AC.
DEAC	6616	Clear the AC then loads the contents of the disk extended address register into the AC to allow program evaluation. Skip next instruction if address confirmed flag is a 1.

Basic IOT Microinstructions (Cont)

Mnemonic	Octal	Operation
Random Access Disk File (Type DF32)(Cont)		
DFSE	6621	Skips next instruction if parity error, data request late, or write-lock switch flag is a zero. Indicates no errors.
DFSC	6622	Skip next instruction if the completion flag is a 1. Indicates data transfer is complete.
DMAC	6626	Clear the AC then loads contents of disk memory address register into the AC to allow program evaluation.
Automatic Line Printer and Control Type 645		
LSE	6651	Skip if line printer error flag is a 1.
LCB	6652	Clear both sections of the printing buffer.
LLB	6654	Load printing buffer from the content of AC 6-11 and clear the AC.
LSD	6661	Skip if the printer done flag is a 1.
LCF	6662	Clear line printer done and error flags.
LPR	6664	Clear the format register, load the format register from the content of AC 9-11, print the line contained in the section of the printer buffer loaded last, clear the AC, and advance the paper in accordance with the selected channel of the format tape if the content of AC 8 = 1. If the content of AC 8 = 0, the line is printed and paper advance is inhibited.
DECtape Transport Type TU55 and DECtape Control Type TC01		
DTRA	6761	The content of status register A is read into AC0-9 by an OR transfer. The bit assignments are: AC0-2 = Transport unit select number AC3-4 = Motion AC5 = Mode AC6-8 = Function AC9 = Enable/disable DECtape control flag
DTCA	6762	Clear status register A. All flags undisturbed.
DTXA	6764	Status register A is loaded by an exclusive OR transfer from the content of the AC, and AC10 and AC11 are sampled. If AC10 = 0, the error flags are cleared. If AC11 = 0, the DECtape control flag is cleared.
DTSF	6771	Skip if error flag is a 1 or if DECtape control flag is a 1.
DTRB	6772	The content of status register B is read into the AC by an OR transfer. The bit assignments are: AC0 = Error flag AC1 = Mark track error AC2 = End of tape AC3 = Select error

Mnemonic	Octal	Operation
DECtape Transport Type TU55 and DECtape Control Type TC01 (Cont)		
		AC4 = Parity error AC5 = Timing error AC6-8 = Memory field AC9-10 = Unused AC11 = DECtape flag
DTLB	6774	The memory field portion of status register B is loaded from the content of AC6-8.
Card Reader and Control Type CR8/I		
RCSF	6631	Skip if card reader data ready flag is a 1.
RCRA	6632	The alphanumeric code for the column is read into AC6-11, and the data ready flag is cleared.
RCRB	6634	The binary data in a card column is transferred into AC0-11, and the data ready flag is cleared.
RCSP	6671	Skip if card reader card done flag is a 1.
RCSE	6672	Clear the card done flag, select the card reader and start card motion towards the read station, and skip if the reader-not-ready flag is a 1.
RCRD	6674	Clear card done flag.
Automatic Magnetic Tape Control Type TC58		
MTSF	6701	Skip on error flag or magnetic tape flag. The status of the error flag (EF) and the magnetic tape flag (MTF) are sampled. If either or both are set to 1, the content of the PC is incremented by one to skip the next sequential instruction.
MTCR	6711	Skip on tape control ready (TCR). If the tape control is ready to receive a command, the PC is incremented by one to skip the next sequential instruction.
MTTR	6721	Skip on tape transport ready (TTR). The next sequential instruction is skipped if the tape transport is ready.
MTAF	6712	Clear the status and command registers, and the EF and MTF if tape control ready. If tape control not ready, clears MTF and EF flags only.
- -	6724	Inclusively OR the contents of the command register into bits 0-11 of the bits 0-11 of the AC.
MTCM	6714	Inclusively OR the contents of AC bits 0-5, 9-11 into the command register; JAM transfer bits 6, 7, 8 (command function).
MTLC	6716	Load the contents of AC bits 0-11 into the command register.
- -	6704	Inclusively OR the contents of the status register into bits 0-11 of the AC.

Mnemonic	Octal	Operation
Automatic Magnetic Tape Control Type TC58 (Cont)		
MTRS	6706	Read the contents of the status register into bits 0-11 of the AC.
MTGO	6722	Set "go" bit to execute command in the command register if command is legal.
- -	6702	Clear the accumulator.
General Purpose Converter and Multiplexer Control Type AF01A		
ADSF	6531	Skip if A/D converter flag is a 1.
ADVC	6532	Clear A/D converter flag and convert input voltage to a digital number, flag will set to 1 at end of conversion. Number of bits in converted number determined by switch setting, 11 bits maximum.
ADRB	6534	Read A/D converter buffer into AC, left justified, and clear flag.
ADCC	6541	Clear multiplexer channel address register.
ADSC	6542	Set up multiplexer channel as per AC 6-11. Maximum of 64 single ended or 32 differential input channels.
ADIC	6544	Index multiplexer channel address (present address + 1). Upon reaching address limit, increment will cause channel 00 to be selected.
Guarded Scanning Digital Voltmeter Type AF04A		
VSEL	6542	The contents of the accumulator are transferred to the AF04A control register.
VCNV	6541	The contents of the accumulator are transferred to the AF04A channel address register. Analog signal on selected channel is automatically digitized.
VINX	6544	The last channel address is incremented by one and the analog signal on the selected channel is automatically digitized.
VSDR	6531	Skip if data ready flag is a 1.
VRD	6532	Selected byte of voltmeter is transferred to the accumulator and the data ready flag is cleared.
VBA	6534	Byte Advance command requests next 12 bits, data ready flag is set.
VSCC	6571	Sample Current Channel when required to digitize analog signal on current channel repeatedly.

APPENDIX C
PERFORATED TAPE LOADER SEQUENCE

C.1 READIN MODE LOADER

The readin mode (RIM) loader is a minimum length, basic, perforated-tape reader program for the ASR33. It is initially stored in memory by manual use of the operator console keys and switches. The loader is stored permanently in 18 locations of page 37.

The RIM loader can only be used in conjunction with the ASR33 reader (not the high-speed perforated-tape reader). Because a tape in RIM format is, in effect, twice as long as it need be, it is suggested that the RIM loader be used only to read the binary loader when using the ASR33. (Note that PDP-8 diagnostic program tapes are in RIM format.)

The complete PDP-8/I RIM loader (SA = 7756) is as follows:

A perforated tape to be read by the RIM loader must be in RIM format:

Tape Channel 8 7 6 5 4 S 3 2 1	Format
1 0 0 0 0 . 0 0 0	Leader-trailer code
0 1 A1 . A2 0 0 A3 . A4	Absolute address to contain next 4 digits
0 0 X1 . X2 0 0 X3 . X4	Content of previous 4-digit address
0 1 A1 . A2 0 0 A3 . A4	Address
0 0 X1 . X2 0 0 X3 . X4	Content
(Etc.)	(Etc.)
1 0 0 0 0 . 0 0 0	Leader-trailer code

Absolute Address	Octal Content	Tag	Instruction I Z	Comments
7756,	6032	BEG,	KCC	/CLEAR AC AND FLAG
7757,	6031		KSF	/SKIP IF FLAG = 1
7760,	5357		JMP . -1	/LOOKING FOR CHARACTER
7761,	6036		KRB	/READ BUFFER
7762,	7106		CLL RTL	
7763,	7006		RTL	/CHANNEL 8 IN AC0
7764	7510		SPA	/CHECKING FOR LEADER
7765,	5357		JMP BEG+1	/FOUND LEADER
7766,	7006		RTL	/OK,CHANNEL 7 IN LINK
7767,	6031		KSF	
7770,	5367		JMP . -1	
7771,	6034		KRS	/READ,DO NOT CLEAR
7772,	7420		SNL	/CHECKING FOR ADDRESS
7773,	3776		DCA I TEMP	/STORE CONTENT
7774,	3376		DCA TEMP	/STORE ADDRESS
7775,	5356		JMP BEG	/NEXT WORD
7776,	0	TEMP,	0	/TEMP STORAGE
7777,	5XXX		JMP X	/JMP START OF BIN LOADER

Placing the RIM loader in core memory by way of the operator console keys and switches is accomplished as follows.

1. Set the starting address 7756 in the switch register (SR).
2. Press LOAD ADDRESS key.
3. Set the first instruction (6032) in the SR.
4. Press the DEPOSIT key.
5. Set the next instruction (6031) in the SR.
6. Press DEPOSIT key.
7. Repeat steps 5 and 6 until all 16 instructions have been deposited.

To load a tape in RIM format, place the tape in the reader, set the SR to the starting address 7756 of the RIM loader (not of the program being read), press the Load Address key, press the Start key, and start the teletype reader.

Refer to Digital Program Library document Digital-8-1-U for additional information on the Readin Mode Loader program.

C.2 BINARY LOADER

The binary loader (BIN) is used to read machine language tapes (in binary format) produced by the program assembly language (PAL). A tape in binary format is about one half the length of the comparable RIM format tape. It can, therefore, be read about twice as fast as a RIM tape and is, for this reason, the more desirable format to use with the 10 cps ASR33 reader or the Type PR8/I High Speed Perforated-Tape Reader.

The format of a binary tape is as follows.

LEADER: about 2 ft of leader-trailer codes.

BODY: characters representing the absolute, machine language program in easy-to-read binary (or octal) form. The section of tape may contain characters representing instructions (channels 8 and 7 not punched) or origin re-settings (channel 8 not punched, channel 7 punched) and is concluded by 2 characters

Example of the format of a binary tape.

Tape Channel 8 7 6 5 4 S 3 2 1	Memory Location	Content	Comments
1 0 0 0 0 . 0 0 0			leader-trailer code
0 1 0 0 0 . 0 1 0		0200	
0 0 1 1 1 . 0 1 0			
0 0 0 0 0 . 0 0 0	0200	CLA	origin setting
0 0 0 0 1 . 0 1 0			
0 0 1 1 1 . 1 1 1	0201	TAD 277	
0 0 0 1 1 . 0 1 0			
0 0 1 1 1 . 1 1 0	0202	DCA 276	
0 0 1 1 1 . 1 0 0			
0 0 0 0 0 . 0 1 0	0203	HLT	
0 1 0 0 0 . 0 1 0			
0 0 1 1 1 . 1 1 1		0277	origin setting
0 0 0 0 0 . 0 0 0			
0 0 1 0 1 . 0 1 1	0277	0053	
0 0 0 0 1 . 0 0 0			
0 0 0 0 0 . 1 1 1		1007	sum check
1 0 0 0 0 . 0 0 0			leader-trailer code

(channels 8 and 7 not punched) that represent a checksum for the entire section.

TRAILER: same as leader.

After a BIN tape has been read in, one of the two following conditions exists.

1. No checksum error: halt with AC = 0
2. Checksum error : halt with AC = (computed checksum) - (tape checksum)

Operation of the BIN loader in no way depends upon or uses the RIM loader. To load a tape in BIN format place the tape in the reader, set the SR to 7777 (the starting address of the BIN loader), press the Load Address key, set SR switch 0 up for loading via the teletype unit or down for loading via the high speed reader, then press the Start key, and start the tape reader.

Refer to Digital Program Library document Digital-8-2-U-RIM for additional information on the Binary Loader program.

APPENDIX D
PROGRAMS

The following programs, which were produced for or are usable with the PDP-8/I are available from the Digital Program Library.

Program Number	Function
DEC-08-AEAA	Pal III Definitions for 338
DEC-08-AFCO	4K FORTRAN
DEC-08-AJAE	FOCAL and INIT (4K, INIT)
DEC-08-AJ1E	FOCAL UTILITY OVERLAYS (4 word, 8K)
DEC-08-AJ2E	FOCAL GRAPHIC OVERLAYS
DEC-08-AJ3E	FOCAL 3D SURFACE PLOT Demonstration Program
DEC-08-AJ4E	FOCAL EXTENDED FUNCTIONS
DEC-08-AJ5E	FOCAL DF32 Option MULTI-USER OVERLAYS
DEC-08-AJ6E	FOCAL RF08 Option MULTI-USER OVERLAYS
DEC-08-AJ7E	FOCAL PT08 Option FOUR USER OVERLAYS
DEC-08-AJ8E	FOCAL DC02 Option FOUR USER OVERLAYS
DEC-08-ASB1	Pal III
DEC-08-CDDB	DDT-8
DEC-08-CMAB	MACRO-8
DEC-08-COCO	ODT-8
DEC-08-ESAB	Symbolic Editor
DEC-08-EUFA	DECtape Formatter
DEC-08-FFAC	Program Library MATH ROUTINES
DEC-08-FMAA	Single Precision Square Root
DEC-08-FMBA	Single Precision Signed Mult
DEC-08-FMCB	Single Precision Signed Div
DEC-08-FMDA	Double Precision Signed Mult
DEC-08-FMEA	Double Precison Signed Div
DEC-08-FMFC	Double Precision Sine
DEC-08-FMGB	Double Precision Cosine
DEC-08-FMHA	Four Word Floating Point Package
DEC-08-FMIA	Logical Subroutines
DEC-08-FMJA	Arithmetic Shift Subroutines
DEC-08-FMKA	Logical Shift Subroutines
DEC-08-A2B1	8K FORTRAN
DEC-08-A2D2	8K FORTRAN SABR Assembler
DEC-08-A2C3	FORTRAN 8K-32K Linking Loader
DEC-08-A2B4	8K FORTRAN Library Subroutines 1 of 2
DEC-08-A2B5	8K FORTRAN Library Subroutines 2 of 2
DEC-08-A2B6	8K FORTRAN DECtape I/O Subroutines
DEC-08-A2C7	FORTRAN 8K-32K Linking Loader (Disk)
DEC-08-A2A8	8K FORTRAN SABR - DISK I/O
DEC-08-LBAA	Binary Loader
DEC-08-LHAA	Help Loader
DEC-08-LRAA	RIM Loader
DEC-08-LUAA	TC01 Bootstrap Loader
DEC-08-PMPO	Read-In-Mode (RIM) Punch
DEC-08-PMP1	RIM Punch Low Memory ASR-33
DEC-08-PMP2	RIM Punch High Memory ASR-33
DEC-08-PMP3	RIM Punch High Memory ASR-75

Program Number	Function
DEC-08-PMP4	RIM Punch Low Memory ASR-75
DEC-08-SUCO	TC01 DECtape Subroutines (Paper tape source only)
DEC-08-USA0	Multianalyzer
DEC-08-USA1	Single Parameter Height Analysis AC
DEC-08-USA2	Dual Parameter Height Analysis AC
DEC-08-USYA	Multichannel Analyzer Program Group
DEC-08-US1B	Multichannel Analyzer Program SING.8I
DEC-08-US2B	Multichannel Analyzer Program-DUAL 8I
DEC-08-US3B	Multichannel Analyzer Program-SING.8L
DEC-08-US4A	Multichannel Analyzer Program-PKLOC8
DEC-08-YIRA	Variable Stroke Character (Double Size) Generator
DEC-08-YISB	Variable Stroke Character (Single Size) Generator
DEC-08-YPPA	Octal Memory Dump
DEC-08-YPTA	DECtape Copy Routine
DEC-08-YXYA	Binary Punch (Binary Code Dump for High Speed or Teletype Punch)
DEC-08-YX1A	Binary Punch-Teletype (ASR-33)
DEC-08-YX2A	Binary Punch-High Speed (ASR-75)
DEC-08-YQYA	Floating Point Package
DEC-08-ZJ1B	EDGRIN
DEC-08-ZJ2B	EDGRIN Translator
DEC-08-ZJ3B	EDGRIN Link Generator
DEC-08-ZJ4B	EDGRIN Cursor Mosaic
DEC-08-ZJ5B	EDGRIN Disk Editor Translator
DEC-D8-SBAF	DISK System Builder, DF32/RF08
DEC-D8-PDAD	DISK System PIP for DF32 Option Only
DEC-D8-PDZE	DISK System PIP for RF08 Option Only
DEC-D8-ESAB	DISK Editor
DEC-D8-ASAC	DISK System Assembler PAL-D
DEC-D8-AFA1	FORTRAN-D (4K FORTRAN) Compiler Loader
DEC-D8-AFA2	FORTRAN-D Compiler
DEC-D8-AFA3	FORTRAN-D Operating System Loader
DEC-D8-AFA4	FORTRAN-D Operating System
DEC-D8-AFA5	FORTRAN-D Symbol Print
DEC-D8-AFA6	FORTRAN-D Debugging Program (DIAGnose)
DEC-D8-CDE1	Disk DDT Driver
DEC-D8-CDE2	Disk DDT System
DEC-D8-RWDA	DISK System Restore
Digital-8-21-F	Signed Multiply Single Precision EAE
Digital-8-22-F	Signed Divide Single precision EAE
Digital-8-23-F	Double Precision EAE
Digital-8-25-F	Floating Point EAE
Digital-8-15-S	Oceanographic Analizer
Digital-8-15S	Master Tape Duplicator
Digital-8-35-S-A	TTY 680 5-Bit Character Assembly
Digital-8-35-S-B	TTY 680 5-Bit Character Assembly
Digital-8-3-U	DECtape Loader 552
Digital-8-10-U	BCD to Binary Conversion Subroutines
Digital-8-11-U	Double Precision BCD to Binary Converter
Digital-8-12-U	Incremental Plotter Routine
Digital-8-14-U	Binary to BCD Conversion
Digital-8-15-U	Binary to BCD Conversion (4 Digit)
Digital-8-17-U	EAE Instruction Set Simulator
Digital-8-18-U	Alphanumeric Message Typeout

Program Number	Function
Digital-8-19-U	Teletype Output Subroutines
Digital-8-20-U	Character String Typeout
Digital-8-21-U	Symbolic Tape Format Generator
Digital-8-23-U	Signed Decimal Print, Single Precision
Digital-8-24-U	Unsigned Decimal Print, Double Precision
Digital-8-25-U	Signed Decimal Print, Double Precision
Digital-8-28-U	Single Precision Decimal-to-Binary Conversion and Input ASR-33, Signed or Unsigned
Digital-8-29-U	Double Precision Decimal-to-Binary Conversion and Input ASR-33, Signed or Unsigned
Digital-8-33-U	5/8 TOG (552)
Digital-8-34-U	DECEX for 552
Maindec-828	LT08/PT08 Teleprinter Test
Maindec-08-D0UA	Family-of-8 Random Add Rotate Test
Maindec-08-D02B	Instruction Test 2B
Maindec-08-D04B	Random JMP Test
Maindec-08-D05B	Random JMP-JMS Test
Maindec-08-D07B	Random ISZ Test
Maindec-08-D1AC	Memory Power ON/OFF Test
Maindec-08-D1B0	Memory Address Test
Maindec-08-D1EB	Extended Memory Checkerboard Test
Maindec-08-D1GB	Extended Memory Control Test
Maindec-08-D1HA	Extended Memory Address Test
Maindec-08-D1KA	KR01/KP8I Power Fail Test
Maindec-08-D1L0	Basic Checkerboard Test
Maindec-08-D2AA	Family-of-8 Teletype Test
Maindec-08-D2FC	High Speed Reader Test
Maindec-08-D2GE	High Speed Reader and Punch Test
Maindec-08-D20A	CR03 Card Reader Test
Maindec-08-D2PE	Teletype Test Part 1
Maindec-08-D2QD	Teletype Test Part 2
Maindec-08-D3BC	TC01 Basic Exerciser
Maindec-08-D3EB	TC01 Extended Memory Exerciser
Maindec-08-D3FC	Incremental Tape Delay Test
Maindec-08-D3RA	TC01 DECTREX
Maindec-08-D4A0	Basic Memory Parity Checkerboard
Maindec-08-D4BA	Extended Memory Parity Checkerboard
Maindec-08-D4CB	Incremental Compatibility Test
Maindec-08-D4EB	Incremental Instruction Test
Maindec-08-D4FA	Incremental Random Exerciser
Maindec-08-D5BB	DF32 Diskless, Mini Test
Maindec-08-D5CC	DF32 Disk Data Test
Maindec-08-D5DB	DF32 Multi Disk Test
Maindec-08-D5EB	RF08 Disk Data
Maindec-08-D5FA	Multi Disk
Maindec-08-D6GC	A to D Calibration Test
Maindec-08-D6HA	AF04A Diagnostic and Demo
Maindec-08-D6JD	AD08A/B Diagnostic
Maindec-08-D6KB	34D/VC8I Display Test
Maindec-08-D6MA	VS38 Diagnostic
Maindec-08-D6QA	Low Level Multiplexer AM03/AM08
Maindec-08-D6RA	AF04 Diagnostic Test
Maindec-08-D6TA	AA05A/AA07A Diagnostic Exerciser
Maindec-08-D8EB	DP01A IOT and Data Test
Maindec-08-D8FA	IOT & Data Test for 637
Maindec-08-D8HB	DP01A Test 6301-6354
Maindec-08-D8LB	DP01A Test 6501-6564
Maindec-08-D8MB	DP01A Test 6701-6764
Maindec-08-D8NA	VA38 Character Generator Test

Program Name	Function
Maindec-08-D8PA	PT08 Test for Dataphone
Maindec-08-D8QA	689 ADF On-line Diagnostic
Maindec-08-D8RA	689 Control & Data Test
Maindec-08-D8SB	DM01 Exerciser
Maindec-08-D8WA	DC02 Diagnostic
Maindec-08-D8XA	XOR Buffer for DP01A
Maindec-08-D9AC	TC58 Data Reliability Test 7 Track
Maindec-08-D9BA	TC58 Drive Function Timer
Maindec-08-D9CB	TC58 Random Exerciser
Maindec-08-D9DD	TC58 Instruction Test 1
Maindec-08-D9EC	TC58 Instruction Test 2
Maindec-08-D9FC	TC58 Data Reliability Test 9 Track
Maindec-08-D9GA	TC58 Data Reliability Test 9 Track
Maindec-8I-F8VA	680I 8-Bit Character Subroutines
Maindec-8I-D0AA	EAE Test Part 1
Maindec-8I-D01C	Instruction Test 1
Maindec-8I-D02B	Instruction Test 2
Maindec-8I-D0BA	EAE Instruction Test
Maindec-8I-D4CA	Memory Parity IOT Test
Maindec-8I-D5BB	DF32 Logic, Mini Test
Maindec-8I-D6AC	AX08 Diagnostic
Maindec-8I-D6CE	KV 8/I Display Diagnostic
Maindec-8I-D8AD	KW8I Real Time Clock Test
Maindec-8I-D8AC	DC08T1-DC08 Off Line Diagnostic
Maindec-8I-D8CA	689 AGT1-689 AG Control and Data Test
Maindec-8I-D8DA	689 AFT-2-689 AG On Line Exerciser

APPENDIX E
TELETYPE CODES

The 8-bit code used by the Model ASR33 Teletype unit is the American Standard Code for Information Interchange (ASCII) modified. To convert the ASCII code to teletype code, add 200 octal (ASCII + 200_8 = Teletype). This code punched in the paper tape reads in reverse of the normal octal form used in the PDP-8/I since bits are numbered from right to left, from 1 through 8, with bit 1 having the most significance. Therefore, perforated tape is read. The Model ASR33 set can generate all assigned codes except 340 through 374 and 376. Generally, codes 207, 212, 215, 240 through 377, and 377 are sufficient for Teletype operation. The Model ASR33 set can detect all characters, but does not interrupt all of the codes that it can generate as commands.

The standard number of characters printed per line is 72. The sequnece for proceeding to the next line is a carriage return followed by a line feed (as opposed to a line feed followed by a carriage return). Key or key combinations are required to produce octal codes from 200 through 337, 375, and 377 are indicated in Table E-1 with the associated ASCII character.

	AC04	AC05	AC06	AC07	AC08		AC09	AC10	AC11
	8	7	6	5	4	Feed Hole	3	2	1
			Most-Significant Octal Bit				Least-Significant Octal Bit		
Tape is loaded into the reader:	1	2	3	Feed Hole ↓ Tape Motion	4	5	6	7	8

Table E-1
Teletype Code (Numerical Order)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
220	Null/Idle	NULL	---	CTRL @
201	Start of Message	SOM	---	CTRL A
202	End of Address	EOA	---	CTRL B
203	End of Message	EOM	---	CTRL C
204	End of Transmission	EOT	---	CTRL D
205	Who Are You	WRU	---	CTRL E
206	Are You	RU	---	CTRL F
207	Audible Signal	BELL	---	CTRL G

Table E-1 (Cont)
Teletype Code (Numerical Order)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
210	Format Effector	FE	---	CTRL H
211	Horizontal Tabulation	H TAB	---	CTRL I
212	Line Feed	LF	---	CTRL J
213	Vertical Tabulation	V TAB	---	CTRL K
214	Form Feed	FF	---	CTRL L
215	Carriage Return	CR	---	CTRL M
216	Shift Out	SO	---	CTRL N
217	Shift In	SI	---	CTRL O
220	Device Control Reversed for Data Line Escape	DC0	---	CTRL P
221	Device Control ON	DC1	---	CTRL Q
222	Device Control (TAPE)	DC2	---	CTRL R
223	Device Control OFF	DC3	---	CTRL S
224	Device Control ~~(TAPE)~~	DC4	---	CTRL T
225	Error	ERR	---	CTRL U
226	Synchronous Idle	SYNC	---	CTRL V
227	Logical End of Media	LEM	---	CTRL W
230	Separator, Information	S0	---	CTRL X
231	Separator, Data Delimiters	S1	---	CTRL Y
232	Separator, Words	S2	---	CTRL Z
233	Separator, Groups	S3	---	SHIFT CTRL K
234	Separator, Records	S4	---	SHIFT CTRL L
235	Separator, Files	S5	---	SHIFT CTRL M
236	Separator, Misc.	S6	---	SHIFT CTRL N
237	Separator, Misc.	S7	---	SHIFT CTRL O
240	Space	SP	Space	Space Bar
241	Exclamation Point	!	!	SHIFT !
242	Quotation Marks	"	"	SHIFT "
243	Number Sign	#	#	SHIFT #
244	Dollar Sign	$	$	SHIFT $
245	Percent Sign	%	%	SHIFT %
246	Ampersand	&	&	SHIFT &
247	Apostrophe	'	'	SHIFT '
250	Parenthesis, Beginning	(	(	SHIFT (
251	Parenthesis, Ending	)	)	SHIFT)
252	Asterisk	*	*	SHIFT *

Table E-1 (Cont)
Teletype Code (Numerical Order)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
253	Plus Sign	+	+	SHIFT +
254	Comma	,	,	,
255	Hyphen	-	-	-
256	Period	.	.	.
257	Virgule	/	/	/
260	Numeral 0	0	0	0
261	Numeral 1	1	1	1
262	Numeral 2	2	2	2
263	Numeral 3	3	3	3
264	Numeral 4	4	4	4
265	Numeral 5	5	5	5
266	Numeral 6	6	6	6
267	Numeral 7	7	7	7
270	Numeral 8	8	8	8
271	Numeral 9	9	9	9
272	Colon	:	:	:
273	Semicolon	;	;	;
274	Less Than	<	<	SHIFT <
275	Equals	=	=	SHIFT =
276	Greater Than	>	>	SHIFT >
277	Interrogation Point	?	?	SHIFT ?
300	At	@	@	SHIFT @
301	Letter A	A	A	A
302	Letter B	B	B	B
303	Letter C	C	C	C
304	Letter D	D	D	D
305	Letter E	E	E	E
306	Letter F	F	F	F
307	Letter G	G	G	G
310	Letter H	H	H	H
311	Letter I	I	I	I
312	Letter J	J	J	J
313	Letter K	K	K	K
314	Letter L	L	L	L
315	Letter M	M	M	M

Table E-1 (Cont)
Teletype Code (Numerical Order)

Octal Code	Character Name	ASCII Character	Teletype Character	Key or Key Combinations
316	Letter N	N	N	N
317	Letter O	O	O	O
320	Letter P	P	P	P
321	Letter Q	Q	Q	Q
322	Letter R	R	R	R
323	Letter S	S	S	S
324	Letter T	T	T	T
325	Letter U	U	U	U
326	Letter V	V	V	V
327	Letter W	W	W	W
330	Letter X	X	X	X
331	Letter Y	Y	Y	Y
332	Letter Z	Z	Z	Z
333	Bracket, Left	[	[	SHIFT K
334	Reverse Virgule	\	\	SHIFT L
335	Bracket, Right	]	]	SHIFT M
336	Up Arrow (exponentiation)	↑	↑	SHIFT
337	Left Arrow	←	←	SHIFT
340 through 374 are not available				
375	Unassigned Control	]	---	ALT MODE
376	Not Available			
377	Delete/Idle/Rub Out	DEL	---	RUB OUT

Table E-2
Teletype Code (Character Order)

Character	8-Bit Code (in octal)	Character	8-Bit Code (in octal)
A	301	!	241
B	302	"	242
C	303	#	243
D	304	$	244
E	305	%	245
F	306	&	246
G	307	'	247
H	310	(	250

Table E-2 (Cont)
Teletype Code (Character Order)

Character	8-Bit Code (in octal)	Character	8-Bit Code (in octal)
I	311	)	251
J	312	*	252
K	313	+	253
L	314	,	254
M	315	-	255
N	316	.	256
O	317	/	257
P	320	:	272
Q	321	;	273
R	322	<	274
S	323	=	275
T	324	>	276
U	325	?	277
V	326	@	300
W	327	[	333
X	330	\	334
Y	331	]	335
Z	332	↑	336
		←	337
0	260		
1	261	Leader/Trailer	200
2	262	Line-Feed	212
3	263	Carriage-Return	215
4	264	Space	240
5	265	Rub-out	377
6	266	Blank	000
7	267	act-mode	375
8	270	escape	233
9	271		

Table E-3
Model 33 ASR/KSR Teletype Code (ASCII) In Binary Form

1 = HOLE PUNCHED = MARK
0 = NO HOLE PUNCHED = SPACE

Table E-4
Card Reader Code

Card Code		Internal Code	Character
Zone	Num.		
—	—	01 0000	Blank
12	8-3	11 1011	.
12	8-4	11 1100	)
12	8-5	11 1101	]
12	8-6	11 1110	<
12	8-7	11 1111	←
12	—	11 0000	+
11	8-3	10 1011	$
11	8-4	10 1100	*
11	8-5	10 1101	[
11	8-6	10 1110	>
11	8-7	10 1111	&
11	—	10 0000	—
0	1	01 0001	/
0	8-3	01 1011	,
0	8-4	01 1100	(
0	8-5	01 1101	"
0	8-6	01 1110	#
0	8-7	01 1111	%
—	8-3	00 1011	=
—	8-4	00 1100	@
—	8-5	00 1101	↑
—	8-6	00 1110	'
—	8-7	00 1111	\
12	0	11 1010	?
12	1	11 0001	A
12	2	11 0010	B
12	3	11 0011	C
12	4	11 0100	D
12	5	11 0101	E
12	6	11 0110	F
12	7	11 0111	G
12	8	11 1000	H
12	9	11 1001	I

Card Code		Internal Code	Character
Zone	Num.		
11	0	10 1010	↑
11	1	10 0001	J
11	2	10 0010	K
11	3	10 0011	L
11	4	10 0100	M
11	5	10 0101	N
11	6	10 0110	O
11	7	10 0111	P
11	8	10 1000	Q
11	9	10 1001	R
0	8-2	01 1010	:
0	2	01 0010	S
0	3	01 0011	T
0	4	01 0100	U
0	5	01 0101	V
0	6	01 0110	W
0	7	01 0111	X
0	8	01 1000	Y
0	9	01 1001	Z
—	0	00 1010	0
—	1	00 0001	1
—	2	00 0010	2
—	3	00 0011	3
—	4	00 0100	4
—	5	00 0101	5
—	6	00 0110	6
—	7	00 0111	7
—	8	00 1000	8
—	9	00 1001	9
All other codes		00 0000	←

Table E-5
Automatic Line Printer Code

Character (ASCII)	6-Bit Code (in octal)	Character (ASCII)	6-Bit Code (in octal)
@	0		40
A	1	!	41
B	2	"	42
C	3	#	43
D	4	$	44
E	5	%	45
F	6	&	46
G	7	'	47
H	10	(	50
I	11	)	51
J	12	*	52
K	13	+	53
L	14	,	54
M	15	-	55
N	16	.	56
O	17	/	57
P	20	0	60
Q	21	1	61
R	22	2	62
S	23	3	63
T	24	4	64
U	25	5	65
V	26	6	66
W	27	7	67
X	30	8	70
Y	31	9	71
Z	32	:	72
[	33	;	73
\	34	<	74
]	35	=	75
↑	36	>	76
←	37	?	77

APPENDIX F
MATHEMATICAL DATA

Scales of Notation

2^x IN Decimal

x	2^x	x	2^x	x	2^x
0.001	1.00069 33874 62581	0.01	1.00695 55500 56719	0.1	1.07177 34625 36293
0.002	1.00138 72557 11335	0.02	1.01395 94797 90029	0.2	1.14869 83549 97035
0.003	1.00208 16050 79633	0.03	1.02101 21257 07193	0.3	1.23114 44133 44916
0.004	1.00277 64359 01078	0.04	1.02811 38266 56067	0.4	1.31950 79107 72894
0.005	1.00347 17485 09503	0.05	1.03526 49238 41377	0.5	1.41421 35623 73095
0.006	1.00416 75432 38973	0.06	1.04246 57608 41121	0.6	1.51571 65665 10398
0.007	1.00486 38204 23785	0.07	1.04971 66836 23067	0.7	1.62450 47927 12471
0.008	1.00556 05803 98468	0.08	1.05701 80405 61380	0.8	1.74110 11265 92248
0.009	1.00625 78234 97782	0.09	1.06437 01824 53360	0.9	1.86606 59830 73615

10^{+n} IN Octal

10^n	n	10^{-n}	10^n	n	10^{-n}
1	0	1.000 000 000 000 000 000 000 00	112 402 762 000	10	0.000 000 000 006 676 337 66
12	1	0.063 146 314 631 463 146 31	1 351 035 564 000	11	0.000 000 000 000 537 657 77
144	2	0.005 075 341 217 270 243 66	16 432 451 210 000	12	0.000 000 000 000 043 136 32
1 750	3	0.000 406 111 564 570 651 77	221 411 634 520 000	13	0.000 000 000 000 003 411 35
23 420	4	0.000 032 155 613 530 704 15	2 657 142 036 440 000	14	0.000 000 000 000 000 264 11
303 240	5	0.000 002 476 132 610 706 64	34 327 724 461 500 000	15	0.000 000 000 000 000 022 01
3 641 100	6	0.000 000 206 157 364 055 37	434 157 115 760 200 000	16	0.000 000 000 000 000 001 63
46 113 200	7	0.000 000 015 327 745 152 75	5 432 127 413 542 400 000	17	0.000 000 000 000 000 000 14
575 360 400	8	0.000 000 001 257 143 561 06	67 405 553 164 731 000 000	18	0.000 000 000 000 000 000 01
7 346 545 000	9	0.000 000 000 104 560 276 41			

$n \log_{10} 2$, $n \log_2 10$ IN Decimal

n	$n \log_{10} 2$	$n \log_2 10$	n	$n \log_{10} 2$	$n \log_2 10$
1	0.30102 99957	3.32192 80949	6	1.80617 99740	19.93156 85693
2	0.60205 99913	6.64385 61898	7	2.10720 99696	23.25349 66642
3	0.90308 99870	9.96578 42847	8	2.40823 99653	26.57542 47591
4	1.20411 99827	13.28771 23795	9	2.70926 99610	29.89735 28540
5	1.50514 99783	16.60964 04744	10	3.01029 99566	33.21928 09489

Addition and Multiplication Tables

Addition

Multiplication

Binary Scale

$$0 + 1 = \begin{matrix} 0+0=0 \\ 1+0=1 \\ 1+1=10 \end{matrix}$$

$$0 \times 1 = \begin{matrix} 0\times 0=0 \\ 1\times 0=0 \\ 1\times 1=1 \end{matrix}$$

Octal Scale

0	01	02	03	04	05	06	07
1	02	03	04	05	06	07	10
2	03	04	05	06	07	10	11
3	04	05	06	07	10	11	12
4	05	06	07	10	11	12	13
5	06	07	10	11	12	13	14
6	07	10	11	12	13	14	15
7	10	11	12	13	14	15	16

1	02	03	04	05	06	07
2	04	06	10	12	14	16
3	06	11	14	17	22	25
4	10	14	20	24	30	34
5	12	17	24	31	36	43
6	14	22	30	36	44	52
7	16	25	34	43	52	61

Mathematical Constants in Octal Scale

π = 3.11037 552421$_8$	e = 2.55760 521305$_8$	γ = 0.44742 147707$_8$
π^{-1} = 0.24276 301556$_8$	e^{-1} = 0.27426 530661$_8$	$\ln \gamma$ = −0.43127 233602$_8$
$\sqrt{\pi}$ = 1.61337 611067$_8$	$\sqrt{e}$ = 1.51411 230704$_8$	$\log_2 \gamma$ = −0.62573 030645$_8$
$\ln \pi$ = 1.11206 404435$_8$	$\log_{10} e$ = 0.33626 754251$_8$	$\sqrt{2}$ = 1.32404 746320$_8$
$\log_2 \pi$ = 1.51544 163223$_8$	$\log_2 e$ = 1.34252 166245$_8$	$\ln 2$ = 0.54271 027760$_8$
$\sqrt{10}$ = 3.12305 407267$_8$	$\log_2 10$ = 3.24464 741136$_8$	$\ln 10$ = 2.23273 067355$_8$

Powers of Two

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125
1 099 511 627 776	40	0.000 000 000 000 909 494 701 772 928 237 915 039 062 5
2 199 023 255 552	41	0.000 000 000 000 454 747 350 886 464 118 957 519 531 25
4 398 046 511 104	42	0.000 000 000 000 227 373 675 443 232 059 478 759 765 625
8 796 093 022 208	43	0.000 000 000 000 113 686 837 721 616 029 739 379 882 812 5
17 592 186 044 416	44	0.000 000 000 000 056 843 418 860 808 014 869 689 941 406 25
35 184 372 088 832	45	0.000 000 000 000 028 421 709 430 404 007 434 844 970 703 125
70 368 744 177 664	46	0.000 000 000 000 014 210 854 715 202 003 717 422 485 351 562 5
140 737 488 355 328	47	0.000 000 000 000 007 105 427 357 601 001 858 711 242 675 781 25
281 474 976 710 656	48	0.000 000 000 000 003 552 713 678 800 500 929 355 621 337 890 625
562 949 953 421 312	49	0.000 000 000 000 001 776 356 839 400 250 464 677 810 668 945 312 5
1 125 899 906 842 624	50	0.000 000 000 000 000 888 178 419 700 125 232 338 905 334 472 656 25
2 251 799 813 685 248	51	0.000 000 000 000 000 444 089 209 850 062 616 169 452 667 236 328 125
4 503 599 627 370 496	52	0.000 000 000 000 000 222 044 604 925 031 308 084 726 333 618 164 062 5
9 007 199 254 740 992	53	0.000 000 000 000 000 111 022 302 462 515 654 042 363 166 809 082 031 25
18 014 398 509 481 984	54	0.000 000 000 000 000 055 511 151 231 257 827 021 181 583 404 541 015 625
36 028 797 018 963 968	55	0.000 000 000 000 000 027 755 575 615 628 913 510 590 791 702 270 507 812 5
72 057 594 037 927 936	56	0.000 000 000 000 000 013 877 787 807 814 456 755 295 395 851 135 253 906 25
144 115 188 075 855 872	57	0.000 000 000 000 000 006 938 893 903 907 228 377 647 697 925 567 626 953 125
288 230 376 151 711 744	58	0.000 000 000 000 000 003 469 446 951 953 614 188 823 848 962 783 813 476 562 5
576 460 752 303 423 488	59	0.000 000 000 000 000 001 734 723 475 976 807 094 411 924 481 391 906 738 281 25
1 152 921 504 606 846 976	60	0.000 000 000 000 000 000 867 361 737 988 403 547 205 962 240 695 953 369 140 625
2 305 843 009 213 693 952	61	0.000 000 000 000 000 000 433 680 868 994 201 773 602 981 120 347 976 684 570 312 5
4 611 686 018 427 387 904	62	0.000 000 000 000 000 000 216 840 434 497 100 886 801 490 560 173 988 342 285 156 25
9 223 372 036 854 775 808	63	0.000 000 000 000 000 000 108 420 217 248 550 443 400 745 280 086 994 171 142 578 125
18 446 744 073 709 551 616	64	0.000 000 000 000 000 000 054 210 108 624 275 221 700 372 640 043 497 085 571 289 062 5
36 893 488 147 419 103 232	65	0.000 000 000 000 000 000 027 105 054 312 137 610 850 186 320 021 748 542 785 644 531 25
73 786 976 294 838 206 464	66	0.000 000 000 000 000 000 013 552 527 156 068 805 425 093 160 010 874 271 392 822 265 625
147 573 952 589 676 412 928	67	0.000 000 000 000 000 000 006 776 263 578 034 402 712 546 580 005 437 135 696 411 132 812
295 147 905 179 352 825 856	68	0.000 000 000 000 000 000 003 388 131 789 017 201 356 273 290 002 718 567 848 205 566 406
590 295 810 358 705 651 712	69	0.000 000 000 000 000 000 001 694 065 894 508 600 678 136 645 001 359 283 924 102 783 203 125
1 180 591 620 717 411 303 424	70	0.000 000 000 000 000 000 000 847 032 947 254 300 339 068 322 500 679 641 962 051 391 601 562 5
2 361 183 241 434 822 606 848	71	0.000 000 000 000 000 000 000 423 516 473 627 150 169 534 161 250 339 820 981 025 695 800 781 25
4 722 366 482 869 645 213 696	72	0.000 000 000 000 000 000 000 211 758 236 813 575 084 767 080 625 169 910 490 512 847 900 390 625

Octal-Decimal Integer Conversion Table

0000 (Octal)	0000 (Decimal)
to	to
0777 (Octal)	0511 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
0000	0000	0001	0002	0003	0004	0005	0006	0007
0010	0008	0009	0010	0011	0012	0013	0014	0015
0020	0016	0017	0018	0019	0020	0021	0022	0023
0030	0024	0025	0026	0027	0028	0029	0030	0031
0040	0032	0033	0034	0035	0036	0037	0038	0039
0050	0040	0041	0042	0043	0044	0045	0046	0047
0060	0048	0049	0050	0051	0052	0053	0054	0055
0070	0056	0057	0058	0059	0060	0061	0062	0063
0100	0064	0065	0066	0067	0068	0069	0070	0071
0110	0072	0073	0074	0075	0076	0077	0078	0079
0120	0080	0081	0082	0083	0084	0085	0086	0087
0130	0088	0089	0090	0091	0092	0093	0094	0095
0140	0096	0097	0098	0099	0100	0101	0102	0103
0150	0104	0105	0106	0107	0108	0109	0110	0111
0160	0112	0113	0114	0115	0116	0117	0118	0119
0170	0120	0121	0122	0123	0124	0125	0126	0127
0200	0128	0129	0130	0131	0132	0133	0134	0135
0210	0136	0137	0138	0139	0140	0141	0142	0143
0220	0144	0145	0146	0147	0148	0149	0150	0151
0230	0152	0153	0154	0155	0156	0157	0158	0159
0240	0160	0161	0162	0163	0164	0165	0166	0167
0250	0168	0169	0170	0171	0172	0173	0174	0175
0260	0176	0177	0178	0179	0180	0181	0182	0183
0270	0184	0185	0186	0187	0188	0189	0190	0191
0300	0192	0193	0194	0195	0196	0197	0198	0199
0310	0200	0201	0202	0203	0204	0205	0206	0207
0320	0208	0209	0210	0211	0212	0213	0214	0215
0330	0216	0217	0218	0219	0220	0221	0222	0223
0340	0224	0225	0226	0227	0228	0229	0230	0231
0350	0232	0233	0234	0235	0236	0237	0238	0239
0360	0240	0241	0242	0243	0244	0245	0246	0247
0370	0248	0249	0250	0251	0252	0253	0254	0255

	0	1	2	3	4	5	6	7
0400	0256	0257	0258	0259	0260	0261	0262	0263
0410	0264	0265	0266	0267	0268	0269	0270	0271
0420	0272	0273	0274	0275	0276	0277	0278	0279
0430	0280	0281	0282	0283	0284	0285	0286	0287
0440	0288	0289	0290	0291	0292	0293	0294	0295
0450	0296	0297	0298	0299	0300	0301	0302	0303
0460	0304	0305	0306	0307	0308	0309	0310	0311
0470	0312	0313	0314	0315	0316	0317	0318	0319
0500	0320	0321	0322	0323	0324	0325	0326	0327
0510	0328	0329	0330	0331	0332	0333	0334	0335
0520	0336	0337	0338	0339	0340	0341	0342	0343
0530	0344	0345	0346	0347	0348	0349	0350	0351
0540	0352	0353	0354	0355	0356	0357	0358	0359
0550	0360	0361	0362	0363	0364	0365	0366	0367
0560	0368	0369	0370	0371	0372	0373	0374	0375
0570	0376	0377	0378	0379	0380	0381	0382	0383
0600	0384	0385	0386	0387	0388	0389	0390	0391
0610	0392	0393	0394	0395	0396	0397	0398	0399
0620	0400	0401	0402	0403	0404	0405	0406	0407
0630	0408	0409	0410	0411	0412	0413	0414	0415
0640	0416	0417	0418	0419	0420	0421	0422	0423
0650	0424	0425	0426	0427	0428	0429	0430	0431
0660	0432	0433	0434	0435	0436	0437	0438	0439
0670	0440	0441	0442	0443	0444	0445	0446	0447
0700	0448	0449	0450	0451	0452	0453	0454	0455
0710	0456	0457	0458	0459	0460	0461	0462	0463
0720	0464	0465	0466	0467	0468	0469	0470	0471
0730	0472	0473	0474	0475	0476	0477	0478	0479
0740	0480	0481	0482	0483	0484	0485	0486	0487
0750	0488	0489	0490	0491	0492	0493	0494	0495
0760	0496	0497	0498	0499	0500	0501	0502	0503
0770	0504	0505	0506	0507	0508	0509	0510	0511

1000 (Octal)	0512 (Decimal)
to	to
1777 (Octal)	1023 (Decimal)

	0	1	2	3	4	5	6	7
1000	0512	0513	0514	0515	0516	0517	0518	0519
1010	0520	0521	0522	0523	0524	0525	0526	0527
1020	0528	0529	0530	0531	0532	0533	0534	0535
1030	0536	0537	0538	0539	0540	0541	0542	0543
1040	0544	0545	0546	0547	0548	0549	0550	0551
1050	0552	0553	0554	0555	0556	0557	0558	0559
1060	0560	0561	0562	0563	0564	0565	0566	0567
1070	0568	0569	0570	0571	0572	0573	0574	0575
1100	0576	0577	0578	0579	0580	0581	0582	0583
1110	0584	0585	0586	0587	0588	0589	0590	0591
1120	0592	0593	0594	0595	0596	0597	0598	0599
1130	0600	0601	0602	0603	0604	0605	0606	0607
1140	0608	0609	0610	0611	0612	0613	0614	0615
1150	0616	0617	0618	0619	0620	0621	0622	0623
1160	0624	0625	0626	0627	0628	0629	0630	0631
1170	0632	0633	0634	0635	0636	0637	0638	0639
1200	0640	0641	0642	0643	0644	0645	0646	0647
1210	0648	0649	0650	0651	0652	0653	0654	0655
1220	0656	0657	0658	0659	0660	0661	0662	0663
1230	0664	0665	0666	0667	0668	0669	0670	0671
1240	0672	0673	0674	0675	0676	0677	0678	0679
1250	0680	0681	0682	0683	0684	0685	0686	0687
1260	0688	0689	0690	0691	0692	0693	0694	0695
1270	0696	0697	0698	0699	0700	0701	0702	0703
1300	0704	0705	0706	0707	0708	0709	0710	0711
1310	0712	0713	0714	0715	0716	0717	0718	0719
1320	0720	0721	0722	0723	0724	0725	0726	0727
1330	0728	0729	0730	0731	0732	0733	0734	0735
1340	0736	0737	0738	0739	0740	0741	0742	0743
1350	0744	0745	0746	0747	0748	0749	0750	0751
1360	0752	0753	0754	0755	0756	0757	0758	0759
1370	0760	0761	0762	0763	0764	0765	0766	0767

	0	1	2	3	4	5	6	7
1400	0768	0769	0770	0771	0772	0773	0774	0775
1410	0776	0777	0778	0779	0780	0781	0782	0783
1420	0784	0785	0786	0787	0788	0789	0790	0791
1430	0792	0793	0794	0795	0796	0797	0798	0799
1440	0800	0801	0802	0803	0804	0805	0806	0807
1450	0808	0809	0810	0811	0812	0813	0814	0815
1460	0816	0817	0818	0819	0820	0821	0822	0823
1470	0824	0825	0826	0827	0828	0829	0830	0831
1500	0832	0833	0834	0835	0836	0837	0838	0839
1510	0840	0841	0842	0843	0844	0845	0846	0847
1520	0848	0849	0850	0851	0852	0853	0854	0855
1530	0856	0857	0858	0859	0860	0861	0862	0863
1540	0864	0865	0866	0867	0868	0869	0870	0871
1550	0872	0873	0874	0875	0876	0877	0878	0879
1560	0880	0881	0882	0883	0884	0885	0886	0887
1570	0888	0889	0890	0891	0892	0893	0894	0895
1600	0896	0897	0898	0899	0900	0901	0902	0903
1610	0904	0905	0906	0907	0908	0909	0910	0911
1620	0912	0913	0914	0915	0916	0917	0918	0919
1630	0920	0921	0922	0923	0924	0925	0926	0927
1640	0928	0929	0930	0931	0932	0933	0934	0935
1650	0936	0937	0938	0939	0940	0941	0942	0943
1660	0944	0945	0946	0947	0948	0949	0950	0951
1670	0952	0953	0954	0955	0956	0957	0958	0959
1700	0960	0961	0962	0963	0964	0965	0966	0967
1710	0968	0969	0970	0971	0972	0973	0974	0975
1720	0976	0977	0978	0979	0980	0981	0982	0983
1730	0984	0985	0986	0987	0988	0989	0990	0991
1740	0992	0993	0994	0995	0996	0997	0998	0999
1750	1000	1001	1002	1003	1004	1005	1006	1007
1760	1008	1009	1010	1011	1012	1013	1014	1015
1770	1016	1017	1018	1019	1020	1021	1022	1023

Octal-Decimal Integer Conversion Table (Cont)

	0	1	2	3	4	5	6	7
2000	1024	1025	1026	1027	1028	1029	1030	1031
2010	1032	1033	1034	1035	1036	1037	1038	1039
2020	1040	1041	1042	1043	1044	1045	1046	1047
2030	1048	1049	1050	1051	1052	1053	1054	1055
2040	1056	1057	1058	1059	1060	1061	1062	1063
2050	1064	1065	1066	1067	1068	1069	1070	1071
2060	1072	1073	1074	1075	1076	1077	1078	1079
2070	1080	1081	1082	1083	1084	1085	1086	1087
2100	1088	1089	1090	1091	1092	1093	1094	1095
2110	1096	1097	1098	1099	1100	1101	1102	1103
2120	1104	1105	1106	1107	1108	1109	1110	1111
2130	1112	1113	1114	1115	1116	1117	1118	1119
2140	1120	1121	1122	1123	1124	1125	1126	1127
2150	1128	1129	1130	1131	1132	1133	1134	1135
2160	1136	1137	1138	1139	1140	1141	1142	1143
2170	1144	1145	1146	1147	1148	1149	1150	1151
2200	1152	1153	1154	1155	1156	1157	1158	1159
2210	1160	1161	1162	1163	1164	1165	1166	1167
2220	1168	1169	1170	1171	1172	1173	1174	1175
2230	1176	1177	1178	1179	1180	1181	1182	1183
2240	1184	1185	1186	1187	1188	1189	1190	1191
2250	1192	1193	1194	1195	1196	1197	1198	1199
2260	1200	1201	1202	1203	1204	1205	1206	1207
2270	1208	1209	1210	1211	1212	1213	1214	1215
2300	1216	1217	1218	1219	1220	1221	1222	1223
2310	1224	1225	1226	1227	1228	1229	1230	1231
2320	1232	1233	1234	1235	1236	1237	1238	1239
2330	1240	1241	1242	1243	1244	1245	1246	1247
2340	1248	1249	1250	1251	1252	1253	1254	1255
2350	1256	1257	1258	1259	1260	1261	1262	1263
2360	1264	1265	1266	1267	1268	1269	1270	1271
2370	1272	1273	1274	1275	1276	1277	1278	1279

	0	1	2	3	4	5	6	7
2400	1280	1281	1282	1283	1284	1285	1286	1287
2410	1288	1289	1290	1291	1292	1293	1294	1295
2420	1296	1297	1298	1299	1300	1301	1302	1303
2430	1304	1305	1306	1307	1308	1309	1310	1311
2440	1312	1313	1314	1315	1316	1317	1318	1319
2450	1320	1321	1322	1323	1324	1325	1326	1327
2460	1328	1329	1330	1331	1332	1333	1334	1335
2470	1336	1337	1338	1339	1340	1341	1342	1343
2500	1344	1345	1346	1347	1348	1349	1350	1351
2510	1352	1353	1354	1355	1356	1357	1358	1359
2520	1360	1361	1362	1363	1364	1365	1366	1367
2530	1368	1369	1370	1371	1372	1373	1374	1375
2540	1376	1377	1378	1379	1380	1381	1382	1383
2550	1384	1385	1386	1387	1388	1389	1390	1391
2560	1392	1393	1394	1395	1396	1397	1398	1399
2570	1400	1401	1402	1403	1404	1405	1406	1407
2600	1408	1409	1410	1411	1412	1413	1414	1415
2610	1416	1417	1418	1419	1420	1421	1422	1423
2620	1424	1425	1426	1427	1428	1429	1430	1431
2630	1432	1433	1434	1435	1436	1437	1438	1439
2640	1440	1441	1442	1443	1444	1445	1446	1447
2650	1448	1449	1450	1451	1452	1453	1454	1455
2660	1456	1457	1458	1459	1460	1461	1462	1463
2670	1464	1465	1466	1467	1468	1469	1470	1471
2700	1472	1473	1474	1475	1476	1477	1478	1479
2710	1480	1481	1482	1483	1484	1485	1486	1487
2720	1488	1489	1490	1491	1492	1493	1494	1495
2730	1496	1497	1498	1499	1500	1501	1502	1503
2740	1504	1505	1506	1507	1508	1509	1510	1511
2750	1512	1513	1514	1515	1516	1517	1518	1519
2760	1520	1521	1522	1523	1524	1525	1526	1527
2770	1528	1529	1530	1531	1532	1533	1534	1535

2000	1024
to	to
2777	1535
(Octal)	(Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
3000	1536	1537	1538	1539	1540	1541	1542	1543
3010	1544	1545	1546	1547	1548	1549	1550	1551
3020	1552	1553	1554	1555	1556	1557	1558	1559
3030	1560	1561	1562	1563	1564	1565	1566	1567
3040	1568	1569	1570	1571	1572	1573	1574	1575
3050	1576	1577	1578	1579	1580	1581	1582	1583
3060	1584	1585	1586	1587	1588	1589	1590	1591
3070	1592	1593	1594	1595	1596	1597	1598	1599
3100	1600	1601	1602	1603	1604	1605	1606	1607
3110	1608	1609	1610	1611	1612	1613	1614	1615
3120	1616	1617	1618	1619	1620	1621	1622	1623
3130	1624	1625	1626	1627	1628	1629	1630	1631
3140	1632	1633	1634	1635	1636	1637	1638	1639
3150	1640	1641	1642	1643	1644	1645	1646	1647
3160	1648	1649	1650	1651	1652	1653	1654	1655
3170	1656	1657	1658	1659	1660	1661	1662	1663
3200	1664	1665	1666	1667	1668	1669	1670	1671
3210	1672	1673	1674	1675	1676	1677	1678	1679
3220	1680	1681	1682	1683	1684	1685	1686	1687
3230	1688	1689	1690	1691	1692	1693	1694	1695
3240	1696	1697	1698	1699	1700	1701	1702	1703
3250	1704	1705	1706	1707	1708	1709	1710	1711
3260	1712	1713	1714	1715	1716	1717	1718	1719
3270	1720	1721	1722	1723	1724	1725	1726	1727
3300	1728	1729	1730	1731	1732	1733	1734	1735
3310	1736	1737	1738	1739	1740	1741	1742	1743
3320	1744	1745	1746	1747	1748	1749	1750	1751
3330	1752	1753	1754	1755	1756	1757	1758	1759
3340	1760	1761	1762	1763	1764	1765	1766	1767
3350	1768	1769	1770	1771	1772	1773	1774	1775
3360	1776	1777	1778	1779	1780	1781	1782	1783
3370	1784	1785	1786	1787	1788	1789	1790	1791

	0	1	2	3	4	5	6	7
3400	1792	1793	1794	1795	1796	1797	1798	1799
3410	1800	1801	1802	1803	1804	1805	1806	1807
3420	1808	1809	1810	1811	1812	1813	1814	1815
3430	1816	1817	1818	1819	1820	1821	1822	1823
3440	1824	1825	1826	1827	1828	1829	1830	1831
3450	1832	1833	1834	1835	1836	1837	1838	1839
3460	1840	1841	1842	1843	1844	1845	1846	1847
3470	1848	1849	1850	1851	1852	1853	1854	1855
3500	1856	1857	1858	1859	1860	1861	1862	1863
3510	1864	1865	1866	1867	1868	1869	1870	1871
3520	1872	1873	1874	1875	1876	1877	1878	1879
3530	1880	1881	1882	1883	1884	1885	1886	1887
3540	1888	1889	1890	1891	1892	1893	1894	1895
3550	1896	1897	1898	1899	1900	1901	1902	1903
3560	1904	1905	1906	1907	1908	1909	1910	1911
3570	1912	1913	1914	1915	1916	1917	1918	1919
3600	1920	1921	1922	1923	1924	1925	1926	1927
3610	1928	1929	1930	1931	1932	1933	1934	1935
3620	1936	1937	1938	1939	1940	1941	1942	1943
3630	1944	1945	1946	1947	1948	1949	1950	1951
3640	1952	1953	1954	1955	1956	1957	1958	1959
3650	1960	1961	1962	1963	1964	1965	1966	1967
3660	1968	1969	1970	1971	1972	1973	1974	1975
3670	1976	1977	1978	1979	1980	1981	1982	1983
3700	1984	1985	1986	1987	1988	1989	1990	1991
3710	1992	1993	1994	1995	1996	1997	1998	1999
3720	2000	2001	2002	2003	2004	2005	2006	2007
3730	2008	2009	2010	2011	2012	2013	2014	2015
3740	2016	2017	2018	2019	2020	2021	2022	2023
3750	2024	2025	2026	2027	2028	2029	2030	2031
3760	2032	2033	2034	2035	2036	2037	2038	2039
3770	2040	2041	2042	2043	2044	2045	2046	2047

3000	1536
to	to
3777	2047
(Octal)	(Decimal)

Octal-Decimal Integer Conversion Table (Cont)

4000 (Octal)	2048 (Decimal)
to	to
4777 (Octal)	2559 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
4000	2048	2049	2050	2051	2052	2053	2054	2055
4010	2056	2057	2058	2059	2060	2061	2062	2063
4020	2064	2065	2066	2067	2068	2069	2070	2071
4030	2072	2073	2074	2075	2076	2077	2078	2079
4040	2080	2081	2082	2083	2084	2085	2086	2087
4050	2088	2089	2090	2091	2092	2093	2094	2095
4060	2096	2097	2098	2099	2100	2101	2102	2103
4070	2104	2105	2106	2107	2108	2109	2110	2111
4100	2112	2113	2114	2115	2116	2117	2118	2119
4110	2120	2121	2122	2123	2124	2125	2126	2127
4120	2128	2129	2130	2131	2132	2133	2134	2135
4130	2136	2137	2138	2139	2140	2141	2142	2143
4140	2144	2145	2146	2147	2148	2149	2150	2151
4150	2152	2153	2154	2155	2156	2157	2158	2159
4160	2160	2161	2162	2163	2164	2165	2166	2167
4170	2168	2169	2170	2171	2172	2173	2174	2175
4200	2176	2177	2178	2179	2180	2181	2182	2183
4210	2184	2185	2186	2187	2188	2189	2190	2191
4220	2192	2193	2194	2195	2196	2197	2198	2199
4230	2200	2201	2202	2203	2204	2205	2206	2207
4240	2208	2209	2210	2211	2212	2213	2214	2215
4250	2216	2217	2218	2219	2220	2221	2222	2223
4260	2224	2225	2226	2227	2228	2229	2230	2231
4270	2232	2233	2234	2235	2236	2237	2238	2239
4300	2240	2241	2242	2243	2244	2245	2246	2247
4310	2248	2249	2250	2251	2252	2253	2254	2255
4320	2256	2257	2258	2259	2260	2261	2262	2263
4330	2264	2265	2266	2267	2268	2269	2270	2271
4340	2272	2273	2274	2275	2276	2277	2278	2279
4350	2280	2281	2282	2283	2284	2285	2286	2287
4360	2288	2289	2290	2291	2292	2293	2294	2295
4370	2296	2297	2298	2299	2300	2301	2302	2303

	0	1	2	3	4	5	6	7
4400	2304	2305	2306	2307	2308	2309	2310	2311
4410	2312	2313	2314	2315	2316	2317	2318	2319
4420	2320	2321	2322	2323	2324	2325	2326	2327
4430	2328	2329	2330	2331	2332	2333	2334	2335
4440	2336	2337	2338	2339	2340	2341	2342	2343
4450	2344	2345	2346	2347	2348	2349	2350	2351
4460	2352	2353	2354	2355	2356	2357	2358	2359
4470	2360	2361	2362	2363	2364	2365	2366	2367
4500	2368	2369	2370	2371	2372	2373	2374	2375
4510	2376	2377	2378	2379	2380	2381	2382	2383
4520	2384	2385	2386	2387	2388	2389	2390	2391
4530	2392	2393	2394	2395	2396	2397	2398	2399
4540	2400	2401	2402	2403	2404	2405	2406	2407
4550	2408	2409	2410	2411	2412	2413	2414	2415
4560	2416	2417	2418	2419	2420	2421	2422	2423
4570	2424	2425	2426	2427	2428	2429	2430	2431
4600	2432	2433	2434	2435	2436	2437	2438	2439
4610	2440	2441	2442	2443	2444	2445	2446	2447
4620	2448	2449	2450	2451	2452	2453	2454	2455
4630	2456	2457	2458	2459	2460	2461	2462	2463
4640	2464	2465	2466	2467	2468	2469	2470	2471
4650	2472	2473	2474	2475	2476	2477	2478	2479
4660	2480	2481	2482	2483	2484	2485	2486	2487
4670	2488	2489	2490	2491	2492	2493	2494	2495
4700	2496	2497	2498	2499	2500	2501	2502	2503
4710	2504	2505	2506	2507	2508	2509	2510	2511
4720	2512	2513	2514	2515	2516	2517	2518	2519
4730	2520	2521	2522	2523	2524	2525	2526	2527
4740	2528	2529	2530	2531	2532	2533	2534	2535
4750	2536	2537	2538	2539	2540	2541	2542	2543
4760	2544	2545	2546	2547	2548	2549	2550	2551
4770	2552	2553	2554	2555	2556	2557	2558	2559

5000 (Octal)	2560 (Decimal)
to	to
5777 (Octal)	3071 (Decimal)

	0	1	2	3	4	5	6	7
5000	2560	2561	2562	2563	2564	2565	2566	2567
5010	2568	2569	2570	2571	2572	2573	2574	2575
5020	2576	2577	2578	2579	2580	2581	2582	2583
5030	2584	2585	2586	2587	2588	2589	2590	2591
5040	2592	2593	2594	2595	2596	2597	2598	2599
5050	2600	2601	2602	2603	2604	2605	2606	2607
5060	2608	2609	2610	2611	2612	2613	2614	2615
5070	2616	2617	2618	2619	2620	2621	2622	2623
5100	2624	2625	2626	2627	2628	2629	2630	2631
5110	2632	2633	2634	2635	2636	2637	2638	2639
5120	2640	2641	2642	2643	2644	2645	2646	2647
5130	2648	2649	2650	2651	2652	2653	2654	2655
5140	2656	2657	2658	2659	2660	2661	2662	2663
5150	2664	2665	2666	2667	2668	2669	2670	2671
5160	2672	2673	2674	2675	2676	2677	2678	2679
5170	2680	2681	2682	2683	2684	2685	2686	2687
5200	2688	2689	2690	2691	2692	2693	2694	2695
5210	2696	2697	2698	2699	2700	2701	2702	2703
5220	2704	2705	2706	2707	2708	2709	2710	2711
5230	2712	2713	2714	2715	2716	2717	2718	2719
5240	2720	2721	2722	2723	2724	2725	2726	2727
5250	2728	2729	2730	2731	2732	2733	2734	2735
5260	2736	2737	2738	2739	2740	2741	2742	2743
5270	2744	2745	2746	2747	2748	2749	2750	2751
5300	2752	2753	2754	2755	2756	2757	2758	2759
5310	2760	2761	2762	2763	2764	2765	2766	2767
5320	2768	2769	2770	2771	2772	2773	2774	2775
5330	2776	2777	2778	2779	2780	2781	2782	2783
5340	2784	2785	2786	2787	2788	2789	2790	2791
5350	2792	2793	2794	2795	2796	2797	2798	2799
5360	2800	2801	2802	2803	2804	2805	2806	2807
5370	2808	2809	2810	2811	2812	2813	2814	2815

	0	1	2	3	4	5	6	7
5400	2816	2817	2818	2819	2820	2821	2822	2823
5410	2824	2825	2826	2827	2828	2829	2830	2831
5420	2832	2833	2834	2835	2836	2837	2838	2839
5430	2840	2841	2842	2843	2844	2845	2846	2847
5440	2848	2849	2850	2851	2852	2853	2854	2855
5450	2856	2857	2858	2859	2860	2861	2862	2863
5460	2864	2865	2866	2867	2868	2869	2870	2871
5470	2872	2873	2874	2875	2876	2877	2878	2879
5500	2880	2881	2882	2883	2884	2885	2886	2887
5510	2888	2889	2890	2891	2892	2893	2894	2895
5520	2896	2897	2898	2899	2900	2901	2902	2903
5530	2904	2905	2906	2907	2908	2909	2910	2911
5540	2912	2913	2914	2915	2916	2917	2918	2919
5550	2920	2921	2922	2923	2924	2925	2926	2927
5560	2928	2929	2930	2931	2932	2933	2934	2935
5570	2936	2937	2938	2939	2940	2941	2942	2943
5600	2944	2945	2946	2947	2948	2949	2950	2951
5610	2952	2953	2954	2955	2956	2957	2958	2959
5620	2960	2961	2962	2963	2964	2965	2966	2967
5630	2968	2969	2970	2971	2972	2973	2974	2975
5640	2976	2977	2978	2979	2980	2981	2982	2983
5650	2984	2985	2986	2987	2988	2989	2990	2991
5660	2992	2993	2994	2995	2996	2997	2998	2999
5670	3000	3001	3002	3003	3004	3005	3006	3007
5700	3008	3009	3010	3011	3012	3013	3014	3015
5710	3016	3017	3018	3019	3020	3021	3022	3023
5720	3024	3025	3026	3027	3028	3029	3030	3031
5730	3032	3033	3034	3035	3036	3037	3038	3039
5740	3040	3041	3042	3043	3044	3045	3046	3047
5750	3048	3049	3050	3051	3052	3053	3054	3055
5760	3056	3057	3058	3059	3060	3061	3062	3063
5770	3064	3065	3066	3067	3068	3069	3070	3071

Octal-Decimal Integer Conversion Table (Cont)

	0	1	2	3	4	5	6	7
6000	3072	3073	3074	3075	3076	3077	3078	3079
6010	3080	3081	3082	3083	3084	3085	3086	3087
6020	3088	3089	3090	3091	3092	3093	3094	3095
6030	3096	3097	3098	3099	3100	3101	3102	3103
6040	3104	3105	3106	3107	3108	3109	3110	3111
6050	3112	3113	3114	3115	3116	3117	3118	3119
6060	3120	3121	3122	3123	3124	3125	3126	3127
6070	3128	3129	3130	3131	3132	3133	3134	3135
6100	3136	3137	3138	3139	3140	3141	3142	3143
6110	3144	3145	3146	3147	3148	3149	3150	3151
6120	3152	3153	3154	3155	3156	3157	3158	3159
6130	3160	3161	3162	3163	3164	3165	3166	3167
6140	3168	3169	3170	3171	3172	3173	3174	3175
6150	3176	3177	3178	3179	3180	3181	3182	3183
6160	3184	3185	3186	3187	3188	3189	3190	3191
6170	3192	3193	3194	3195	3196	3197	3198	3199
6200	3200	3201	3202	3203	3204	3205	3206	3207
6210	3208	3209	3210	3211	3212	3213	3214	3215
6220	3216	3217	3218	3219	3220	3221	3222	3223
6230	3224	3225	3226	3227	3228	3229	3230	3231
6240	3232	3233	3234	3235	3236	3237	3238	3239
6250	3240	3241	3242	3243	3244	3245	3246	3247
6260	3248	3249	3250	3251	3252	3253	3254	3255
6270	3256	3257	3258	3259	3260	3261	3262	3263
6300	3264	3265	3266	3267	3268	3269	3270	3271
6310	3272	3273	3274	3275	3276	3277	3278	3279
6320	3280	3281	3282	3283	3284	3285	3286	3287
6330	3288	3289	3290	3291	3292	3293	3294	3295
6340	3296	3297	3298	3299	3300	3301	3302	3303
6350	3304	3305	3306	3307	3308	3309	3310	3311
6360	3312	3313	3314	3315	3316	3317	3318	3319
6370	3320	3321	3322	3323	3324	3325	3326	3327

	0	1	2	3	4	5	6	7
6400	3328	3329	3330	3331	3332	3333	3334	3335
6410	3336	3337	3338	3339	3340	3341	3342	3343
6420	3344	3345	3346	3347	3348	3349	3350	3351
6430	3352	3353	3354	3355	3356	3357	3358	3359
6440	3360	3361	3362	3363	3364	3365	3366	3367
6450	3368	3369	3370	3371	3372	3373	3374	3375
6460	3376	3377	3378	3379	3380	3381	3382	3383
6470	3384	3385	3386	3387	3388	3389	3390	3391
6500	3392	3393	3394	3395	3396	3397	3398	3399
6510	3400	3401	3402	3403	3404	3405	3406	3407
6520	3408	3409	3410	3411	3412	3413	3414	3415
6530	3416	3417	3418	3419	3420	3421	3422	3423
6540	3424	3425	3426	3427	3428	3429	3430	3431
6550	3432	3433	3434	3435	3436	3437	3438	3439
6560	3440	3441	3442	3443	3444	3445	3446	3447
6570	3448	3449	3450	3451	3452	3453	3454	3455
6600	3456	3457	3458	3459	3460	3461	3462	3463
6610	3464	3465	3466	3467	3468	3469	3470	3471
6620	3472	3473	3474	3475	3476	3477	3478	3479
6630	3480	3481	3482	3483	3484	3485	3486	3487
6640	3488	3489	3490	3491	3492	3493	3494	3495
6650	3496	3497	3498	3499	3500	3501	3502	3503
6660	3504	3505	3506	3507	3508	3509	3510	3511
6670	3512	3513	3514	3515	3516	3517	3518	3519
6700	3520	3521	3522	3523	3524	3525	3526	3527
6710	3528	3529	3530	3531	3532	3533	3534	3535
6720	3536	3537	3538	3539	3540	3541	3542	3543
6730	3544	3545	3546	3547	3548	3549	3550	3551
6740	3552	3553	3554	3555	3556	3557	3558	3559
6750	3560	3561	3562	3563	3564	3565	3566	3567
6760	3568	3569	3570	3571	3572	3573	3574	3575
6770	3576	3577	3578	3579	3580	3581	3582	3583

6000 to 6777 (Octal)	3072 to 3583 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
7000	3584	3585	3586	3587	3588	3589	3590	3591
7010	3592	3593	3594	3595	3596	3597	3598	3599
7020	3600	3601	3602	3603	3604	3605	3606	3607
7030	3608	3609	3610	3611	3612	3613	3614	3615
7040	3616	3617	3618	3619	3620	3621	3622	3623
7050	3624	3625	3626	3627	3628	3629	3630	3631
7060	3632	3633	3634	3635	3636	3637	3638	3639
7070	3640	3641	3642	3643	3644	3645	3646	3647
7100	3648	3649	3650	3651	3652	3653	3654	3655
7110	3656	3657	3658	3659	3660	3661	3662	3663
7120	3664	3665	3666	3667	3668	3669	3670	3671
7130	3672	3673	3674	3675	3676	3677	3678	3679
7140	3680	3681	3682	3683	3684	3685	3686	3687
7150	3688	3689	3690	3691	3692	3693	3694	3695
7160	3696	3697	3698	3699	3700	3701	3702	3703
7170	3704	3705	3706	3707	3708	3709	3710	3711
7200	3712	3713	3714	3715	3716	3717	3718	3719
7210	3720	3721	3722	3723	3724	3725	3726	3727
7220	3728	3729	3730	3731	3732	3733	3734	3735
7230	3736	3737	3738	3739	3740	3741	3742	3743
7240	3744	3745	3746	3747	3748	3749	3750	3751
7250	3752	3753	3754	3755	3756	3757	3758	3759
7260	3760	3761	3762	3763	3764	3765	3766	3767
7270	3768	3769	3770	3771	3772	3773	3774	3775
7300	3776	3777	3778	3779	3780	3781	3782	3783
7310	3784	3785	3786	3787	3788	3789	3790	3791
7320	3792	3793	3794	3795	3796	3797	3798	3799
7330	3800	3801	3802	3803	3804	3805	3806	3807
7340	3808	3809	3810	3811	3812	3813	3814	3815
7350	3816	3817	3818	3819	3820	3821	3822	3823
7360	3824	3825	3826	3827	3828	3829	3830	3831
7370	3832	3833	3834	3835	3836	3837	3838	3839

	0	1	2	3	4	5	6	7
7400	3840	3841	3842	3843	3844	3845	3846	3847
7410	3848	3849	3850	3851	3852	3853	3854	3855
7420	3856	3857	3858	3859	3860	3861	3862	3863
7430	3864	3865	3866	3867	3868	3869	3870	3871
7440	3872	3873	3874	3875	3876	3877	3878	3879
7450	3880	3881	3882	3883	3884	3885	3886	3887
7460	3888	3889	3890	3891	3892	3893	3894	3895
7470	3896	3897	3898	3899	3900	3901	3902	3903
7500	3904	3905	3906	3907	3908	3909	3910	3911
7510	3912	3913	3914	3915	3916	3917	3918	3919
7520	3920	3921	3922	3923	3924	3925	3926	3927
7530	3928	3929	3930	3931	3932	3933	3934	3935
7540	3936	3937	3938	3939	3940	3941	3942	3943
7550	3944	3945	3946	3947	3948	3949	3950	3951
7560	3952	3953	3954	3955	3956	3957	3958	3959
7570	3960	3961	3962	3963	3964	3965	3966	3967
7600	3968	3969	3970	3971	3972	3973	3974	3975
7610	3976	3977	3978	3979	3980	3981	3982	3983
7620	3984	3985	3986	3987	3988	3989	3990	3991
7630	3992	3993	3994	3995	3996	3997	3998	3999
7640	4000	4001	4002	4003	4004	4005	4006	4007
7650	4008	4009	4010	4011	4012	4013	4014	4015
7660	4016	4017	4018	4019	4020	4021	1022	4023
7670	4024	4025	4026	4027	4028	4029	4030	4031
7700	4032	4033	4034	4035	4036	4037	4038	4039
7710	4040	4041	4042	4043	4044	4045	4046	4047
7720	4048	4049	4050	4051	4052	4053	4054	4055
7730	4056	4057	4058	4059	4060	4061	4062	4063
7740	4064	4065	4066	4067	4068	4069	4070	4071
7750	4072	4073	4074	4075	4076	4077	4078	4079
7760	4080	4081	4082	4083	4084	4085	4086	4087
7770	4088	4089	4090	4091	4092	4093	4094	4095

7000 to 7777 (Octal)	3584 to 4095 (Decimal)

Octal-Decimal Fraction Conversion Table

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000	.000000	.100	.125000	.200	.250000	.300	.375000
.001	.001953	.101	.126953	.201	.251953	.301	.376953
.002	.003906	.102	.128906	.202	.253906	.302	.378906
.003	.005859	.103	.130859	.203	.255859	.303	.380859
.004	.007812	.104	.132812	.204	.257812	.304	.382812
.005	.009765	.105	.134765	.205	.259765	.305	.384765
.006	.011718	.106	.136718	.206	.261718	.306	.386718
.007	.013671	.107	.138671	.207	.263671	.307	.388671
.010	.015625	.110	.140625	.210	.265625	.310	.390625
.011	.017578	.111	.142578	.211	.267578	.311	.392578
.012	.019531	.112	.144531	.212	.269531	.312	.394531
.013	.021484	.113	.146484	.213	.271484	.313	.396484
.014	.023437	.114	.148437	.214	.273437	.314	.398437
.015	.025390	.115	.150390	.215	.275390	.315	.400390
.016	.027343	.116	.152343	.216	.277343	.316	.402343
.017	.029296	.117	.154296	.217	.279296	.317	.404296
.020	.031250	.120	.156250	.220	.281250	.320	.406250
.021	.033203	.121	.158203	.221	.283203	.321	.408203
.022	.035156	.122	.160156	.222	.285156	.322	.410156
.023	.037109	.123	.162109	.223	.287109	.323	.412109
.024	.039062	.124	.164062	.224	.289062	.324	.414062
.025	.041015	.125	.166015	.225	.291015	.325	.416015
.026	.042968	.126	.167968	.226	.292968	.326	.417968
.027	.044921	.127	.169921	.227	.294921	.327	.419921
.030	.046875	.130	.171875	.230	.296875	.330	.421875
.031	.048828	.131	.173828	.231	.298828	.331	.423828
.032	.050781	.132	.175781	.232	.300781	.332	.425781
.033	.052734	.133	.177734	.233	.302734	.333	.427734
.034	.054687	.134	.179687	.234	.304687	.334	.429687
.035	.056640	.135	.181640	.235	.306640	.335	.431640
.036	.058593	.136	.183593	.236	.308593	.336	.433593
.037	.060546	.137	.185546	.237	.310546	.337	.435546
.040	.062500	.140	.187500	.240	.312500	.340	.437500
.041	.064453	.141	.189453	.241	.314453	.341	.439453
.042	.066406	.142	.191406	.242	.316406	.342	.441406
.043	.068359	.143	.193359	.243	.318359	.343	.443359
.044	.070312	.144	.195312	.244	.320312	.344	.445312
.045	.072265	.145	.197265	.245	.322265	.345	.447265
.046	.074218	.146	.199218	.246	.324218	.346	.449218
.047	.076171	.147	.201171	.247	.326171	.347	.451171
.050	.078125	.150	.203125	.250	.328125	.350	.453125
.051	.080078	.151	.205078	.251	.330078	.351	.455078
.052	.082031	.152	.207031	.252	.332031	.352	.457031
.053	.083984	.153	.208984	.253	.333984	.353	.458984
.054	.085937	.154	.210937	.254	.335937	.354	.460937
.055	.087890	.155	.212890	.255	.337890	.355	.462890
.056	.089843	.156	.214843	.256	.339843	.356	.464843
.057	.091796	.157	.216796	.257	.341796	.357	.466796
.060	.093750	.160	.218750	.260	.343750	.360	.468750
.061	.095703	.161	.220703	.261	.345703	.361	.470703
.062	.097656	.162	.222656	.262	.347656	.362	.472656
.063	.099609	.163	.224609	.263	.349609	.363	.474609
.064	.101562	.164	.226562	.264	.351562	.364	.476562
.065	.103515	.165	.228515	.265	.353515	.365	.478515
.066	.105468	.166	.230468	.266	.355468	.366	.480468
.067	.107421	.167	.232421	.267	.357421	.367	.482421
.070	.109375	.170	.234375	.270	.359375	.370	.484375
.071	.111328	.171	.236328	.271	.361328	.371	.486328
.072	.113281	.172	.238281	.272	.363281	.372	.488281
.073	.115234	.173	.240234	.273	.365234	.373	.490234
.074	.117187	.174	.242187	.274	.367187	.374	.492187
.075	.119140	.175	.244140	.275	.369140	.375	.494140
.076	.121093	.176	.246093	.276	.371093	.376	.496093
.077	.123046	.177	.248046	.277	.373046	.377	.498046

Octal-Decimal Fraction Conversion Table (Cont)

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000000	.000000	.000100	.000244	.000200	.000488	.000300	.000732
.000001	.000003	.000101	.000247	.000201	.000492	.000301	.000736
.000002	.000007	.000102	.000251	.000202	.000495	.000302	.000740
.000003	.000011	.000103	.000255	.000203	.000499	.000303	.000743
.000004	.000015	.000104	.000259	.000204	.000503	.000304	.000747
.000005	.000019	.000105	.000263	.000205	.000507	.000305	.000751
.000006	.000022	.000106	.000267	.000206	.000511	.000306	.000755
.000007	.000026	.000107	.000270	.000207	.000514	.000307	.000759
.000010	.000030	.000110	.000274	.000210	.000518	.000310	.000762
.000011	.000034	.000111	.000278	.000211	.000522	.000311	.000766
.000012	.000038	.000112	.000282	.000212	.000526	.000312	.000770
.000013	.000041	.000113	.000286	.000213	.000530	.000313	.000774
.000014	.000045	.000114	.000289	.000214	.000534	.000314	.000778
.000015	.000049	.000115	.000293	.000215	.000537	.000315	.000782
.000016	.000053	.000116	.000297	.000216	.000541	.000316	.000785
.000017	.000057	.000117	.000301	.000217	.000545	.000317	.000789
.000020	.000061	.000120	.000305	.000220	.000549	.000320	.000793
.000021	.000064	.000121	.000308	.000221	.000553	.000321	.000797
.000022	.000068	.000122	.000312	.000222	.000556	.000322	.000801
.000023	.000072	.000123	.000316	.000223	.000560	.000323	.000805
.000024	.000076	.000124	.000320	.000224	.000564	.000324	.000808
.000025	.000080	.000125	.000324	.000225	.000568	.000325	.000812
.000026	.000083	.000126	.000328	.000226	.000572	.000326	.000816
.000027	.000087	.000127	.000331	.000227	.000576	.000327	.000820
.000030	.000091	.000130	.000335	.000230	.000579	.000330	.000823
.000031	.000095	.000131	.000339	.000231	.000583	.000331	.000827
.000032	.000099	.000132	.000343	.000232	.000587	.000332	.000831
.000033	.000102	.000133	.000347	.000233	.000591	.000333	.000835
.000034	.000106	.000134	.000350	.000234	.000595	.000334	.000839
.000035	.000110	.000135	.000354	.000235	.000598	.000335	.000843
.000036	.000114	.000136	.000358	.000236	.000602	.000336	.000846
.000037	.000118	.000137	.000362	.000237	.000606	.000337	.000850
.000040	.000122	.000140	.000366	.000240	.000610	.000340	.000854
.000041	.000125	.000141	.000370	.000241	.000614	.000341	.000858
.000042	.000129	.000142	.000373	.000242	.000617	.000342	.000862
.000043	.000133	.000143	.000377	.000243	.000621	.000343	.000865
.000044	.000137	.000144	.000381	.000244	.000625	.000344	.000869
.000045	.000141	.000145	.000385	.000245	.000629	.000345	.000873
.000046	.000144	.000146	.000389	.000246	.000633	.000346	.000877
.000047	.000148	.000147	.000392	.000247	.000637	.000347	.000881
.000050	.000152	.000150	.000396	.000250	.000640	.000350	.000885
.000051	.000156	.000151	.000400	.000251	.000644	.000351	.000888
.000052	.000160	.000152	.000404	.000252	.000648	.000352	.000892
.000053	.000164	.000153	.000408	.000253	.000652	.000353	.000896
.000054	.000167	.000154	.000411	.000254	.000656	.000354	.000900
.000055	.000171	.000155	.000415	.000255	.000659	.000355	.000904
.000056	.000175	.000156	.000419	.000256	.000663	.000356	.000907
.000057	.000179	.000157	.000423	.000257	.000667	.0003..	.000911
.000060	.000183	.000160	.000427	.000260	.000671	.000360	.000915
.000061	.000186	.000161	.000431	.000261	.000675	.000361	.000919
.000062	.000190	.000162	.000434	.000262	.000679	.000362	.000923
.000063	.000194	.000163	.000438	.000263	.000682	.000363	.000926
.000064	.000198	.000164	.000442	.000264	.000686	.000364	.000930
.000065	.000202	.000165	.000446	.000265	.000690	.000365	.000934
.000066	.000205	.000166	.000450	.000266	.000694	.000366	.000938
.000067	.000209	.000167	.000453	.000267	.000698	.000367	.000942
.000070	.000213	.000170	.000457	.000270	.000701	.000370	.000946
.000071	.000217	.000171	.000461	.000271	.000705	.000371	.000949
.000072	.000221	.000172	.000465	.000272	.000709	.000372	.000953
.000073	.000225	.000173	.000469	.000273	.000713	.000373	.000957
.000074	.000228	.000174	.000473	.000274	.000717	.000374	.000961
.000075	.000232	.000175	.000476	.000275	.000720	.000375	.000965
.000076	.000236	.000176	.000480	.000276	.000724	.000376	.000968
.000077	.000240	.000177	.000484	.000277	.000728	.000377	.000972